

**FAIRCHILD**  
SEMICONDUCTOR™

September 1986  
Revised February 2000

## DM7476

### Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs

#### General Description

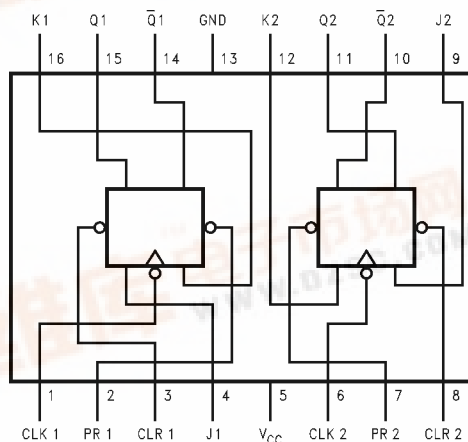
This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is LOW the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is HIGH the J and K inputs are disabled. On the

negative transition of the clock, the data from the master is transferred to the slave. The logic state of J and K inputs must not be allowed to change while the clock is HIGH. The data is transferred to the outputs on the falling edge of the clock pulse. A LOW logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

#### Ordering Code:

Order Number	Package Number	Package Description
DM7476N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

#### Connection Diagram



#### Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	$\neg$	L	L	$Q_0$	$\bar{Q}_0$
H	H	$\neg$	H	L	H	L
H	H	$\neg$	L	H	L	H
H	H	$\neg$	H	H	Toggle	Toggle

H = HIGH Logic Level

L = LOW Logic Level

X = Either LOW or HIGH Logic Level

$\neg$  = Positive pulse data. The J and K inputs must be held constant while the clock is HIGH. Data is transferred to the outputs on the falling edge of the clock pulse.

$Q_0$  = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete active HIGH level clock pulse.

**Note 1:** This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (HIGH) level.

DM7476 Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs



## Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

**Note 2:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
$V_{CC}$	Supply Voltage	4.75	5	5.25	V
$V_{IH}$	HIGH Level Input Voltage	2			V
$V_{IL}$	LOW Level Input Voltage			0.8	V
$I_{OH}$	HIGH Level Output Current			–0.4	mA
$I_{OL}$	LOW Level Output Current			16	mA
$f_{CLK}$	Clock Frequency (Note 3)	0		15	MHz
$t_W$	Pulse Width (Note 3)	Clock HIGH	20		ns
		Clock LOW	47		
		Preset LOW	25		
		Clear LOW	25		
$t_{SU}$	Input Setup Time (Note 3)(Note 4)	0↑			ns
$t_H$	Input Hold Time (Note 3)(Note 4)	0↓			ns
$T_A$	Free Air Operating Temperature	0		70	°C

**Note 3:**  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5\text{V}$ .

**Note 4:** The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference (↑) for rising edge, (↓) for falling edge.

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}$ , $I_I = -12\text{ mA}$			–1.5	V
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$ , $V_{IH} = \text{Min}$	2.4	3.4		V
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OL} = \text{Max}$ $V_{IH} = \text{Min}$ , $V_{IL} = \text{Max}$		0.2	0.4	V
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ , $V_I = 5.5\text{V}$			1	mA
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}$ $V_I = 2.4\text{V}$	J, K		40	$\mu\text{A}$
			Clock		80	
			Clear		80	
			Preset		80	
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}$ $V_I = 0.4\text{V}$ (Note 6)	J, K		–1.6	mA
			Clock		–3.2	
			Clear		–3.2	
			Preset		–3.2	
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 7)	–18		–55	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 8)		18	34	mA

**Note 5:** All typicals are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .

**Note 6:** Clear is measured with preset HIGH and preset is measured with clear HIGH.

**Note 7:** Not more than one output should be shorted at a time.

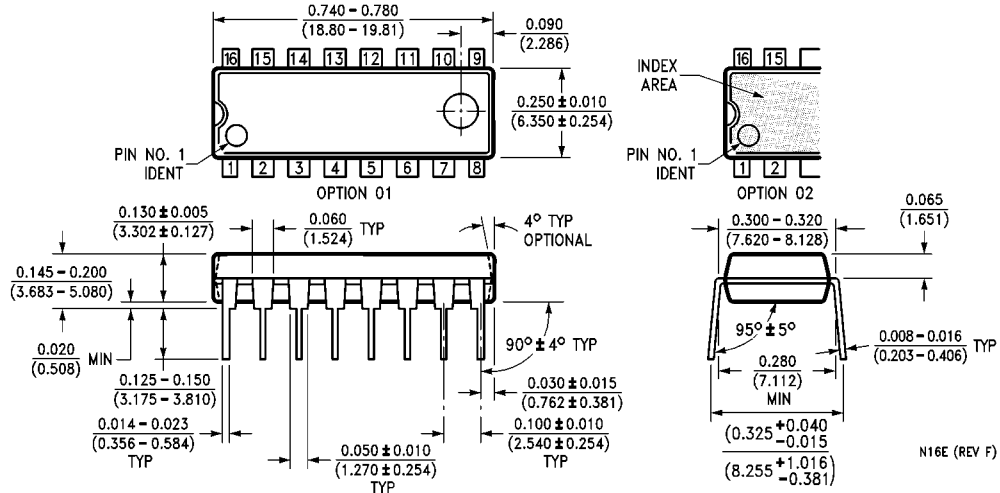
**Note 8:** With all outputs OPEN,  $I_{CC}$  is measured with the Q and  $\bar{Q}$  outputs HIGH in turn. At the time of measurement the clock input is grounded.

## Switching Characteristics

at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$ , $C_L = 15\text{ pF}$		Units
			Min	Max	
$f_{MAX}$	Maximum Clock Frequency		15		MHz
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\overline{Q}$		40	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		25	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		40	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		25	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		40	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		25	ns

## Physical Dimensions inches (millimeters) unless otherwise noted



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)