



DM9102D

Single Chip Fast Ethernet NIC Controller

1. General Description

The DM9102D is a fully integrated and cost effective single chip Fast Ethernet NIC controller. It is designed with low power and high performance process. It is a 2.5/3.3V device with 5V tolerance.

The DM9102D provides direct interface to the PCI bus and supports bus master mode to achieve the high performance of the PCI bus. It fully complies with PCI 2.2. In the media side, the DM9102D interfaces to the UTP3, 4, 5 in 10Base-T and the UTP5 in 100Base-TX. It is fully compliant with the IEEE 802.3u Spec. The auto-negotiation and auto-MDI/MDIX function can automatically configure the

DM9102D to take the maximum advantage of its abilities. The DM9102D also supports IEEE 802.3x's full-duplex flow control to prevent the receive overflow of link partner. The IPv4 IP/TCP/UDP checksum generation and checking can reduce the system CPU utilization.

The DM9102D supports two types of power management mechanisms. The main mechanism is based on the OnNow architecture, which is required for PC99. The alternative mechanism is based upon the remote Wake-On-LAN mechanism.

2. Block Diagram

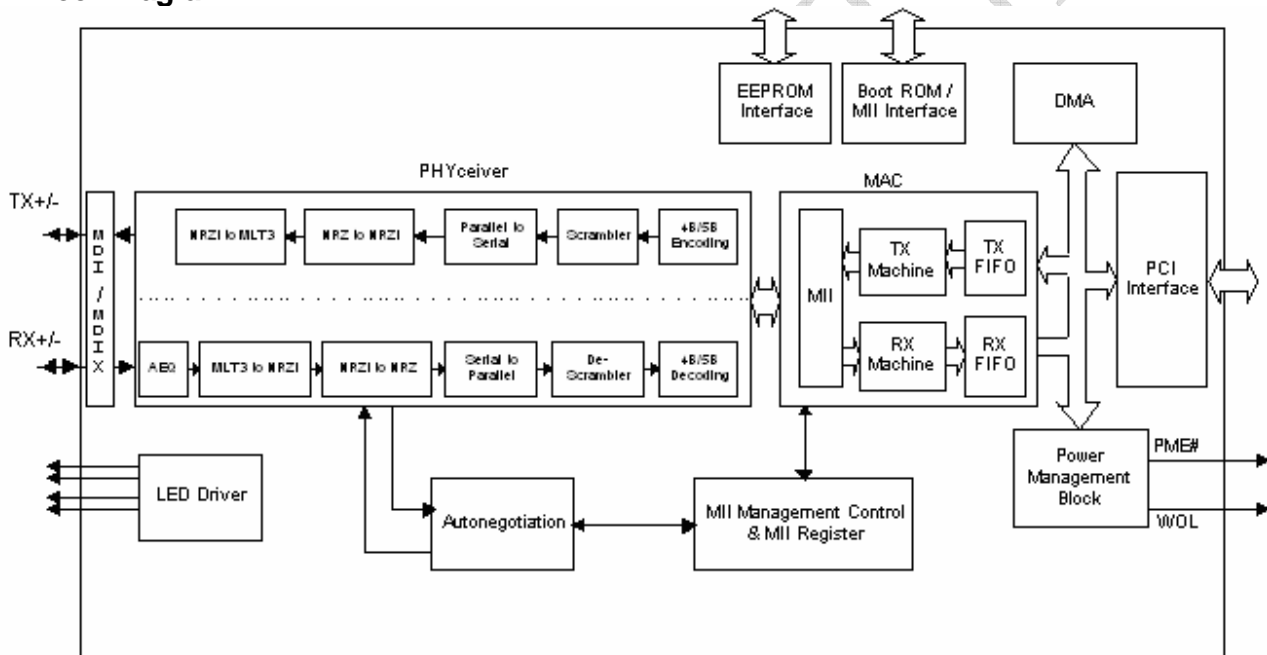




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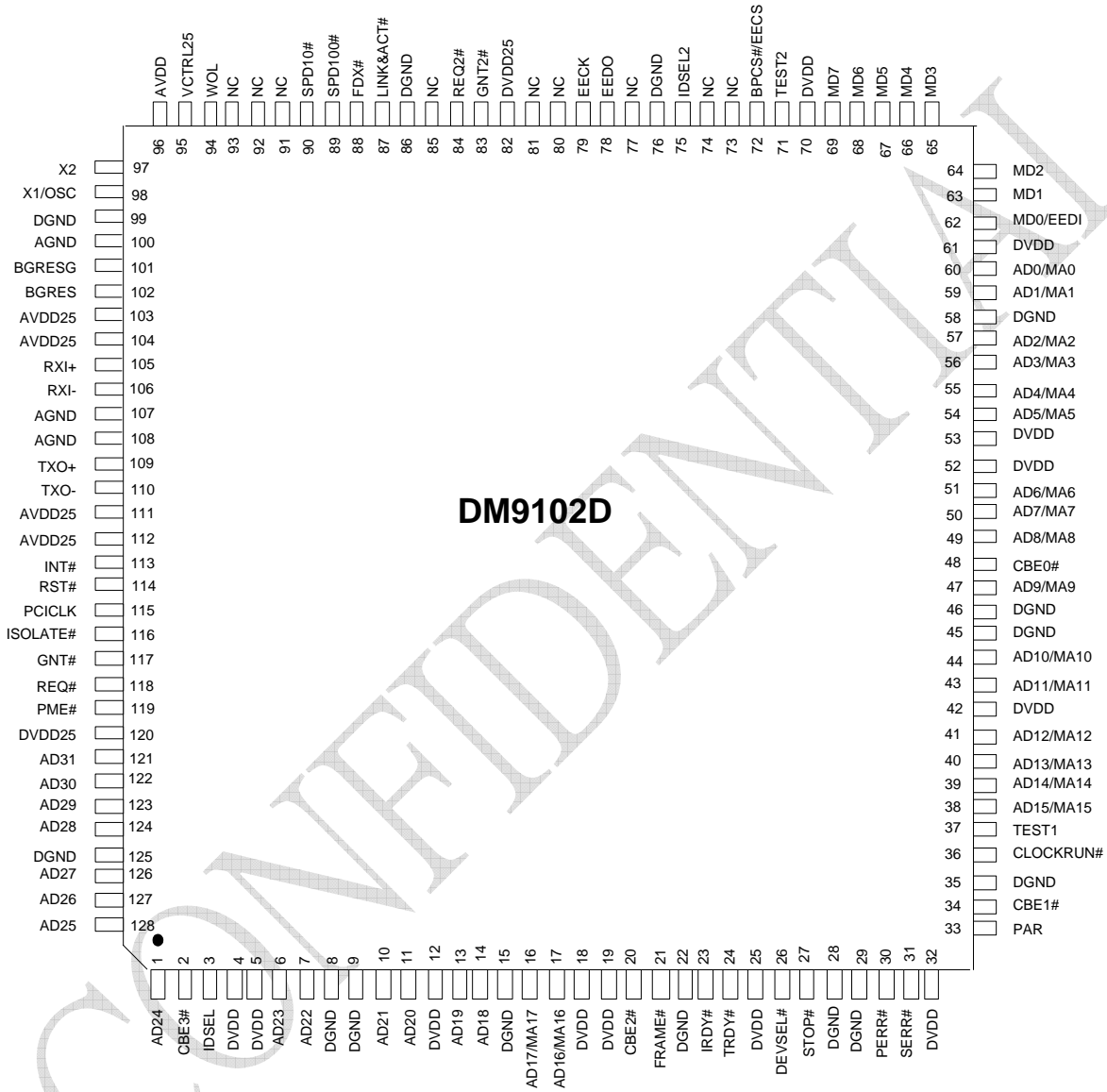
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3. Features

- Integrated Fast Ethernet MAC, Physical Layer and transceiver in one chip.
- 128 pin LQFP with CMOS process.
- +2.5/3.3V Power supply with +5V tolerant I/O.
- Comply with PCI specification 2.2.
- PCI bus master architecture.
- PCI bus burst mode data transfer.
- Two large independent transmission and receipt FIFO.
- Up to 256K bytes Boot EPROM or Flash interface.
- EEPROM 93C46 interface automatically supports node ID load and configuration information.
- Comply with IEEE 802.3u 100Base-TX and 802.3 10Base-T.
- Comply with IEEE 802.3u auto-negotiation protocol for automatic link type selection.
- Support IEEE 802.3x Full Duplex Flow Control.
- VLAN frame length support.
- IP/TCP/UDP checksum generation and checking.
- Zero copy supporting.
- Comply with ACPI and PCI Bus Power Management.
- Support the MII (Media Independent Interface) for an external PHY.
- Support Wake-On-LAN function and remote wake-up (Magic packet, Link Change and Microsoft® wake-up frame).
- Support 4 Wake-On-LAN (WOL) signals (active high pulse, active low pulse, active high, active low.)
- High performance 100Mbps clock generator and data recovery circuit.
- Digital clock recovery circuit, using advanced digital algorithm to reduce jitter.
- Adaptive equalization circuit and Baseline wandering restoration circuit for 100Mbps receiver.
- Provides Loopback mode for easy system diagnostics.
- Support auto-MDI/MDIX.
- Low power consumption modes:
 - Power reduced mode (cable detection)
 - Power down mode
 - Selectable TX drivers for 1:1 or 1.25:1 transformers for additional power reduction. (1.25:1 transformers for Non Auto MDIX only).

4. Pin Configuration : 128 pin LQFP



5. Pin Description

I = Input, O = Output, I/O = Input / Output, O/D = Open Drain, P = Power,
= asserted Low

5.1 PCI Bus Interface Signals

Pin No.	Pin Name	I/O	Description
128LQFP			
113	INT#	O/D	Interrupt Request This signal will be asserted low when an interrupted condition as defined in CR5 is set, and the corresponding mask bit in CR7 is et.
114	RST#	I	System Reset When this signal is low, the DM9102D performs the internal system reset to its initial state.
115	PCICLK	I	PCI system clock PCI bus clock that provides timing for DM9102D related to PCI bus transactions.
117	GNT#	I	Bus Grant This signal is asserted low to indicate that DM9102D has been granted ownership of the bus by the central arbiter.
118	REQ#	O	Bus Request The DM9102D will assert this signal low to request the ownership of the bus.
119	PME#	O/D	Power Management Event. The DM9102D drives it low to indicates that a power management event has occurred.
3	IDSEL	I	Initialization Device Select This signal is asserted high during the Configuration Space read/write access.
21	FRAME#	I/O	Cycle Frame This signal is driven low by the DM9102D master mode to indicate the beginning and duration of a bus transaction.
23	IRDY#	I/O	Initiator Ready This signal is driven low when the master is ready to complete the current data phase of the transaction. A data phase is completed on any clock when both IRDY# and TRDY# are sampled asserted.
24	TRDY#	I/O	Target Ready This signal is driven low when the target is ready to complete the current data phase of the transaction. During a read, it indicates that valid data is asserted. During a write, it indicates that the target is prepared to accept data.
26	DEVSEL#	I/O	Device Select The DM9102D asserts the signal low when it recognizes its target address after FRAME# is asserted. As a bus master, the DM9102D will sample this signal which insures its destination address of the data transfer is recognized by a target.
27	STOP#	I/O	Stop This signal is asserted low by the target device to request the

			master device to stop the current transaction.
30	PERR#	I/O	Parity Error The DM9102D as a master or slave will assert this signal low to indicate a parity error on any incoming data.
31	SERR#	I/O	System Error This signal is asserted low when address parity is detected with enabled PCICS bit31 (detected parity error.) The system error asserts two clock cycles after the falling address if an address parity error is detected.
33	PAR	I/O	Parity This signal indicates even parity across AD0~AD31 and C/BE0#~C/BE3# including the PAR pin. This signal is an output for the master and an input for the slave device. It is stable and valid one clock after the address phase.
2,20,34,48	C/BE3# C/BE2# C/BE1# C/BE0#	I/O	Bus Command/Byte Enable During the address phase, these signals define the bus command or the type of bus transaction that will take place. During the data phase these pins indicate which byte lanes contain valid data. C/BE0# applies to bit7-0 and C/BE3# applies to bit31-24.
121,122,123,124,126,127, 128,1,6,7,10,11,13,14,16, 17,38,39,40,41,43,44,47, 49,50,51,54,55,56,57,59, 60	AD31~AD0/ MA17~MA0	I/O	Address & Data or Boot ROM Address These are multiplexed address and data bus signals. As a bus master, the DM9102D will drive address during the first bus phase. During subsequent phases, the DM9102D will either read or write data expecting the target to increment its address pointer. As a target, the DM9102D will decode each address on the bus and respond if it is the target being addressed. AD17~AD0 can also be used as boot ROM address MA17~MA0 when the boot ROM is accessed.

5.2 Boot ROM and EEPROM Interfaces

Pin No.	Pin Name	I/O	Description
128LQFP			
62	MD0/EEDI	I	Boot ROM Data Input/EEPROM Data In This is a multiplexed pin used by EEDI and MD0. When boot ROM is selected, it acts as boot ROM data input, otherwise the DM9102D will read the contents of EEPROM serially through this pin.
63,64,65,66,67,68,69	MD1~MD7	I	Boot ROM Data Input Bus
72	BPCS#/EECS	O	Boot ROM (active low) or EEPROM Chip Selection.
78	EEDO	O	EEPROM Data Out This pin is used serially to write op-codes, addresses and data into the EEPROM.
79	EECK	O	EEPROM Serial Clock This pin is used as the clock for the EEPROM data transfer.

5.3 LED Pins

Pin No.	Pin Name	I/O	Description
128LQFP			
87	LINK&ACT#	O/D	LED Output Pin, Active Low

			mode 0 = Link and traffic LED. Active low to indicate normal link, and it will flash as a traffic LED when transmitting or receiving. mode 1 = traffic LED only
88	FDX#	O/D	LED Output Pin, Active Low mode 0 = Full duplex LED mode 1 = Full duplex LED
89	SPD100#	O/D	LED Output Pin, Active Low mode 0 = 100Mbps LED mode 1 = 100Mbps LED
90	SPD10#	O/D	LED Output Pin, Active Low mode 0 = 10Mbps LED mode 1 = Link LED

5.4 Network Interface

Pin No. 128LQFP	Pin Name	I/O	Description
105,106	RXI+ RX-	I	100M/10Mbps Differential Input Pair. These two pins are differential receive input pair for 100BASE-TX and 10BASE-T. They are capable of receiving 100BASE-TX MLT-3 or 10BASE-T Manchester encoded data.
109,110	TXO+ TXO-	O	100M/10Mbps differential output pair. These two pins are differential output pair for 100BASE-TX and 10BASE-T. This output pair provides controlled rising and falling time, designed to filter the transmitter's output.

5.5 Miscellaneous Pins

Pin No. 128LQFP	Pin Name	I/O	Description
75	IDSEL2	O	PCI IDSEL 2. When this pin is pulled high, the PCI multiple function is present, and it act as PCI IDSEL2 function.
84	REQ2#	O	PCI Request 2 If the PCI multiple function mode is selected, this pin act as the PCI REQ2# function.
83	GNT2#	I	PCI GNT2# If the PCI multiple function mode is selected, this pin act as GNT2# function. When this pin is pulled high, the DM9102D is in LED mode 1 otherwise the led mode 0 is selected.
36	CLOCKRUN#	I/O	Clockrun# The clockrun# signal is used by the system to pause or slow down the PCI clock signal. It is used by the DM9102D to enable or disable suspension or restart of the PCI clock. When the CLOCKRUN# pin is not used, this pin should be connected to an external pulled down resistor.
71	TEST2	I	TEST mode control 2 In normal operation, tie high to this pin.

37	TEST1	I	TEST Mode Control 1 In normal operation, tie low to this pin.
94	WOL	O	Wake up signal. The DM9102D can assert this pin if it detects link status change, magic packet, or sample frame match. The default is low active pulse mode. The DM9102D also supports High/Low and Pulse/Level options from EEPROM setting.
97	X2	O	Crystal feedback output This pin is used for crystal connection only. Leave this pin open if oscillator is used.
98	X1/OSC	I	Crystal or Oscillator Input. (25MHz±50ppm) Connect to a 25MHz Oscillator or series resonance, fundamental frequency crystal.
102	BGRES	I	Bandgap Voltage Reference Resistor. It connects to a 6.8K 1% error tolerance resistor between this pin and BGRESG pin, to provide an accurate current reference for DM9102D (10Base-T/100Base-TX Application).
116	ISOLATE#	I	Isolate This pin is used to isolate the DM9102D from the PCI bus.
95	VCTRL25	O	Voltage 2.5V control This pin can be used to control a BJT transistor 's base pin to generate a stable 2.5V power in BJT's drain pin .

5.6 Power Pins

Pin No.	Pin Name	I/O	Description
128LQFP			
101	BGRESG	P	Bandgap Ground It is used together with the BGRES pin.
100,107,108	AGND	P	Analog Ground
103,104,111,112	AVDD25	P	Analog Power, +2.5V
96	AVDD	P	Analog Power, +3.3V
8,9,15,22,28,29,35,45, 46,58,76,86,99,125	DGND	P	Digital Ground
82,120	DVDD25	P	Digital Power, +2.5V
4,5,12,18,19,25,32,42,52, 53,61,70	DVDD	P	Digital Power, +3.3V

5.7 NC Pins

Pin No.	Pin Name	I/O	Description
128LQFP			
73,74,77,80,81,85,91,92,93	NC	-	These pins are unused in application and should let them unconnected.

5.8 strap pins table

1: pull-high 1K~10K, 0: default floating.

Pin No.	Pin Name	Description
72	BPCS#/EECS	Disable Auto-MDIX 1: auto-MDIX disabled 0: auto-MDIX enabled
75	IDSEL2	PCI multiple function 1: enable PCI multiple function 0: disable PCI multiple function
83	GNT2#	LED mode 1: LED mode 1 0: LED mode 0

6. Register Definition

6.1 PCI Configuration Registers

The definitions of PCI Configuration Registers are based on the PCI specification revision 2.2 and it provides the initialization and configuration information to operate the PCI interface in the DM9102D. All registers can be accessed

with byte, word, or double word mode. As defined in PCI specification 2.1, read accesses to reserve or unimplemented registers will return a value of "0." These registers are to be described in the following sections.

The default value of PCI configuration registers after reset.

Description	Identifier	Address Offset	Value of Reset
Identification	PCIID	00H	91021282H
Command & Status	PCICS	04H	02100000H*
Revision	PCIRV	08H	02000050H
Miscellaneous	PCILT	0CH	BIOS determine
I/O Base Address	PCIIO	10H	System allocate
Memory Base Address	PCIMEM	14H	System allocate
Reserved	-----	18H - 28H	00000000H
Subsystem Identification	PCISID	2CH	load from EEPROM
Expansion ROM Base Address	PCIROM	30H	00000000H
Capability Pointer	CAP_PTR	34H	00000050H
Reserved	-----	38H	00000000H
Interrupt & Latency	PCIINT	3CH	System allocate bit7~0
Device Specific Configuration Register	PCIUSR	40H	00000000H**
Power Management Register	PCIPMR	50H	C0310001H**
Power Management Control & Status	PMCSR	54H	00000100H

* It is written to 02100007H by most BIOS.

** It may be changed from EEPROM in application.

Key to Default

In the register description that follows, the default column takes the form <Reset Value>

Where :

<Reset Value>:

- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value

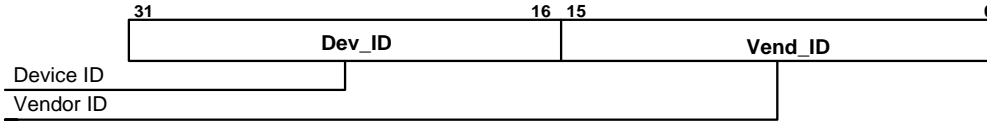
<Access Type>:

RO = Read only

RW = Read/Write

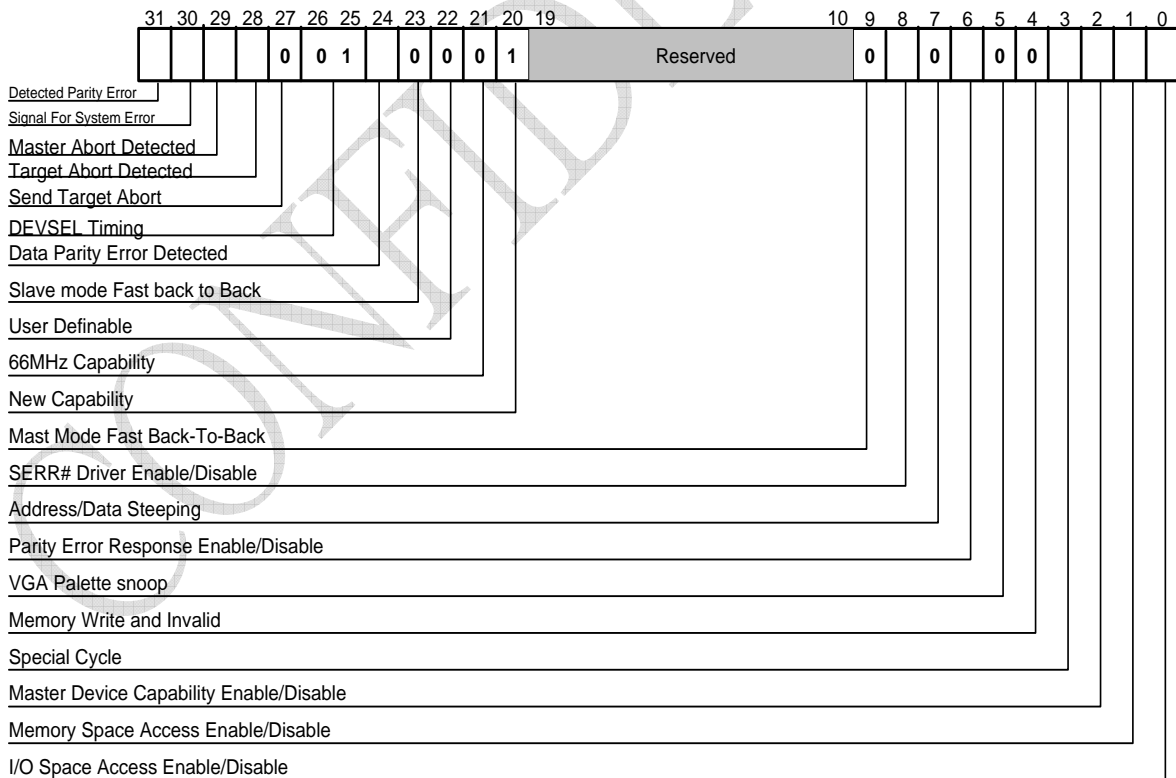
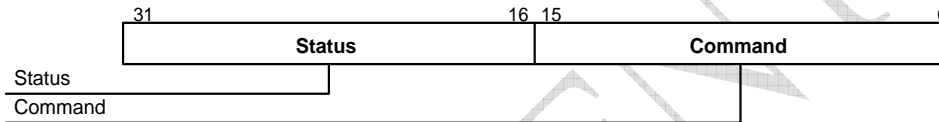
R/C: means Read / Write & Write "1" for Clear.

6.1.1 Identification ID (xxxxxx00H - PCIID)



Bit	Default	Type	Description
16:31	9102H	RO	The field identifies the particular device. Unique and fixed number for the DM9102D is 9102H.
0:15	1282H	RO	This field identifies the manufacturer of the device. Unique and fixed number for Davicom is 1282H.

6.1.2 Command & Status (xxxxxx04H - PCICS)

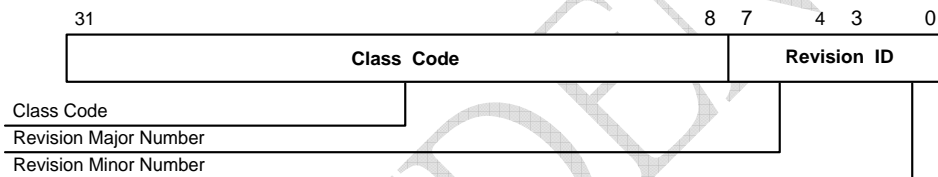


Bit	Default	Type	Description
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31	0	R/C	<p>Detected Parity Error</p> <p>The DM9102D samples the AD[0:31], C/BE[0:3]#, and the PAR signal to check parity and to set parity errors. In slave mode, the parity check falls on command phase and data valid phase (IRDY# and TRDY# both active). In master mode, the DM9102D will check each data phase, during a memory read cycle, for parity error. During a memory write cycle, if an error occurs, the PERR# signal will be driven by the target. This bit is set by the DM9102D and cleared by writing "1". There is no effect by writing "0"</p>
30	0	R/C	<p>Signal For System Error</p> <p>This bit is set when the SERR# signal is driven by the DM9102D. This system error occurs when an address parity is detected under the condition that bit 8 and bit 6 in command register below are set</p>
29	0	R/C	<p>Master Abort Detected</p> <p>This bit is set when the DM9102D terminates a master cycle with the master-abort bus transaction</p>
28	0	R/C	<p>Target Abort Detected</p> <p>This bit is set when the DM9102D terminates a master cycle due to a target-abort signal from other targets</p>
27	0	R/C	<p>Send Target Abort (0 for No Implementation)</p> <p>The DM9102D will never assert the target-abort sequence</p>
26:25	01	R/C	<p>DEVSEL Timing (01 Select Medium Timing)</p> <p>Medium timing of DEVSEL# means the DM9102D will assert DEVSEL# signal two clocks after FRAME# is sample "asserted"</p>
24	0	R/C	<p>Data Parity Error Detected</p> <p>This bit will take effect only when operating as a master and when a Parity Error Response Bit in command configuration register is set. It is set under two conditions:</p> <ul style="list-style-type: none"> (i) PERR# asserted by the DM9102D in memory data read error (ii) PERR# sent from the target due to memory data write error
23	0	RO	<p>Slave Mode Fast Back-To-Back Capable (0 for No Support)</p> <p>This bit is always reads "1" to indicate that the DM9102D is capable of accepting fast back-to-back transaction as a slave mode device</p>
22	0	RO	User-Definable Feature Supported (0 for No Support)
21	0	RO	66 MHz (0 for No Capability)
20	1	RO	<p>New Capability</p> <p>This bit indicates whether this function implements a list of extended capabilities such as PCI power management. This bit may be updated by EEPROM. When set this bit indicates the presence of New Capability. A value of 0 means that this function does not implement New Capability</p>
19:10	0	RO	Reserved
9	0	RO	<p>Master Mode Fast Back-To-Back (0 for No Support)</p> <p>The DM9102D does not support master mode fast back-to-back capability and will not generate fast back-to-back cycles</p>
8	0	RW	<p>SERR# Driver Enable/Disable</p> <p>This bit controls the assertion of SERR# signal output. The SERR# output will be asserted on detection of an address parity error and if both this bit and bit 6 are set</p>
7	0	RO	Address/Data Stepping (0 for No Stepping)
6	0	RW	<p>Parity Error Response Enable/Disable</p> <p>Setting this bit will enable the DM9102D to assert PERR# on the detection</p>

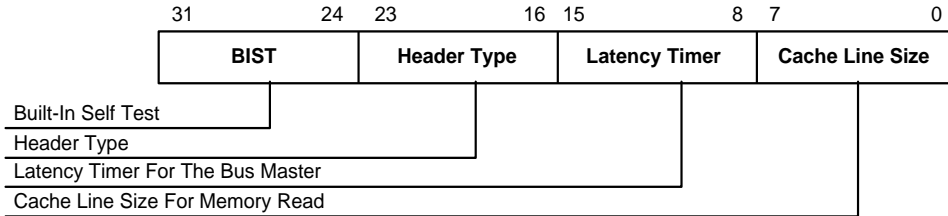
			of a data parity error and to assert SERR# for reporting address parity error
5	0	RO	VGA Palette Snooping (0 for No Support)
4	0	RO	Memory Write and Invalid (0 for No Implementation) The DM9102D only generates memory write cycle
3	0	RO	Special Cycles (0 for No Implementation)
2	1	RW	Master Device Capability Enable/Disable When this bit is set, DM9102D has the ability of master mode operation
1	1	RW	Memory Space Access Enable/Disable This bit controls the ability of memory space access. The memory access includes memory mapped I/O access and Boot ROM access. As the system boots up, this bit will be enabled by BIOS for Boot ROM memory access. While in normal operation, using memory mapped I/O access, this bit should be set by driver before memory access cycles
0	1	RW	I/O Space Access Enable/Disable This bit controls the ability of I/O space access. It will be set by BIOS after power on

6.1.3 Revision ID (xxxxxx08H - PCIRV)



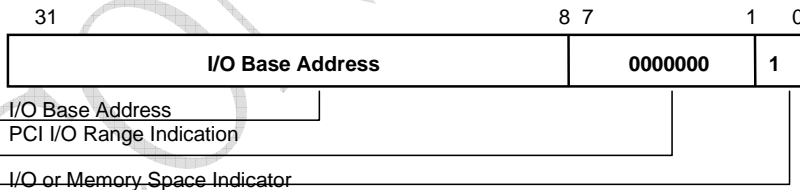
Bit	Default	Type	Description
31:8	020000H	RO	Class Code (020000H) This is the standard code for Ethernet LAN controller
7:4	0101	RO	Revision Major Number This is the silicon-major revision number that will increase for the subsequent versions of the DM9102D
3:0	0000	RO	Revision Minor Number This is the silicon-minor revision number that will increase for the subsequent versions of the DM9102D

6.1.4 Miscellaneous Function (xxxxxx0cH - PCILT)



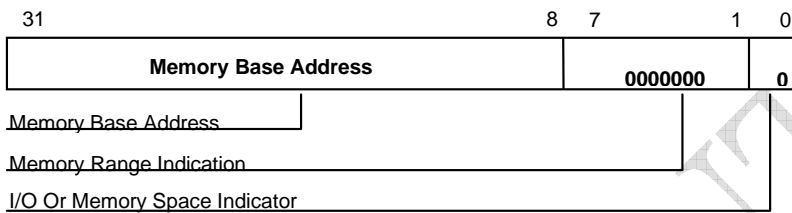
Bit	Default	Type	Description
31:24	00H	RO	Built In Self Test (00H means No Implementation)
23:16	00H	RO	Header Type (00H means single function with Predefined Header Type) If pin 75 IDSEL2 is pull-high, header type is 80H means multiple function is present.
15:8	00H	RW	Latency Timer For The Bus Master The latency timer is guaranteed by the system and measured by clock cycles. When the FRAME# is asserted at the beginning of a master period by the DM9102D, the value will be copied into a counter and start counting down. If the FRAME# is de-asserted prior to count expiration, this value is meaningless. When the count expires before GNT# is de-asserted, the master transaction will be terminated as soon as the GNT# is removed While GNT# signal is removed and the counter is non-zero, the DM9102D will continue with its data transfers until the count expires. The system host will read MIN_GNT and MAX_LAT registers to determine the latency requirement for the device and then initialize the latency timer with an appropriate value The reset value of Latency Timer is determined by BIOS
7:0	00H	RO	Cache Line Size For Memory Read Mode Selection (00H means No Implementation For Use)

6.1.5 I/O Base Address (xxxxxx10H - PCIIO)



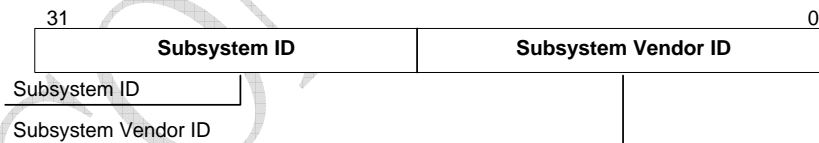
Bit	Default	Type	Description
31:7	Undefined	RW	PCI I/O Base Address This is the base address value for I/O accesses cycles. It will be compared to AD[31:7] in the address phase of bus command cycle for the I/O resource access
6:1	000000	RO	PCI I/O Range Indication It indicates that the minimum I/O resource size is 80h
0	1	RO	I/O Space Or Memory Space Base Indicator Determines that the register maps into the I/O space (= 1 Indicates I/O Base)

6.1.6 Memory Mapped Base Address (xxxxxx14H - PCIMEM)



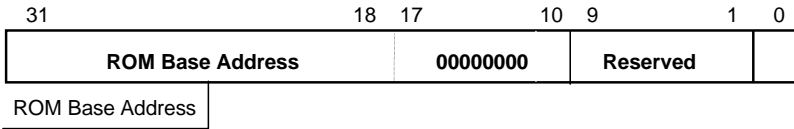
Bit	Default	Type	Description
31:7	Undefined	R/W	PCI Memory Base Address This is the base address value for memory accesses cycles. It will be compared to the AD [31:7] in the address phase of bus command cycle for the Memory resource access
6:1	000000	RO	PCI Memory Range Indication It indicates that the minimum memory resource size is 80h
0	0	RO	I/O Space Or Memory Space Base Indicator Determines that the register maps into the memory space(= 0 Indicates Memory Base)

6.1.7 Subsystem Identification (xxxxxx2cH - PCISID)



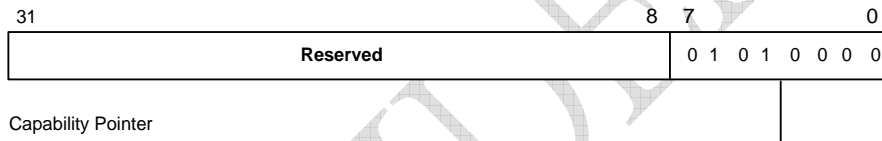
Bit	Default	Type	Description
31:16	XXXXH	RO	Subsystem ID It can be loaded from EEPROM word 1
15:0	XXXXH	RO	Subsystem Vendor ID It can be loaded from EEPROM word 0

6.1.8 Expansion ROM Base Address (xxxxxx30 - PCIROM)



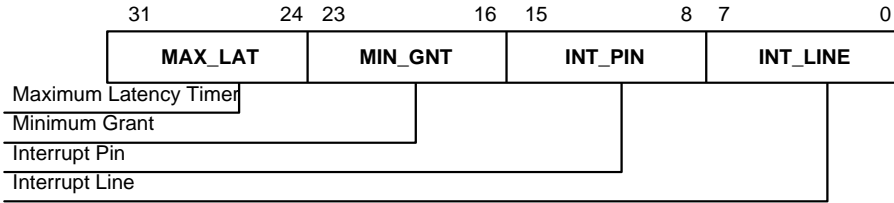
Bit	Default	Type	Description
31:10	00H	RW	ROM Base Address With 256K Boundary PCIROM bit17~10 are hardwired to 0, indicating ROM Size is up to 256K Size
9:1	000000000	RO	Reserved Bits Read As 0
0	0	RW	Expansion ROM Decoder Enable/Disable If this bit and the memory space access bit are both set to 1, the DM9102D will respond to its expansion ROM

6.1.9 Capabilities Pointer (xxxxxx34H - Cap_Ptr)



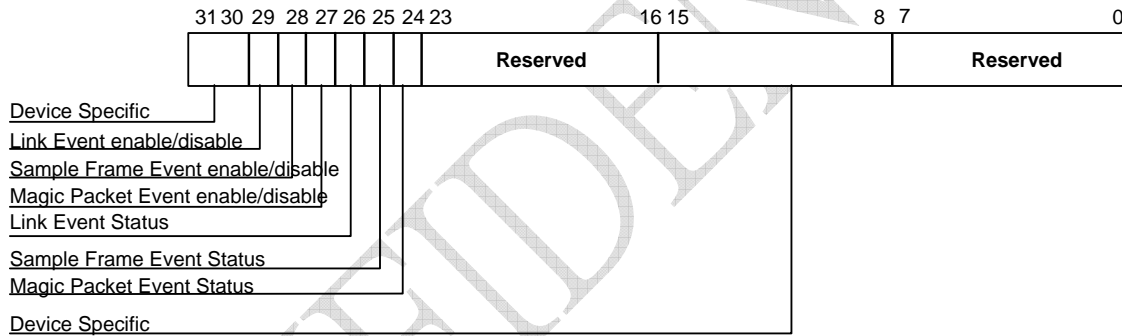
Bit	Default	Type	Description
31:8	000000H	RO	Reserved
7:0	01010000	RO	Capability Pointer The Cap_Ptr provides an offset (default is 50H) into the function's PCI Configuration Space for the location of the first term in the Capabilities Linked List. The Cap_Ptr offset is double word aligned so the two least significant bits are always "0"s

6.1.10 Interrupt & Latency Configuration (xxxxxx3cH - PCIINT)



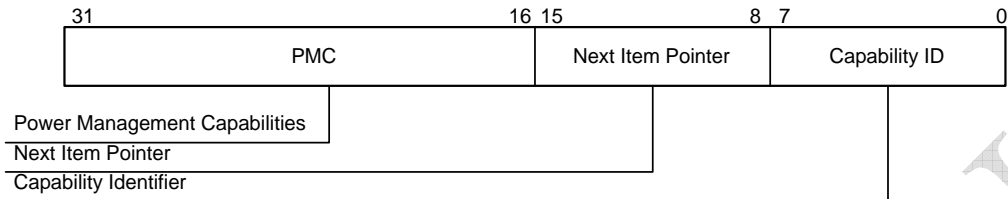
Bit	Default	Type	Description
31:24	28H	RO	Maximum Latency Timer that can be sustained.
23:16	14H	RO	Minimum Grant Minimum Length of a Burst Period.
15:8	01H	RO	Interrupt Pin read as 01H to indicate INTA#
7:0	XXH	RW	Interrupt Line that Is routed to the Interrupt Controller The value depends on system software.

6.1.11 Device Specific Configuration Register (xxxxxx40H- PCIUSR)



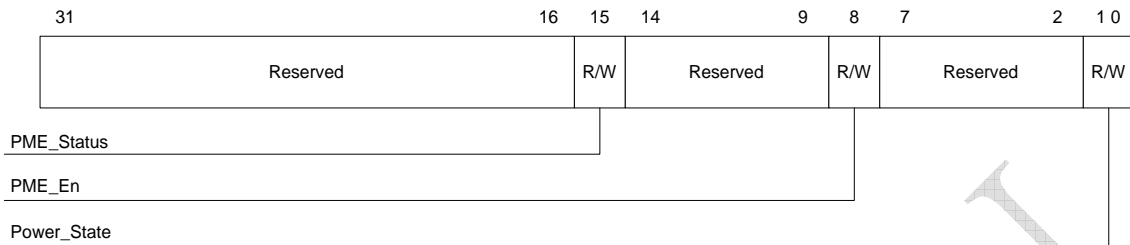
Bit	Default	Type	Description
31	0	RW	Device Specific Bit (sleep mode)
30	0	RW	Device Specific Bit (snooze mode)
29	0	RW	When set, enables Link Status Change Wake up Event
28	0	RW	When set, enables Sample Frame Wake up Event
27	0	RW	When set, enables Magic Packet Wake up Event
26	0	RO	When set, indicates the Link Change and the Link Status Change Event occurred
25	0	RO	When set, indicates the Sample Frame is received and the Sample Frame match Event occurred
24	0	RO	When set, indicates the Magic Packet is received and the Magic packet Event occurred
23:16	00H	RO	Reserved Bits Read As 0
15:8	00H	RW	Device Specific
7:0	00H	RO	Reserved Bits Read As 0

6.1.12 Power Management Register (xxxxxx50H-PCIPMR)



Bit	Default	Type	Description
31:27	11000	RO	<p>PME_Support</p> <p>This field indicates that the power states in which the function may assert PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PME# signal while in that power state</p> <p>bit27 → PME# support D0 bit28 → PME# support D1 bit29 → PME# support D2 bit30 → PME# support D3(hot) bit31 → PME# support D3(cold)</p> <p>DM9102D's bit31~27=11000 indicates PME# can be asserted from D3(hot) & D3(cold)</p> <p>These bits can be load from EEPROM word 7 bit [7:3]</p>
26:25	00	RO	<p>Reserved</p> <p>These two bits can be load from EEPROM word 7 bit [1:0]</p>
24:22	011	RO	<p>Aux_Current</p> <p>This field reports the 3.3Vaux auxiliary current requirement for the PCI function. The default value of this field is 011 means 160mA and it can be loaded from EEPROM word 4 bit [15:13] if EEPROM word 4 bit [9] is 1</p>
21	1	RO	<p>A "1" indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state</p> <p>This bit can be load from EEPROM word 7 bit [2]</p>
20	0	RO	Reserved
19	0	RO	<p>PME# Clock</p> <p>"0" indicates that no PCI clock is required for the function to generate PME#</p>
18:16	010	RO	<p>Version</p> <p>A default value of 010 indicates that this function complies with the Revision 1.1 of the PCI Power Management Interface Specification</p> <p>This value can be loaded from EEPROM word 4 bit [12:10] if EEPROM word 4 bit [9] is 1</p>
15:8	00H	RO	<p>Next Item Pointer</p> <p>The offset into the function's PCI Configuration Space pointing to the location of next item in the function's capability list is "00H"</p>
7:0	01H	RO	<p>Capability Identifier</p> <p>When "01H" indicates the linked list item as being the PCI Power Management Registers</p>

6.1.13 Power Management Control/Status (xxxxxx54H~PMCSR)



Bit	Default	Type	Description
31:16	0000H	RO	Reserved
15	0	R/W/C	<p>PME_Status</p> <p>This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit. Writing a “1” to this bit will clear it. This bit defaults to “0” if the function does not support PME# generation from D3 (cold). If the function supports PME# from D3 (cold) then this bit is sticky and must be explicitly cleared by the operating system whenever the operating system is initially loaded.</p>
14:9	000000	RO	<p>Reserved</p> <p>It means that the DM9102D does not support reporting power consumption.</p>
8	1	RW	<p>PME_En</p> <p>Write “1” to enables the function to assert PME#, write “0” to disable PME# assertion</p> <p>This bit defaults to “0” if the function does not support PME# generation from D3 (cold)</p> <p>If the function supports PME# from D3(cold) then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.</p>
7:2	000000	RO	Reserved
1:0	00	RW	<p>This two bits field is both used to determine the current power state of a function and to set the function into a new power state. The definitions given below</p> <p>00: D0</p> <p>11: D3 (hot)</p>

6.2 Control and Status Registers (CR)

The DM9102D implements 16 control and status registers, which can be accessed by the host. These CRs are double word aligned. All CRs are set to their default values by

hardware or software reset unless otherwise specified. All Control and Status Registers with their definitions and offset from IO or memory Base Address are shown below:

Register	Description	Offset from CSR Base Address	Default value after reset
CR0	System Control Register	00H	DE000000H
CR1	Transmit Descriptor Poll Demand	08H	FFFFFFFFH
CR2	Receive Descriptor Poll Demand	10H	FFFFFFFFH
CR3	Receive Descriptor Base Address Register	18H	00000000H
CR4	Transmit Descriptor Base Address Register	20H	00000000H
CR5	Network Status Report Register	28H	FC000000H
CR6	Network Operation Mode Register	30H	02040000H
CR7	Interrupt Mask Register	38H	FFFE0000H
CR8	Statistical Counter Register	40H	00000000H
CR9	External Management Access Register	48H	000083F0H
CR10	Reserved	50H	FFFFFFFFH
CR11	Reserved	58H	FFFE0000H
CR12	PHY Status Register	60H	FFFFFFXXH
CR13	Sample Frame Access Register	68H	XXXXXX00H
CR14	Sample Frame Data Register	70H	Unpredictable
CR15	Watchdog And Jabber Timer Register	78H	00000000H

Key to Default

In the register description that follows, the default column takes the form:

<Reset Value>, <Access Type>

Where :

<Reset Value>:

- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value

<Access Type>:

- RO = Read only
- RW = Read/Write
- RW/C = Read/Write and Clear
- WO = Write only
- RO/C = Read only and cleared after read.

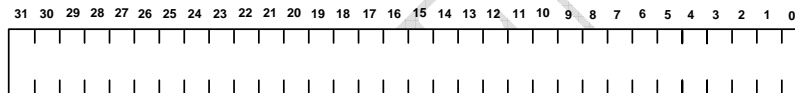
Reserved bits are shaded and should be written with 0.
Reserved bits are undefined on read access.

6.2.1 System Control Register (CR0)



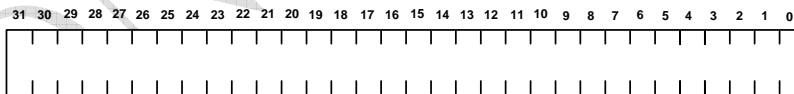
Bit	Name	Default	Description
31:24	Reserved	DEH,RO	Reserved
25:22	Reserved	00,RO	Reserved
21	MRM	0,RW	Memory Read Multiple When set, the DM9102D will use memory read multiple command (C/BE3~0 1100) when it initialize the memory read burst transaction as a master device When reset, it will use memory read command (C/BE3 ~ 0 = 0110) for the same master operation
20:1	Reserved	0,RO	Reserved
0	SR	0,RW	Software Reset When set, the DM9102D will make a internal reset cycle. All consequent action to DM9102D2 should wait at least 32 PCI clock cycles for its self-cleared.

6.2.2 Transmit Descriptor Poll Demand (CR1)



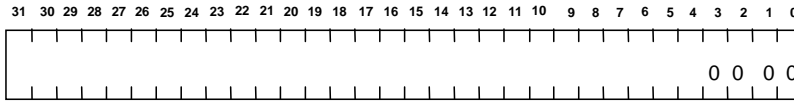
Bit	Name	Default	Description
31:0	TDP	FFFFFFFFH ,WO	Transmit Descriptor Polling Command Writing any value to this port will force DM9102D to poll the transmit descriptor. If the acting descriptor is not available, transmit process will return to suspend state. If the descriptor shows buffer available, transmit process will begin the data transfer.

6.2.3 Receive Descriptor Poll Demand (CR2)



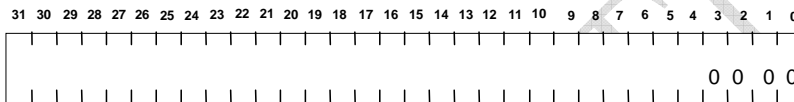
Bit	Name	Default	Description
31:0	RDP	FFFFFFFFH ,WO	Receive Descriptor Polling Command Writing any value to this port will force DM9102D to poll the receive descriptor. If the acting descriptor is not available, receive process will return to suspend state. If the descriptor shows buffer available, receive process will begin the data transfer.

6.2.4 Receive Descriptor Base Address (CR3)



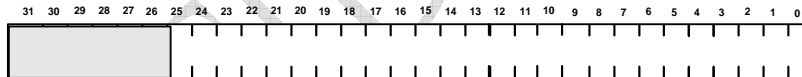
Bit	Name	Default	Description
31:0	RDBA	00000000H, RW	Receive Descriptor Base Address This register defines base address of receive descriptor-chain. The receive descriptor- polling command, after CR3 is set, will make DM9102D to fetch the descriptor at the Base-Address. This is a working register, so the value of reading is unpredictable.

6.2.5 Transmit Descriptor Base Address (CR4)



Bit	Name	Default	Description
31:0	TDBA	00000000H, RW	Transmit Descriptor Base Address This register defines base address of transmit descriptor-chain. The transmit descriptor- polling command after CR4 is set to make DM9102D fetch the descriptor at the Base-Address. This is a working register, so the value of reading is unpredictable.

6.2.6 Network Status Report Register (CR5)



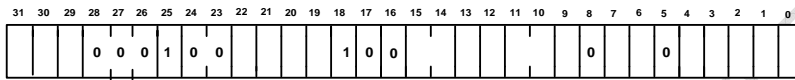
Note: Bits [13:0] can be cleared by written 1 to them respectively.

Bit	Name	Default	Description																								
31:26	Reserved	000000,RO	Reserved																								
25:23	SBEB	000,RO	System Bus Error Bits These bits are read only and used to indicate the type of system bus fatal error. Valid only when System Bus Error is set. The mapping bits are shown below <table border="1"> <thead> <tr> <th>Bit25</th> <th>Bit24</th> <th>Bit23</th> <th>Bus Error Type</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Parity error</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Master abort</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Slave abort</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>Reserved</td> </tr> </tbody> </table>	Bit25	Bit24	Bit23	Bus Error Type	0	0	0	Parity error	0	0	1	Master abort	0	1	0	Slave abort	0	1	1	Reserved	1	X	X	Reserved
Bit25	Bit24	Bit23	Bus Error Type																								
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0	0	1	Master abort																								
0	1	0	Slave abort																								
0	1	1	Reserved																								
1	X	X	Reserved																								
22:20	TXPS	000,RO	Transmit Process State These bits are read only and used to indicate the state of transmit process The mapping table is shown below <table border="1"> <thead> <tr> <th>Bit22</th> <th>Bit21</th> <th>Bit20</th> <th>Process State</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Transmit process stopped</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Fetch transmit descriptor</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Move Setup Frame from the host memory</td> </tr> </tbody> </table>	Bit22	Bit21	Bit20	Process State	0	0	0	Transmit process stopped	0	0	1	Fetch transmit descriptor	0	1	0	Move Setup Frame from the host memory								
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			<table> <tr><td>0</td><td>1</td><td>1</td><td>Move data from host memory to transmit FIFO</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>Close descriptor by clearing owner bit of descriptor</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>Waiting end of transmit</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>Transmit end and Close descriptor by writing status</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>Transmit process suspend</td></tr> </table>	0	1	1	Move data from host memory to transmit FIFO	1	0	0	Close descriptor by clearing owner bit of descriptor	1	0	1	Waiting end of transmit	1	1	0	Transmit end and Close descriptor by writing status	1	1	1	Transmit process suspend																
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1	1	1	Transmit process suspend																																				
19:17	RXPS	000,RO	<p>Receive Process State</p> <p>These bits are read only and used to indicate the state of receive process. The mapping table is shown below</p> <table> <thead> <tr> <th>Bit19</th> <th>Bit18</th> <th>Bit17</th> <th>Process State</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>Receive process stopped</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>Fetch receive descriptor</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>Wait for receive packet under buffer available</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>Move data from receive FIFO to host memory</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>Close descriptor by clearing owner bit of descriptor</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>Close descriptor by writing status</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>Receive process suspended due to buffer unavailable</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>Purge the current frame from received FIFO because of the unavailable received buffer</td></tr> </tbody> </table>	Bit19	Bit18	Bit17	Process State	0	0	0	Receive process stopped	0	0	1	Fetch receive descriptor	0	1	0	Wait for receive packet under buffer available	0	1	1	Move data from receive FIFO to host memory	1	0	0	Close descriptor by clearing owner bit of descriptor	1	0	1	Close descriptor by writing status	1	1	0	Receive process suspended due to buffer unavailable	1	1	1	Purge the current frame from received FIFO because of the unavailable received buffer
Bit19	Bit18	Bit17	Process State																																				
0	0	0	Receive process stopped																																				
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1	0	1	Close descriptor by writing status																																				
1	1	0	Receive process suspended due to buffer unavailable																																				
1	1	1	Purge the current frame from received FIFO because of the unavailable received buffer																																				
16	NIS	0,RW	<p>Normal Interrupt Summary</p> <p>Normal interrupt includes any of the three conditions: CR5<0> – TXCI: Transmit Complete Interrupt CR5<2> – TXDU: Transmit Buffer Unavailable CR5<6> – RXCI: Receive Complete Interrupt</p>																																				
15	AIS	0,RW	<p>Abnormal Interrupt Summary</p> <p>Abnormal interrupt includes any interrupt condition as shown below, excluding Normal Interrupt conditions. They are TXPS (bit1), TXJT (bit3), TXFU (bit5), RXDU (bit7), RXPS (bit8), RXWT (bit9), SBE (bit13).</p>																																				
14	Reserved	0,RO	Reserved																																				
13	SBE	0,RW	<p>System Bus Error</p> <p>The PCI system bus errors will set this bit. The type of system bus error is shown in CR5<25:23>.</p>																																				
12:10	Reserved	0,RO	Reserved																																				
9	RXWT	0,RW	<p>Receive Watchdog Timer Expired</p> <p>This bit is set to indicate that the receive watchdog timer has expired</p>																																				
8	RXPS	0,RW	<p>Receive Process Stopped</p> <p>This bit is set to indicate that the receive process enters the stopped state.</p>																																				
7	RXDU	0,RW	<p>Receive Buffer Unavailable</p> <p>This bit is set when the DM9102D fetches the next receive descriptor that is still owned by the host. Receive process will be suspended until a new frame enters or the receive polling command is set.</p>																																				
6	RXCI	0,RW	<p>Receive Complete Interrupt</p> <p>This bit is set when a received frame is fully moved into host memory and receive status has been written to descriptor. Receive process is still running and continues to fetch next descriptor.</p>																																				
5	TXFU	0,RW	<p>Transmit FIFO Underrun</p> <p>This bit is set when transmit FIFO has underrun condition during the packet transmission. It may happen due to the heavy load on bus, cause transmit buffer unavailable before end of packet. In this case, transmit process is placed in the suspend state and underrun error TDES0<1> is set.</p>																																				
4	Reserved	0,RO	Reserved																																				
3	TXJT	0,RW	<p>Transmit Jabber Expired</p> <p>This bit is set when the transmitted data is over 2048 byte</p>																																				

			Transmit process will be aborted and placed in the stop state. It also causes transmit jabber timeout TDES0<14> to assert.
2	TXDU	0,RW	Transmit Buffer Unavailable This bit is set when the DM9102D fetches the next transmit descriptor that is still owned by the host. Transmit process will be suspended until the transmission polling command is set.
1	TXPS	0,RW	Transmit Process Stopped This bit is set to indicate transmit process enters the stopped state.
0	TXCI	0,RW	Transmit Complete Interrupt This bit is set when a frame is fully transmitted and transmit status has been written to descriptor (the TDES1<31> is also asserted). Transmit process is still running and continues to fetch next descriptor.

6.2.7 Network Operation Mode Register (CR6)



Bit	Name	Default	Description
31	Reserved	0,RO	Must be Zero
30	RXA	0,RW	Receive All When set, all incoming packet will be received, regardless the destination address. The address match is checked according to the CR6<7>, CR6<6>, CR6<4>, CR6<2>, CR6<0>, and RDES0<30> will show this match
29	NPFIFO	0,RW	Set to not purge RX FIFO for test only if RX buffer unavailable.
28:26	Reserved	000,RO	Must be Zero
25	Reserved	1,RO	Must be One
24:23	Reserved	00,RO	Must be Zero
22	TXTM	1,RW	Transmit Threshold Mode When set, the transmit threshold mode is 10Mb/s. When reset, the threshold mode is 100Mb/s. This bit is used together with CR6<15:14> to decide the exact threshold level.
21	SFT	0,RW	Store and Forward Transmit When set, the packet transmission will be started after a full frame has been moved from the host memory to transmit FIFO. When reset, the packet transmission's start will depend on the threshold value specified in CR6<15:14>.
20	Reserved	0,RW	Reserved
19	Reserved	0,RW	Reserved
18	External MII_Mode	1,RW	In external MII mode, use this bit to enable or disable internal PHY See page 56 "7.8 External MII Interface" for details.
17	Reserved	0,RO	Reserved
16	1PKT	0,RW	One Packet Mode When this bit is set, only one packet is stored at TX FIFO

15:14	TSB	0,RW	<p>Threshold Bits</p> <p>These bits are set together with CR6 [22] and will decide the exact FIFO threshold level. The packet transmission will start after the data in the FIFO exceeds the threshold value.</p> <table border="1"> <thead> <tr> <th>Bit 22</th> <th>Bit15</th> <th>Bit14</th> <th>Threshold</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>128 bytes</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>256 bytes</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>512 bytes</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1024 bytes</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>64 bytes</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>128 bytes</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>192 bytes</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>256 bytes</td> </tr> </tbody> </table>	Bit 22	Bit15	Bit14	Threshold	0	0	0	128 bytes	0	0	1	256 bytes	0	1	0	512 bytes	0	1	1	1024 bytes	1	0	0	64 bytes	1	0	1	128 bytes	1	1	0	192 bytes	1	1	1	256 bytes
Bit 22	Bit15	Bit14	Threshold																																				
0	0	0	128 bytes																																				
0	0	1	256 bytes																																				
0	1	0	512 bytes																																				
0	1	1	1024 bytes																																				
1	0	0	64 bytes																																				
1	0	1	128 bytes																																				
1	1	0	192 bytes																																				
1	1	1	256 bytes																																				
13	TXSC	0,RW	<p>Transmit Start/Stop Command</p> <p>When set, the transmit process will begin by fetching the transmit descriptor for available packet data to be transmitted (running state). If the fetched descriptor is owned by the host, transmit process will enter the suspend state and transmit buffer unavailable (CR5<2>) is set. Otherwise it will begin to move data from host to FIFO and transmit out after reaching threshold value.</p> <p>When reset, the transmit process is placed in the stopped state after completing the transmission of the current frame.</p>																																				
12	FCM	0,RW	<p>Force Collision Mode</p> <p>When set, the transmission process is forced to be the collision status. Meaningful only in the internal loop-back mode.</p>																																				
11:10	LBM	0,RW	<p>Loop-back Mode</p> <p>These bits decide two loop-back modes, MAC and PHY, besides normal operation. These loop-back modes expect transmitted data back to receive path and ignore collision detection.</p> <table border="1"> <thead> <tr> <th>Bit11</th> <th>Bit10</th> <th>Loop-back Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Normal</td> </tr> <tr> <td>0</td> <td>1</td> <td>Internal loop-back</td> </tr> <tr> <td>1</td> <td>0</td> <td>Internal PHY digital loop-back</td> </tr> <tr> <td>1</td> <td>1</td> <td>Internal PHY analog loop-back</td> </tr> </tbody> </table>	Bit11	Bit10	Loop-back Mode	0	0	Normal	0	1	Internal loop-back	1	0	Internal PHY digital loop-back	1	1	Internal PHY analog loop-back																					
Bit11	Bit10	Loop-back Mode																																					
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0	1	Internal loop-back																																					
1	0	Internal PHY digital loop-back																																					
1	1	Internal PHY analog loop-back																																					
9	FDM	0,RW	<p>Full-duplex Mode</p> <p>When internal PHY is selected, this bit is the status of full-duplex mode of internal PHY.</p> <p>When external PHY is selected, set this bit to make the MAC of the DM9102D operate in the full-duplex mode.</p>																																				
8	Reserved	0,RO	Must be Zero																																				
7	PAM	0,RW	<p>Pass All Multicast</p> <p>When set, any packet with a multicast destination address is received by the DM9102D. The packet with a physical address will also be filtered based on the filter mode setting</p>																																				
6	PM	0,RW	<p>Promiscuous Mode</p> <p>When set, any incoming valid frame is received by the DM9102D, and no matter what the destination address is. The DM9102D is initialized to this mode after reset operation.</p>																																				
5	Reserved	0,RO	Must be Zero																																				

4	IAFM	0,RO	Inverse Address Filtering Mode It is set to indicate the DM9102D operate in Inverse filtering mode. This is a read only bit and decoded from the setup frame of TDES1 bit 28 and bit 22.
3	PBF	0,RW	Pass Bad Frame When set, the DM9102 is indicated that receiving the bad frames, including runt packets and truncated frames, is caused by the FIFO overflow. The bad frame also has to pass the address filtering if the DM9102D is not set in promiscuous mode.
2	HOFM	0,RO	Hash-only Filter Mode It is set to indicate the DM9102D operate in Hash-only filtering mode. This is a read only bit and decoded from the setup frame of TDES1 bit 28 and bit 22.
1	RXRC	0,RW	Receive Start/Stop Command When set, receive process will begin by fetching the receive descriptor for available buffer to store the new-coming packet (placed in the running state). If the fetched descriptor is owned by the host (no descriptor is owned by the DM9102D), the receive process will enter the suspend state and receive buffer unavailable CR5<7> sets. Otherwise it runs to wait for the packet's incoming. When reset, receive process is placed in the stopped state after completing the reception of the current frame.
0	HPFM	0,RO	Hash/Perfect Filter Mode It is set to indicate the DM9102D operate in Hash-only or Hash filtering mode and it is cleared to indicate the DM9102D operate in Perfect filtering mode. This is a read only bit and decoded from the setup frame of TDES1 bit 28 and bit 22.

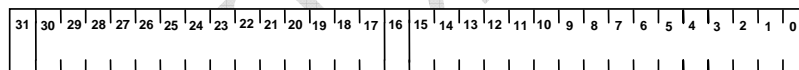
6.2.8 Interrupt Mask Register (CR7)



Bit	Name	Default	Description
16	NISE	0,RW	Normal Interrupt Summary Enable This bit is set to enable the interrupt for Normal Interrupt Summary. Normal interrupt includes three conditions: CR5<0> – TXCI: Transmit Complete Interrupt CR5<2> – TXDU: Transmit Buffer Unavailable CR5<6> – RXCI: Receive Complete Interrupt
15	AISE	0,RW	Abnormal Interrupt Summary Enable This bit is set to enable the interrupt for Abnormal Interrupt Summary. Abnormal interrupt includes all interrupt conditions as shown below, excluding Normal Interrupt conditions. They are TXPS(bit1), TXJT(bit3), TXFU(bit5), RXDU(bit7), RXPS(bit8), RXWT(bit9), SBE(bit13).
14	Reserved	0,RO	Reserved
13	SBEE	0,RW	System Bus Error Enable When set together with CR7<15>, CR5<13>, it enables the interrupt for System Bus Error. The type of system bus error is shown in CR5<24:23>.
12:10	Reserved	0,RO	Reserved
9	RXWTE	0,RW	Receive Watchdog Timer Expired Enable When this bit and CR7<15>, (CR5<9>) are set together, it enable the interrupt of the condition of the receive watchdog timer expired.

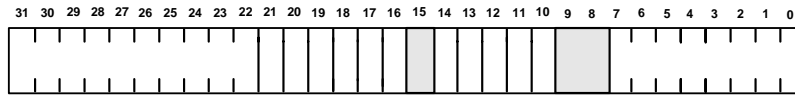
8	RXPSE	0,RW	Receive Process Stopped Enable When set together with CR7<15> and CR5<8>. This bit is set to enable the interrupt of receive process stopped condition.
7	RXDUE	0,RW	Receive Buffer Unavailable Enable When this bit and CR7<15>, CR5<7> are set together, it will enable the interrupt of receive buffer unavailable condition.
6	RXCIE	0,RW	Receive Complete Interrupt Enable When this bit and CR7<16>, CR5<6> are set together, it will enable the interrupt of receive process complete condition.
5	TXFUE	0,RW	Transmit FIFO Underrun Enable When set together with CR7<15>, CR5<5>, it will enable the interrupt of transmit FIFO underrun condition.
4	Reserved	0,RO	Reserved
3	TXJTE	0,RW	Transmit Jabber Expired Enable When this bit and CR7<15>, CR5<3> are set together, it enables the interrupt of transmit Jabber Timer Expired condition.
2	TXDUE	0,RW	Transmit Buffer Unavailable Enable When this bit and CR7<16>, CR5<2> are set together, the interrupt of transmit buffer unavailable is enabled.
1	TXPSE	0,RW	Transmit Process Stopped Enable When this bit is set together with CR7<15> and CR5<1>, it will enable the interrupt of the transmit process to stop.
0	TXCIE	0,RW	Transmit Complete Interrupt Enable When this bit and CR7<16>, CR5<0> are set, the transmit interrupt is enabled.

6.2.9 Statistical Counter Register (CR8)



Bit	Name	Default	Description
31	ROCO	0,RO/C	Receive Overflow Counter Overflow This bit is set when the Purged Packet Counter (RXDU) has an overflow condition.
30:25	Reserved	0,RO	Reserved
24:17	RXDU	0,RO/C	Receive Purged Packet Counter This is a statistic counter to indicate the purged received packet counts upon FIFO overflow.
16	RXPS	0,RO/C	Receive Missed Counter Overflow This bit is set when the Receive Missed Frame Counter (RXCI) has an overflow condition.
15:7	Reserved	0,RO	Reserved
6:0	RXCI	0,RO/C	Receive Missed Frame Counter This is a statistic counter to indicate the Receive Missed Frame Count when there is a host buffer unavailable condition for receive process.

6.2.10 Management Access Register (CR9)



Bit	Name	Default	Description
31	MDIX	0,RO	Status of disable auto-MDIX function
30	MFUN	0,RO	Multi-function strap pin status
29	LEDM	0,RO	LED mode strap pin status
28:27	Reserved	0,RO	Reserved
26	FDX	X,RO	Full-duplex status of internal PHY.
25	LNK100	X,RO	100M link status of internal PHY.
24	LNK10	X,RO	10M link status of internal PHY
23	RSTPHY	0,RW	PHY Reset Write 1 to this bit will reset internal PHY.
22	Reserved	0,RO	Reserved
21	LES	0,RO	Load EEPROM status It is set to indicate the load of EEPROM is in progress.
20	RLM	0,RW	Reload EEPROM Set to reload the content of EEPROM.
19	MDIN	0,RO	MII Management Data_In This is a read-only bit to indicate the MDIO input data, when bit 18 MRW is set.
18	MRW	0,RW	MII Management Read/Write Mode Selection This bit defines the Read/Write Mode for PHY MII management register access. 1 for read and 0 for write.
17	MDOUT	0,RW	MII Management Data_Out This bit is used to generate the output data signal for PHY MII management register access.
16	MDCLK	0,RW	MII Management Clock This bit is used to generate the output clock signal for PHY MII management register access.
15:12	Reserved	1000,RO	Reserved.
11	ERS	0,RW	EEPROM Selected This bit is used to enable EEPROM access.
10:8	Reserved	011,RW	Reserved
7:4	Reserved	FH,RO	Reserved
3	CRDOUT	0,RW	Data_Out from EEPROM This bit reflects the status of EEDI pin when the EEPROM access is enabled.
2	CRDIN	0,RW	Data_In to EEPROM This bit maps to EEDO pin when the EEPROM access is enabled.
1	CRCLK	0,RW	Clock to EEPROM This bit maps to EECK pin when the EEPROM access is enabled
0	CRCS	0,RW	Chip_Select to EEPROM This bit maps to EECS pin when the EEPROM access is enabled

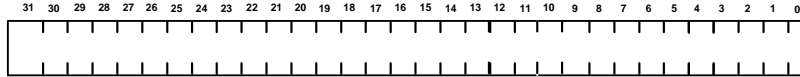
6.2.11 PHY Status Register (CR12)



Bit	Name	Default	Description
31:9	Reserved	FFFFFFH, RO	Reserved
8:4	Reserved	0,RO	Reserved
3:0	PHYST	XXXX ,RW	PHY Status bit 3:Internal PHY Link status (the same as bit2 of PHY Register) bit 2:Full-duplex bit 1:Speed 100Mbps link bit 0:Speed 10Mbps link

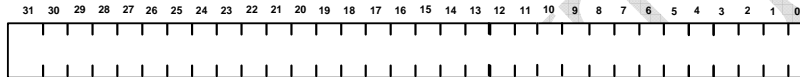
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6.2.12 Sample Frame Access Register (CR13) (reference to section 7.5 Power Management)

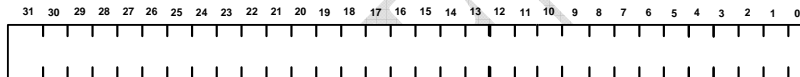


Register	General definition	bit8 ~ 3	R/W
TxFIFO	Transmit FIFO access port	32H	R/W
RxFIFO	Receive FIFO access port	35H	R/W
DiagReset	General reset for diagnostic pointer port	38H	W

6.2.13 Sample Frame Data Register (CR14) (reference to section 7.5 Power Management)



6.2.14 Watchdog and Jabber Timer Register (CR15)



Bit	Name	Default	Description
31	TXSUMC	0,WO	in transmit, generate IP/TCP/UDP chksum depend-on TX desc. control
30	IPSUM	0,WO	in transmit, generate IP chksum to all packets
29	TCPSUM	0,WO	in transmit, generate TCP chksum to all packets
28	UDPSUM	0,WO	in transmit, generate UDP chksum to all packets
27	RXSUM	0,WO	In receiving, report IP/TCP/UDP checksum status to RDES0
26:15	Reserved	0,RO	Reserved
14	TXP0	0,RW	Transmit pause packet Set to transmit pause packet with pause timer = 0000h, this bit will be cleared if the pause packet had transmitted.
13	TXPF	0,RW	Transmit pause packet Set to transmit pause packet with pause timer = FFFFh, this bit will be cleared if the pause packet had transmitted.
12:11	Reserved	0,RO	Reserved
10	FLCE	0,RW	Flow Control Enable Set to enable the decode of the pause packet.
9	RXPS	0,R/C	The latched status of the decode of the pause packet.
8	Reserved	0,RO	Reserved.
7	RXPCS	0,RO	It is set to indicate that the current pause timer of pause packet is not down count to zero yet.
6	VLAN	0,RW	VLAN length Capability Enable It is set to enable the VLAN length mode and will not report the frame_too_long bit status to RDES0 if receive packet size under 1526-byte.

5	Reserved	0,RO	Reserved
4	TWDE	0,RW	Watchdog Timer Disable When set, the Watchdog Timer is disabled. Otherwise it is enabled.
3:1	Reserved	0,RO	Reserved
0	TJE	0,RW	Transmit Jabber Disable When set, the transmit Jabber is disabled. Otherwise it is enabled.

6.3 PHY Management Register Set

Offset	Register Name	Description	Default value after reset
0	BMCR	Basic Mode Control Register	3100H
1	BMSR	Basic Mode Status Register	7849H
2	PHYIDR1	PHY Identifier Register #1	0181H
3	PHYIDR2	PHY Identifier Register #2	B8A0H
4	ANAR	Auto-Negotiation Advertisement Register	01E1H
5	ANLPAR	Auto-Negotiation Link Partner Ability Register	0000H
6	ANER	Auto-Negotiation Expansion Register	0000H
7-15	Reserved	Reserved	0000H
10H	DSCR	DAVICOM Specified Configuration Register	0414H
11H	DSCSR	DAVICOM Specified Configuration/Status Register	F210H
12H	10BTCSR	10BASE-T Configuration/Status Register	7800H
13H	PWDOR	Power Down Control Register	0000H
14H	MDIX	Auto-MDI/MDIX Control Register	0000H
Others	Reserved	Reserved for future use, do not read/write to these Registers	0000H

Key to Default

In the register description that follows, the default column takes the form:

<Reset Value>, <Access Type> / <Attribute(s)>

Where :

<Reset Value>:

- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value
- (PIN#) Value latched in from pin # at reset

<Access Type>:

- RO = Read only
- RW = Read/Write
- RC = cleared after read

<Attribute (s)>:

- SC = Self clearing
- P = Value permanently set
- LL = Latching low
- LH = Latching high

6.3.1 Basic Mode Control Register (BMCR) – 0

Bit	Name	Default	Description
15	Reset	0, RW/SC	Reset: 1=Software reset 0=Normal operation This bit resets the status and controls the PHY registers of the DM9102D to their default states. This bit, which is self-clearing, will keep its value until the reset process is completed
14	Loopback	0, RW	Loopback: 1=Loop-back enabled 0=Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data to the MAC.
13	Speed Selection	1, RW	Speed Select: 1=100Mbps 0=10Mbps Link speed may be selected either by this bit or by Auto-negotiation. When Auto-negotiation is enabled and bit 12 is set, this bit will reflect Auto-negotiation selected media type.
12	Auto-negotiation Enable	1, RW	Auto-negotiation Enable: 1= Auto-negotiation enabled: bit 8 and 13 will report Auto-negotiation status 0= Auto-negotiation disabled: bit 8 and 13 will determine the link speed and duplex mode
11	Power Down	0, RW	Power Down: Setting this bit will power down the internal PHY except crystal / oscillator circuit. 1=Power Down 0=Normal Operation
10	Reserved	0,RO	Reserved. Write as 0, ignore on read.
9	Restart Auto-negotiation	0,RW/SC	Restart Auto-negotiation: 1= Restart Auto-negotiation. Re-initiates the Auto-negotiation process. When Auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep its value until Auto-negotiation is initiated by the DM9102D. The operation of the Auto-negotiation process will not be affected by the management entity that clears this bit. 0= Normal Operation
8	Duplex Mode	1,RW	Duplex Mode: 1= Full Duplex operation. Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With Auto-negotiation enabled, this bit reflects the duplex capability selected by Auto-negotiation. 0= Normal operation
7	Collision Test	0,RW	Collision Test: 1= Collision Test enabled. When set in half duplex mode, the DM9102D will enter collision state if packet transmission is in progress. 0= Normal Operation
6:0	Reserved	<0000000>, RO	Reserved. Write as 0, ignore on read

6.3.2 Basic Mode Status Register (BMSR) – 1

Bit	Name	Default	Description
15	100BASE-T4	0,RO/P	100BASE-T4 Capable: 1=DM9102D is able to perform in 100BASE-T4 mode. 0=DM9102D is not able to perform in 100BASE-T4 mode.
14	100BASE-TX Full Duplex	1,RO/P	100BASE-TX FULL DUPLEX CAPABLE: 1= DM9102D is able to perform 100BASE-TX in Full Duplex mode. 0= DM9102D is not able to perform 100BASE-TX in Full Duplex mode.
13	100BASE-TX Half Duplex	1,RO/P	100BASE-TX Half Duplex Capable: 1=DM9102D is able to perform 100BASE-TX in Half Duplex mode. 0=DM9102D is not able to perform 100BASE-TX in Half Duplex mode.
12	10BASE-T Full Duplex	1,RO/P	10BASE-T Full Duplex Capable: 1=DM9102D is able to perform 10BASE-T in Full Duplex mode. 0=DM9102D is not able to perform 10BASE-T in Full Duplex mode.
11	10BASE-T Half Duplex	1,RO/P	10BASE-T Half Duplex Capable: 1=DM9102D is able to perform 10BASE-T in Half Duplex mode. 0=DM9102D is not able to perform 10BASE-T in Half Duplex mode .
10:7	Reserved	0000,RO	Reserved: Write as 0, ignore on read
6	MF Preamble Suppression	1,RW	MII Frame Preamble Suppression: 1=PHY will accept management frames with preamble suppressed. 0=PHY will not accept management frames with preamble suppressed.
5	Auto-negotiation Complete	0,RO	Auto-negotiation Complete: 1=Auto-negotiation process is completed. 0=Auto-negotiation process is not completed.
4	Remote Fault	0,RC/LH	Remote Fault: 1= Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM9102D specific implementation. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0= No remote fault condition detected
3	Auto-negotiation Ability	1,RO/P	Auto Configuration Ability: 1=DM9102D is able to perform Auto-negotiation 0=DM9102D is not able to perform Auto-negotiation
2	Link Status	0,RC/LL	Link Status: 1=Valid link established (for either 10Mbps or 100Mbps operation) 0=Link not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the Link Status bit to be cleared and remain cleared until it is read via the management interface
1	Jabber Detect	0,RC/LH	Jabber Detect: 1=Jabber condition detected 0=No jabber This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a DM9102D reset. This bit works only in 10Mbps mode
0	Extended Capability	1,RO/P	Extended Capability: 1=Extended register capability 0=Basic register capability only

6.3.3 PHY Identifier Register #1 (PHYIDR1) – 2

The PHY Identifier Register#1 and Register#2 work together in a single identifier of the DM9102D. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Name	Default	Description
15:0	OUI_MSB	<0181H>, RO/P	OUI Most Significant Bits: This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

6.3.4 PHY Identifier Register #2 (PHYIDR2) - 3

Bit	Name	Default	Description
15:10	OUI_LSB	<101110>, RO/P	OUI Least Significant Bits: Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
9:4	VNDR_MDL	<001010>, RO/P	Vendor Model Number: Six bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3:0	MDL_REV	<0000>, RO/P	Model Revision Number: Four bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 3)

6.3.5 Auto-negotiation Advertisement Register (ANAR) – 4

This register contains the advertised abilities of this DM9102D device as they will be transmitted to its link partner during Auto-negotiation.

Bit	Name	Default	Description
15	NP	0,RO/P	Next Page Indication: 0=No next page available 1=Next page available The DM9102D has no next page, so this bit is permanently set to 0
14	ACK	0,RO	Acknowledge: 1=Link partner ability data reception acknowledged 0=Not acknowledged The DM9102D's Auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the Auto-negotiation process. Software should not attempt to write to this bit.
13	RF	0, RW	Remote Fault: 1=Local Device senses a fault condition 0=No fault detected
12:11	Reserved	00, RW	Reserved: Write as 0, ignore on read
10	FCS	0, RW	Flow Control Support: 1=Controller chip supports flow control ability. 0=Controller chip doesn't support flow control ability.
9	T4	0, RW	100BASE-T4 Support: 1=100BASE-T4 is supported by the local device. 0=100BASE-T4 is not supported. The DM9102D does not support 100BASE-T4 so this bit is 0 permanently
8	TX_FDX	1, RW	100BASE-TX Full Duplex Support: 1=100BASE-TX Full Duplex is supported by the local device. 0=100BASE-TX Full Duplex is not supported.

7	TX_HDX	1, RW	100BASE-TX Support: 1=100BASE-TX is supported by the local device. 0=100BASE-TX is not supported.
6	10_FDX	1, RW	10BASE-T Full Duplex Support: 1=10BASE-T Full Duplex is supported by the local device. 0=10BASE-T Full Duplex is not supported.
5	10_HDX	1, RW	10BASE-T Support: 1=10BASE-T is supported by the local device. 0=10BASE-T is not supported.
4:0	Selector	<00001>, RW	Protocol Selection Bits: These bits contain the binary encoded protocol selector supported by this node. <00001> indicates that this device supports IEEE 802.3 CSMA/CD.

6.3.6 Auto-negotiation Link Partner Ability Register (ANLPAR) – 5

This register contains the advertised abilities of the link partner when received during Auto-negotiation.

Bit	Name	Default	Description
15	NP	0, RO	Next Page Indication: 1= Link partner, next page available 0= Link partner, no next page available
14	ACK	0, RO	Acknowledge: 1=Link partner ability data reception acknowledged 0=Not acknowledged The DM9102D's Auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit.
13	RF	0, RO	Remote Fault: 1=Remote fault is indicated by link partner. 0=No remote fault is indicated by link partner.
12:10	Reserved	000, RO	Reserved: Write as 0, ignore on read
9	T4	0, RO	100BASE-T4 Support: 1=100BASE-T4 is supported by the link partner. 0=100BASE-T4 is not supported by the link partner.
8	TX_FDX	0, RO	100BASE-TX Full Duplex Support: 1=100BASE-TX Full Duplex is supported by the link partner. 0=100BASE-TX Full Duplex is not supported by the link partner.
7	TX_HDX	0, RO	100BASE-TX Support: 1=100BASE-TX Half Duplex is supported by the link partner. 0=100BASE-TX Half Duplex is not supported by the link partner.
6	10_FDX	0, RO	10BASE-T Full Duplex Support: 1=10BASE-T Full Duplex is supported by the link partner. 0=10BASE-T Full Duplex is not supported by the link partner.
5	10_HDX	0, RO	10BASE-T Support: 1=10BASE-T Half Duplex is supported by the link partner. 0=10BASE-T Half Duplex is not supported by the link partner.
4:0	Selector	<00000>, RO	Protocol Selection Bits: Link partner's binary encoded protocol selector

6.3.7 Auto-negotiation Expansion Register (ANER) – 6

Bit	Name	Default	Description
15:5	Reserved	0, RO	Reserved:

			Write as 0, ignore on read
4	PDF	0, RO/LH	Local Device Parallel Detection Fault: PDF=1: A fault detected via parallel detection function. PDF=0: No fault detected via parallel detection function
3	LP_NP_ABLE	0, RO	Link Partner Next Page Able: LP_NP_ABLE=1: Link partner, next page available LP_NP_ABLE=0: Link partner, no next page
2	NP_ABLE	0,RO/P	Local Device Next Page Able: NP_ABLE=1: DM9102D, next page available NP_ABLE=0: DM9102D, no next page DM9102D does not support this function, so this bit is always 0.
1	PAGE_RX	0, RC/LH	New Page Received: A new link of code-word page received. This bit will be automatically cleared when the register (Register 6) is read by management.
0	LP_AN_ABLE	0, RO	Link Partner Auto-negotiation Able: A "1" in this bit indicates that the link partner supports Auto-negotiation.

6.3.8 DAVICOM Specified Configuration Register (DSCR) – 10H

Bit	Name	Default	Description
15	BP_4B5B	0,RW	Bypass 4B5B Encoding and 5B4B Decoding 1 = 4B5B encoder and 5B4B decoder function bypassed 0 = Normal 4B5B and 5B4B operation
14	BP_SCR	0, RW	Bypass Scrambler/Descrambler Function 1 = Scrambler and descrambler function bypassed 0 = Normal scrambler and descrambler operation
13	BP_ALIGN	0, RW	Bypass Symbol Alignment Function 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0 = Normal operation
12:11	Reserved	0, RW	Reserved
10	Reserved	1, RW	Reserved
9:8	Reserved	0, RW	Reserved
7	F_LINK_100	0, RW	Force Good Link in 100Mbps: 1 = Force 100Mbps good link status 0 = Normal 100Mbps operation This bit is useful for diagnostic purposes.
6:5	Reserved	00,RW	Reserved
4	RPDCTR_EN	1,RW	Reduced Power Down Control Mode: This bit is used to enable automatic reduced power down 1 = Enable automatic reduced power down 0 = Disable automatic reduced power down
3	SMRST	0,RC	Reset State Machine: When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed.
2	MFPSC	1,RW	MF Preamble Suppression Control: MII frame preamble suppression control bit 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off

1	SLEEP	0,RW	Sleep Mode: Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset.
0	RLOUT	0,RW	Remote Loop out Control: When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for testing bit error rate.

6.3.9 DAVICOM Specified Configuration and Status Register (DSCSR) – 11H

Bit	Name	Default	Description
15	100FDX	1, RO	100M Full Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation mode is a 100Mbps Full Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
14	100HDX	1, RO	100M Half Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation mode is a 100Mbps Half Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
13	10FDX	1, RO	10M Full Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation mode is a 10Mbps Full Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
12	10HDX	1, RO	10M Half Duplex Operation Mode: After Auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation mode is a 10Mbps Half Duplex mode. The software can read bit[15:12] to see which mode is selected after Auto-negotiation. This bit is invalid when it is not in the Auto-negotiation mode.
11:10	Reserved	00, RO	Reserved:
9	Reserved	1, RW	Reserved: Write as 0, ignore on read
8:4	PHYAD[4:0]	00001, RW	PHY Address Bit 4:0
3:0	ANMB[3:0]	0000, RO	Auto-negotiation Monitor Bits: These bits are for debug only. The Auto-negotiation status will be written to these bits.

			b3	b2	b1	b0	
			0	0	0	0	In IDLE state
			0	0	0	0	Ability match
			0	0	1	0	Acknowledge match
			0	0	1	1	Acknowledge match fail
			0	1	0	0	Consistency match
			0	1	0	1	Consistency match fail
			0	1	1	0	Parallel detects signal_link_ready
			0	1	1	1	Parallel detects signal_link_ready fail
			1	0	0	0	Auto-negotiation completed successfully

6.3.10 10BASE-T Configuration/Status (10BTCRCSR) – 12H

Bit	Name	Default	Description
15	Reserved	0, RO	Reserved: Write as 0, ignore on read
14	LP_EN	1, RW	Link Pulse Enable: 1=Transmission of link pulses enabled 0=Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation.
13	HBE	1,RW	Heartbeat Enable: 1=Heartbeat function enabled 0=Heartbeat function disabled When the DM9102D is configured for Full Duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in Full Duplex mode). It must set to be 1.
12	SQUELCH	1, RW	Squelch Enable 1 = normal squelch 0 = low squelch
11	JABEN	1, RW	Jabber Enable: Enables or disables the Jabber function when the DM9102D is in 10BASE-T Full Duplex or 10BASE-T Transceiver Loopback mode 1= Jabber function enabled 0= Jabber function disabled
10	Reserved	0,RW	Reserved
9:2	Reserved	0, RO	Reserved
1	Reserved	1,RW	Reserved
0	POLR	0, RO	Polarity Reversed When this bit is set to 1, it indicates that the 10Mbps cable polarity is reversed.

6.3.11 Power Down Control Register (PWDOR) – 13H

Bit	Bit Name	Default	Description
15:9	Reserved	0, RO	Reserved Read as 0, ignore on write
8	PD10DRV	0, RW	Vendor powerdown control test
7	PD100DL	0, RW	Vendor powerdown control test
6	PDchip	0, RW	Vendor powerdown control test
5	PDcom	0, RW	Vendor powerdown control test
4	PDaeq	0, RW	Vendor powerdown control test
3	PDdrv	0, RW	Vendor powerdown control test
2	PDedi	0, RW	Vendor powerdown control test
1	PDedo	0, RW	Vendor powerdown control test
0	PD10	0, RW	Vendor powerdown control test

* when selected , the powerdown value is control by Register 20.0

6.3.12 Auot-MDI/MDIX Control Register – 14H

Bit	Bit Name	Default	Description
15:13	Reserved	0,RW	Reserved
11:8	Reserved	0, RO	Reserved Read as 0, ignore on write
7	MDIX_CNTL	MDI/MDIX,RO	The polarity of MDI/MDIX value 1: MDIX mode 0: MDI mode
6	AutoNeg_dpbk	0,RW	Auto-negotiation loopback 1: test internal digital auto-negotiation loopback 0: normal.
5	Mdix_fix Value	0, RW	MDIX_CNTL force value: When MDIX_DOWN = 1, MDIX_CNTL value depend on the register value.
4	Mdix_down	0,RW	MDIX Down Manual force MDI/MDIX. 0: Enable auto MDI/MDIX 1: Disable auto MDI/MDIX, MDIX_CNTL value depend on bit 5.
3:1	Reserved	0,RW	Reserved
0	PD_value	0,RW	Powerdown control value Decide the value of each field Register 13H. 1: powerdown 0: normal

7. Functional Description

7.1 System Buffer Management

7.1.1 Overview

The data buffers for reception and the transmission of data reside in the host memory. They are addressed by the descriptor list that is also located in another region of the host memory. All actions for the buffer management are operated by the DM9102D in conjunction with the software driver. The data structures and processing algorithms are described in the following text.

7.1.2 Data Structure and Descriptor List

There are two types of buffers that reside in the host memory, the transmit buffer and the receive buffer. The buffers are composed of many distributed regions in the host memory. They are linked together and controlled by the descriptor lists that reside in another region of the host

memory. The descriptor list is a chain structure. The content of each descriptor includes pointer to the buffer, size of the buffer, command and status for the packet to be transmitted or received. Each descriptor list starts from the address setting of CR3 (receive descriptor base address) and CR4 (transmit descriptor base address). Refer to Figure 7-1.

7.1.3 Buffer Management – Chain Structure Method

As the Chain structure depicted below, each descriptor contains two pointers, one point to a single buffer and the other to the next descriptor chained. The first descriptor is chained to the last descriptor under host driver's control to form a looped chain. With this structure, a descriptor can be allocated anywhere in host memory and is chained to the next descriptor.

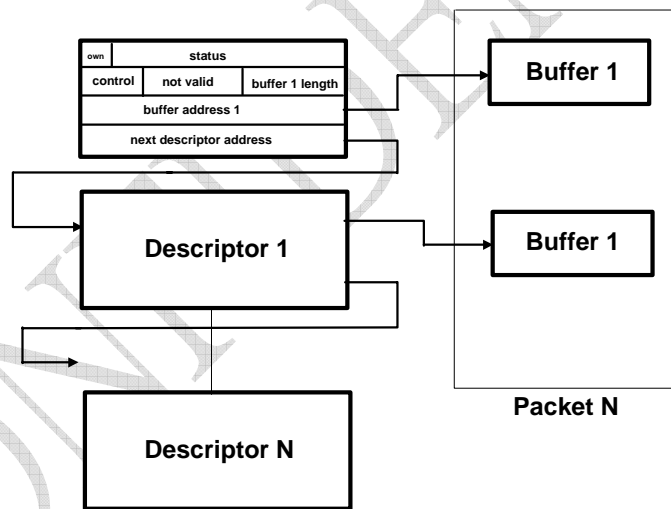


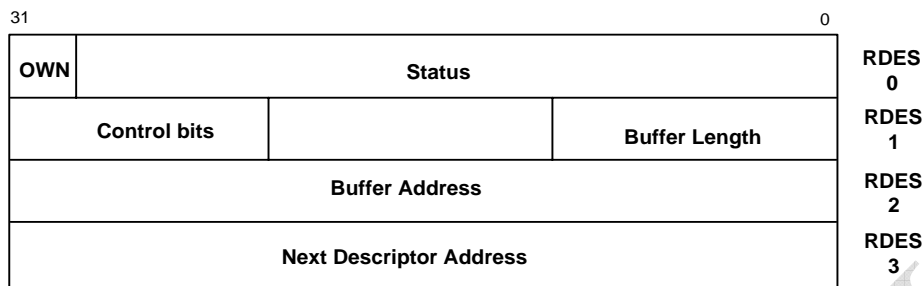
Figure 7-1

7.1.4 Descriptor List: Buffer Descriptor Format

(a). Receive Descriptor Format

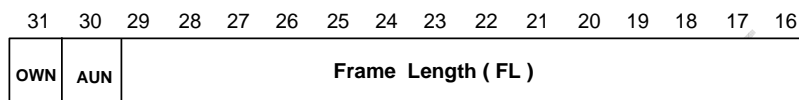
Each receive descriptor has four double word entries and may be read or written by the host or the DM9102D. The

descriptor format is shown below with a detailed functional description.



Receive Descriptor Format

RDES0:

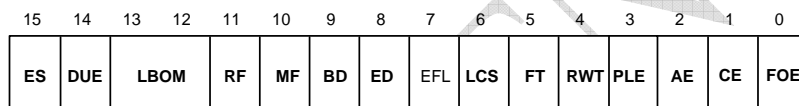


Bit 31: OWN, Owner bit of received status

1=owned by DM9102, 0=owned by host
This bit will be reset after packet reception is completed. The host will set this bit after received data is removed.

Bit 30: AUN, Received address unmatched.

Bit 29-16: FL, Frame Length
Frame length indicates total byte count of received packet.



This word-wide content includes status of received frame. They are loaded after the received buffer that belongs to the corresponding descriptor is full. All status bits are valid only when the last descriptor (End Descriptor) bit is set.

00 --- Normal
01 --- Internal loopback
10 --- Internal PHY digital loopback
11 --- Internal PHY analog loopback

Bit 15: ES, Error Summary

It is set for the following error conditions: Descriptor Unavailable Error (DUE =1), Runt Frame (RF=1), Excessive Frame Length (EFL=1), Late Collision Seen (LCS=1), CRC error (CE=1), FIFO Overflow error (FOE=1). Valid only when ED is set.

Bit 11: RF, Runt Frame

It is set to indicate the received frame has the size smaller than 64 bytes. It is valid only when ED is set and FOE is reset.

Bit 14: DUE, Descriptor Unavailable Error

It is set when the frame is truncated due to the buffer unavailable. It is valid only when ED is set.

Bit 10: MF, Multicast Frame

It is set to indicate the received frame has a multicast address. It is valid only when ED is set.

Bit 13,12: LBOM, Loopback Operation Mode or IP/TCP/UDP checksum status

If CR15 bit 27 is set, these two bits present the IP/TCP/UDP status:

- 0X -- IP checksum OK
- 1X --IP checksum FAIL
- X0 -- TCP or UDP checksum OK
- X1 -- TCP or UDP checksum FAIL

; otherwise
these two bits show the received frame is derived from:

Bit 9: BD, Begin Descriptor

This bit is set for the descriptor indicating the start of a received frame.

Bit 8: ED, End Descriptor

This bit is set for descriptor to indicate the end of a received frame.

Bit 7: EFL, Excessive Frame Length

It is set to indicate the received frame length exceeds 1518 bytes. Valid only when ED is set.

Bit 6: LCS: Late Collision Seen

It is set to indicate a late collision found during the frame reception. Valid only when ED is set.

Bit 5: FT, Frame Type or IP packet

If CR15 bit 27 is set, this bit present the flag that this is IP packet; otherwise it is set to indicate the received frame is the Ethernet-type. It is reset to indicate that the received frame is the IEEE802.3-type. Valid only when ED is set

Bit 4: RWT, Receive Watchdog Time-Out or TCP packet

If CR15 bit 27 is set, this bit present the flag that this is TCP packet; otherwise it is set to indicate the received watchdog time-out during the frame reception. CR5<9> will also be set. Valid only when ED is set.

Bit 3: PLE, Physical Layer Error or UDP packet

If CR15 bit 27 is set, this bit present the flag that this is UDP packet; otherwise it is set to indicate a physical layer error found during the frame reception.

Bit 2: AE, Alignment Error

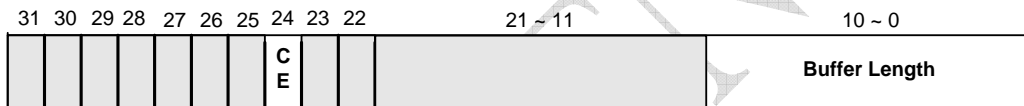
It is set to indicate the received frame ends with a non-byte boundary.

Bit 1: CE, CRC Error

It is set to indicate the received frame ends with a CRC error. Valid only when ED is set.

Bit 0: FOE, FIFO Overflow Error

This bit is valid only when End Descriptor is set. (ED = 1). It is set to indicate a FIFO overflow error happens during the frame reception.

RDES1: Descriptor Status and Buffer Size

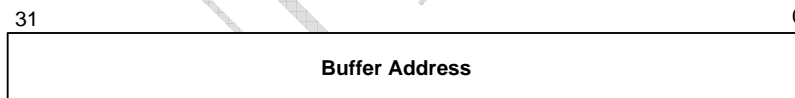
Bit 24: Must be 1.

Bit 10-0: Buffer Length

Indicates the size of the buffer.

RDES2: Buffer Starting Address

Indicates the physical starting address of buffer. This address must be double word aligned.

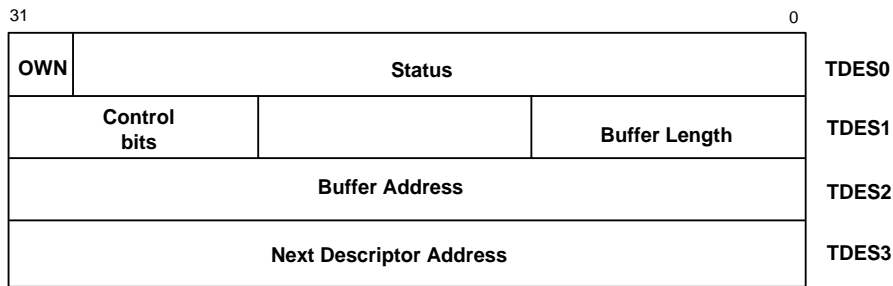
**RDES3: Next descriptor Address**

Indicates the physical starting address of the chained descriptor under the Chain descriptor structure. This address must be eight-word aligned.

**(b). Transmit Descriptor Format**

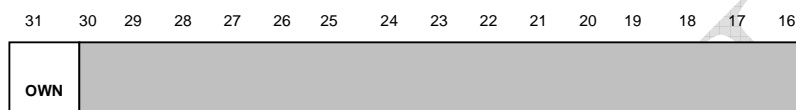
Each transmit descriptor has four double word content and may be read or written by the host or by the DM9102D.

The descriptor format is shown below with detailed description



Transmit Descriptor Format

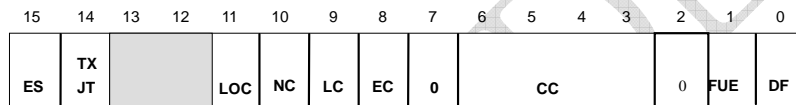
TDES0: Owner Bit with Transmit Status



Bit 31: OWN,

1=owned by DM9102D, 0=owned by host, this bit should be set when the transmitting buffer is filled with data and ready

to be transmitted. It will be reset by DM9102D after transmitting the whole data buffer.



This word wide content includes status of transmitted frame. They are loaded after the data buffer that belongs to the corresponding descriptor is transmitted.

Bit 15: ES, Error Summary

It is set for the following error conditions: Transmit Jabber Time-out (TXJT=1), Loss of Carrier (LOC=1), No Carrier (NC=1), Late Collision (LC=1), Excessive Collision (EC=1), FIFO Underrun Error (FUE=1).

Bit 14: TXJT, Transmit Jabber Time Out

It is set to indicate the transmitted frame is truncated due to transmit jabber time out condition. The transmit jabber time out interrupt CR5<3> is set.

Bit 11: LOC, Loss of Carrier

It is set to indicate the loss of carrier during the frame transmission. It is not valid in internal loopback mode.

Bit 10: NC, No Carrier

It is set to indicate that no carrier signal from transceiver is found. It is not valid in internal loopback mode.

Bit 9: LC, Late Collision

It is set to indicate a collision occurs after the collision window of 64 bytes. Not valid if FUE is set.

Bit 8: EC, Excessive collision

It is set to indicate that the transmission is aborted due to 16 excessive collisions.

Bit 7: Reserved

This bit is 0 when read.

Bits 6-3: CC, Collision Count

These bits show the number of collision before transmission. Not valid if excessive collision bit is also set.

Bit 2: Reserved

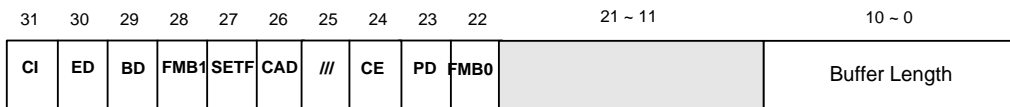
This bit is 0 when read.

Bit 1: FUE, FIFO Underrun Error

It is set to indicate that the transmission aborted due to transmit FIFO underrun condition.

Bit 0: DF, Deferred

It is set to indicate that the frame is deferred before ready to transmit.

TDES1: Transmit buffer control and buffer size**Bit 31: CI, Completion Interrupt**

It is set to enable transmit interrupt after the present frame has been transmitted. It is valid only when TDES1<30> is set or when it is a setup frame.

This bit is set to disable the padding field for a packet shorter than 64 bytes.

Bit 30: ED, Ending Descriptor

It is set to indicate the pointed buffer contains the last segment of a frame.

Bit 22: FMB0, Filtering Mode Bit 0

This bit is used with FMB1 to indicate the filtering type when the present frame is a setup frame.

Bit 29: BD, Begin Descriptor

It is set to indicate the pointed buffer contains the first segment of a frame.

FMB1	FMB0	Filtering Type
0	0	Perfect Filtering
0	1	Hash Filtering
1	0	Inverse Filtering
1	1	Hash-Only Filtering.

Bit 28: FMB1, Filtering Mode Bit 1

This bit is used with FMB0 to indicate the filtering type when the present frame is a setup frame.

Bit 21: IP Packet Checksum Generation

This bit is set to enable the IP packet checksum generation, if per-packet checksum in CR15 bit 31 is enabled

Bit 27: SETF, Setup Frame

It is set to indicate the current frame is a setup frame.

Bit 20: TCP Packet Checksum Generation

This bit is set to enable the TCP packet checksum generation, if per-packet checksum in CR15 bit 31 is enabled.

Bit 26: CAD, CRC Append Disable

It is set to disable the CRC appending at the end of the transmitted frame. Valid only when TDES1<29> is set.

Bit 19: UDP Packet Checksum Generation

This bit is set to enable the UDP packet checksum generation, if per-packet checksum in CR15 bit 31 is enabled.

Bit 24: CE, Chain Enable

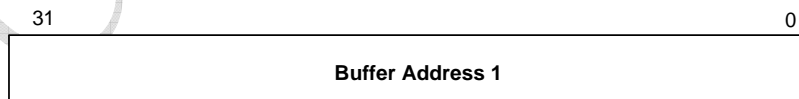
Must be "1".

Bit 10-0: Buffer 1 length

Indicates the size of buffer in Chain type structure.

Bit 23: PD, Padding Disable

TDES2: Buffer Starting Address indicates the physical starting address of buffer.

**TDES3: Address indicates the next descriptor starting address**

Indicates the physical starting address of the chained descriptor under the Chain descriptor structure.

This address must be eight-word alignment.

31

0

Buffer Address 2

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7.2 Initialization Procedure

After hardware or software reset, transmit and receive processes are placed in the state of STOP. The DM9102D can accept the host commands to start operation. The general procedure for initialization is described below:

- (1) Read/write suitable values for the PCI configuration registers.
- (2) Write CR3 and CR4 to provide the starting address of each descriptor list.
- (3) Write CR0 to set global host bus operation parameters.
- (4) Write CR7 to mask causes of unnecessary interrupt.
- (5) Write CR6 to set global parameters and start both receive and transmit processes. Receive and transmit processes will enter the running state and attempt to acquire descriptors from the respective descriptor lists.
- (6) Wait for any interrupt.

7.2.1 Data Buffer Processing Algorithm

The data buffer process algorithm is based on the cooperation of the host and the DM9102D. The host sets CR3 (receive descriptor base address) and CR4 (transmit descriptor base address) for the descriptor list initialization. The DM9102D will start the data buffer transfer after the descriptor polling and get the ownership. For detailed processing procedure, please see below.

7.2.2 Receive Data Buffer Processing

Refer to Figure 7-2. The DM9102D always attempts to acquire an extra descriptor in anticipation of the incoming frames. Any incoming frame size covers a few buffer regions and descriptors. The following conditions satisfy the descriptor acquisition attempt:

When start/stop receive sets immediately after being placed in the running state.

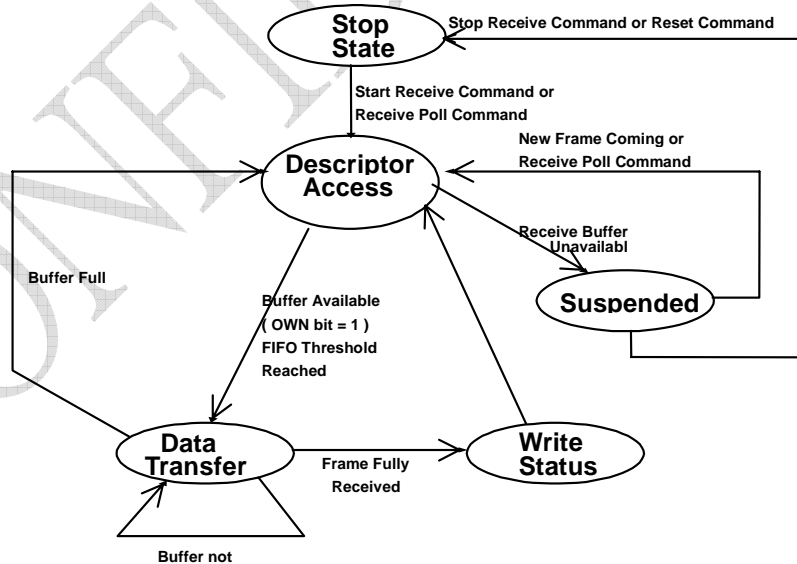
When the DM9102D begins writing frame data to a data buffer pointed to by the current descriptor and the buffer ends before the frame ends.

When the DM9102D completes the reception of a frame and the current receiving descriptor is closed.

When receive process is suspended due to no free buffer for the DM9102D and a new frame is received.

When receive polling demand is issued. After acquiring the free descriptor, the DM9102D processes the incoming frame and places it in the acquired descriptor's data buffer.

When the whole received frame data has been transferred, the DM9102D will write the status information to the last descriptor. The same process will repeat until it encounters a descriptor flagged as being owned by the host. If this occurs, receive process enters the suspended state and waits the host to service



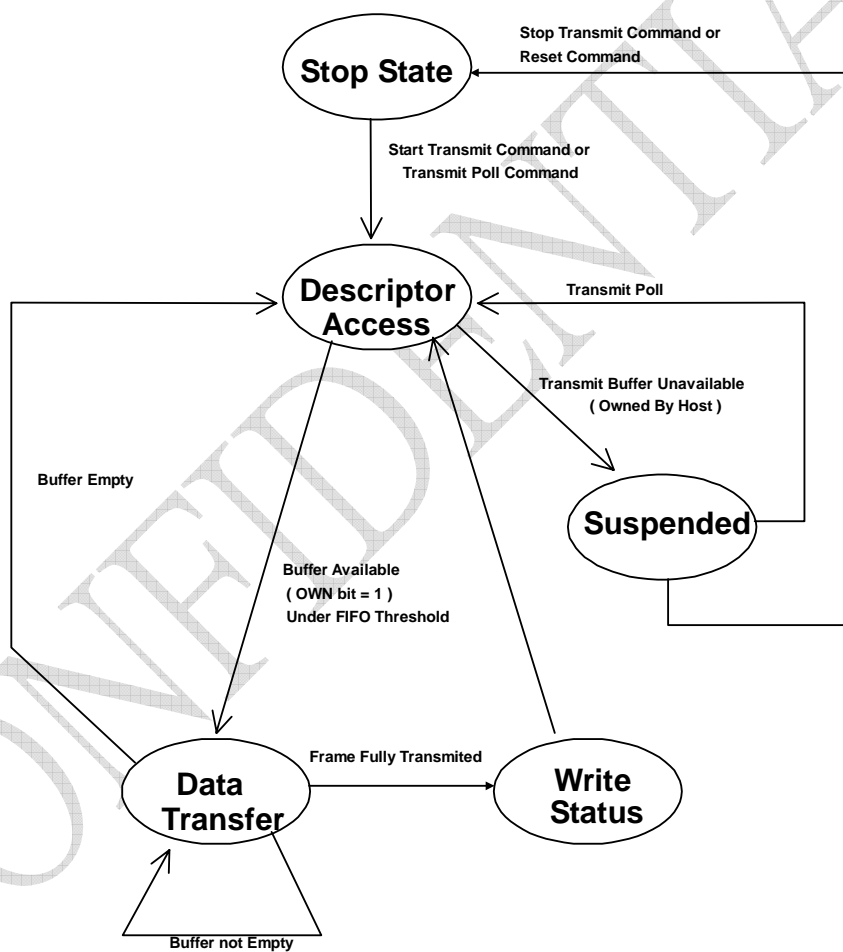
Receive Buffer Management State Transition
Figure 7-2

7.2.3 Transmit Data Buffer Processing

Refer to Figure 7-3. When start/stop transmit command is set and the DM9102D is in running state, transmit process polls transmit descriptor list for frames requiring transmission. When it completes a frame transmission, the status related to the transmitted frame will be written into the transmit descriptor. If the DM9102D detects a descriptor flagged as owned by the host and no transmit buffers are available, transmit process will be suspended. While in the running state, transmit process can simultaneously acquire two frames. As transmit process completes copying the first

frame, it immediately polls transmit descriptor list for the second frame. If the second frame is valid, transmit process copies the frame before writing the status information of the first frame.

Both conditions will make transmit process suspend. (i) The DM9102D detects a descriptor owned by the host. (ii) A frame transmission is aborted when a locally induced error is detected. Under either condition, the host driver has to service the condition before the DM9102D can resume.



Transmit Buffer Management State Transition

Figure 7-3

7.3 Network Function

7.3.1 Overview

This chapter will introduce the normal state machine operation and MAC layer management like collision back-off algorithm. In transmit mode, the DM9102D initiates a DMA cycle to access data from a transmit buffer. It prefaces the data with the preamble, the SFD pattern, and it appends a 32-bit CRC. In receive mode, the data is de-serialized by receive mechanism and is fed into the internal FIFO. For detailed process, please see below.

7.3.2 Receive Process and State Machine

a. Reception Initiation

As a preamble being detected on receive data lines, the DM9102D synchronizes itself to the data stream during the preamble and waits for the SFD. The synchronization process is based on byte boundary and the SFD byte is 10101011. If the DM9102D receives a 00 or a 11 after the first 8 preamble bits and before receiving the SFD, the reception process will be terminated.

b. Address Recognition

After initial synchronization, the DM9102D will recognize the 6-byte destination address field. The first bit of the destination address signifies whether it is a physical address (=0) or a multicast address (=1). The DM9102D filters the frame based on the node address of receive address filter setting. If the frame passes the filter, the subsequent serial data will be delivered into the host memory.

c. Frame Decapsulation

The DM9102D checks the CRC bytes of all received frames before releasing the frame along with the CRC to the host processor.

7.3.3 Transmit Process and State Machine

a. Transmission Initiation

Once the host processor prepares a transmit descriptor for the transmit buffer, the host processor signals the DM9102D to take it. After the DM9102D has been notified of this transmit list, the DM9102D will start to move the data bytes from the host memory to the internal transmit FIFO. When the transmit FIFO is adequately filled to the programmed threshold level, or when there is a full frame buffered into the transmit FIFO, the DM9102D begins to encapsulate the

frame. The transmit encapsulation is performed by the transmit state machine, which delays the actual transmission onto the network until the network has been idle for a minimum inter frame gap time.

b. Frame Encapsulation

The transmit data frame encapsulation stream consists of two parts: Basic frame beginning and basic frame end. The former contains 56 preamble bits and SFD, the later, FCS. The basic frame read from the host memory includes the destination address, the source address, the type/length field, and the data field. If the data field is less than 46 bytes, the DM9102D will pad the frame with pattern up to 46 bytes.

c. Collision

When concurrent transmissions from two or more nodes occur (termed; collision), the DM9102D halts the transmission of data bytes and begins a jam pattern consisting of AAAAAAAAAA. At the end of the jam transmission, it begins the backoff wait time. If the collision was detected during the preamble transmission, the jam pattern is transmitted after completing the preamble. The backoff process is called truncated binary exponential backoff. The delay is a random integer multiple of slot times. The number of slot times of delay before the Nth retransmission attempt is chosen as a uniformly distributed random integer in the range:

$$0 \leq r < 2^k$$

$$k = \min(n, N) \text{ and } N=10$$

7.3.4 Physical Layer Overview

The DM9102D supports 100Mbps and 10Mbps operation. It provides a direct interface either to Unshielded Twisted Pair cable UTP5 for 100BASE-TX fast Ethernet, or UTP5/UTP3 cable for 10BASE-T Ethernet. In physical level operation, it consists of the following functions:

- PCS: 4B5B encode/decode, scramble/de-scramble, and data serialize/parallelize
- NRZ/NRZI, MLT-3 encoder/decoder and driver
- MANCHESTER encoder/decoder
- 10BASE-T filter, driver/receiver, and MANCHESTER encoder/decoder
- Auto. MDI/MDIX detection

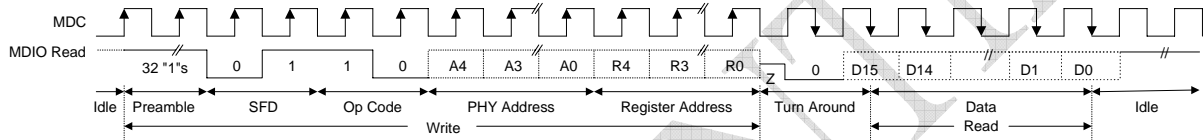
7.4 Serial Management Interface

The serial management interface is used to obtain and control the status of PHY management register set through the internal MDC and MDIO signals, which is control by CR9 bits 19:16. The Management Data Clock (MDC) is equipped with a maximum clock rate of 2.5MHz.

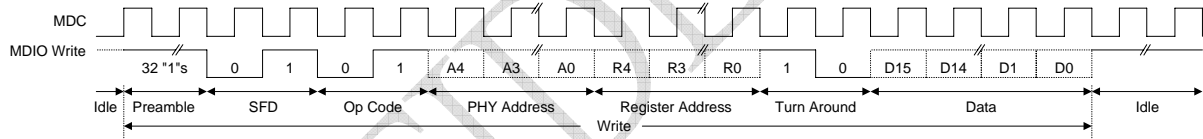
In read/write operation, the management data frame is 64-bit long start with 32 contiguous logic one bits (preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by

the operation code (OP): <10> indicates Read operation and <01> indicates Write operation. Following the OP Code is the 5-bit PHY Address field that is fixed to 00001b. For read operation, a 2-bit turnaround (TA) field between Register Address field and Data field is provided for MDIO to avoid contention. "Z" stands for the state of high impedance. Following turnaround time, a 16-bit data is read from or written onto management registers.

7.4.1 Management Interface - Read Frame Structure



7.4.2 Management Interface - Write Frame Structure



7.5 Power Management

7.5.1 Overview

The DM9102D supports power management mechanism. It complies with the ACPI Specification Rev 1.0, the Network Device Class Power Management Specification Rev 1.0, and the PCI Bus Power Management Interface Specification Rev 1.0. In addition, it also supports the Wake-On LAN (WOL) which is the feature of the AMD's Magic Packet™ technology. With this function, it can wakeup a remote sleeping station.

7.5.2 PCI Function Power Management States

The DM9102D supports PCI function power states D0, D3(hot), D3(cold), and does not support D1, D2 states. In addition, PCI signals PME# (power management event, open drain) to pin A19 of the standard PCI connector.

D0: normal & fully functional state

D3 (hot): For controller, configuration space, that can be accessed and wake up on LAN circuit, can be enabled. PME# operational circuit is active, full function is supported to detect the wake up Frame & Link status. Because of functions in D3(hot) must respond to configuration space accesses as long as power and clock are supplied so that they can be returned to D0 state by software.

D3 (cold): If Vcc is removed from a PCI device, all of its PCI functions transition immediately to D3(cold), no bus transaction is active without pci_clk condition and wake up on LAN operation should be alive. PME# operational circuit is active. Full function is supported under auxiliary power to detect the magic packet & Link status. When power restored, PCI RST# must be asserted and functions will return to D0 with a full PCI Spec. 2.2 compliant power-on reset sequence. The power required in D3(cold) must be provided by some auxiliary power source.

7.5.3 The Power Management Operation

It complies with the PCI Bus Power Management Interface Specification Rev. 1.0. The Power Management Event (PME#) signal is an optional open drain, active low signal that is intended to be driven low by a PCI function to request a change in its current power management state and/or to indicate that a power management event has occurred.

The PME# signal has been assigned to pin A19 of the standard PCI Connector configuration. The assertion and de-assertion of PME# is asynchronous to the PCI clock.

Software will enable its use by setting the PME_En bit in the PMCSR (write 1 to PMCSR<8>). When a PCI function generates or detects an event that requires the system to change its power state, the function will assert PME#. It must continue to assert PME# until software either clears the PME_En bit (PMCSR<8> is set to 0) or clears the PME_Status bit in the PMCSR (write 1 to PMCSR<15>).

DM9102D supports three main categories of network device wake up events specified in Network Device Class Power Management Rev1.0. That is, the DM9102D can monitor the network for a Link Change, Magic Packet or a Wake-up Frame and notify the system by generating PME# if any of the three events occurs. Programming the PCIUSR (offset = 40h) can select the PME# event, and writing 1 to PMCSR<15> will clear the PME#.

a. Detect Network Link State Change

Any link status change will set the wake up event.

1. Writes 1 into PMCSR<15>(54h) to clear previous PME# status
2. Writes 1 into PMCSR<8> to enable PME# function
3. Writes 1 into PCIUSR<29> to enable the link status change function

b. Active Magic Packet Function

It can be enabled by PCIUSR<27> or optionally enabled by EEPROM setting. The magic node address stored at node address table can use setup frame perfect address filtering mode or loading from EEPROM WORD 10~12 after power on .

1. Writes 1 into PMCSR<15> to clear previous PME status
2. Writes 1 into PMCSR<8> to enable PME# function
3. Writes 1 into PCIUSR<27> to enable magic packet function.

c. Active the Sample Frame Function

It can be enabled by PCIUSR<28>. Sample frame data and corresponding byte mask are loaded into transmit FIFO & receive FIFO before entering D3(hot). The software driver has to stop the TX/RX process before setting the sample frame and byte mask into the FIFO. Transmit & receive FIFO can be accessed from CR13 & CR14 by programming CR6<28:25> = 0011.

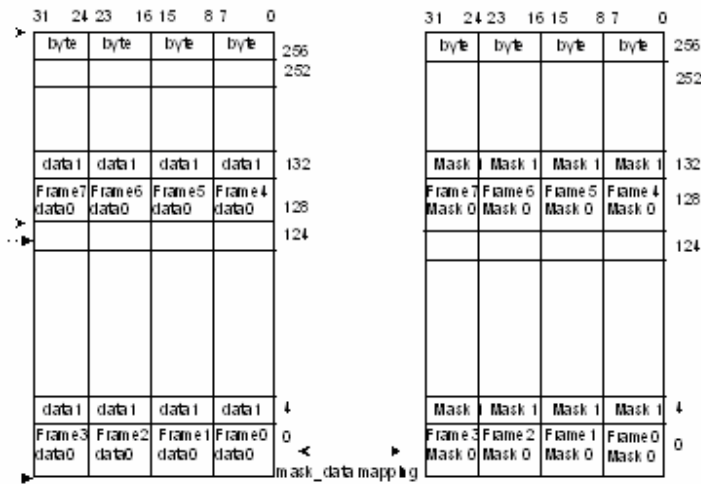
The operational sequence from D0 to D3 should be:
 Stop TX/RX process → wait for entering stop state → set
 test mode, CR6<28:25> = 0011 → programming FIFO
 contents → exit test mode → enter D3 (hot) state

The sample frame data comparison is completed when the
 received frame data has exceeded the programmed frame
 length or when the whole packet has been fully received.
 The operation procedure is shown below.

DM9102D can handle 8 sample frames.
 The max. byte count is 128 byte each
 sample frame.

bit1	bit0	description
0	0	this byte don't care
0	1	this byte mask clock
1	0	this byte don't care
1	1	end of mask (sample frame)

Frame mask definition: only use 8 bits per byte



CR13: Sample Frame Access Register

Name	General definition	Bit8:3	Type
TxFIFO	Transmit FIFO access port	32h	R/W
RxFIFO	Receive FIFO access port	35h	RW
DiagReset	General reset for diagnostic pointer port	38h	RW

In DiagReset port there are 7 bits:

- Bit 0: Clear TX FIFO write_ address to 0
- Bit 1: Clear TX FIFO read_ address to 0
- Bit 2: Clear RX FIFO write_ address to 0
- Bit 3: Clear RX FIFO read_ address to 0

- Bit 4: Reserved
- Bit 5: Set TX FIFO write_ address to 080H
- Bit 6: Set RX FIFO write_ address to 080H

7.6 Sample Frame Programming Guide:

1. Enter the sample frame access mode:

Set CR6<28:25>=0011

2. Reset the TX/RX FIFO, write pointer to offset 0:

Write 38H to CR13<8:3>

Write 01h to CR14 (reset)

Write 00h to CR14 (clear)

3. Write the sample frame 0-3 data to RX FIFO:

Write 35H to CR13<8:3>

Write xxxxxxxh to CR14 (Frame1~3 first byte)

Write xxxxxxxh to CR14 (Frame1~3 second byte)

⋮

Repeat write until all frame data written to RX FIFO

4. Reset RX FIFO, write pointer to offset 080H:

Write 38H to CR13<8:3>

Write 40H to CR14 (reset)

Write 00H to CR14 (clear)

5. Write the sample frame 4-7 to RX FIFO:

Write 35H to CR13<8:3>

Write xxxxxxxh to CR14 (Frame4~7 first byte)

Write xxxxxxxh to CR14 (Frame4~7 second byte)

⋮

Repeat write until all frame data written to RX FIFO

6. Write the sample frame 0-3 mask to TX FIFO:

Write 32H to CR13<8:3>

Write xxxxxxxh to CR14 (Frame0~3 first mask byte)

Write xxxxxxxh to CR14 (Frame0~3 second mask byte)

⋮

Repeat write until all frame mask which is written to TX FIFO

7. Reset TX FIFO, write pointer to offset 080H:

Write 38H to CR13<8:3>

Write 20H to CR14 (reset)

Write 00H to CR14 (clear)

8. Write the sample frame 4-7 mask to TX FIFO:

Write 32H to CR13<8:3>

Write xxxxxxxh to CR14 (Frame4~7 first mask byte)

Write xxxxxxxh to CR14 (Frame4~7 second mask byte)

⋮

Repeat write until all frame mask is written to TX FIFO

7.7 EEPROM Overview

The first 13 words of Configuration EEPROM are loaded into the DM9102D after power-on-reset for the settings of

the power management, system ID and Ethernet address. The format of the EEPROM is as followed

The format of EEPROM

Field Name	Word Offset	Word Size
Subsystem Vendor ID	0	1
Subsystem ID	1	1
Reserved	2	2
NCE and Auto_load_control	4	1
PCI Vendor ID	5	1
PCI Device ID	6	1
PMCSR and PMC	7	1
Reserved	8	2
Ethernet Address	10	3

**7.7.4 Word Offset (04):
New_Capabilities_**

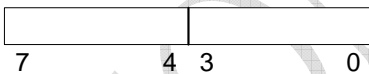
7.7.1 Subsystem ID Block

Every card has a Subsystem ID to indicate the information of system vendor. The content will be transferred into the PCI configuration space 2CH.

7.7.2 Vendor ID

Vendor ID & Device ID can be set in EEPROM content & auto-loaded to PCI configuration register after reset.(default value = 1282H, 9102H) This function must be selectable for enable by Auto_Load_Control (word offset 04 bit[3:0] of EEPROM).

7.7.3 Word Offset (04): Auto_Load_Control

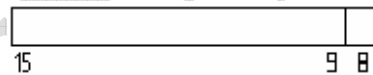


Bit3~0: "1010" to enable auto-load of PCI Vendor_ID & Device_ID.

Bit7~4: "1X1X" to enable auto-load of NCE, PME & PMC & PMCSR to PCI configuration space. Bit 4 and 6 are used to control the polarity and pulse mode of the WOL pin.

If bit4 = 0, WOL is Active HIGH.
If bit4=1, WOL is Active LOW
If bit6 = 0, WOL is PULSE signal
If bit6=1, WOL is LEVEL signal.

Enable



Bit0: Directly mapping to bit20 (New Capabilities) of the PCICS

If Bit9=1, Bit [12:10] mapping to bit [18:16] of the PCIPMR and Bit [15:13] mapping to bit [24:22] of the PCIPMR.

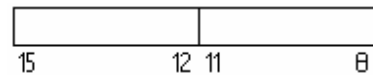
7.7.5 Word Offset (07): PMC



Bit7~3: Directly mapping to bit[31:27] of the PCIPMR.

Bit2~0: Directly mapping to bit[21,26:25] of the PCIPMR.

7.7.6 Word Offset (07): Control



Bit 15: Disable PHY auto-MDIX function
Bit 14: Disable to power-down PHY if ISOLATE pin is low.
Bit 13: Clear PMCSR[1:0] if RST# pin is low
Bit 12: PME# is not pulse mode
Bit 11: Set to disable the output of WOL pin.
Bit 10: Set to disable the output of PME# pin.
Bit 9: Set to enable the link change wake up event.
Bit 8: Set to enable the Magic packet wake up event.

7.7.7 Word Offset (10~12): Ethernet Address

Address 0 = EEPROM Word 10 low byte

Address 1 = EEPROM Word 10 high byte

Address 2 = EEPROM Word 11 low byte

Address 3 = EEPROM Word 11 high byte

Address 4 = EEPROM Word 12 low byte

Address 5 = EEPROM Word 12 high byte

7.7.8 Example of DM9102D EEPROM Format

Total Size: 128 Bytes

Field Name	Offset (Byte)	Size (Bytes)	Value (Hex)	Commentary
Sub-Vendor ID	0	2	1282H	ID Block
Sub-Device ID	2	2	9102H	
Reserved1	4	4	00000000	
Auto_Load_Control	8	1	00	Auto-load function definition: Bit 3~0 = 1010 → Auto-Load PCI Vendor ID/Device ID enabled Bit 7~4 = 1x1x → Auto-Load NCE, PMC/PMCSR enabled
New_Capabilities_Enable (NCE)	9	1	00	Please refer to DM9102D Spec.
PCI Vendor ID	10	2	1282H	If Auto-Load PCI Vendor ID/Device ID function disabled, the PCI Vendor ID/Device ID will use the default values (1282H, 9102H).
PCI Device ID	12	2	9102H	
Power Management Capabilities (PMC)	14	1	00	Please refer to DM9102D Spec.
Power Management Control/Status (PMCSR)	15	1	00	Please refer to DM9102D Spec.
Reserved2	16	4	00	
IEEE Network Address	20	6	-	Controller Info Header
Driver area	26	102	-	For software driver

7.8 External MII Interface

DM9102D provides one external MII interface sharing with all the pins with Boot ROM interface. This external MII interface can be connected with external PHYceiver such as Home Networking PHYceiver or other future technology

applications. This external MII interface can be set up by hardware and software. The setup methods are listed as below:

	Test 1 (pin 37)	Test 2 (pin 71)	Clkrun# (pin 36)	EECK (pin 79)	EEDO (pin 78)
Normal Operation	0	1	X	X	X
External MII mode	0	0	0	0	1/0
Internal Test mode	1	X	X	X	X

Note 1

Note 1: External MII mode

EEDO = 1(pulled high): only external PHY is selected.

EEDO= 0(floating) & MII_Mode = 1: Select external PHY

EEDO = 0(float) & MII_Mode = 0: Select internal PHY

Where MII_Mode is the bit 18 of CR6

7.8.1 The Sharing Pin Table

(o): output, (i): input, (b): bi-direction

	Normal Operation	External MII Interface
	Boot ROM interface	External MII interface
	TEST2=1	TEST2= 0
Pin		
62	MD0/EEDI	MII_MDIO/EEDI(b)
63	MD1	MII_RXD2 (i)
64	MD2	MII_RXD1 (i)
65	MD3	MII_RXD0 (i)
66	MD4	MII_RXDV (i)
67	MD5	MII_RXER (i)
68	MD6	MII_CRIS (i)
69	MD7	MII_RXCLK (i)
75	IDSEL2	MII_COL(i)
78	EEDO	MII_TXD0/EEDO(o)
79	EECK	MII_TXD1/EECK (o)
83	LED_MODE	MII_TXEN(o)
84	REQ2#	MII_TXCLK (i)
87	TRF_LED	MII_TXD2(o)
88	FDX_LED	MII_TXD3(o)
89	SPD100_LED	MII_MDC(o)
90	SPD10_LED	MII_RXD3(i)

8. DC and AC Electrical Characteristics

8.1 Absolute Maximum Ratings (25°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVDD, AVDD	Supply Voltage	-0.3	3.6	V	
DVDD25, AVDD25	Supply Voltage	-0.3	2.7	V	
V _{IN}	DC Input Voltage (V _{IN})	-0.5	5.5	V	
V _{OUT}	DC Output Voltage (V _{OUT})	-0.3	3.6	V	
T _c	Case Temperature Range	0	85	°C	
T _{stg}	Storage Temperature Rang (T _{stg})	-65	150	°C	
LT	Lead Temp. (TL, Soldering, 10 sec.)	---	235	°C	

8.2 Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVDD, AVDD	Supply Voltage	3.135	3.465	V	
DVDD25, AVDD25	Supply Voltage	2.375	2.625	V	
T _c	Case Temperature	0	85	°C	@Ta=0 ~ 70
T _a	Ambient Temperature	0	70	°C	
PD (Power Dissipation)	100BASE-TX	---	93	mA	2.5V
	100BASE-TX IDLE	---	91	mA	2.5V
	10BASE-T TX	---	99	mA	2.5V
	10BASE-T IDLE	---	40	mA	2.5V
	Auto-negotiation	---	51	mA	2.5V
	Power Reduced Mode (without cable)	---	29	mA	2.5V
	Power-Down Mode	---	12	mA	2.5V

Comments

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated

in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

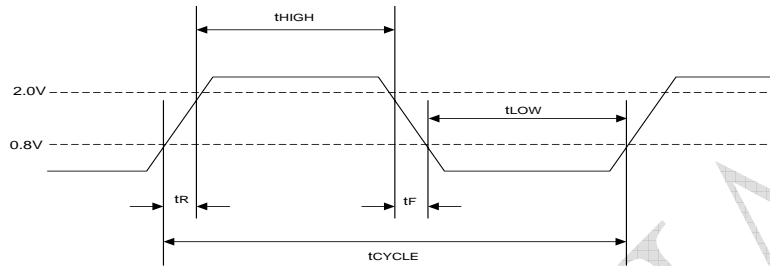
8.3 DC Electrical Characteristics

(0°C<T_c<85°C, 3.135V<AV_{DD}, DV_{DD}<3.465V, 2.375V<AV_{DD25}, DV_{DD25}<2.625V unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Inputs						
V _{IL}	Input Low Voltage	-	-	0.8	V	
V _{IH}	Input High Voltage	2.0	-	-	V	
I _{IL}	Input Low Leakage Current	---	-	5	μA	V _{IN} = 0V
I _{IH}	Input High Leakage Current	5	-	-	μA	V _{IN} = 3.3V
Outputs						
V _{OL}	Output Low Voltage	-	-	0.4	V	I _{OL} = 4mA
V _{OH}	Output High Voltage	2.4	-	-	V	I _{OH} = -4mA
Receiver						
V _{ICM}	RX+/RX- Common mode Input Voltage	---	2.5	-	V	100 Ω Termination Across
Transmitter						
V _{TD100}	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
V _{TD10}	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
I _{TD100}	100TX+/- Differential Output Current	19	20	21	mA	Absolute Value
I _{TD10}	10TX+/- Differential Output Current	44	50	56	mA	Absolute Value

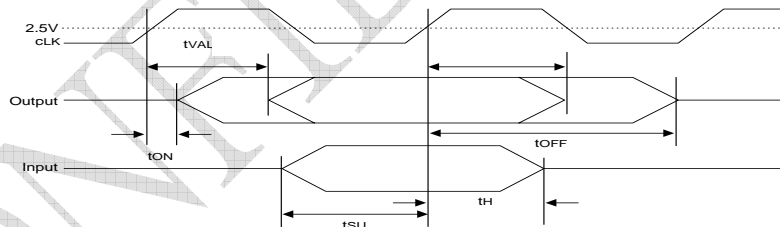
8.4 AC Electrical Characteristics & Timing Waveforms

8.4.1 PCI Clock Specifications Timing



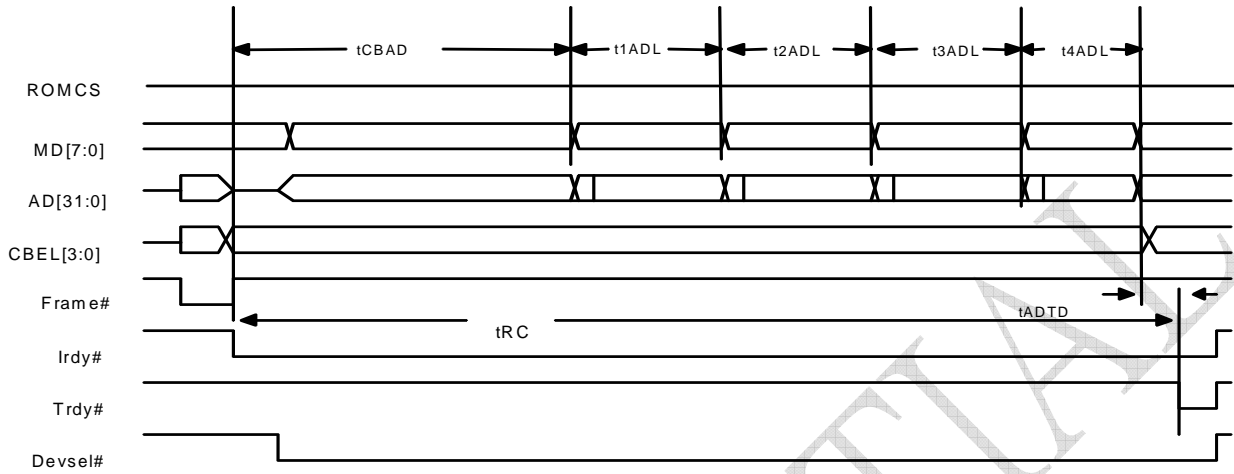
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tR	PCI_CLK Rising Time	-	-	4	ns	-
tF	PCI_CLK Falling Time	-	-	4	ns	-
tCYCLE	Cycle Time	25	30	-	ns	-
tHIGH	PCI_CLK High Time	12	-	-	ns	-
tLOW	PCI_CLK Low Time	12	-	-	ns	-

8.4.2 Other PCI Signals Timing Diagram



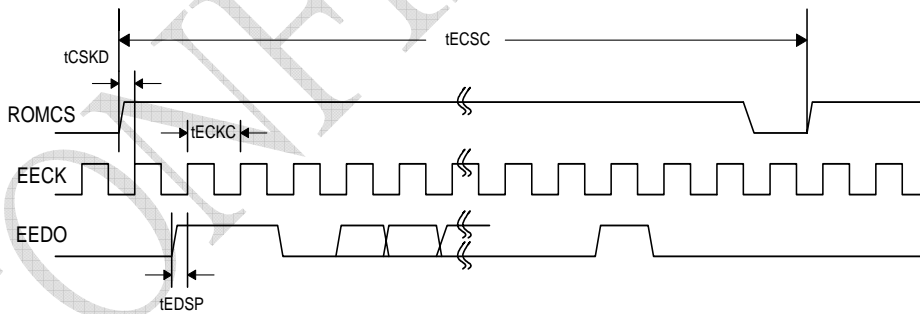
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tVAL	Clk-To-Signal Valid Delay	2	-	13	ns	Clod = 50 pF
tON	Float-To-Active Delay From Clk	2	-	-	ns	-
tOFF	Active-To-Float Delay From Clk	-	-	28	ns	-
tSU	Input Signal Valid Setup Time Before Clk	7	-	-	ns	-
tH	Input Signal Hold Time From Clk	0	-	-	ns	-

8.4.3 Boot ROM Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tRC	Read Cycle Time	-	50	-	PCI clock	-
tCBAD	Bus Command to First Address Delay	-	18	-	PCI clock	-
T1ADL	First Address Length	-	8	-	PCI clock	-
T2ADL	Second Address Length	-	8	-	PCI clock	-
T3ADL	Third Address Length	-	8	-	PCI clock	-
T4ADL	Fourth Address Length	-	7	-	PCI clock	-
tADTD	End of Address to Trdy Active	-	1	-	PCI clock	-

8.4.4 EEPROM Read Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tECKC	Serial ROM Clock EECK Period	-	2560	-	ns	-
tECSC	Read Cycle Time	-	71680	-	ns	-
tCSKD	Delay from ROMCS High to EECK High	-	1600	-	ns	-
tEDSP	Setup Time of EEDO to EECK	-	960	-	ns	-

8.4.5 TP Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tTR/F	100TX+/- Differential Rise/Fall Time	3.0	-	5.0	ns	
tTM	100TX+/- Differential Rise/Fall Time Mismatch	0	-	0.5	ns	
tTDC	100TX+/- Differential Output Duty Cycle Distortion	0	-	0.5	ns	
tT/T	100TX+/- Differential Output Peak-to-Peak Jitter	0	-	1.4	ns	
XOST	100TX+/- Differential Voltage Overshoot	0	-	5	%	

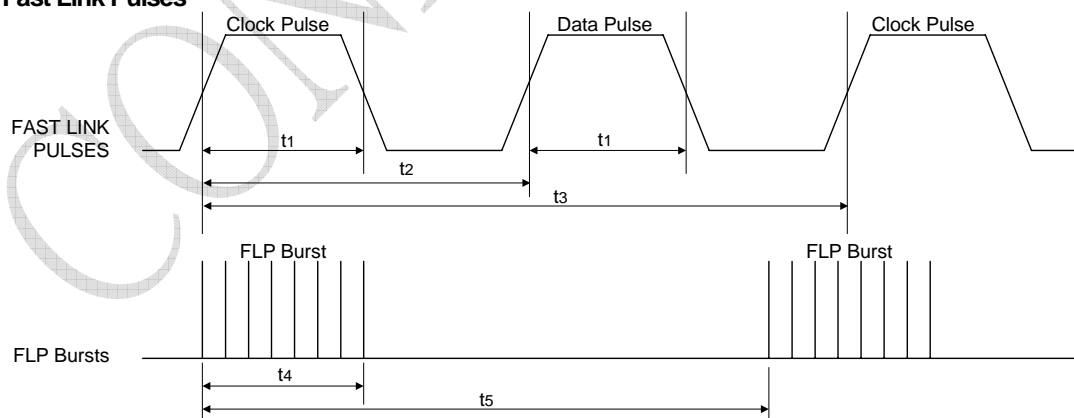
8.4.6 Oscillator/Crystal Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tCKC	OSC Cycle Time	39.998	40	40.002	ns	+/-50ppm
TPWH	OSC Pulse Width High	16	20	24	ns	
TPWL	OSC Pulse Width Low	16	20	24	ns	

8.4.7 Auto-negotiation and Fast Link Pulse Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t1	Clock/Data Pulse Width	-	100	-	ns	
t2	Clock Pulse To Data Pulse Period	55.5	62.5	69.5	us	DATA = 1
t3	Clock Pulse To Clock Pulse Period	111	125	139	us	
t4	FLP Burst Width	-	2	-	ms	
t5	FLP Burst To FLP Burst Period	8	16	24	ms	
-	Clock/Data Pulses in a Burst	17		33	#	

8.4.8 Fast Link Pulses



9. Application Notes

9.1 Network Interface Signal Routing

Place the transformer as close as possible to the RJ-45 connector. Place all the 50 Ω resistors as close as possible to the DM9102D RX± and TX± pins. Traces routed from RX± and TX± to the transformer should run in close pairs directly to the transformer. The designer should be careful not to cross the transmit and receive pairs. As always, vias should be avoided as much as possible. The network interface should be void of any signals other than the TX± and RX± pairs between the RJ-45 to the transformer and the transformer to the DM9102D. There should be no power

or ground planes in the area under the network side of the transformer to include the area under the RJ-45 connector (Refer to Figure 9-4-1 and 9-5). Keep chassis ground away from all active signals. The RJ-45 connector and any unused pins should be tied to chassis ground through a resistor divider network and a 2KV bypass capacitor.

The Band Gap resistor should be placed as physically close to pin 101 and 102 as possible (refer to Figure 9-1 and 9-2). The designer should not run any high-speed signal near the Band Gap resistor placement.

9.2 10Base-T/100Base-TX Application

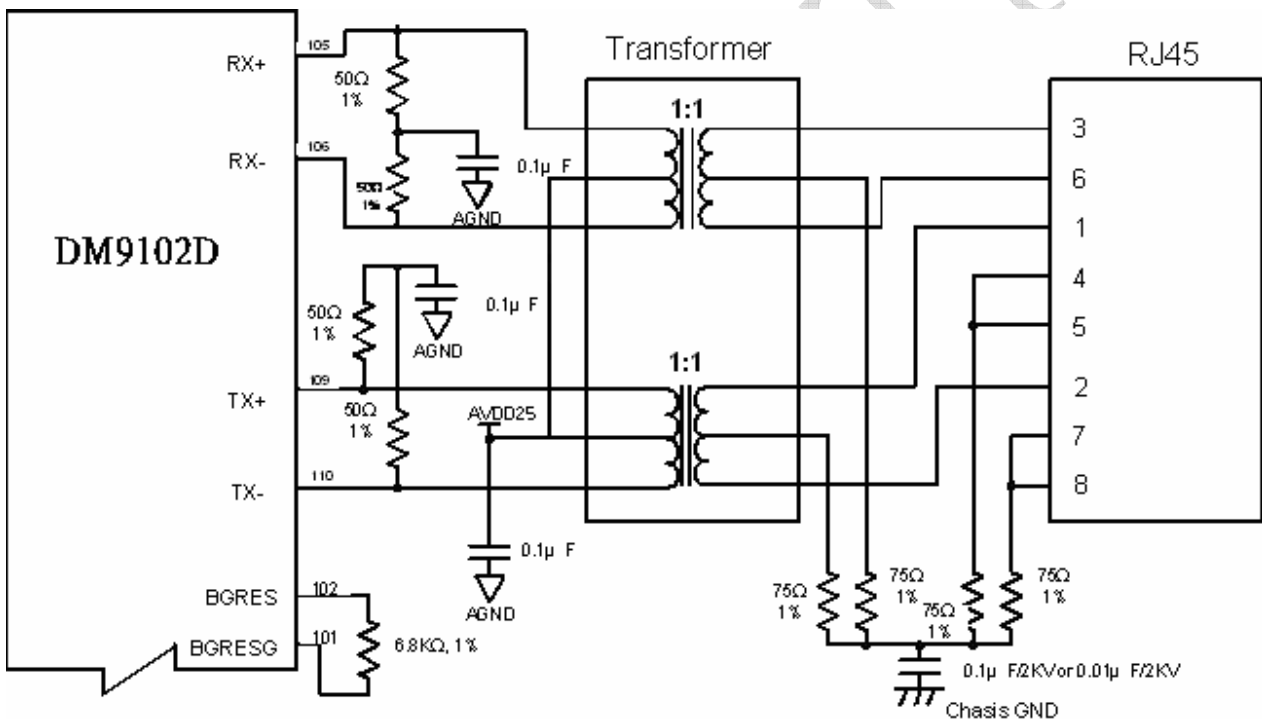


Figure 9-1

9.3 10Base-T/100Base-TX (Power Reduction and non-auto MDIX Application)

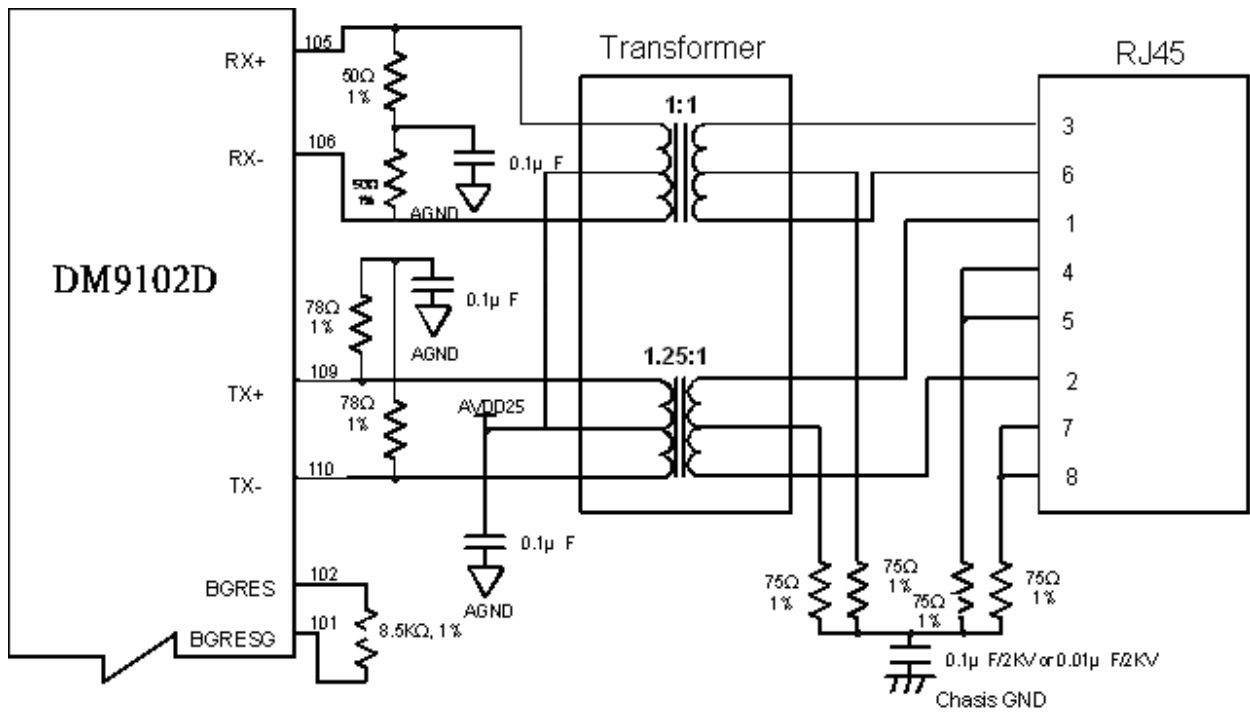


Figure 9-2

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9.4 Power Supply Decoupling Capacitors

- Place all the decoupling capacitors for all the power supply pins as close as possible to the power pads of the DM9102D (no more than 2.5mm from the pins mentioned above.) The recommended decoupling capacitor is 0.1 μ F or 0.01 μ F.
- The decoupling of PCB layout and power supply should provide sufficient decoupling to achieve the following when measured at the device:
 - All DVDDs and AVDDs should be within 50mVpp of each other,
 - All DGNDs and AGNDs should be within 50mVpp of each other.
 - The resultant AC noise voltage measured across each DVDD/DGND set and AVDD/AGND set should be less than 100mVpp.
- The 0.1-0.01 μ F decoupling capacitor should be connected between each DVDD/DGND set and AVDD/AGND set be placed as close as possible to the pins of DM9102D. The conservative approach is to use two decoupling capacitors on each DVDD/DGND set and AVDD/AGND set. The 0.1 μ F capacitor is used for low frequency noise and the 0.01 μ F one is for high frequency noise on the power supply.
- The AVDD connection to the transmit center tap of the magnetic has to be well decoupled to minimize common mode noise injection from the power supply into the twisted pair cable. It is recommended that a 0.01 μ F decoupling capacitor should be placed between the center tap AVDD to AGND ground plane. This decoupling capacitor should be placed as close as possible to the center tap of the magnetic.

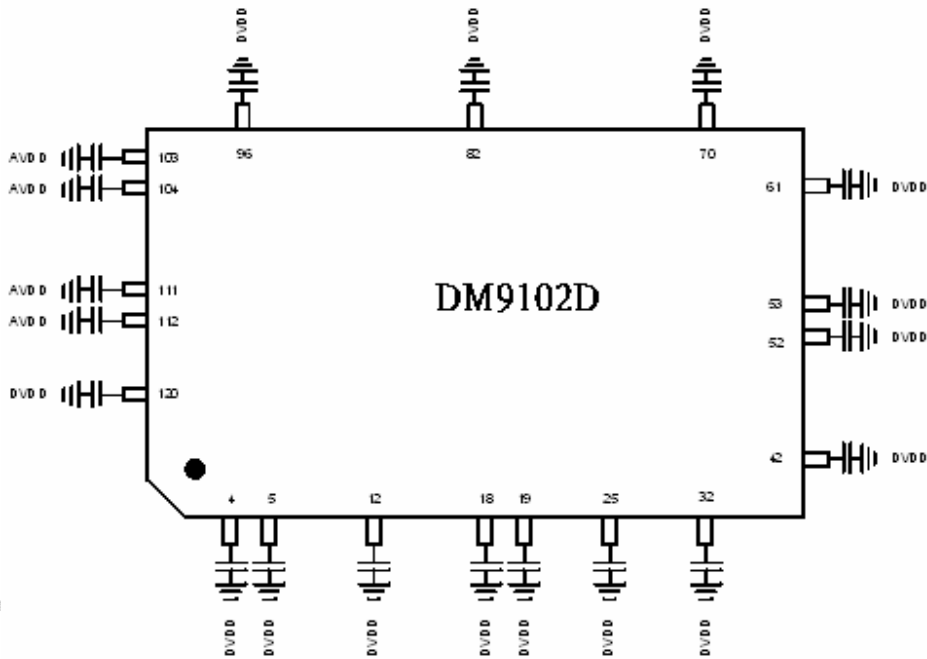


Figure 9-3

9.5 Ground Plane Layout

- Place a single ground plane approach to minimize EMI. Bad ground plane partitioning can cause more EMI emissions that could make the network interface card (NIC) not compliant with specific FCC part 15 and CE regulations.
- The ground plane must be separated into Analog ground domain and Digital ground domain. The line which connects the analog ground domain and digital ground domain should be far away from the AGND pins of DM9102D (see Figure 9-4-1).
- All AGND pins (pin 100, 107, 108) could not directly short each other (see Figure 9-4-3). It must be directly connected to the analog ground domain (see Figure 9-4-2).
- The analog ground domain area is as large as possible

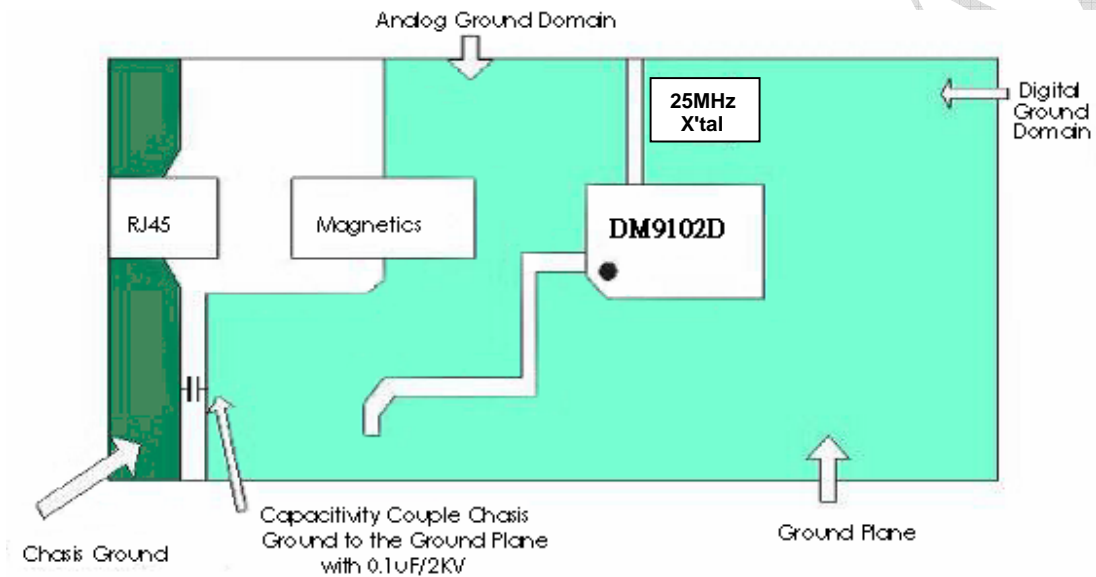


Figure 9-4-1

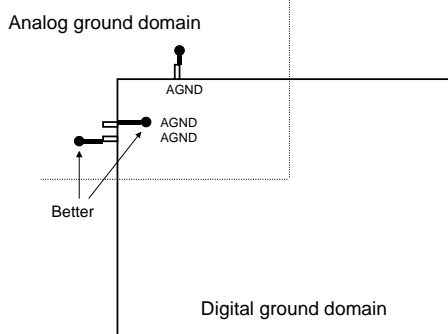


Figure 9-4-2

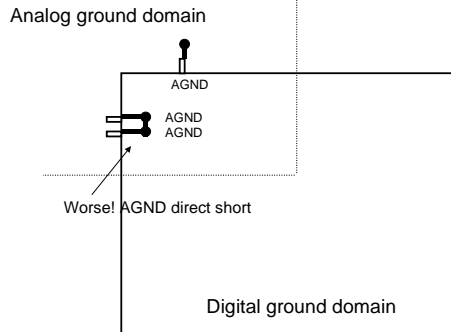


Figure 9-4-3

9.6 Power Plane Partitioning

- The power planes are approximately illustrated in Figure 9-4. The ferrite bead used should have an impedance 100 Ω at 100MHz and 250mA above. A suitable bead is the Panasonic surface mound bead, part number EXCCL4532U or an equivalent. 10 μ F, 0.1 μ F and 0.01 μ F

electrolytic bypass capacitors should be connected between VDD and GND at each side of the ferrite bead.

- Separate analog power planes from noisy logic power planes.

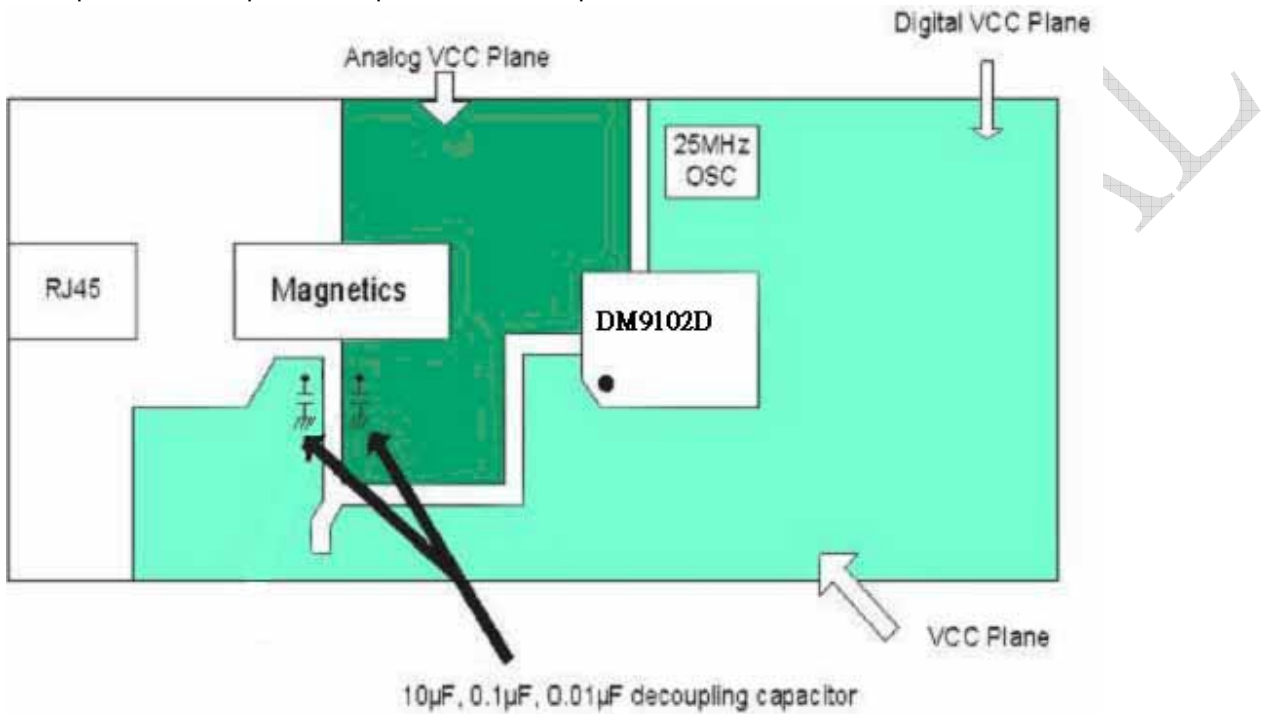


Figure 9-5

9.7 Magnetics Selection Guide

- Refer to the following tables 9-1 and 9-2 for 10/100M magnetic sources and specification requirements. The magnetics which meets these requirements are available from a variety of magnetic manufacturers. Designers should test

and qualify all magnetic specifications before using them in an application. The magnetics listed in the following tables are electrical equivalents, but may not be pin-to-pin equivalents.

Manufacturer	Part Number
Pulse Engineering	PE-68515, H1078, H1012, H1102
Delta	LF8200, LF8221x
YCL	20PMT04, 20PMT05
Halo	TG22-3506ND, TG22-3506G1, TG22-S010ND TG22-S012ND
Nano Pulse Inc.	NPI 6181-37, NPI 6120-30, NPI 6120-37, NPI 6170-30
Fil-Mag	PT41715
Bel Fuse	S558-5999-01
Valor	ST6114, ST6118
Macronics	HS2123, HS2213
Bothhand	TS6121CX, LU1S041CX TS6121C, 16ST8515, 16ST1086

Table 9-1: 10/100M Magnetic Sources

Parameter	Values	Units	Test Condition
Tx / RX turns ratio	1:1 CT / 1:1	-	-
Inductance	350	μH (Min)	-
Insertion loss	1.1	dB (Max)	1 – 100 MHz
Return loss	-18	dB (Min)	1 – 30 MHz
	-14	dB (Min)	30 – 60 MHz
	-12	dB (Min)	60 – 80 MHz
Differential to common mode rejection	-40	dB (Min)	1 – 60 MHz
	-30	dB (Min)	60 – 100 MHz
Transformer isolation	1500	V	-

Table 9-2: Magnetic Specification Requirements

9.8 Crystal Selection Guide

- A crystal can be used to generate the 25MHz reference clock instead of an oscillator. The crystal must be a fundamental type, series-resonant, connected to X1 and X2, and shunt to ground with 22pF capacitors. (See Table 9-3 and Figure 9-66.)

PARAMETER	SPEC
Type	Fundamental, series-resonant
Frequency	25 MHz +/-0.005%
Equivalent Series Resistance	25 ohms max
Load Capacitance	22 pF typ.
Case Capacitance	7 pF max.
Power Dissipation	1mW max.

Table 9-3: Crystal Specifications

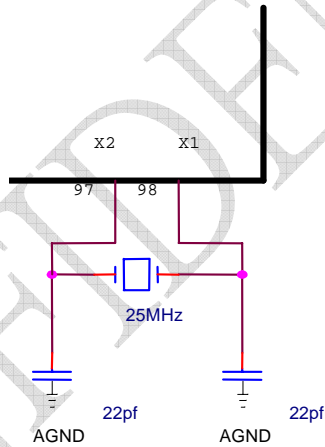
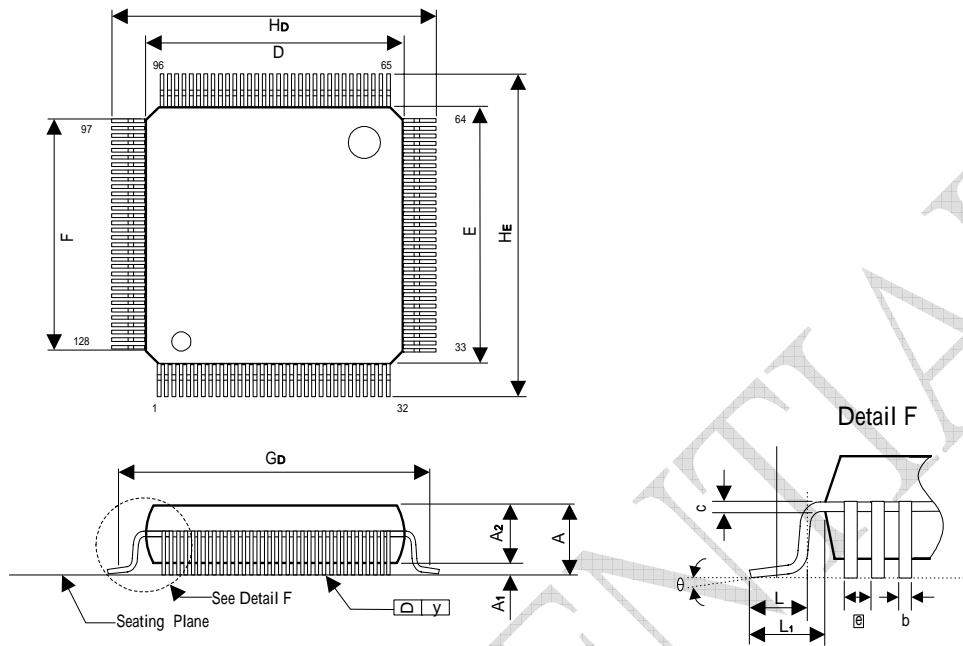


Figure 9-6
Crystal Circuit Diagram

10. Package Information

LQFP 128L Outline Dimensions

Unit: Inches/mm



Symbol	Dimensions In Inches	Dimensions In mm
A	0.063 Max.	1.60 Max.
A ₁	0.004 ± 0.002	0.1 ± 0.05
A ₂	0.055 ± 0.002	1.4 ± 0.05
b	0.006 ^{+0.003} _{-0.001}	0.16 ^{+0.07} _{-0.03}
c	0.006 ± 0.002	0.15 ± 0.05
D	0.551 ± 0.005	14.00 ± 0.13
E	0.551 ± 0.005	14.00 ± 0.13
e	0.016 BSC.	0.40 BSC.
F	0.494 NOM.	12.56 NOM.
G _D	0.606 NOM.	15.40 NOM.
H _D	0.630 ± 0.006	16.00 ± 0.15
H _E	0.630 ± 0.006	16.00 ± 0.15
L	0.024 ± 0.006	0.60 ± 0.15
L ₁	0.039 Ref.	1.00 Ref.
y	0.003 Max.	0.08 Max.
θ	0° ~ 12°	0° ~ 12°

Notes:

1. Dimension D & E do not include resin fins.
2. Dimension G_D is for PC Board surface mount, pad pitch design reference only.
3. All dimensions are based on metric system.

11. Ordering Information

Part Number	Pin Count	Package
DM9102DE	128	LQFP

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WARNING

Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.

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