

**FAIRCHILD**  
SEMICONDUCTOR™

June 1989  
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## DM93L14 Quad Latch

### General Description

The DM93L14 is a multifunctional 4-bit latch designed for general purpose storage applications in high speed digital systems. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good noise immunity.

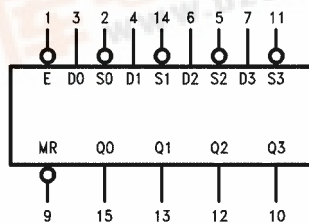
### Features

- Can be used as single input D latches or set/reset latches
- Active low enable gate input
- Overriding master reset

### Ordering Code:

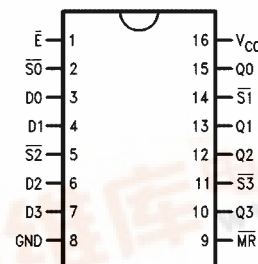
Order Number	Package Number	Package Description
DM93L14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

### Logic Symbol



V<sub>CC</sub> = Pin 16  
GND = Pin 8

### Connection Diagram



### Pin Descriptions

Pin Names	Description
$\bar{E}$	Enable Input (Active LOW)
D0 – D3	Data Inputs
$\bar{S}0$ – $\bar{S}3$	Set Inputs (Active LOW)
$\bar{MR}$	Master Reset Input (Active LOW)
Q0 – Q3	Latch Outputs

DM93L14 Quad Latch



## Functional Description

The DM93L14 consists of four latches with a common active LOW Enable input and active LOW Master Reset input. When the Enable goes HIGH, data present in the latches is stored and the state of the latch is no longer affected by the  $S_n$  and  $D_n$  inputs. The Master Reset when activated overrides all other input conditions forcing all latch outputs LOW. Each of the four latches can be operated in one of two modes:

**D-TYPE LATCH**—For D-type operation the  $\bar{S}$  input of a latch is held LOW. While the common Enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the Enable goes HIGH.

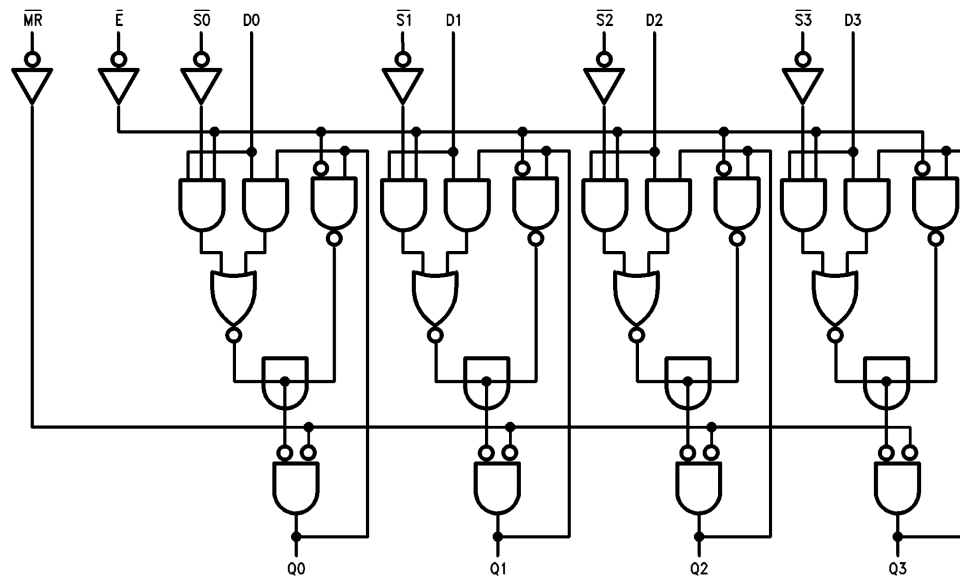
**SET/RESET LATCH**—During set/reset operation when the common Enable is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the  $\bar{S}$  input if the D input is HIGH. If both  $\bar{S}$  and D inputs are LOW, the D input will dominate and the latch will be reset. When the Enable goes HIGH, the latch remains in the last state prior to disablement. The two modes of latch operation are shown in the Truth Table.

## Truth Table

$\overline{MR}$	$\bar{E}$	D	$\bar{S}$	$Q_n$	Operation
H	L	L	L	L	D Mode
H	L	H	L	L	
H	H	X	X	$Q_{n-1}$	
H	L	L	L	L	R/S Mode
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	$Q_{n-1}$	
H	H	X	X	$Q_{n-1}$	
L	X	X	X	L	RESET

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 $Q_{n-1}$  = Previous Output State  
 $Q_n$  = Present Output State

## Logic Diagram



**Absolute Maximum Ratings**(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

**Note 1:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions table will define the conditions for actual device operation.

**Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.7	V
I <sub>OH</sub>	HIGH Level Output Voltage			−400	μA
I <sub>OL</sub>	LOW Level Output Current			4.8	mA
T <sub>A</sub>	Free Air Operating Temperature	−55		125	°C
t <sub>S</sub> (H)	Setup Time HIGH or LOW	10			ns
t <sub>S</sub> (L)	D <sub>n</sub> to $\overline{E}$	20			
t <sub>H</sub> (H)	Hold Time HIGH or LOW	0			ns
t <sub>H</sub> (L)	D <sub>n</sub> to $\overline{E}$	10			
t <sub>S</sub> (H)	Setup time HIGH, D <sub>n</sub> to $\overline{S}_n$	15			ns
t <sub>H</sub> (L)	Hold time LOW, D <sub>n</sub> to $\overline{S}_n$	5			ns
t <sub>W</sub> (L)	$\overline{E}$ Pulse Width LOW	30			ns
t <sub>W</sub> (L)	$\overline{MR}$ Pulse Width LOW	25			ns
t <sub>REC</sub>	Recovery time, $\overline{MR}$ to $\overline{E}$	5			ns

## Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
$V_I$	Input Clamp Voltage	$V_{CC} = \text{Min}$ , $I_I = -10 \text{ mA}$			-1.5	V
$V_{OH}$	HIGH Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OH} = \text{Max}$ , $V_{IL} = \text{Max}$ , $V_{IH} = \text{Min}$	2.4			V
$V_{OL}$	LOW Level Output Voltage	$V_{CC} = \text{Min}$ , $I_{OL} = \text{Max}$ , $V_{IH} = \text{Min}$ , $V_{IL} = \text{Max}$			0.3	V
$I_I$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$ , $V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$	HIGH Level Input Current	$V_{CC} = \text{Max}$ , $V_I = 2.4 \text{ V}$	Inputs		20	$\mu\text{A}$
			$D_n$		30	
$I_{IL}$	LOW Level Input Current	$V_{CC} = \text{Max}$ , $V_I = 0.3 \text{ V}$	Inputs		-400	$\mu\text{A}$
			$D_n$		-600	
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)	-2.5		-25	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ (Note 4)			16.5	mA

**Note 2:** All typicals are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

**Note 3:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

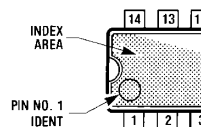
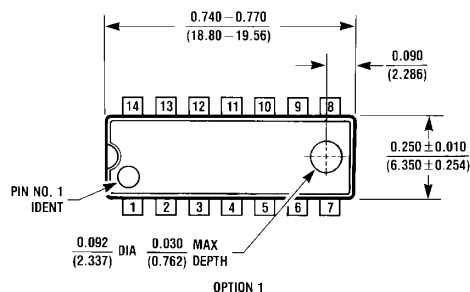
**Note 4:**  $I_{CC}$  is measured with all outputs open and all inputs grounded.

## Switching Characteristics

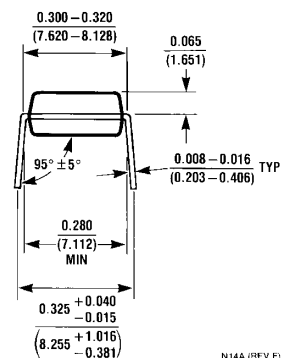
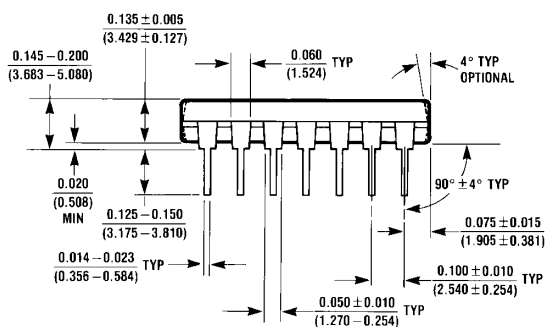
$V_{CC} = +5.0 \text{ V}$ ,  $T_A = +25^\circ\text{C}$  (See Waveforms and Load Configurations)

Symbol	Parameter	Min	Max	Units
$t_{PLH}$	Propagation Delay		45	ns
$t_{PHL}$	$\overline{E}$ to $Q_n$		36	
$t_{PLH}$	Propagation Delay		30	ns
$t_{PHL}$	$D_n$ to $Q_n$		30	
$t_{PLH}$	Propagation Delay, $\overline{MR}$ to $Q_n$		30	ns
$t_{PHL}$	Propagation Delay, $\overline{S}_n$ to $Q_n$		33	ns

# Physical Dimensions inches (millimeters) unless otherwise noted



OPTION 02



N14A (REV F)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N14A

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