



National Semiconductor

August 1998

## 54ACT823 9-Bit D Flip-Flop

### General Description

The ACT823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The ACT823 offers noninverting outputs and is fully compatible with AMD's Am29823.

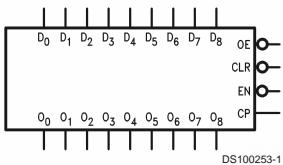
### Features

- Outputs source/sink 24 mA

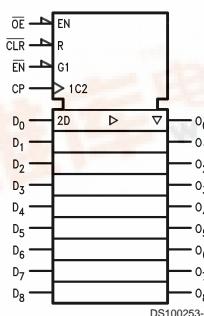
### Ordering Code

Order Number	Package Number	Package Description
54ACT823DMQB	J24A	24-Lead Ceramic Dual-in-line
54ACT823FMQB	W24C	24-Lead Cerpack
54ACT823LMQB	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C

### Logic Symbols



IEEE/IEC

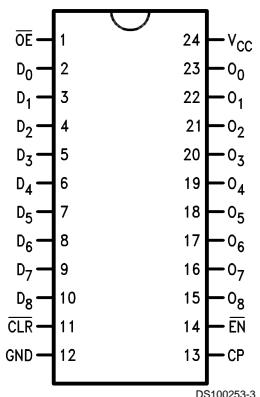


Pin Names	Description
D <sub>0</sub> -D <sub>8</sub>	Data Inputs
O <sub>0</sub> -O <sub>8</sub>	Data Outputs
OE	Output Enable
CLR	Clear
CP	Clock Input
EN	Clock Enable

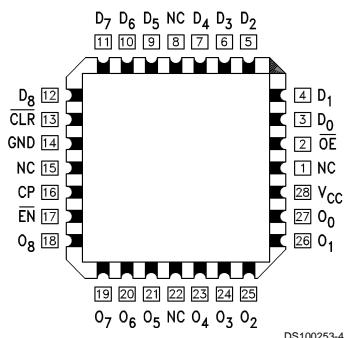
FACT™ is a trademark of Fairchild Semiconductor Corporation.  
TRI-STATE™ is a trademark of National Semiconductor Corporation.

## Connection Diagrams

Pin Assignment for DIP  
and Cerpak



Pin Assignment  
for LCC



## Functional Description

The ACT823 consists of nine D-type edge-triggered flip-flops. These have TRI-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With  $\overline{OE}$  LOW, the contents of the flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops. In addition to the Clock and Output En-

able pins, there are Clear ( $\overline{CLR}$ ) and Clock Enable ( $\overline{EN}$ ) pins. These devices are ideal for parity bus interfacing in high performance systems.

When  $\overline{CLR}$  is LOW and  $\overline{OE}$  is LOW, the outputs are LOW. When  $\overline{CLR}$  is HIGH, data can be entered into the flip-flops. When  $\overline{EN}$  is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the  $\overline{EN}$  is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

## Function Table

$\overline{OE}$	Inputs					Internal	Output	Function
	$\overline{CLR}$	$\overline{EN}$	CP	D	Q			
H	X	L	N	L	L	Z	High Z	
H	X	L	N	H	H	Z	High Z	
H	L	X	X	X	L	Z	Clear	
L	L	X	X	X	L	L	Clear	
H	H	H	X	X	NC	Z	Hold	
L	H	H	X	X	NC	NC	Hold	
H	H	L	N	L	L	Z	Load	
H	H	L	N	H	H	Z	Load	
L	H	L	N	L	L	L	Load	
L	H	L	N	H	H	H	Load	

H = HIGH Voltage Level

L = LOW Voltage Level

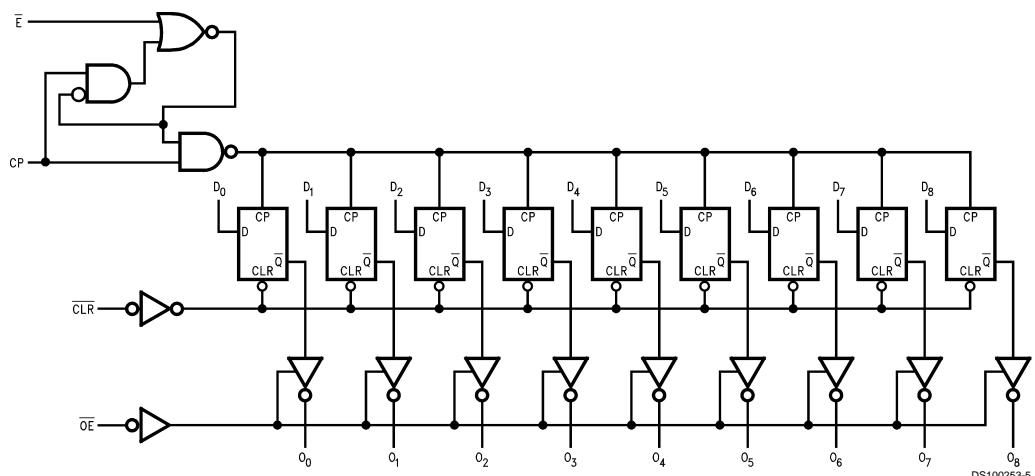
X = Immaterial

Z = High Impedance

N = LOW-to-HIGH Transition

NC = No Change

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to 7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C

Junction Temperature ( $T_J$ )

CDIP

175°C

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
54ACT	-55°C to +125°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$	Units	Conditions
$V_{IH}$	Minimum High Level Input Voltage	4.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	2.0		
$V_{IL}$	Maximum Low Level Input Voltage	4.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	0.8		
$V_{OH}$	Minimum High Level Output Voltage	4.5	3.7	V	$I_{OH} = -24\text{ mA}$
$V_{OL}$	Maximum Low Level Output Voltage	4.5	0.5	V	$I_{OL} = 24\text{ mA}$
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}, \text{ GND}$
$I_{OZ}$	Maximum TRI-STATE Current	5.5	±10.0	µA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{ GND}$
$I_{CCT}$	Maximum $I_{CC}$ /Input	5.5	1.6	mA	$V_I = V_{CC} - 2.1V$
$I_{OLD}$	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	$V_{OLD} = 1.65V \text{ Max}$
$I_{OHD}$		5.5	-50	mA	$V_{OHD} = 3.85V \text{ Min}$
$I_{CC}$	Maximum Quiescent Supply Current	5.5	160	µA	$V_{IN} = V_{CC}$ or GND

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V) (Note 4)	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $C_L = 50\text{ pF}$		Units
			Min	Max	
$f_{max}$	Maximum Clock Frequency	5.0	95		MHz
$t_{PLH}$	Propagation Delay CP to $O_n$	5.0	1.0	12.0	ns

### AC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V) (Note 4)	T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		Units
			Min	Max	
t <sub>PHL</sub>	Propagation Delay CP to O <sub>n</sub>	5.0	1.0	12.0	ns
t <sub>PHL</sub>	Propagation Delay CLR to O <sub>n</sub>	5.0	1.0	18.0	ns
t <sub>PZH</sub>	Output Enable Time OĒ to O <sub>n</sub>	5.0	1.0	11.5	ns
t <sub>PZL</sub>	Output Enable Time OĒ to O <sub>n</sub>	5.0	1.0	12.0	ns
t <sub>PHZ</sub>	Output Disable Time OĒ to O <sub>n</sub>	5.0	1.0	13.5	ns
t <sub>PLZ</sub>	Output Disable Time OĒ to O <sub>n</sub>	5.0	1.0	12.0	ns

Note 4: Voltage Range 5.0 is 5.0V ±0.5V

### AC Operating Requirements

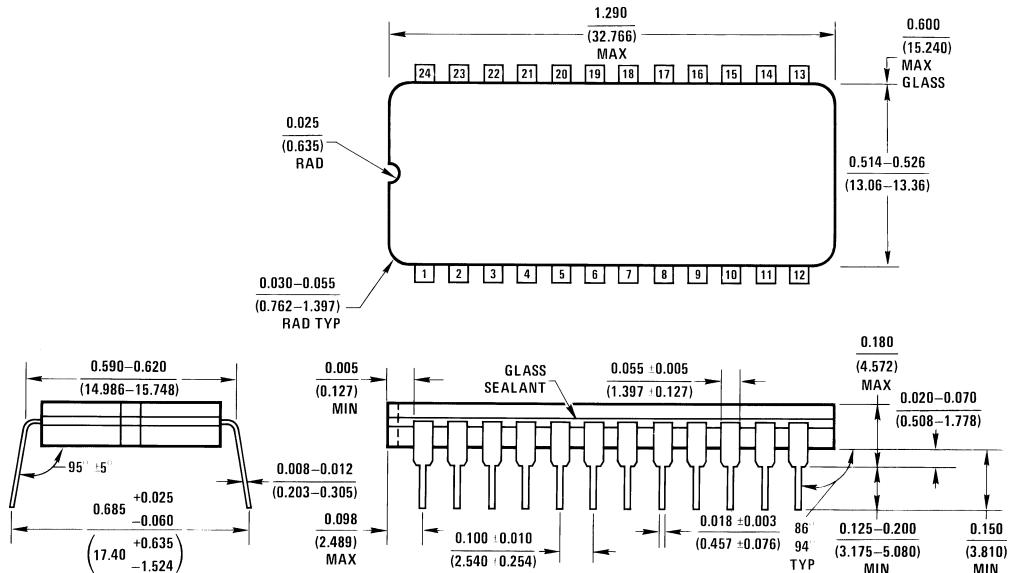
Symbol	Parameter	V <sub>CC</sub> (V) (Note 5)	T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		Units
			Guaranteed Minimum		
t <sub>s</sub>	Setup Time, HIGH or LOW D to CP	5.0	4.0		ns
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	3.0		ns
t <sub>s</sub>	Setup Time, HIGH or LOW EN̄ to CP	5.0	4.0		ns
t <sub>h</sub>	Hold Time, HIGH or LOW EN̄ to CP	5.0	3.0		ns
t <sub>w</sub>	CP Pulse Width HIGH or LOW	5.0	6.0		ns
t <sub>w</sub>	CLR Pulse Width, LOW	5.0	7.5		ns
t <sub>rec</sub>	CLR to CP Recovery Time	5.0	4.5		ns

Note 5: Voltage Range 5.0 is 5.0V ±0.5V

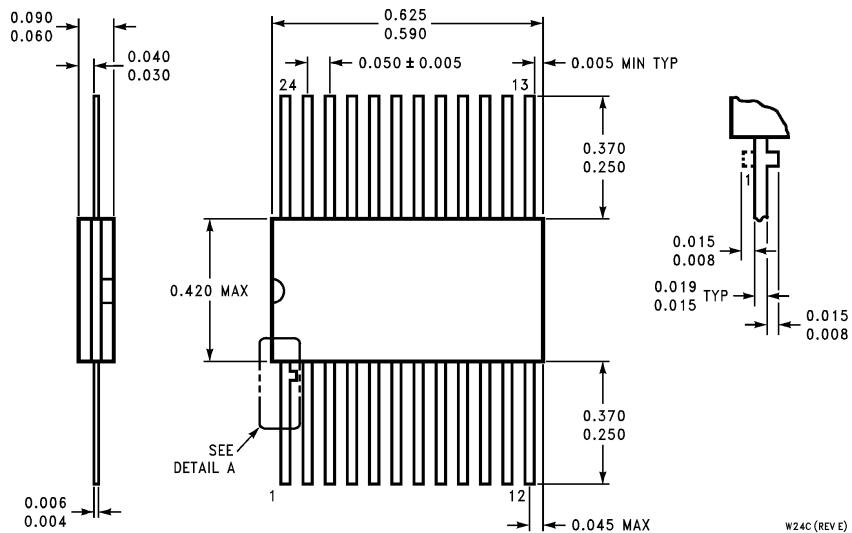
## Capacitance

Symbol	Parameter	Max	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = \text{OPEN}$
$C_{PD}$	Power Dissipation Capacitance	4.4	pF	$V_{CC} = 5.0V$

**Physical Dimensions** inches (millimeters) unless otherwise noted



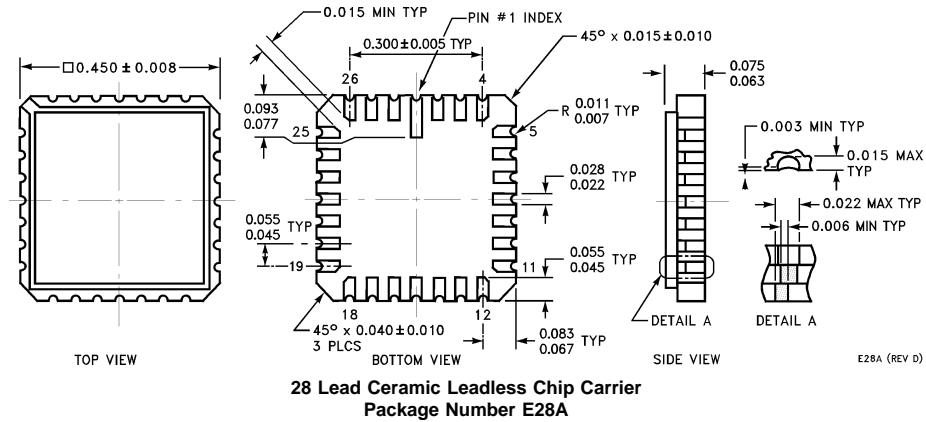
**24 Lead Ceramic Dual-in-line  
Package Number J24A**



24 Lead Cerpack  
Package Number W24C

## 54ACT823 9-Bit D Flip-Flop

### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28 Lead Ceramic Leadless Chip Carrier  
Package Number E28A

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMI-CONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor  
Corporation  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com

[www.national.com](http://www.national.com)

National Semiconductor  
Europe  
Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 1 80-530 85 85  
English Tel: +49 (0) 1 80-532 78 32  
Français Tel: +49 (0) 1 80-532 93 58  
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor  
Asia Pacific Customer  
Response Group  
Tel: 65-2544466  
Fax: 65-2504466  
Email: sea.support@nsc.com

National Semiconductor  
Japan Ltd.  
Tel: 81-3-5620-6175  
Fax: 81-3-5620-6179