

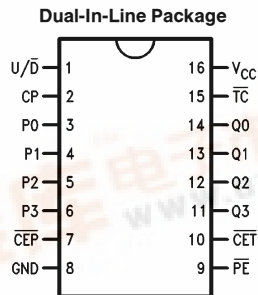
June 1989

## 54LS168 Synchronous Bi-Directional BCD Decade Counter

### General Description

The 54LS168 is a fully synchronous 4-state up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. It counts in the BCD (8421) sequence and all state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

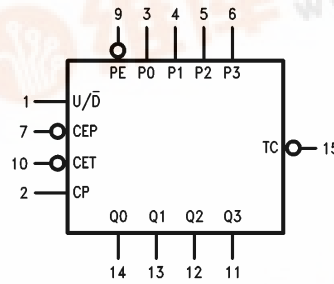
### Connection Diagram



TL/F/10207-1

Order Number 54LS168DMQB,  
54LS168FMQB or 54LS168LMQB  
See NS Package Number  
E20A, J16A or W16A

### Logic Symbol



TL/F/10207-2

V<sub>CC</sub> = Pin 16  
GND = Pin 8

| Pin Names | Description                              |
|-----------|--|
| CEP       | Count Enable Parallel Input (Active LOW) |
| CET       | Count Enable Trickle Input (Active LOW)  |
| CP        | Clock Pulse Input (Active Rising Edge)   |
| P0-P3     | Parallel Data Inputs                     |
| PE        | Parallel Enable Input (Active LOW)       |
| U/D       | Up-Down Count Control Input              |
| Q0-Q3     | Flip-Flop Outputs                        |
| TC        | Terminal Count Output (Active LOW)       |

54LS168 Synchronous Bi-Directional BCD Decade Counter



## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 5.5V            |
| Operating Free Air Temperature Range |                 |
| 54LS                                 | -55°C to +125°C |
| Storage Temperature Range            | -65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol             | Parameter                         | 54LS168 |     |      | Units |
|--------------------|-----------------------------------|---------|-----|------|-------|
|                    |                                   | Min     | Nom | Max  |       |
| V <sub>CC</sub>    | Supply Voltage                    | 4.5     | 5   | 5.5  | V     |
| V <sub>IH</sub>    | High Level Input Voltage          | 2       |     |      | V     |
| V <sub>IL</sub>    | Low Level Input Voltage           |         |     | 0.7  | V     |
| I <sub>OH</sub>    | High Level Output Current         |         |     | -0.4 | mA    |
| I <sub>OL</sub>    | Low Level Output Current          |         |     | 4    | mA    |
| T <sub>A</sub>     | Free Air Operating Temperature    | -55     |     | 125  | °C    |
| t <sub>s</sub> (H) | Setup Time HIGH or LOW            | 15      |     |      | ns    |
| t <sub>s</sub> (L) | P <sub>n</sub> , CEP or CET to CP | 15      |     |      | ns    |
| t <sub>h</sub> (H) | Hold Time HIGH or LOW             | 5       |     |      | ns    |
| t <sub>h</sub> (L) | P <sub>n</sub> , CEP or CET to CP | 5       |     |      | ns    |
| t <sub>s</sub> (H) | Setup Time HIGH or LOW            | 20      |     |      | ns    |
| t <sub>s</sub> (L) | $\overline{PE}$ to CP             | 20      |     |      | ns    |
| t <sub>h</sub> (H) | Hold Time HIGH or LOW             | 0       |     |      | ns    |
| t <sub>h</sub> (L) | $\overline{PE}$ to CP             | 0       |     |      | ns    |
| t <sub>s</sub> (H) | Setup Time HIGH or LOW            | 25      |     |      | ns    |
| t <sub>s</sub> (L) | U/ $\overline{D}$ to CP           | 25      |     |      | ns    |
| t <sub>h</sub> (H) | Hold Time HIGH or LOW             | 0       |     |      | ns    |
| t <sub>h</sub> (L) | U/ $\overline{D}$ to CP           | 0       |     |      | ns    |
| t <sub>w</sub> (H) | CP Pulse Width HIGH or LOW        | 20      |     |      | ns    |
| t <sub>w</sub> (L) |                                   | 20      |     |      | ns    |

## Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol   | Parameter                         | Conditions   | Min  | Typ (Note 1) | Max  | Units         |
|----------|-----------------------------------|--|--|--------------|------|---------------|
| $V_I$    | Input Clamp Voltage               | $V_{CC} = \text{Min}, I_I = -18 \text{ mA}$  |  |              | -1.5 | V             |
| $V_{OH}$ | High Level Output Voltage         | $V_{CC} = \text{Min}, I_{OH} = \text{Max}, V_{IL} = \text{Max}, V_{IH} = \text{Min}$ | 2.5  |              |      | V             |
| $V_{OL}$ | Low Level Output Voltage          | $V_{CC} = \text{Min}, I_{OL} = \text{Max}, V_{IH} = \text{Min}, V_{IL} = \text{Max}$ |  |              | 0.4  | V             |
| $I_I$    | Input Current @ Max Input Voltage | $V_{CC} = \text{Max}, V_I = 10.0\text{V}$  |  |              | 0.1  | mA            |
| $I_{IH}$ | High Level Input Current          | $V_{CC} = \text{Max}, V_I = 2.7\text{V}$   | Inputs   |              | 20   | $\mu\text{A}$ |
|          |                                   |  | $\overline{\text{CET}}$  |              | 40   |               |
| $I_{IL}$ | Low Level Input Current           | $V_{CC} = \text{Max}, V_I = 0.5\text{V}$   | Data   | -0.5         | -400 | $\mu\text{A}$ |
|          |                                   |  | CP, $\overline{\text{PE}}, U/\overline{\text{D}}, \overline{\text{CEP}}$ | -30          | -400 |               |
|          |                                   |  | $\overline{\text{CET}}$  | -60          | -800 |               |
| $I_{OS}$ | Short Circuit Output Current      | $V_{CC} = \text{Max}$ (Note 2)   | -20  |              | -100 | mA            |
| $I_{CC}$ | Supply Current                    | $V_{CC} = \text{Max}$ (Note 3)   |  |              | 34   | mA            |

**Note 1:** All typicals are at  $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$ .

**Note 2:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 3:**  $I_{CC}$  is measured with all outputs open and all inputs grounded.

## Switching Characteristics

$V_{CC} = +5.0\text{V}, T_A = +25^\circ\text{C}$  (See Section 1 for test waveforms and output load)

| Symbol                               | Parameter  | 54LS168               |          | Units |
|--------------------------------------|--|-----------------------|----------|-------|
|                                      |  | $C_L = 15 \text{ pF}$ |          |       |
|                                      |  | Min                   | Max      |       |
| $f_{\text{Max}}$                     | Maximum Clock Frequency  | 25                    |          | MHz   |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation Delay<br>CP to $Q_n$                                       |                       | 20<br>20 | ns    |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation Delay<br>CP to $\overline{\text{TC}}$                      |                       | 30<br>30 | ns    |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation Delay<br>$\overline{\text{CET}}$ to $\overline{\text{TC}}$ |                       | 15<br>20 | ns    |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation Delay<br>$U/\overline{\text{D}}$ to $\overline{\text{TC}}$ |                       | 25<br>25 | ns    |

## Functional Description

The 'LS168 uses edge-triggered D-type flip-flops and has no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When  $\overline{PE}$  is LOW, the data on the P0–P3 inputs enters the flip-flops on the next rising edge of the clock. In order for counting to occur, both  $\overline{CEP}$  and  $\overline{CET}$  must be LOW and  $\overline{PE}$  must be HIGH. The U/D input then determines the direction of counting. The Terminal Count ( $\overline{TC}$ ) output is normally HIGH and goes LOW, provided that  $\overline{CET}$  is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 9 in the COUNT UP mode. The  $\overline{TC}$  output state is not a function of the Count Enable Parallel ( $\overline{CEP}$ ) input level. The  $\overline{TC}$  output of the 'LS168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'LS168 will return to the legitimate sequence within two counts. Since the  $\overline{TC}$  signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on  $\overline{TC}$ . For this reason the use of  $\overline{TC}$  as a clock signal is not recommended (see logic equation below).

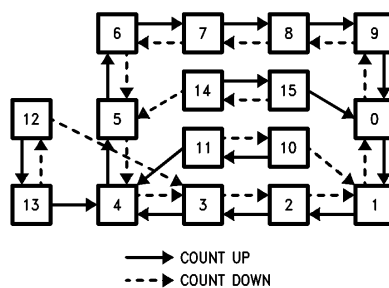
1. Count Enable =  $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$
2. Up:  $\overline{TC} = Q_0 \cdot Q_3 \cdot (U/D) \cdot \overline{CET}$
3. Down:  $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/D) \cdot \overline{CET}$

'LS168 Mode Select Table

| $\overline{PE}$ | $\overline{CEP}$ | $\overline{CET}$ | U/D | Action on Rising Clock Edge    |
|-----------------|------------------|------------------|-----|--------------------------------|
| L               | X                | X                | X   | Load ( $P_n \rightarrow Q_n$ ) |
| H               | L                | L                | H   | Count Up (Increment)           |
| H               | L                | L                | L   | Count Down (Decrement)         |
| H               | H                | X                | X   | No Change (Hold)               |
| H               | X                | H                | X   | No Change (Hold)               |

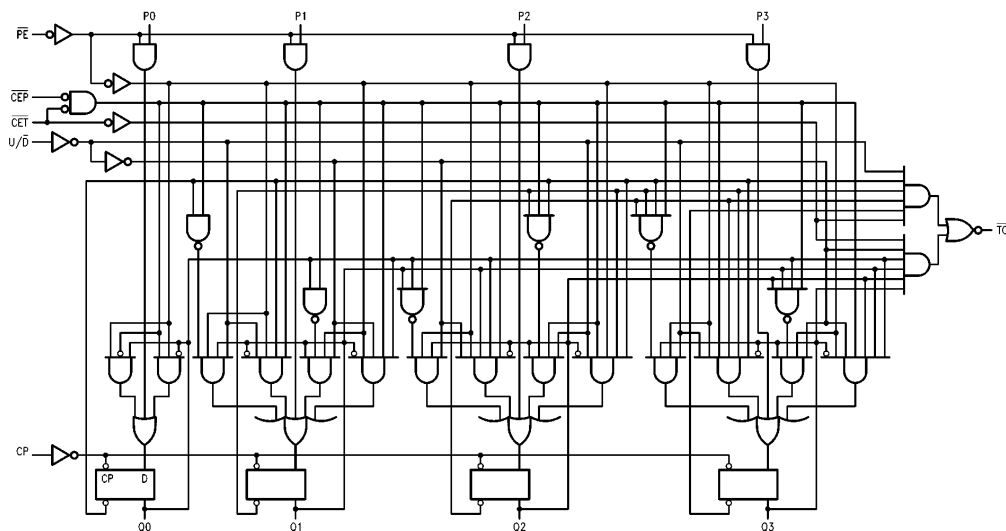
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## State Diagram



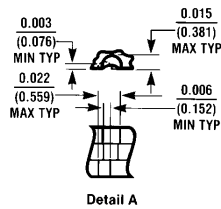
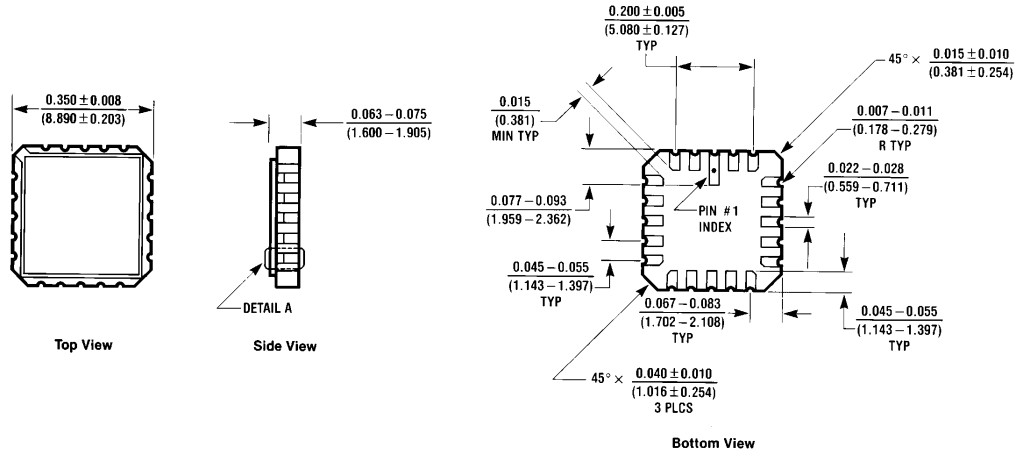
TL/F/10207-3

## Logic Diagram



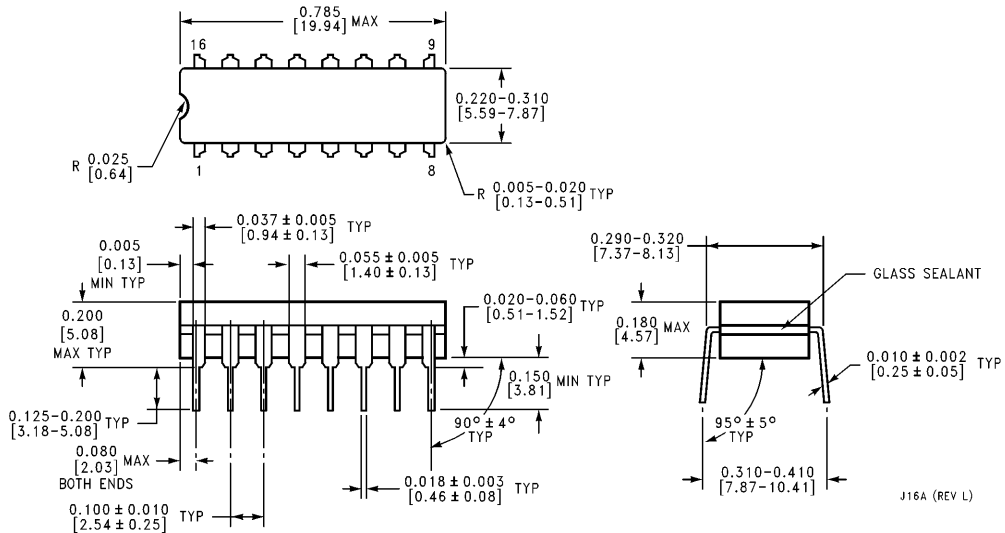
TL/F/10207-4

**Physical Dimensions** inches (millimeters)



**Ceramic Leadless Chip Carrier Package (E)**  
**Order Number 54LS168LMQB**  
**NS Package Number E20A**

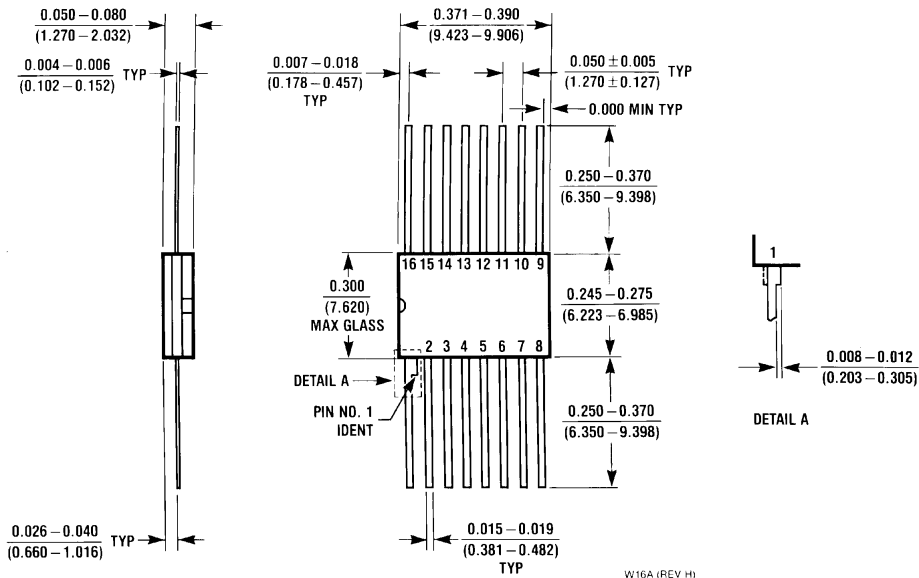
E20A (REV D)



**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number 54LS168DMQB**  
**NS Package Number J16A**

J16A (REV L)

**Physical Dimensions** inches (millimeters) (Continued)



**16-Lead Ceramic Flat Package (W)**  
**Order Number 54LS168FMQB**  
**NS Package Number W16A**

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**National Semiconductor Corporation**  
 1111 West Bardin Road  
 Arlington, TX 76017  
 Tel: 1(800) 272-9959  
 Fax: 1(800) 737-7018

**National Semiconductor Europe**  
 Fax: (+49) 0-180-530 85 86  
 Email: cnjwge@tevm2.nsc.com  
 Deutsch Tel: (+49) 0-180-530 85 85  
 English Tel: (+49) 0-180-532 78 32  
 Français Tel: (+49) 0-180-532 93 58  
 Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**  
 13th Floor, Straight Block,  
 Ocean Centre, 5 Canton Rd.  
 Tsimshatsui, Kowloon  
 Hong Kong  
 Tel: (852) 2737-1600  
 Fax: (852) 2736-9960

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 Tel: 81-043-299-2309  
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