

LS273



54LS273/DM74LS273 8-Bit Register with Clear

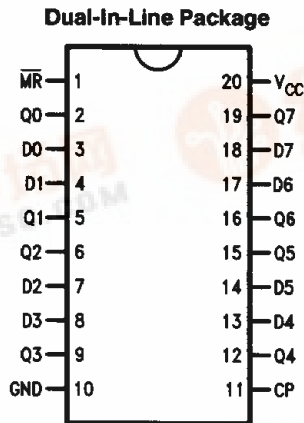
General Description

The 'LS273 is a high speed 8-bit register, consisting of eight D-type flip-flops with a common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch row spacing.

Features

- Edge-triggered
- 8-bit high speed register
- Parallel in and out
- Common clock and master reset

Connection Diagram



TL/F/9825-1

**Order Number 54LS273DMQB, 54LS273FMQB,
54LS273LMQB, DM74LS273M or DM74LS273N
See NS Package Number E20A, J20A, M20B,
N20A or W20A**

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D0-D7	Data Inputs
MR	Asynchronous Master Reset Input (Active LOW)
Q0-Q7	Flip-Flop Outputs



Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	-55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	54LS273			DM74LS273			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			-0.4			-0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
T _A	Free Air Operating Temperature	-55		125	0		70	°C
t _{s(H)} t _{s(L)}	Setup Time HIGH or LOW D _n to CP	15			15			ns
t _{h(H)} t _{h(L)}	Hold Time HIGH or LOW D _n to CP	5			5			ns
t _{w(H)} t _{w(L)}	CP Pulse Width HIGH or LOW	20			20			ns
t _{w(L)}	MR Pulse Width LOW	20			20			ns
t _{rec}	Recovery Time MR to CP	15			15			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max	54LS	2.5		V
			DM74	2.7	3.4	
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IH} = Min	54LS		0.4	V
			DM74		0.35	
		I _{OL} = 4 mA, V _{CC} = Min	DM74		0.25	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 10V			0.1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			-0.4	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	54LS	-20	-100	mA
			DM74	-20	-100	
I _{CC}	Supply Current	V _{CC} = Max			27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics



V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C _L = 15 pF				Units
		54LS		DM74LS		
		Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	30		30		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n		32		24	ns
t _{PLH}	Propagation Delay MR to Q _n		32		27	ns

Functional Description

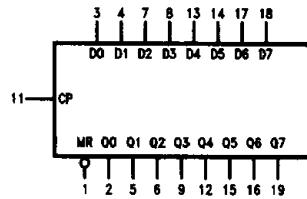
The 'LS273 is an 8-bit parallel register with a common Clock and common Master Reset. When the MR input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

Truth Table

MR	Inputs		Outputs
	CP	D _n	
L	X	X	L
H		H	H
H		L	L

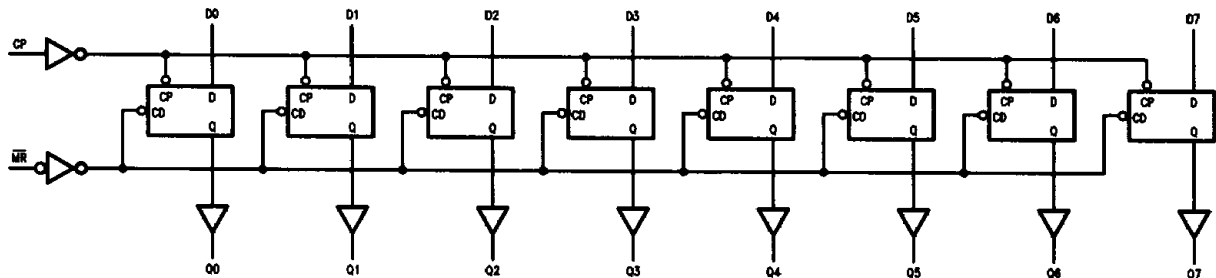
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Symbol



TL/F/9825-2
V_{CC} = Pin 20
GND = Pin 10

Logic Diagram



TL/F/9825-3