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National Semiconductor

April 1990

# DP8483 TTL to 100k ECL Level Translator with Latch

DP8483 TTL to 100k ECL Level Translator with Latch

## General Description

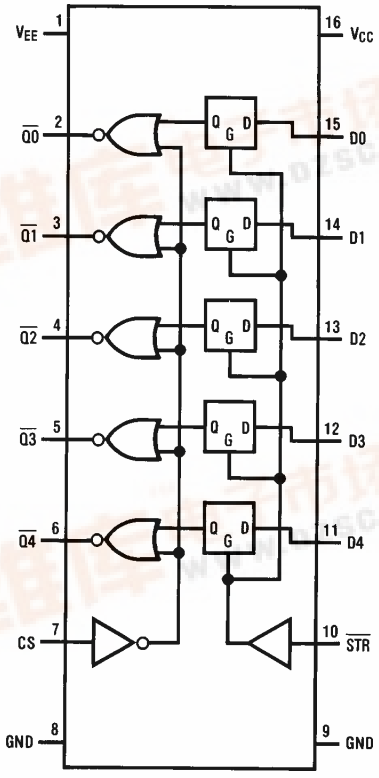
This circuit translates TTL input levels to ECL output levels and provides a fall-through latch. The outputs are gated with CS providing for wire ORing of outputs. The strobe and chip select inputs operate at ECL levels.

## Features

- 16-pin DIP or S.O.
- ECL control inputs
- CS provided for wire ORing of output bus
- 100k ECL I/O compatible
- 3.0 ns typical propagation delay

## Logic and Connection Diagram

Dual-In-Line Package




TL/F/5864–1

Top View

## Truth Table

| D | $\overline{Q}$ | $\overline{STR}$ | CS |
|---|---|---|---|
| H | L | L | H |
| L | H | L | H |
| X | $\overline{Q}$ | H | H |
| X | L | X | L |

H = high level (most positive)
L = low level (most negative)
X = don't care

**Order Number DP8483J,**
**DP8483M or DP8483N**
**See NS Package Number J16A, M16B or N16A**

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RRD-B30M105/Printed in U. S. A.

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## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| $V_{EE}$ Supply Voltage | −8V |
| $V_{CC}$ Supply Voltage | 7V |
| Input Voltage (ECL) | GND to $V_{EE}$ |
| Input Voltage (TTL) | −1V to 5.5V |
| Output Current | 50 mA |
| Maximum Power Dissipation* at 25°C | |
| Molded Package | 1476 mW |
| Storage Temperature | −65°C to +150°C |

*Derate molded package 11.8 mW/°C above 25°C.

## Recommended Operating Conditions

| | |
|---|---|
| $V_{EE}$ Supply Voltage | −4.5V +7% |
| $V_{CC}$ Supply Voltage | 5.0V ±10% |
| $T_A$, Ambient Temperature | 0°C to 85°C |

## Electrical Characteristics (TTL Logic) (Notes 2 and 3)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | | | V |
| $I_{IL}$ | Input Low Current | $V_{IN}=0.5V$ | | −25 | −200 | μA |
| $I_{IH}$ | Input High Current | $V_{IN}=2.5V$ | | 1.0 | 40 | μA |
| $V_{CLAMP}$ | Input Clamp Voltage | $I_{IN}=-12$ mA | | −0.9 | −1.2 | V |
| $I_{CC}$ | Supply Current | $V_{CC}=5.5V$ | | 10 | 20 | mA |

## Electrical Characteristics (ECL Logic) (Notes 2 and 3)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | $V_{EE}=-4.5V$ | −1810 | | −1475 | mV |
| $V_{IH}$ | Input High Voltage | $V_{EE}=-4.5V$ | −1165 | | −880 | mV |
| $I_{IL}$ | Input Low Current | $V_{IN}=-1.8V$ | | 45 | 150 | μA |
| $I_{IH}$ | Input High Current | $V_{IN}=-0.8V$ | | 75 | 200 | μA |
| $V_{OL}$ | Output Low Voltage | $V_{EE}=-4.5V$ | −1810 | −1705 | −1620 | mV |
| $V_{OH}$ | Output High Voltage | $V_{EE}=-4.5V$ | −1025 | −955 | −880 | mV |
| $V_{OLC}$ | Output Low Voltage | $V_{EE}=-4.5V$ | | | −1610 | mV |
| $V_{OHC}$ | Output High Voltage | $V_{EE}=-4.5V$ | −1035 | | | mV |
| $I_{EE}$ | Supply Current | $V_{EE}=-4.8V$ | | −65 | −85 | mA |

## Switching Characteristics (Notes 2 and 4)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PD1}$ | Strobe To Output Delay | (Note 4) | 1.5 | 3.0 | 6.0 | ns |
| $t_{PD2}$ | Data To Output Delay | | 2.5 | 4.5 | 7.5 | ns |
| $t_S$ | Data Set-Up Time to Strobe | | 5.0 | 2.0 | | ns |
| $t_H$ | Data Hold Time | | 1.0 | 0 | | ns |
| $t_{PW}$ | Strobe Pulse Width | | 5.0 | 3.0 | | ns |
| $t_{PD3}$ | Chip Select to Output Delay | | 1.0 | 2.5 | 4.0 | ns |
| $t_{SCS}$ | Data Set-Up Time to Chip Select | | 5.5 | 3.0 | | ns |

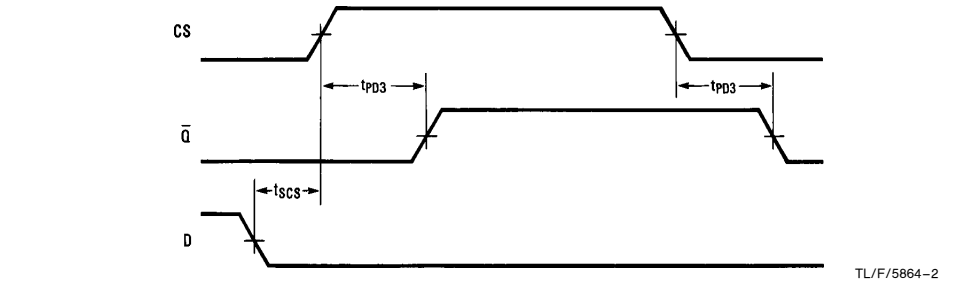
**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Unless otherwise specified, min/max limits apply across the 0°C to 85°C ambient temperature range in still air and across the specified supply variations. All typical values are for 25°C and nominal supply.

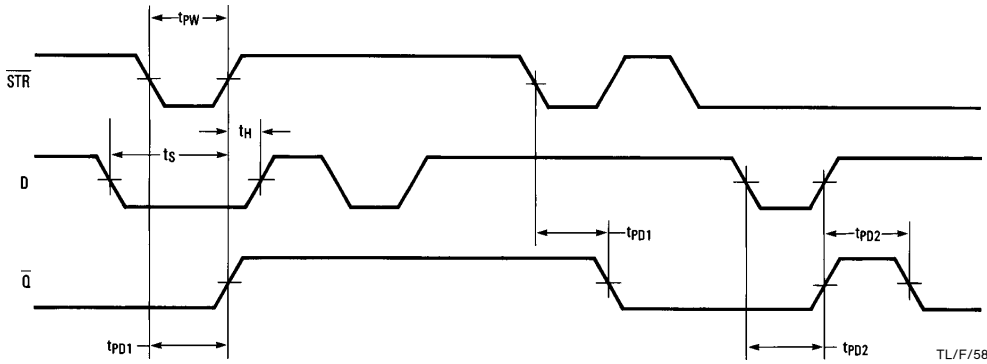
**Note 3:** All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

**Note 4:** Unless otherwise specified, all AC measurements are referenced from the 1.5V level of the TTL input and to/from the 50% point of the ECL signal and a 50Ω resistor to −2V is the load. ECL input rise and fall times are 0.7 ns ±0.1 ns from 20% to 80%. TTL input characteristics is 0V to 3V with $t_r=t_f\leq 3$ ns measured from 10% to 90%.

## Switching Time Waveforms

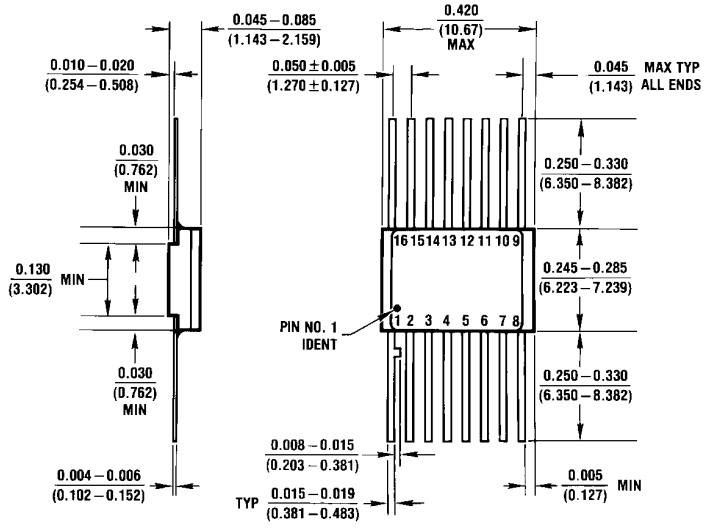



TL/F/5864–2



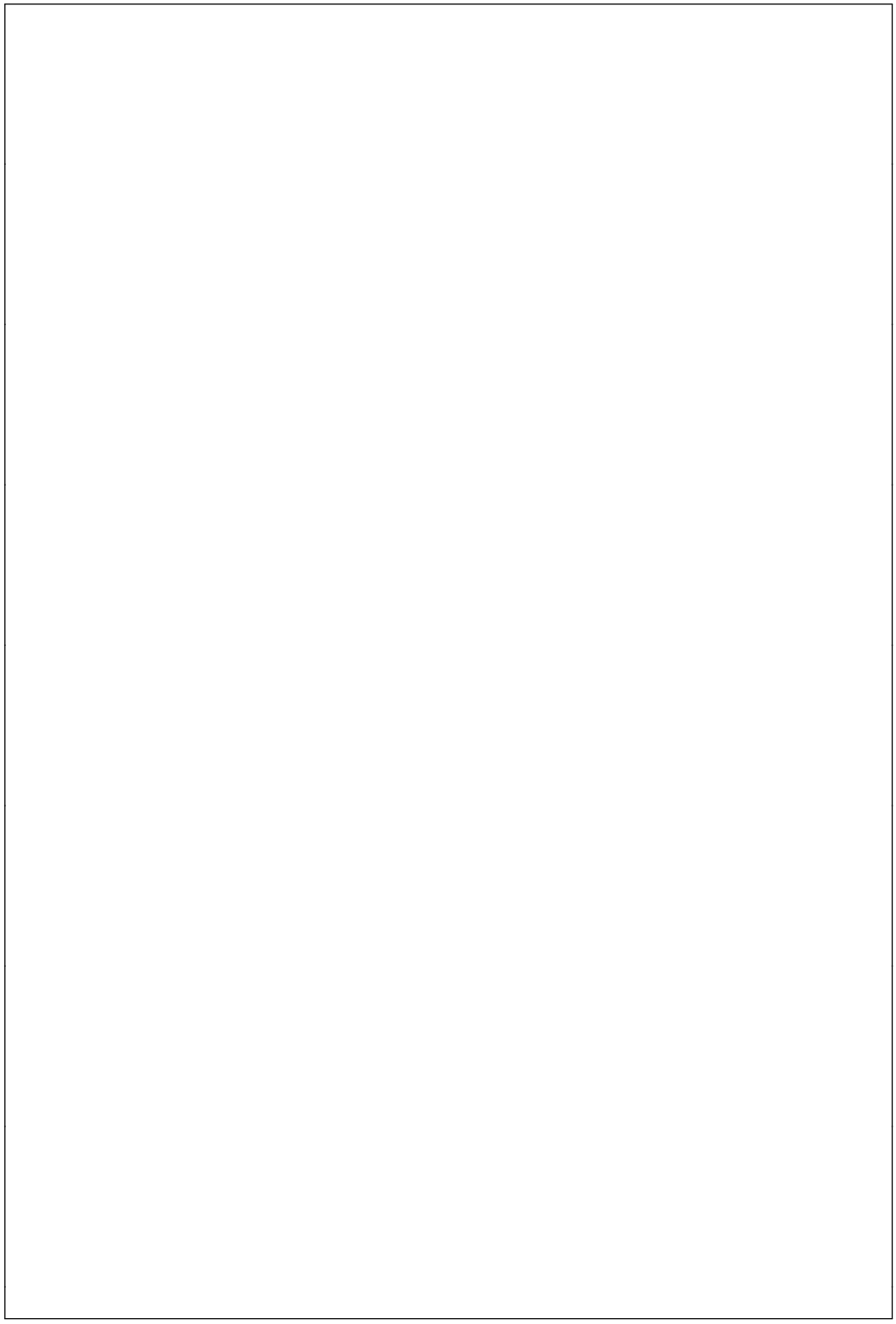

TL/F/5864–3

## Physical Dimensions inches (millimeters)

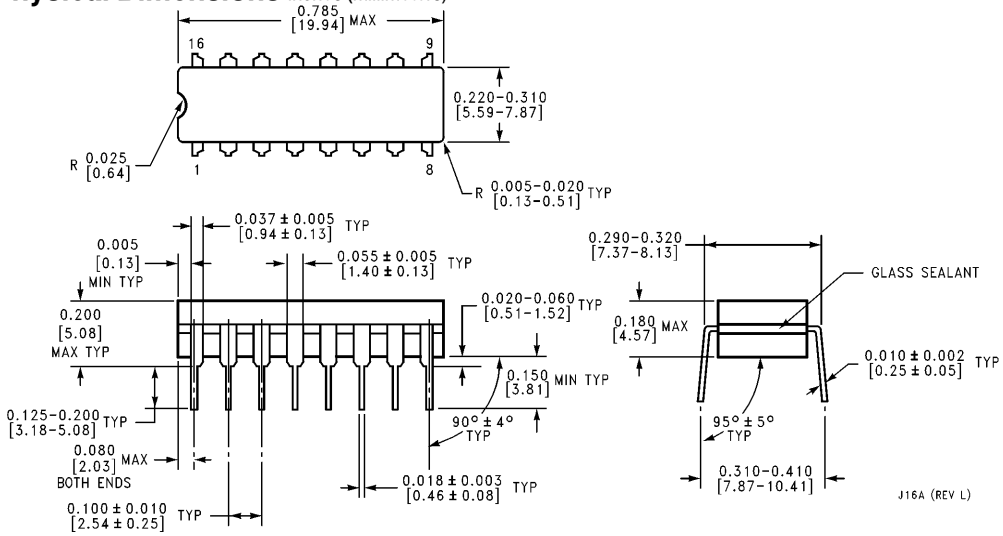



F16B (REV K)

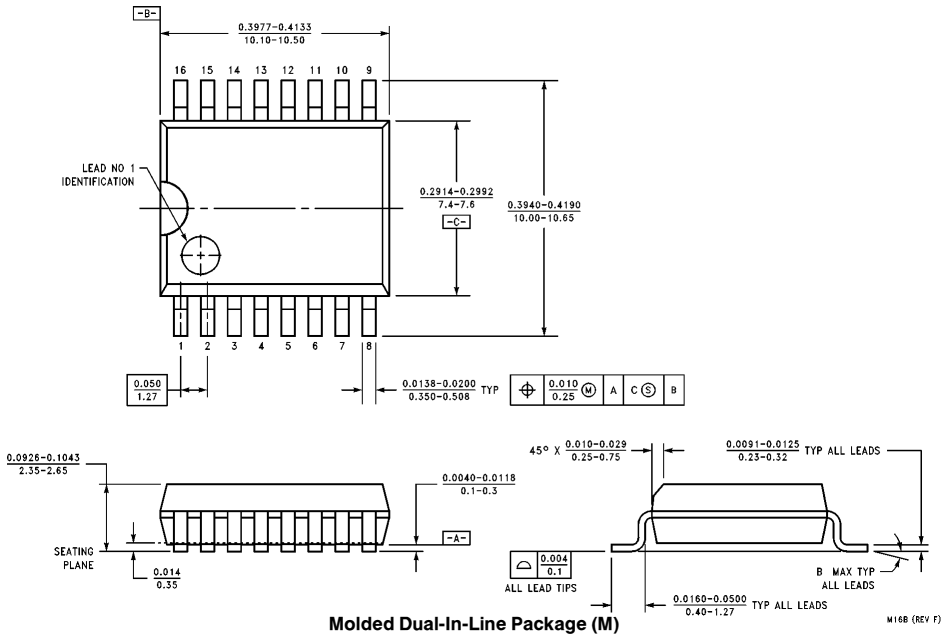
**Ceramic Flat Package (F)**
**Order Number DP8483F**
**NS Package Number F16B**



## Physical Dimensions inches (millimeters)

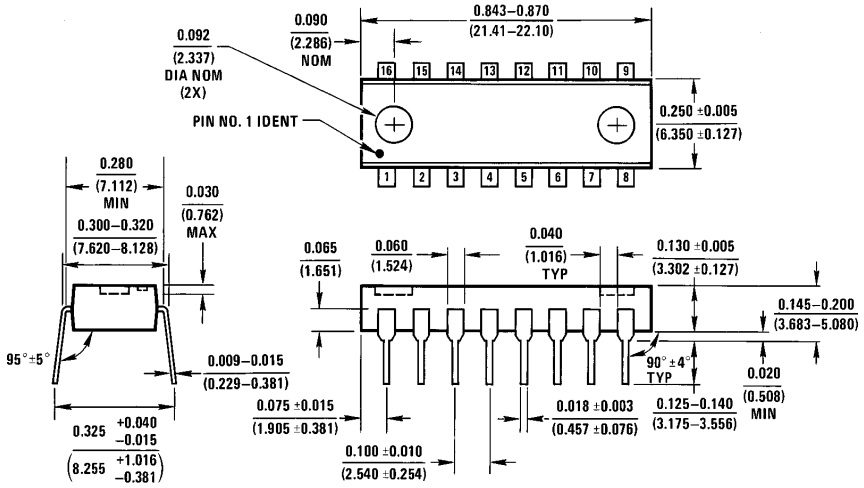



**Ceramic Dual-In-Line Package (J)**
**Order Number DP8483J**
**NS Package Number J16A**




**Molded Dual-In-Line Package (M)**
**Order Number DP8483M**
**NS Package Number M16B**

## Physical Dimensions inches (millimeters) (Continued)




N16A (REV E)

**Molded Dual-In-Line Package (N)**
**Order Number DP8483N**
**NS Package Number N16A**

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**National Semiconductor Corporation**
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

**National Semiconductor Europe**
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**
Tel: 81-043-299-2309
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