



SLVS440A-JANUARY 2003-REVISED SEPTEMBER 2003

# DIGITALLY ADJUSTABLE LCD BOOST CONVERTER

### **FEATURES**

- Input Voltage Range . . . 1.8 V to 6.0 V
- Up to 85% Efficiency

TEXAS

www.ti.com

- Digitally Adjustable Output Voltage Control
- Disconnects Output From Input During Shutdown
- Switching Frequency . . . Up to 1 MHz
- No Load Quiescent Current . . . 40 μA Typ
- Thermal Shutdown Mode
- Shutdown Current . . . 0.1 µA Typ
- Available in Small 3mm × 3mm QFN package

### **APPLICATIONS**

- LCD Bias Supply For Small to Medium LCD Displays
- OLED Display Power Supply
- PDA, Pocket PC, Smart Phones
- Handheld Devices

## DESCRIPTION

The TPS61045 is a high frequency boost converter with digitally programmable output voltage and true shutdown. During shutdown the output is disconnected from the input by opening the internal input switch. This allows a controlled power up/down sequencing of the display. The output voltage can be increased or decreased in digital steps by applying a logic signal to the CTRL pin. The output voltage range, as well as the output voltage step size, can be programmed with the feedback divider network. With a high switching frequency of up to 1 MHz the TPS61045 allows the use of small external components and together, with the small 8-pin QFN package, a miminum system solution size is achieved.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments

2001 CTION DATA information is summark as of sublication data

onvright @ 2003 Toxas Instruments Incorporator



SLVS440A-JANUARY 2003-REVISED SEPTEMBER 2003



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

#### **ORDERING INFORMATION** (1)

T <sub>A</sub>	8 PIN QFN PACKAGE (DRB)	PACKAGE MARKING	
-40°C to 85°C	TPS61045DRB	BHT	

(1) The DRB package is available taped and reeled. Add R suffix (TPS61045DRBR) to order quantities of 3000 units per reel. Add T suffix (TPS61045DBRT) to order quagntities of 250 units per reel.

#### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	TPS61045
Supply voltage, V <sub>(VIN)</sub> (2)	-0.3 V to 7 V
Voltages, V <sub>(CTRL)</sub> , V <sub>(FB)</sub> , V <sub>(L)</sub> , V <sub>(DO)</sub> (2)	-0.3 V to V <sub>I</sub> + 0.3 V
Voltage, V <sub>(SW)</sub> (2)	30 V
Continuous power dissipation	See Dissipation Rating Table
Operating junction temperature range	-40°C to 150°C
Storage temperature range, T <sub>STG</sub>	-65°C to 150°C
Lead temperature (soldering, 10 sec)	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

#### **DISSIPATION RATING**

PACKAGE	T <sub>A</sub> ≤25°C POWER	DERATING FACTOR	T <sub>A</sub> = 70°C POWER	T <sub>A</sub> = 85°C POWER
	RATING	ABOVE T <sub>A</sub> = 25°C	RATING	RATING
8 pin QFN (DRB) (1)	370 mW	3.7 mW/°C	204 mW	148 mW

(1) The thermal resistance junction to ambient of the 8 pin QFN package is  $270^{\circ}$ C/W. Standard 2 layer PCB without vias for the thermal pad. See the application section on how to improve the thermal resistance  $R_{\Theta,A}$ .

#### **RECOMMENDED OPERATING CONDITIONS**

		MIN	ΤΥΡ	MAX	UNIT
V <sub>(VIN)</sub>	Input voltage range	1.8		6.0	V
V <sub>(SW)</sub>	Switch voltage			30	V
L	Inductor (1)		4.7		μH
f	Switching frequency (1)			1	MHz
C <sub>I(C2)</sub>	Input capacitor (C2) (1)		4.7		μF
C <sub>O(C3)</sub>	Output capacitor (C3) (1)		1		μF
T <sub>A</sub>	Operating ambient temperature	-40		85	°C
TJ	Operating junction temperature	-40		125	°C

(1) See application section for further information.



### **ELECTRICAL CHARACTERISTICS**

 $V_1 = 2.4 \text{ V}$ , CTRL =  $V_1$ ,  $V_0 = 18.0 \text{ V}$ ,  $I_0 = 10 \text{ mA}$ ,  $T_A = -40^{\circ}\text{C}$  to 85°C, typical values are at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY	CURRENT					
VI	Input voltage range		1.8		6.0	V
l <sub>Q</sub>	Operating quiescent current	I <sub>O</sub> = 0 mA, not switching		40	65	μA
I <sub>O(SD)</sub>	Shutdown current	CTRL = GND		0.1	1	μA
V <sub>UVLO</sub>	Under-voltage lockout threshold	V <sub>I</sub> falling		1.5	1.7	V
CTRL A	ND DAC OUTPUT					
V <sub>IH</sub>	CTRL high level input voltage		1.3			V
V <sub>IL</sub>	CTRL low level input voltage				0.3	V
l <sub>lkg</sub>	CTRL input leakage current	CTRL = GND or VIN			0.1	μA
V <sub>O(DO)</sub>	DAC output voltage range		0		1.233	V
	DAC resolution	6 Bit		19.6		mV
V <sub>O(DO)</sub>	DAC center output voltage	CTRL = high		607		mV
I <sub>O(SINK)</sub>	Maximum DAC sink current				30	μA
t <sub>(UP)</sub>	Increase output voltage one step	CTRL = high to low	1		60	μs
t <sub>(DWN)</sub>	Decrease the output voltage one step	CTRL = high to low	140		240	μs
t <sub>d1</sub>	Delay time between up/down steps	CTRL = low to high	1			μs
t <sub>(OFF)</sub>	Shutdown	CTRL = high to low	560			μs
INPUT S	WITCH (Q1), MAIN SWITCH (Q2) AND CU	JRRENT LIMIT	-			
V <sub>SW(Q2)</sub>	Main switch maximum voltage (Q2)				30	V
r <sub>ds(ON)</sub>	Main switch MOSFET on-resistance	V <sub>I</sub> = 2.4 V; I <sub>S</sub> = 200 mA		400	800	mΩ
I <sub>lkg(MAIN)</sub>	Main switch MOSFET leakage current	V <sub>S</sub> = 28 V		0.1	10	μA
I <sub>(LIM)</sub>	Main switch MOSFET current limit		300	375	450	mA
r <sub>ds(ON)</sub>	Input switch MOSFET on-resistance	V <sub>I</sub> = 2.4 V; I <sub>S</sub> = 200 mA		1	2	Ω
I <sub>lkg(IN)</sub>	Input switch MOSFET leakage current	$VL = GND, V_I = 6 V$		0.1	10	μA
OUTPUT	г		-i			
Vo	Output voltage range		Vin		28	V
V <sub>ref</sub>	Internal voltage reference			1.233		V
I <sub>(FB)</sub>	Feedback input bias current	VFB = 1.3 V		30	100	nA
$V_{(FB)}$	Feedback trip point voltage	1.8 V $\leq$ VI $\leq$ 6.0 V; V_O = 18 V, I_{(LOAD)}= 10 mA	1.208	1.233	1.258	V





(A) The Exposed Thermal Die Pad is connected to PGND. Connect this pad directly with the GND pin.

.

SLVS440A-JANUARY 2003-REVISED SEPTEMBER 2003



#### **TERMINAL FUNCTIONS**

TERMINAL		1/0	DESCRIPTION			
NAME	NO.	1/0	DESCRIPTION			
CTRL	5	I	Combined enable and digital output voltage programming pin. Pulling CTRL constantly high enables the device. When CTRL is pulled to GND, the device is disabled and the input is disconnected from the output by opening the integrated switch Q1. Pulsing CTRL low increases or decreases the output voltage. Refer to the <i>application information</i> section for further information.			
DO	3	0	Internal DAC output. DO programs the output voltage via the CTRL pin. Refer to the <i>application information</i> section for further information.			
FB	4	I	Feedback. FB must be connected to the output voltage-feedback divider.			
GND	7		Analog ground. GND must be directly connected to the PGND pin. Refer to the <i>application information</i> section for further information.			
L	1	0	Drain of the internal switch (Q1). Connect L to the inductor.			
PGND	6		Power ground			
SW	8	Ι	Drain of the integrated switch Q2. SW is connected to the inductor and anode of the Schottky rectifier diode.			
VIN	2	Ι	Input supply pin			







### **TYPICAL CHARACTERISTICS**

#### Table #IMPLIED. Table of Graphs

			FIGURE
η	Efficiency	vs Load current	Figure 2
		vs Input voltage	Figure 3
I <sub>DD(Q)</sub>	Quiescent current	vs Input voltage	Figure 4
V <sub>(FB)</sub>	Feedback voltage	vs Temperature	Figure 5
I <sub>(FB)</sub>	Feedback current	vs Temperature	Figure 6
r <sub>ds(on)</sub>	r <sub>ds(on)</sub> Main switch Q2	vs Temperature	Figure 7
		vs Input voltage	Figure 8
	r <sub>ds(on)</sub> Input switch Q1	vs Temperature	Figure 9
		vs Input voltage	Figure 10
V <sub>(DO)</sub>	V <sub>(DO)</sub> Voltage	vs CTRL input step	Figure 11
	Line transient response		Figure 12
	Load transient response		Figure 13
	PFM operation		Figure 14
	Soft start		Figure 15





3.6

VI - Input Voltage - V

Figure 4.

4.2

4.8

5.4

6.0

3.0

10 0

1.8

2.4





Figure 3.





### **Typical Characteristics (continued)**



### **Typical Characteristics (continued)**



Figure 14 . PFM Operation



#### **Typical Characteristics (continued)**



#### DETAILED DESCRIPTION

#### **OPERATION**

The TPS61045 operates with an input voltage range of 1.8 V to 6.0 V and generates output voltages up to 28 V. The device operates in a pulse frequency modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range and, with a switching frequency of up to 1 MHz, the device enables the use of small external components.

The converter monitors the output voltage and when the feedback voltage falls below the reference voltage of 1.233 V (typ) the main switch turns on and the current ramps up. The main switch turns off when the inductor current reaches the internally set peak current of 375 mA (typ). Refer to the *peak current control*section for more information. The second criteria that turns off the main switch is the maximum on-time of 6 µs (typ). This limits the maximum on-time of the converter in extreme conditions. As the switch is turned off, the external Schottky diode is forward biased delivering the current to the output. The main switch remains off until the minimum off time of 400 ns (typ) has passed and the feedback voltage is below the reference voltage again. Using this PFM peak current control scheme, the converter operates in discontinuous conduction mode (DCM) where the switching frequency depends on the input voltage, output voltage and output current. This gives a high efficiency over the entire load current range. This regulation scheme is inherently stable which allows a wider range for the selection of the inductor and output capacitor.

#### PEAK CURRENT CONTROL

The internal switch is turned on until the inductor current reaches the typical dc current limit ( $I_{LIM}$ ) of 375 mA. Due to the internal current limit delay of 100 ns (typ) the actual current exceeds the dc current limit threshold by a small amount. The typical peak current limit can be calculated:

$$I_{P(typ)} = I_{(LIM)} + \frac{V_{I}}{L} \times 100 \text{ ns}$$

$$I_{P(typ)} = 400 \text{ mA} + \frac{V_{I}}{L} \times 100 \text{ ns}$$
(1)

The higher the input voltage and the lower the inductor value, the greater the current limit overshoot.



### **DETAILED DESCRIPTION (continued)**

#### SOFTSTART

All inductive step-up converters exhibit high inrush current during start up if no special precautions are taken. This can cause voltage drops at the input rail during start-up, which may result in an unwanted or premature system shut down.

When the device is enabled, the internal input switch (Q1) is slowly turned on to reduce the in-rush current charging the capacitor (C2) connected to pin L. Furthermore, the TPS61045 limits this in-rush current during start-up by increasing the current limit in two steps starting from  $I_{LIM}/4$  for 256 switch cycles to  $I_{LIM}/2$  for the next 256 switch cycles.

#### ENABLE (CTRL PIN)

The CTRL pin serves two functions. One is the enable and disable of the device. The other is the output voltage programming of the device. If the digital interface is not required, the CTRL pin is used as a standard enable pin for the device.

Pulling the CTRL pin high enables the device beginning with the softstart cycle.

Pulling the CTRL pin to ground for a period of  $\geq$  560 µs shuts down the device, reducing the shutdown current to 0.1 µA (typ). During shutdown the internal input switch (Q1) remains open and disconnects the load from the input supply of the device.

This pin must be terminated.

#### DAC OUTPUT (DO)

The TPS61045 allows digital adjustment of the output voltage using the digital CTRL interface as described in the next section. The DAC output pin (DO) drives an external resistor (R3) connected to the external feedback divider. The DO output has a typical output voltage range from 0 V to  $V_{ref}$  (1.233V). If the DO output voltage is set to 0 V, the external resistor (R3) is more or less in parallel to the lower feedback resistor (R2) giving the highest output voltage. Programming the DO output to  $V_{ref}$  gives the lowest output voltage. Internally, a 6-bit DAC is used with 64-steps and 0 as the first step. This gives a typical voltage step of 19.6 mV which is calculated as:

$$\left(V_{O(DO)} = \frac{V_{ref}}{2^{6}-1}\right)$$

See the sectionsetting the output voltage for further information.

After start-up, when the CTRL pin is pulled high, the DO output voltage is set to its center voltage which is the 32nd step of typically  $V_{(DO)}$  = 607mV.

#### DIGITAL INTERFACE (CTRL)

When the CTRL pin is pulled high the device starts up with softstart and the DAC output voltage (DO) sets to its center voltage with a typical output voltage of 607 mV.

The output voltage can be programmed by pulling the CTRL pin low for a certain period of time. Depending on this time period the internal DAC voltage increases or decreases one digital step, as outlined in Table 1 and Figure 16. Programming the DAC output  $V_{(DO)}$  to 0 V places R3 in parallel to R2, which gives the maximum output voltage. If the DAC is programmed to its maximum output voltage equal to the internal reference voltage, typically  $V_{(DO)}$ =1.233 V, then the output has its minimum output voltage.



### DETAILED DESCRIPTION (continued)

Table 1. Timing Table					
DAC OUTPUT DO	TIME	LOGIC LEVEL			
Increase one step	$t_{(UP)}$ = 1 µs to 60 µs	Low			
Decrease one step	t <sub>(DWN)</sub> = 140 μs to 240 μs	Low			
Shutdown	$t_{(OFF)} \ge 560 \ \mu s$	Low			
Delay between steps	t <sub>d1</sub> = 1 μs	High			



Figure 16. CTRL Timing Diagram

#### UNDERVOLTAGE LOCKOUT

An undervoltage lockout feature prevents misoperation of the device at input voltages below 1.5 V (typ). As long as the input voltage is below the undervoltage threshold the device remains off, with the input switch (Q1) and the main switch (Q2) open.

#### THERMAL SHUTDOWN

An internal thermal shutdown is implemented in the TPS61045 that shuts down the device if the typical junction temperature of 160°C is exceeded. If the device is in thermal shutdown mode, the input switch (Q1) and the main switch (Q2) are open.



#### **APPLICATION INFORMATION**

#### INDUCTOR SELECTION, MAXIMUM LOAD CURRENT

Since the PFM peak current control scheme is inherently stable the inductor and capacitor value does not affect the stability of the regulator. The selection of the inductor together with the nominal load current, input, and output voltage of the application determines the switching frequency of the converter. Depending on the application, inductor values between 2.2  $\mu$ H up to 47  $\mu$ H are recommended. The maximum inductor value is determined by the maximum switch on-time of 6  $\mu$ s (typ). The peak current limit of 375 mA (typ) must be reached within this 6  $\mu$ s for proper operation.

The inductor value determines the maximum switching frequency of the converter. Therefore, the inductor value must be selected for the maximum switching frequency, at maximum load current of the converter and should not be exceeded. A good inductor value to start with is  $4.7 \mu$ H. The maximum switching frequency is calculated as:

$$f_{s(max)} = \frac{V_{I} \times (V_{O} - V_{I})}{I_{P} \times L \times V_{O}}$$

with:

I<sub>P</sub> = peak current as described in the previous peak current control section.

$$I_{P(typ)} = 375 \text{ mA} + \frac{V_I}{L} \times 100 \text{ ns}$$
 (2)

L = selected inductor value

If the selected inductor does not exceed the maximum switching frequency of the converter, as a next step, the switching frequency at the nominal load current is estimated as follows:

$$f_{s(ILOAD)} = \frac{2 \times I_{LOAD} \times (V_{O} - V_{I} + V_{F})}{I_{P}^{2} \times L}$$

with:

I<sub>P</sub> = peak current as described in the previous *chapter peak current control* section

$$I_{P(typ)} = 375 \text{ mA} + \frac{V_I}{L} \times 100 \text{ ns}$$

L = selected inductor value

I<sub>(LOAD)</sub> = nominal load current

 $V_F$  = rectifier diode forward voltage (typically 0.3 V)

The smaller the inductor value, the higher the switching frequency of the converter but the lower the efficiency.

The maximum load current of the converter is determined at the operation point where the converter starts to enter continuous conduction mode. The converter must always operate in discontinuous conduction mode to maintain regulation.

Two conditions exist for determining the maximum output current of the converter. One is when the inductor current fall time is <400 ns, and the other is when the inductor current fall time is >400 ns.

One way to calculate the maximum available load current under certain operation conditions is to estimate the expected converter efficiency at the maximum load current. This number can be taken out of the efficiency graphs shown in Figure 2 and Figure 3. Then the maximum load current can be estimated:

Inductor fall time:

www.ti.cor

(3)

SLVS440A-JANUARY 2003-REVISED SEPTEMBER 2003

### APPLICATION INFORMATION (continued)

$$t_{fall} = \frac{I_P \times L}{V_O - V_I}$$

For t<sub>f</sub>≥ 400 ns

$$I_{\text{load max}} = \eta \frac{I_{\text{P}} \times V_{\text{I}}}{2 \times V_{\text{O}}}$$

t<sub>f</sub>≤ 400 ns

$$I_{\text{load max}} = \eta \times \frac{I_P^2 \times L \times V_I}{\left(V_O - V_I\right) \times \left(2 \times I_P \times L + 2 \times 400 \text{ ns } \times V_I\right)}$$

. 2

with:

L = selected inductor value

 $\eta$  = expected converter efficiency (typically between 70% to 85%)

I<sub>P</sub> = peak current as described in the previous *peak current control* section.

$$I_{\rm P} = 300 \,{\rm mA} + \frac{V_{\rm I}}{2} \times 100 \,{\rm ns}$$
 (6)

The above formula contains the expected converter efficiency that allows calculating the expected maximum load current the converter can support. The efficiency can be taken out of the efficiency graphs shown in Figures 2 and 3 or 80% can be used as a good estimation.

The selected inductor must have a saturation current which meets the maximum peak current of the converter as calculated in the peak current control section. Use the maximum value for ILim (450mA) for this calculation.

Another important inductor parameter is the dc resistance. The lower the dc resistance, the higher the efficiency of the converter. Refer to the Table 1 and the inductor selection section under typical applications.

INDUCTOR VALUE **COMPONENT SUPPLIER** COMMENTS 10 µH Sumida CR32-100 High efficiency 10 µH Sumida CDRH3D16-100 High efficiency 10 µH Murata LQH43CN100K01 4.7 µH Sumida CDRH3D16-4R7 Small solution size 4.7 µH muRata LQH32CN4R7M51 Small solution size

#### **Table 2. Possible Inductor Selection**

### SETTING THE OUTPUT VOLTAGE

When the converter is programmed to the minimum output voltage, the DAC output (DO) equals the reference voltage of 1.233 V (typ). Therefore, only the feedback resistor network (R1) and (R2) determines the output voltage under these conditions. This gives the minimum output voltage possible and can be calculated as:

$$V_{O(min)} = V_{(FB)} \times \left(\frac{R1}{R2} + 1\right)$$

The maximum output voltage is determined as the DAC output (DO) is set to 0 V:

$$V_{O(max)} = V_{(FB)} \times \frac{R1}{R3} + V_{(FB)} \times \left(\frac{R1}{R2} + 1\right)$$



(4)

(5)



#### **APPLICATION INFORMATION (continued)**

The output voltage can be digitally programmed by pulling the CTRL pin low for a certain period of time as described in the *Digital Interface* section. Pulling the signal applied to the CTRL pin low increases or decreases the DAC output DO (pin 3) one-step where one step is typically 19.6 mV. A voltage step on DO of 19.6mV (typ) changes the output voltage by one step and is calculated as:

$$V_{O(step)} = \frac{19.6 \text{ mV} \times \text{R1}}{\text{R3}}$$

The possible output voltage range is determined by selecting R1, R2 and R3. A possible larger output voltage range gives a larger output voltage step size. The smaller the possible output voltage range, the smaller the output voltage step size.

To reduce the overall operating quiescent current in battery powered applications a high impedance voltage divider must be used with a typical value for R2 of  $\leq$  200 k $\Omega$  and a maximum value for R1 of 2.2 M $\Omega$ .

Some applications may not need the digital interface to program the output voltage. In this case the output DO can be left open as shown in Figure 18 and the output voltage is calculated as for any standard boost converter:

$$V_{O} = 1.233 V \times \left(1 + \frac{R1}{R2}\right)$$

In such a configuration a high impedance voltage divider must also be used to minimize ground current and a typical value for R2 of  $\leq$  200 k $\Omega$  and a maximum value for R1 of 2.2 M $\Omega$  are recommended.

A feed-forward capacitor  $(C_{(FF)})$ , across the upper feedback resistor (R1), is required to provide sufficient overdrive for the error comparator. Without a feed-forward capacitor or a too small feed-forward capacitor value, the device shows double pulses or a pulse burst instead of single pulses at the switch node (SW). This can cause higher output voltage ripple. If a higher output voltage ripple is acceptable, the feedforward capacitor can be left out too.

The lower the switching frequency of the converter, the larger the feed-forward capacitor value needs to be. A good starting point is the use of a 10 pF feed-forward capacitor. As a first estimation, the required value for the feed-forward capacitor can be calculated at the operation point:

$$C_{FF} \approx \frac{1}{2 \times \pi \times \frac{f_{s}}{20} \times R1}$$

with:

R1 = upper resistor of voltage divider

 $f_{S}$  = switching frequency of the converter at the nominal load current. (For the calculation of the switching frequency see previous section)

For C<sub>(FF)</sub> choose a value which comes closest to the calculation result.

The larger the feed-forward capacitor, the worse the line regulation of the device. Therefore, the feed-forward capacitor must be selected as small as possible if good line regulation is of concern.

#### **OUTPUT CAPACITOR SELECTION**

For better output voltage filtering a low ESR output capacitor is recommended. Ceramic capacitors have low ESR values but depending on the application, tantalum capacitors can also be used. Refer to Table 2 and *typical applications* for the selection of the output capacitor.

Assuming the converter does not show double pulses or pulse bursts on the switch node (SW) the output voltage ripple is calculated as:

## **APPLICATION INFORMATION (continued)**

$$\Delta V_{O} = \frac{I_{O}}{C_{O}} \times \left(\frac{1}{f_{s(ILOAD)}} - \frac{I_{P} \times L}{V_{O} + V_{F} - V_{I}}\right) + I_{P} \times ESR$$

with:

 $I_P$  = peak current as described in the previous section *peak current control* 

$$I_{P} = 375 \text{ mA} + \frac{V_{I}}{2} \times 100 \text{ ns}$$

L = selected inductor value

I<sub>O(LOAD)</sub>=Nominal load current

 $f_{S(ILoad)}$  = switching frequency at the nominal load current as calaculated previously.

 $V_F$  = rectifier diode forward voltage (typically 0.3 V)

C<sub>O</sub> = selected output capacitor

ESR = output capacitor ESR value

## INPUT CAPACITOR SELECTION

The input capacitor (C1) filters the high frequency noise to the control circuit and must be directly connected to the input pin (VIN) of the device. The capacitor (C2) connected to the L pin of the device is the input capacitor for the power stage.

The main purpose of the capacitor (C2), that is connected directly to the L pin, is to smooth the inductor current. A larger capacitor reduces the inductor ripple current present at the L pin. The smaller the ripple current at the L pin, the higher the efficiency of the converter. If a sufficiently large capacitor is used, the input switch must carry only the DC current, filtered by the capacitor (C2), and not the high switching currents of the converter. A 4.7  $\mu$ F or 10- $\mu$ F ceramic capacitor (C2) is sufficient for most applications. For better filtering, this value can be increased without limit. Refer to Table 2 and *typical applications* for input capacitor recommendations.

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER	COMMENTS
4.7 F/X5R/0805	6.3 V	Tayo Yuden JMK212BY475MG	C <sub>I</sub> /C <sub>O</sub>
10 µF/X5R/0805	6.3 V	Tayo Yuden JMK212BJ106MG	C <sub>I</sub> /C <sub>O</sub>
1.0 µF/X7R/1206	25 V	Tayo Yuden TMK316BJ105KL	Co
1.0 µF/X7R/1206	35 V	Tayo Yuden GMK316BJ105KL	Co
4.7 μF/X5R/1210	25 V	Tayo Yuden TMK325BJ475MG	Co

 Table 3. Possible Input and Output Capacitor Selection

## DIODE SELECTION

To achieve high efficiency a Schottky diode must be used. The current rating of the diode must meet the peak current rating of the converter as it is calculated in the *peak current control* section. Use the maximum value for  $I_{(LIM)}$  (450mA) for this calculation. Refer to Table 3 and the *typical applications* for the selection of the Schottky diode.

(7)

### APPLICATION INFORMATION (continued)

#### Table 4. Possible Schottky Diode Selection

COMPONENT SUPPLIER	REVERSE VOLTAGE
ON Semiconductor MBR0530	30 V
ON Semiconductor MBR0520	20 V
ON Semiconductor MBRM120L	20 V
Toshiba CRS02	30 V
Zetex CHZS400	40 V

### LAYOUT CONSIDERATIONS

As for all switching power supplies the layout is an important step in the design, especially at high peak currents and switching frequencies. If the layout is not carefully implemented the regulator can show noise problems and duty cycle jitter.

The input capacitor must be placed as close as possible to the input pin for good input-voltage filtering. The inductor and diode must be placed as close as possible to the switch pin (SW) to minimize noise coupling into other circuits. Since the feedback pin and network is a high impedance circuit, the feedback network must be routed away from the inductor.

### THERMAL CONSIDERATIONS

The TPS61045 is available in a thermally enhanced QFN package. The package includes a thermal pad, improving the thermal capabilities of the package. See QFN/SON PCB attachment application note (SLUA271).

The thermal resistance junction to ambient ( $R_{\Theta JA}$ ) of the QFN package depends on the PCB layout. By using thermal vias and wide PCB, traces improve thermal resistance ( $R_{\Theta JA}$ ). Under normal operation conditions no PCB vias are required for the thermal pad. However, the thermal pad must be soldered to the PCB.



SLVS440A-JANUARY 2003-REVISED SEPTEMBER 2003



Figure 17. Typical Application With Digital Adjusted Output Voltage



Figure 18. Typical Application With Analog Adjusted Output Voltage



### **TYPICAL APPLICATIONS (continued)**



Figure 19. OLED Supply Providing Higher Output Current

11-Feb-2005

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS61045DRBR	ACTIVE	SON	DRB	8	3000	None	CU NIPDAU	Level-2-235C-1 YEAR
TPS61045DRBT	ACTIVE	SON	DRB	8	250	None	CU NIPDAU	Level-2-235C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DRB (S-PDSO-N8)

PLASTIC SMALL OUTLINE



C. Small Outline No-Lead (SON) package configuration.

The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

 $\not riangle$  Metalized features are supplier options and may not be on the package.



#### **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

#### Mailing Address: Texas Instruments

Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated