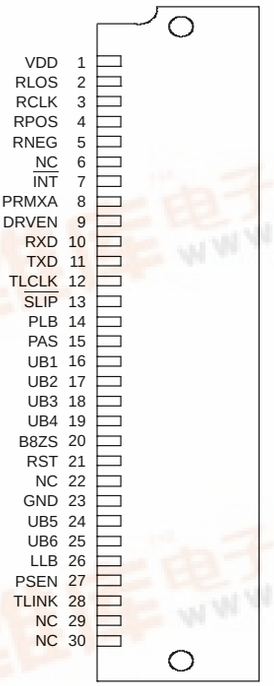
DALLAS SEMICONDUCTOR

DS2282
T1 FDL Controller/Monitor Stik

FEATURES

- Fully implements the FDL message format as described in the ANSI document T1.403–1989
- Fully implements the maintenance message protocol described in AT&T TR 54016 (1986/89)
- Provides high–level monitor counts, namely:
  - Errored Seconds
  - Severely Errored Seconds
  - Unavailable Seconds
- Important counts are stored in nonvolatile memory
- Works in conjunction with the DS2283 Enhanced T1 Line Card Stik or DS2180A T1 Transceiver
- Simple serial port used to retrieve information and control operation
- Can be used without an external controller
- Connects to a standard 30–pin Single In–Line connector
- Single +5V supply

PIN ASSIGNMENT



(actual size)

DESCRIPTION

The DS2282 completely controls the Facility Data Link (FDL) as described in the Bellcore document TR–TSY–000194 (Extended Superframe Format Interface Specification – December 1987) and the ANSI document T1.403–1989 (Carrier to Carrier Installation – DS1 Metallic Interface). It also implements the protocol that is described in the AT&T publication TR 54016 (Requirements for Interfacing DTE to Services Employing ESF – 1986/89). In addition it provides a number of important performance parameters involved in monitoring T1 lines such as Errored Seconds, Severely Errored Seconds, and Unavailable Seconds.

OVERVIEW

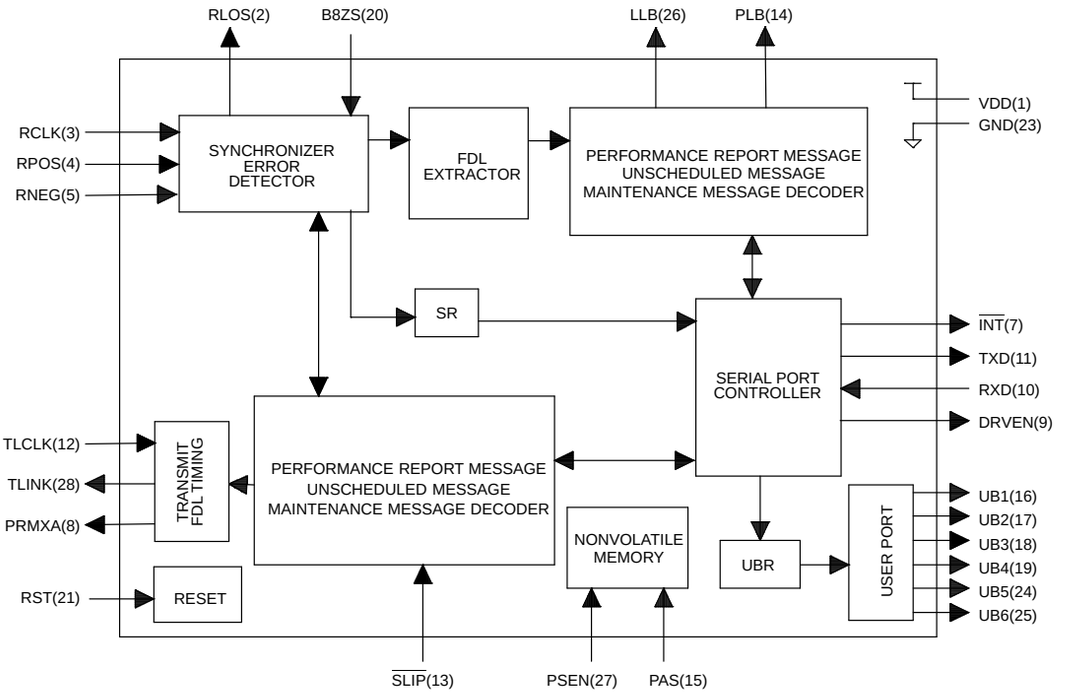
The DS2282 completely controls the Facility Data Link (FDL) in T1 environments. It can handle the FDL requirements outlined in American National Standards Institute (ANSI) document T1.403–1989 or those outlined in the AT&T publication TR 54016 (1986/89). Recovered data from a T1 line is clocked into the DS2282 via the RPOS and RNEG pins with the RCLK signal. See Figure 1. The DS2282 synchronizes to the incoming data stream and extracts the FDL. Then, it will decode the incoming messages on the FDL and properly create the FDL messages that must be transmitted.

An asynchronous serial port is used to control the DS2282 and to retrieve data from it. The port is operated at 19.2 Kbps. Access to the onboard registers is achieved through the serial port via the TXD and RXD pins. An address can be assigned to this serial port. This allows a single external controller to communicate over a single bus to as many as 31 separate DS2282's. See Figure 2. Each DS2282 will listen for its address and only respond when it is asked to do so.

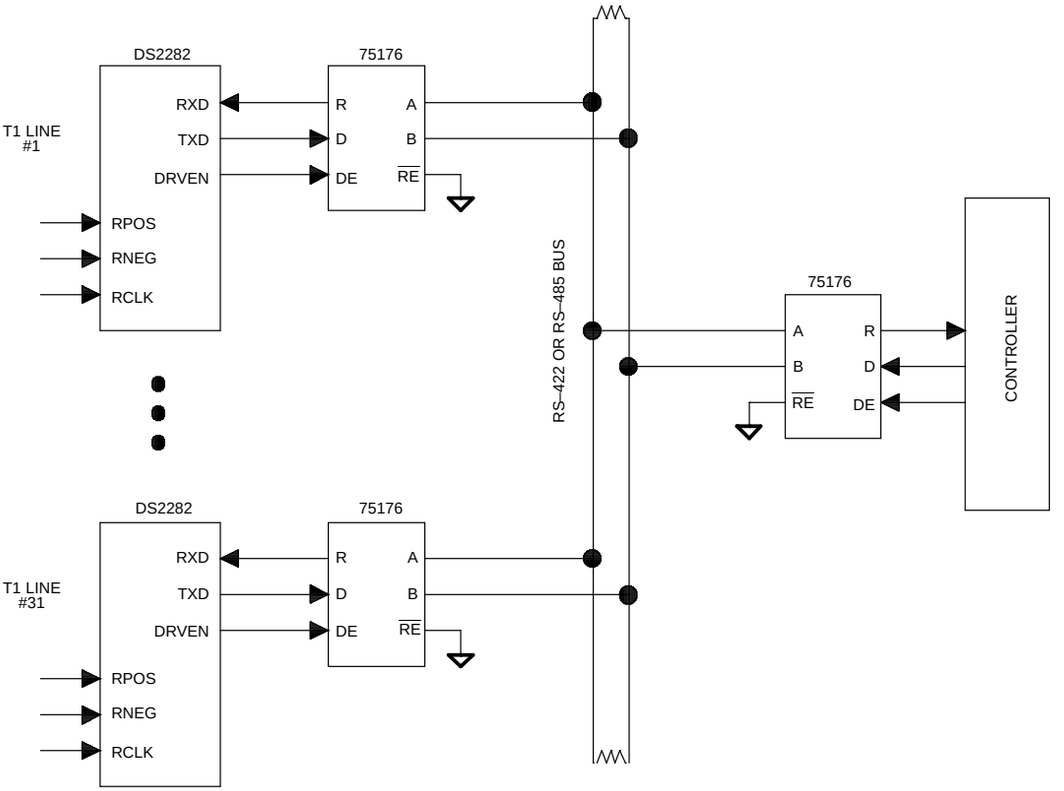
Most of the clearable registers in the DS2282 that either count error events or errored time intervals are recorded in onboard, nonvolatile memory. Hence, in case of a local loss of power, these registers will maintain their counts.

Two typical applications of the DS2282 are shown in Figures 3A and 3B. In these applications, the DS2282 is completely controlling the FDL as well as monitoring the T1 line. The DS2250 Micro Stik is used to configure the DS2282 and to extract any performance data that may be required. In these applications, the DS2250 is also used to control either the DS2283 Enhanced T1 Line Card Stik or the DS2180A T1 Transceiver. The DS2282 can also be operated without an external controller. See Hardware Mode section and Table 7.

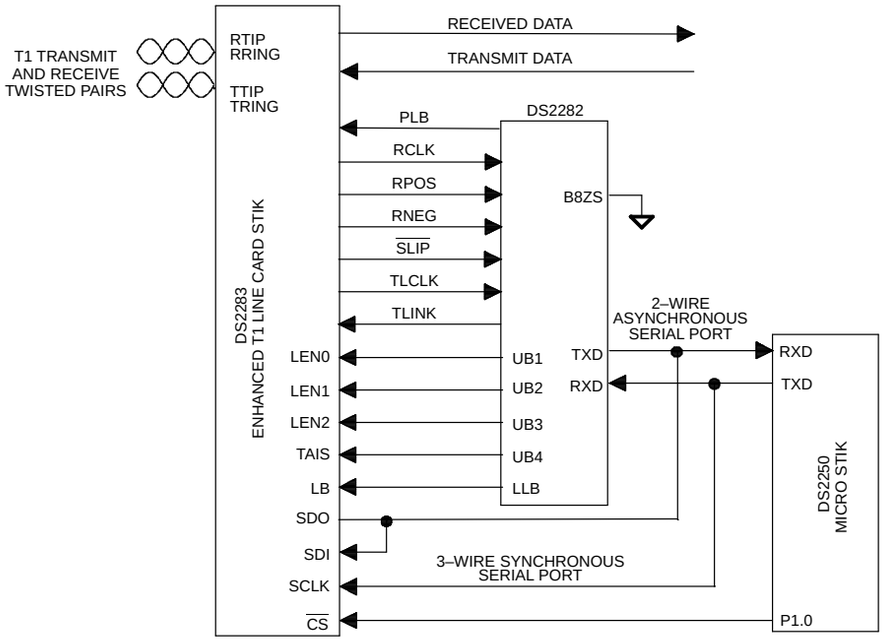
DS2282 BLOCK DIAGRAM Figure 1



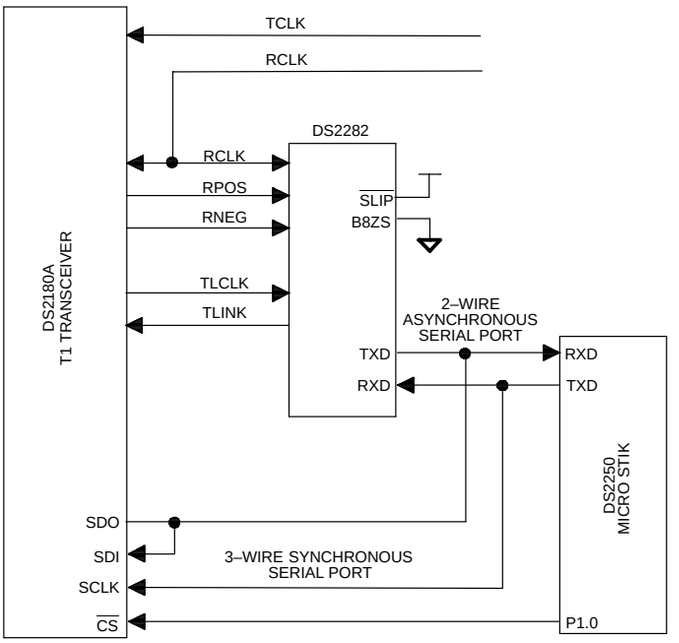
MULTIPLE DS2282 CONNECTION SCHEME Figure 2



SYSTEM APPLICATION WITH DS2283 Figure 3A



SYSTEM APPLICATION WITH DS2180A Figure 3B



PIN DESCRIPTION Table 1

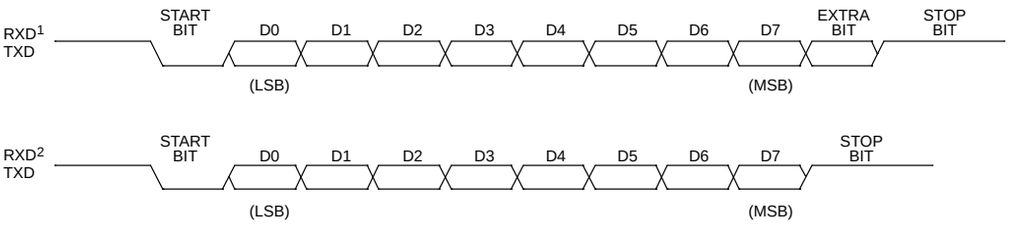
PIN	SYMBOL	TYPE	DESCRIPTION
1	VDD	–	**Positive Supply**. 5.0 volts.
2	RLOS	O	**Receive Loss Of Sync**. Indicates sync status; high when internal resync is in progress, low otherwise.
3	RCLK	I	**Receive Clock**. 1.544 MHz clock input. All internal time intervals are derived from this clock. A clock must be applied to this pin or the DS2282 will not operate properly.
4 5	RPOS RNEG	I	**Receive Bipolar Data**. Sampled on falling edge of RCLK. Can be tied together to receive NRZ data and disable BPV and B8ZS detection circuitry.
6	NC	–	**No Connect**. Do not connect any signal to this pin.
7	$\overline{\text{INT}}$	O	**Interrupt**. Transitions low when bits in the Status Register (SR) change state or when an unscheduled message (T1.403) or request message (54016) is received.
8	PRMXA	O	**PRM Transmit Active**. Transitions high when a Performance Report Message (T1.403) or response message (54016) is being sent via TLINK. DS2282 will transmit 27 flags before each messages. The PRMXA pin will be high for the message and flags.
9	DRVEN	O	**Serial Port Drive Enable**. Driven high when the DS2282 is transmitting data via TXD. Can be used to enable an external line driver. Tie this pin low to invoke 8–bit communications via the serial port.
10	RXD	I	**Serial Port Receive**. Serial data input; data is input asynchronously at 19.2Kbps.
11	TXD	O	**Serial Port Transmit**. Serial data output; data is output asynchronously at 19.2Kbps.
12	TLCLK	I	**Transmit Link Clock**. 4 KHz demand clock for the FDL data.
13	$\overline{\text{SLIP}}$	I	**Slip Occurrence Event**. This edge–triggered pin should be held low for at least 10 µs when a slip occurs locally. If local slip indications are not available, this pin should be tied low to allow model #3 to be sent in 54016 mode.
14	PLB	O	**Payload Loopback**. Transitions high when the code word or message for payload loopback activate has been received; transitions low when the code word or message for payload loopback deactivate has been received.
15	PAS	I	**Program Address Select**. Used to program the serial port address; active high.
16 17 18 19	UB1 UB2 UB3 UB4	O	**User Bits 1 to 4**. Each user bit can be independently configured either high or low via the UBR register. In hardware mode, tied high or low externally to configure DS2282.
20	B8ZS	I	**B8ZS Enable**. Tie low to disable B8ZS; tie high to enable B8ZS. Logically OR'ed with the B8ZS bit in the UBR register; tie low if the B8ZS bit is to be used to select B8ZS mode.
21	RST	I	**Reset**. Active high level will initiate a reset. Contains an internal pull–down resister.

PIN	SYMBOL	TYPE	DESCRIPTION
22	NC	–	**No Connect**. Do not connect any signal to this pin.
23	GND	–	**Ground**. 0.0 volts.
24 25	UB5 UB6	O	**User Bits 5 to 6**. Each user bit can be independently configured either high or low via the UBR register. In hardware mode, tied high or low externally to configure DS2282.
26	LLB	O	**Line Loopback**. Transitions high when the code word for line loopback activate has been received; transitions low when the code word for line loopback deactivate has been received. This pin does not go active in a 54016 environment.
27	PSEN	–	**Program Store Enable**. Used in conjunction with the RST pin to program the onboard nonvolatile memory. In normal applications, do not connect any signal to this pin.
28	TLINK	O	**Transmit Link Data**. FDL data to be transmitted; updated on the falling edge of TLCLK.
29	NC	–	**No Connect**. Do not connect any signal to this pin.
30	NC	–	**No Connect**. Do not connect any signal to this pin.

SERIAL PORT OPERATION

The registers in the DS2282 are controlled via a two–wire, asynchronous serial port. All but four of the registers are read–only; UBR, PAR, LBCR, and TUMR are write only. See Tables 2 through 5. Registers on the DS2282 are read from or written to one at a time. Communication over the serial port to one of the registers normally consists of either three, four, or five bytes. (Note: reads from the ESICR, UASICR, BESICR, SESICR, or CSLFICR consists of 194 bytes: two written to the DS2282 and 192 read from the Stik.) The first byte is always written to the DS2282 and is called the Address Byte. Normally, all communications via the asynchronous serial port on the DS2282 are performed in 11–bit bursts. See Figure 4. There is a Start Bit which is always a zero, followed by eight data bits (LSB first), followed by an Extra Bit which is a one in the Address Byte and a zero in the Register and Data Bytes, followed finally by a Stop Bit which is always a one. If the user wishes to eliminate the need for the Extra Bit in the serial port communications of the DS2282, then either the serial port address on the Stik must be set to decimal 31 (how to set the serial port address on the DS2282 is described in “Initializing the Address of the Serial Port”) or the DRVEN pin (pin 9) must be tied permanently low. If the user ties DRVEN low, then the address defaults to zero.

DS2282 SERIAL PORT COMMUNICATIONS Figure 4



NOTES:

1. If the serial port is programmed for addresses between 0 and 30 decimal (inclusive)
2. If the serial port is programmed for address 31 decimal or if DRVEN tied low

Address Byte

(MSB)								(LSB)
EB	0	0	0	A4	A3	A2	A1	A0

EB Extra Bit. Should always be set to one.
A4 Address Bit 4. The MSB of the serial port address.
A3 Address Bit 3.
A2 Address Bit 2.
A1 Address Bit 1.
A0 Address Bit 0. The LSB of the serial port address.

The second byte is also always written to the DS2282 and is called the Register Byte. The Register Byte contains the address of the register that is to be either read from or written to. The MSB in the Register Byte is the Clear Bit. The Clear Bit is used to clear a register after it has been read; hence, it can only be used in association with read registers. Furthermore, only certain read registers are clearable. See Tables 1 and 2. Typically, the only registers that can be cleared after reading are registers that count events and/or errors.

Register Byte

(MSB)							(LSB)
CB	0	A5	A4	A3	A2	A1	A0

CB Clear Bit. Set to a one if register is to be cleared after reading.
A5 Address Bit 5. The MSB of the register address.
A4 Address Bit 4.
A3 Address Bit 3.
A2 Address Bit 2.
A1 Address Bit 1.
A0 Address Bit 0. The LSB of the register address.

The third through fifth bytes (third through 194th for five of the 54016 registers) are the Data Bytes. The third byte in the communication over the serial port may be either read from or written to the DS2282. Bytes four and five are always read from the DS2282 since there are no write registers longer than one byte. When writing Data Bytes to the DS2282, the Extra Bit must be set to zero and the Extra Bit will be set to zero by the DS2282 for transfers at TXD.

Data is read from and written to the DS2282, least significant bit first. Also in multiple byte registers, the least significant byte is read first and the most significant byte is read last.

As an example, if a DS2282 had been programmed for a serial port address of five (decimal) and the user wished to retrieve and clear the count in the BPV Count Register (BPVCR=09h), then the following transactions would occur:

1. The Address Byte with the Extra Bit set to one and the proper serial port address <100000101> would be written to the DS2282, least significant bit first.
2. The Register Byte with the Clear Bit set to one and the proper register address for the BPVCR selected <100001001> would be written to the DS2282, least significant bit first.
3. The current value in the 24–bit (3–byte) BPVCR is read from the DS2282; the least significant bit in the least significant byte is read first and the most significant bit in the most significant byte is read last.
4. The BPVCR will automatically be reset to zero after the read is completed.

The serial port communication on the DS2282 is handled by the onboard DS5000 Soft Microcontroller. The DS5000 is based on an 8051–type architecture. The DS2282 utilizes the asynchronous Mode 2 operation of an 8051–like microcontroller. Hence, each byte written to the DS2282 must be preceded by a start bit (0) and followed with a stop bit (1). See Figure 4. The DS2282 will append start and stop bits to the bytes that it transmits back to an external controller via the TXD pin. More information on Mode 2 operation can be found in the DS5000 Soft Microcontroller User's Guide.

REGISTER DESCRIPTION

There are five sets of registers in the DS2282: the Status Register, the User Register, the Loopback Control Register, the T1.403 Registers, and the 54016 Registers. See Tables 2 through 6. The Status Register (SR), the User Register (UBR), and the Loopback Control Register (LBCR) are always available for access. Either the T1.403 register set or the 54016 register set will be available depending on whether the DS2282 is programmed via the UBR to operate in either T1.403 or 54016 environments, respectively.

STATUS REGISTER SUMMARY Table 2

NAME	ADDR[2,3]	R/W	CLEARABLE	DESCRIPTION
SR	04	R	Yes	**Status Register**. An 8–bit register that reports alarm conditions. See “Status Register.”

USER REGISTER SUMMARY Table 3

NAME	ADDR[2,3]	R/W	CLEARABLE	DESCRIPTION
UBR[1]	14	W	No	**User Bit Register**. An 8–bit register that sets the position of the six available user bits. See “User Register.”

LOOPBACK CONTROL REGISTER SUMMARY Table 4

NAME	ADDR[2,3]	R/W	CLEARABLE	DESCRIPTION
LBCR	35	W	No	**Loopback Control Register**. An 8–bit register that determines the actions of the PLB and LLB pins. See “Loopback Control.”

SOFTWARE VERSION AND LEVEL REGISTER SUMMARY Table 4A

NAME	ADDR[2,3]	R/W	CLEARABLE	DESCRIPTION
SWVR[1]	3F	R	No	**Software Version Register**. An 8–bit register that reports the DS2282 software version.
SWLR[1]	3E	R	No	**Software Version Level Register**. An 8–bit register that reports the DS2282 software version level in two’s complement format.

T1.403 REGISTER SET SUMMARY Table 5

NAME	ADDR[2,3]	R/W	CLEARABLE	DESCRIPTION
CRCCR[1]	08	R	Yes	**CRC Count Register**. A 16–bit register that counts CRC–6 error events.
BPVCR[1]	09	R	Yes	**BPV Count Register**. A 24–bit register that counts bipolar violations.
OOFCR[1]	0A	R	Yes	**OOF Count Register**. A 16–bit register that counts OOF error events.
FECR[1]	0B	R	Yes	**Frame Error Count Register**. A 16–bit register that counts errors in the FPS framing pattern.
ESR[1]	0C	R	Yes	**Errored Second Register**. A 16–bit register that counts ES.
SESR[1]	0D	R	Yes	**Severely Errored Second Register**. A 16–bit register that counts SES.
UASR[1]	0E	R	Yes	**Unavailable Seconds Register**. A 16–bit register that counts UAS.
PRMR0 PRMR1 PRMR2 PRMR3	10 11 12 13	R R R R	No No No No	**Performance Report Message Registers**. Four 8–bit registers that contain the PRMs that were received in the FDL in the last four seconds.
RUMR	18	R	Yes	**Receive Unscheduled Message Register**. An 8–bit register that reports unscheduled messages as they are received.

NAME	ADDR[2,3]	R/W	CLEARABLE	DESCRIPTION
TUMR	19	W	No	**Transmit Unscheduled Message Register**. An 8–bit register that is used to send unscheduled messages.
PRMESR[1]	1C	R	Yes	**PRM Errored Second Register**. A 16–bit register that counts ES as reported in the PRM.
PRMSESR[1]	1D	R	Yes	**PRM Severely Errored Second Register**. A 16–bit register that counts SES as reported in the PRM.
PRMER[1]	1E	R	Yes	**PRM Error Register**. An 8–bit register that counts PRMs that are received in error.
PAR[1]	1F	W	No	**PRM Address Register**. An 8–bit register determines the action of the PRM opening address.

NOTES:

1. Register is nonvolatile.
2. Values indicated in hexadecimal format.
3. All registers read/written LSB first.

STATUS REGISTER (04)

The Status Register (SR) reports alarms and events. The SR is always cleared when it is read by an external controller, hence the Clear Bit in the Register Byte does not need to be set. All of the bits in the SR operate in a "latched" fashion. That is, once an event or alarm has occurred, the appropriate bit in the SR will remain set until the SR is read. All of the bits in the SR will be cleared when read unless the alarm condition still exists. Also, except for the B8ZSD bit, the $\overline{INT}$ pin will be asserted (transitions low), indicating to an external controller that a bit in the SR has changed status. The $\overline{INT}$ pin will return high as soon as the status register is accessed.

SR: Status Register (04)

(MSB) (LSB)

PLB	LLB	16ZD	RCL	RYEL	RLOS	B8ZSD	AIS

PLB Payload Loopback. Set when payload loopback is active.

LLB Line Loopback. Set when line loopback is active. Will not go active in 54016 environments.

16ZD Sixteen Zero Detect. Set when 16 consecutive zeros are received. An indication of a pulse density violation.

RCL Receive Carrier Loss. Set when 192 consecutive zeros have been received.

RYEL Receive Yellow Alarm. Set when 16 consecutive 00FF Hex codes have been received in the FDL.

RLOS Receive Loss of Sync. Set when the DS2282 loses synchronization.

B8ZSD B8ZS Detect. Set when a B8ZS code word is received; operates whether the DS2282 is set up for B8ZS or not. Does not affect $\overline{INT}$.

AIS Alarm Indication Signal. Set when an unframed all one's signal is received.

SOFTWARE VERSION REGISTER

The software version register (SWVR) (3F) allows the user to display software version information. When accessed, the DS2282 software revision will be returned by the serial port. For example, the serial port will return 0Bh for software version V11.

SOFTWARE LEVEL REGISTER

The software level register (SWLR) (3E) allows the user to display software version level information. When accessed, the two's complement of the DS2282 software revision level will be returned by the serial port. If the returned value is negative, the software revision level is in "beta" or prototype state. If positive, the software revision level is the production release. For example, the serial port will return 05h for production software version level V11.5 (FBh for "beta" release).

USER REGISTER (14)

The DS2282 contains a 6–bit user port (pins UB1 to UB6). An external controller can independently set or clear these user bits via the User Bit Register (UBR). The UBR is also used to select whether the DS2282 is to operate in a T1.403 or a 54016 environment. If the 54016 bit is set to a one, then the DS2282 will operate in a 54016 fashion and the 54016 register set will be selected. If the 54016 bit is cleared (set to zero), then the DS2282 will operate in a T1.403 fashion and the T1.403 register set will be selected. Operation in both modes simultaneously is not allowed. If the user accesses the opposite mode's register set, a value of 00h is returned. For example, 00h will be returned if the DS2282 is programmed for TR54016 mode and the user reads address location 08h (CRCCR). The B8ZS bit should be set to a one when the DS2282 is connected to T1 streams that include B8ZS code words. The default for the UBR is 00 hex.

UBR: User Bit Register (14)

(MSB)							(LSB)
B8ZS	54016	UB6	UB5	UB4	UB3	UB2	UB1

B8ZS	B8ZS Select. Logically OR'ed with the B8ZS pin.
54016	54016 Select. Set to a one in a 54016 environment.
UB6	User Bit 6. Sets or clears the UB6 pin.
UB5	User Bit 5. Sets or clears the UB5 pin.
UB4	User Bit 4. Sets or clears the UB4 pin.
UB3	User Bit 3. Sets or clears the UB3 pin.
UB2	User Bit 2. Sets or clears the UB2 pin.
UB1	User Bit 1. Sets or clears the UB1 pin.

54016 REGISTER SET SUMMARY Table 6

NAME	ADDR[2,3]	R/W	CLEARABLE	DESCRIPTION
CSR	20	R	No	**Current Status Register**. An 8–bit register that indicates unavailable signal state and PLB status.
ESFEER	21	R	No	**ESF Error Event Register**. A 16–bit register that accumulates ESF error events.
CIT	22	R	No	**Current Interval Timer**. A 16–bit register that counts the number of seconds in the current 15–minute interval.
CIESR	23	R	No	**Current Interval ES Register**. A 16–bit register that indicates the number of Errored Seconds in current 15–minute interval.
CIUASR	24	R	No	**Current Interval UAS Register**. A 16–bit register that indicates the number of Unavailable Seconds in current 15–minute interval.
CIBESR	25	R	No	**Current Interval BES Register**. A 16–bit register that indicates the number of Bursty Errored Seconds in current 15–minute interval.
CISESR	26	R	No	**Current Interval SES Register**. A 16–bit register that indicates the number of Severely Errored Seconds in current 15–minute interval.
CICSLFR	27	R	No	**Current Interval CSS & LOFC Register**. A 16–bit register that counts Controlled Slip Seconds and Loss of Frame in current 15–minute interval. The 8–bit CSS count is in the LSB and the 8–bit LOFC count is in the MSB.
ESICR	28	R	No	**ES Interval Count Registers**. A set of 96 16–bit registers that contain the Errored Second counts for the previous 96 individual 15–minute periods. Most recent interval is read first.

NAME	ADDR[2,3]	R/W	CLEARABLE	DESCRIPTION
UASICR	29	R	No	**UAS Interval Count Registers**. A set of 96 16–bit registers that contain the Unavailable Second counts for the previous 96 individual 15–minute periods. Most recent interval is read first.
BESICR	2A	R	No	**BES Interval Count Registers**. A set of 96 16–bit registers that contain the Bursty Errored Second counts for the previous 96 individual 15–minute periods. Most recent interval is read first.
SESICR	2B	R	No	**SES Interval Count Registers**. A set of 96 16–bit registers that contain the Severely Errored Second counts for the previous 96 individual 15–minute periods. Most recent interval is read first.
CSLFICR	2C	R	No	**CSS & LOFC Interval Count Registers**. A set of 96 16–bit registers that contain the Controlled Slip and Loss Of Frame counts for the previous 96 individual 15–minute periods. The 8–bit CSS count is the LSB and the 8–bit LOFC count is in the MSB. Most recent interval is read first.
ESDCR	2D	R	No	**ES Day Count Registers**. A 16–bit register that counts the number of Errored Seconds in the previous 24–hour period.
UEEER	36	R	Yes	**User ESF Error Event Register**. 16–bit register that mimics the ESFEER for user access.
UASDCR	2E	R	No	**UAS Day Count Registers**. A 16–bit register that counts the number of Unavailable Seconds in the previous 24–hour period.
BESDCR	2F	R	No	**BES Day Count Registers**. A 16–bit register that counts the number of Bursty Errored Seconds in the previous 24–hour period.
SESDCR	30	R	No	**SES Day Count Registers**. A 16–bit register that counts the number of Severely Errored Seconds in the previous 24–hour period.
CSLFDCR	31	R	No	**CSS & LOFC Day Count Registers**. A 16–bit register that counts the number of Controlled Slip Seconds and Loss Of Frames in the previous 24–hour period. The 8–bit CSS count is in the LSB and the 8–bit LOFC count is in the MSB.
VITR	32	R	No	**Valid Interval Total Register**. An 8–bit register that indicates the number of valid 15–minute intervals in the previous 24–hour period.
RMSR	33	R	Yes	**Request Message Status Register**. An 8–bit register that indicates which (if any) request message is being received.
CR	34	W	No	**Control Register**. An 8–bit register that selects which address the DS2282 will respond to.

NOTES:

1. All of the registers in the DS2282 that count events will saturate at their maximum possible count; they do not roll over. For example, all the 16–bit registers stop at a count of 65,535. They do not roll over to zero and continue counting.
2. Values indicated in hexadecimal format.
3. All register read/written LSB first.

T1.403 OPERATION

In order to properly operate on T1 lines running the FDL under the definition spelled out in the ANSI document T1.403, the DS2282 must have the 54016 bit in the UBR set to zero (see “User Register”). The DS2282 will decode both the incoming Performance Report Messages (PRM) and unscheduled messages and provide them for the user. The DS2282 also collects data on bipolar violations (BPV), frame errors, CRC–6 errors, and Out–of–Frame errors (OOF). The DS2282 combines the information in these registers along with the indication of local slips via the $\overline{\text{SLIP}}$ signal to create PRMs that are transmitted once a second via the TLINK signal. Also, the user can instruct the DS2282 to transmit unscheduled messages. For more information on the T1.403 definition, refer to the application note “T1.403 FDL Message Overview.”

Monitor Registers

There are two sets of monitor registers. The first set helps support some of the monitoring requirements on T1 lines as spelled out in documents such as TA–TSY–000147 (DS1 Rate Digital Service Monitoring Unit Functional Specifications – October 1987), TR 62411 (Accunet* T1.5 Service Description and Interface Specifications – December 1988), and the CCITT recommendation G.821. This set consists of three registers, the Errored Seconds Register (ESR), the Severely Errored Seconds Register (SESR), and the Unavailable Seconds Register (UASR). Unlike the first set of monitor registers which provides a count of conditioned data, the second set of monitor registers just provides raw data counts of events such as CRC–6 errors, bipolar violations, frame errors, and out of frame errors. The second set of monitor registers consists of four registers: the CRC Count Register (CRCCR), the Bipolar Violation Count Register (BPVCR), the Frame Error Count Register (FECR), and the Out Of Frame Count Register (OOFCR). All of the monitor registers are described below.

ESR: Errored Seconds Register (0C). A 16–bit register that counts Errored Seconds (ES). An ES is any one–second time interval with either a frame bit error, CRC–6 error, OOF event, or controlled slip event.

SESR: Severely Errored Seconds Register (0D). A 16–bit register that counts Severely Errored Seconds (SES). A SES is any one–second time interval with an OOF error event and/or more than 320 CRC–6 errors in it.

UASR: Unavailable Seconds Register (OE). A 16–bit register that counts Unavailable Seconds (UAS). A UAS is the number of seconds between 10 consecutive SES events (inclusive) and 10 consecutive non–SES events (exclusive). The DS2282 starts counting SES events when it receives the first one. If it counts ten SESs in a row, then it increments the UASR by ten and decrements the ES and SES by ten. Counts in the ESR and SESR are inhibited during unavailable seconds. Once the DS2282 has begun counting unavailable seconds, it begins counting non–SES events. At the first non–SES event, it begins counting Errored Seconds in a separate register that is not available to the user. If the DS2282 fails to count ten non–SES events in a row, it clears both the non–SES count and the register counting Errored Seconds during unavailable seconds. If it counts ten non–SES events in a row, it will decrement the UASR by ten and will increment the ESR by the count in the register counting Errored Seconds during unavailable seconds. Also, when the DS2282 detects either an incoming Alarm Indication Signal (AIS) or Receive Carrier Loss (RCL), it will increment the UASR for each second either of these conditions exists.

CRCCR: CRC–6 Error Count Register (80). A 16–bit register that records CRC–6 error events. The DS2282 calculates CRC–6 on the incoming data. Each time the calculation does not match the CRC–6 code word in the incoming ESF data stream, then the CRCCR is incremented by one.

BPVCR: Bipolar Violation Count Register (81). A 24–bit register that records bipolar violations (line code violations). Bipolar violations are counted whether the synchronizer in the DS2282 is in sync (the RLOS signal is low) or not. If the DS2282 is set up to receive B8ZS code words, then B8ZS code words are not counted as bipolar violations.

FECR: Frame Error Count Register (83). A 16–bit register that records errors in the Framing Pattern Sequence (FPS). All individual bit errors in the FPS pattern (001011) are recorded in the FECR.

* Service mark of AT&T Communications

OOFCR: Out Of Frame Count Register (82). A 16–bit register that records Out Of Frame (OOF) error events. An OOF error event occurs whenever 2 or more framing bits out of 6 in the FPS are incorrect. An OOF error event will cause the DS2282 to resynchronize to the incoming data stream.

Receive PRM Operation

The DS2282 decodes the incoming FDL for scheduled Performance Report Messages (PRM). It automatically detects opening flags, deletes any stuffed zero bits that may be present, and it calculates CRC–16 on all the data between the opening and closing flags. The DS2282 normally only decodes the current second's data (octets 5 and 6). Data from the previous three seconds is "bumped" from PRMR0 to PRMR1 to PRMR2 to PRMR3 and finally out of available recall range. If the PRM is received in error (CRC check sum is incorrect), the message will be ignored. The DS2282 will keep track of errored PRMs and properly place the unerrored message when it is received. For example, if a PRM is received that does not correspond to its CRC check sum, then PRMR0 will be set to all zeros indicating that an invalid message was received. If the next scheduled message is received correctly, then the data missed in the last scheduled message will be updated to PRMR1.

NOTE: PRMR0 to PRMR3 are only updated if PRMs are received; if no valid or invalid PRMs are received, then both the SE and FE bits in PRMR0 to PRMR3 will be set to one.

PRMR0: PRM Register 0 (10)
PRMR1: PRM Register 1 (11)
PRMR2: PRM Register 2 (12)
PRMR3: PRM Register 3 (13)

(MSB) (LSB)

PLB	SL	LV	SE	FE	CRC2	CRC1	CRC0

PLB	Payload Loopback Activated
SL	Controlled Slip (slip ≧ 1)
LV	Line Violation (BPV ≧ 1)
SE	Severely Errored Framing Event (2 of 6 OOF ≧ 1)
FE	Frame Sync Bit Error Event
CRC2	See Table Below
CRC1	See Table Below
CRC0	See Table Below

CRC2	CRC1	CRC0	EVENT
0	0	0	Invalid
0	0	1	CRC=0
0	1	0	CRC=1 (G1)
0	1	1	1 < CRC ≦ 5 (G2)
1	0	0	5 < CRC ≦ 10 (G3)
1	0	1	10 < CRC ≦ 100 (G4)
1	1	0	100 < CRC ≦ 319 (G5)
1	1	1	CRC ≧ 320 (G6)

PRM History Registers

There are three registers that keep track of the scheduled PRM and collect data on the receive performance of the remote end. The first two of these registers (PRMESR and PRMSESR) mock the monitor registers in the type of data that they report. ES and SES are calculated off of the received PRM data. The PRM data is pulled from PRMR3 since it has the highest probability of containing valid data. If PRMR3 does not contain valid data, then ES and SES are not calculated. The third register (PRMER) keeps a count of how many PRMs have been received in error.

PRMESR: PRM Errored Seconds Register (1C). A 16–bit register that counts Errored Seconds (ES). An ES is any one second time interval with either a frame bit error (FE or SE=1) or CRC–6 error (G1 to G6=1).

PRMSESR: PRM Severely Errored Seconds Register (1D). A 16–bit register that counts Severely Errored Seconds (SES). A SES is any one second time interval with an OOF error event (SE=1) or more than 320 CRC–6 error events (G6=1).

PRMER: PRM Error Register (1E). An 8–bit register that records the number of PRMs that have been received in error. A PRM is considered to be received in error when the calculated CRC does not match the incoming CRC word.

Transmit PRM Operation

The DS2282 will automatically generate PRMs once a second to be included into the FDL for transmission to the remote end. It automatically pulls together all the

necessary data to create a PRM from both the monitor registers and from the $\overline{SLIP}$ signal. It creates the opening and closing flags as well as the address and control bytes. Once the PRM packet has been assembled, the DS2282 will generate CRC–16 and include it at the end of the PRM. And finally, before the PRM is sent, zeros are inserted to insure that none of the PRM data appears as a flag.

Receive Unscheduled Message Operation

The DS2282 decodes incoming unscheduled messages as they are received. The DS2282 will report the received unscheduled message via the RUMR when the message has been received for three consecutive times. This integration allows the DS2282 to operate properly even on high bit error rate lines. The RUMR is cleared when read via the serial port. The $\overline{INT}$ pin will be asserted (transitions low), indicating to an external controller that an unscheduled message has been received three consecutive times. The user may count incoming unscheduled messages by monitoring the $\overline{INT}$ pin. The $\overline{INT}$ pin will return high as soon as the RUMR is accessed.

Two output signals on the DS2282 will respond to certain unscheduled messages. The PLB (Payload Loopback) signal will transition high if the code word for payload loopback activate (001010) is received three times. It will remain high until the DS2282 has received the payload loopback deactivate code word (011001) three times. The LLB (Line Loopback) signal operates similarly. The LLB signal will transition high when the DS2282 has received the code word for line loopback activate (000111) three times. It will remain high until the DS2282 has received the code word for line loopback deactivate (011100) three times. The user has the option to control the PLB and LLB pins via the Loopback Control Register (LBCR); see “Loopback Control Register.”

RUMR: Receive Unscheduled Message Register (18)

(MSB)							(LSB)
NA	NA	CW5	CW4	CW3	CW2	CW1	CW0

NA Not Assigned. Could be any value when read.

NA Not Assigned. Could be any value when read.

CW5 MSB of the Receive Unscheduled Message Code word.

CW0 LSB of the Receive Unscheduled Message Code word.

Transmit Unscheduled Message Operation

The DS2282 will transmit outgoing unscheduled messages. The DS2282 will continuously transmit the unscheduled message described in TUMR if enabled via the TUM bit in the TUMR. If unscheduled messages are being transmitted, all PRMs are superseded. When the TUM is cleared, the DS2282 will finish sending the unscheduled message that it is currently transmitting before switching to either the idle code or PRMs.

TUMR: Transmit Unscheduled Message Register (19)

(MSB)							(LSB)
TUM	0	CW5	CW4	CW3	CW2	CW1	CW0

TUM Transmit Unscheduled Message Enable

CW5 MSB of the Transmit Unscheduled Message Code word.

CW0 LSB of the Transmit Unscheduled Message Code word.

PAR: PRM Address Register (1F). The DS2282 allows the user to set the PRM opening address C/R bit depending on the source of the PRM. The C/R bit is set to zero for PRMs created by user equipment such as a CPE or set to one for PRMs created by a carrier. The PAR allows the user to control the expected state of the C/R bit as well as control the state of the bit in the PRMs created by the DS2282.

(MSB)							(LSB)
0	0	0	0	0	0	TC/R	RC/R

TC/R Transmit PRM C/R Bit Control
0=force C/R bit to zero in outgoing PRM
1=force C/R bit to one in outgoing PRM

RC/R Receive PRM C/R Bit Control
0=only respond to RPM with the C/R bit set to zero
1=only respond to PRM with the C/R bit set to one

54016 OPERATION

In order to properly operate on T1 lines running the FDL under the definition spelled out in the AT&T Publication TR 54016, the DS2282 must have the 54016 bit in the UBR set to one (see “User Register”). The DS2282 monitors the incoming FDL for maintenance messages from the network. It will decode these messages and respond accordingly. The DS2282 will automatically monitor the T1 and accumulate the statistics that might be requested from the network. All of the information that is gathered by the DS2282 is locally available to the user. The 54016 register set in the DS2282 mimics the registers defined in TR 54016. When the DS2282 is not responding to maintenance messages, it transmits FFh or 7Eh programmed by the control register (CR) of user bits (UB) in the hardware mode.

CSR: Current Status Register (20). The 8–bit Current Status Register (CSR) contains information on whether an unavailable signal state or Payload Loopback is active.

CSR: Current Status Register (20)

(MSB)							(LSB)
F	U	0	0	0	0	L	0

F	F=1 if either U or L is set to a one
U	U=1 if an unavailable signal state exists
L	L=1 if the Payload Loopback (PLB) is active

ESFEER: ESF Error Event Register (21). A 16–bit register that counts ESF error events. Each ESF is checked for the occurrence of an error event. An error event is defined as the logical OR’ing of CRC–6 error events and Out Of Frame (OOF) events. A CRC–6 error event occurs when the locally calculated CRC–6 code does not match the incoming CRC–6 code. An OOF event occurs when 2 out of 4 consecutive framing bits are received in error.

UEEER: User ESF Error Event Register (36). A 16–bit register that mimics the ESF Error Event Register (ESFEER). Unlike the ESFEER, the UEEER is user clearable once saturated by network error events. This simplifies operations when user registers are created external from the DS2282.

CIT: Current Interval Timer (22). A 16–bit register that counts the number of seconds in the current 15 minute interval. Since there can only be 900 seconds in a 15 minute interval, this register will never saturate. Since all of the time intervals in the DS2282 are derived from the T1 source, the accuracy of this timer depends on the accuracy of the RCLK signal.

Current Interval Registers

The current interval registers count the number of events that have occurred in the current 15 minute interval. There are five separate current interval registers. They are:

CIESR (23)	counts Errored Seconds (ES)
CIUASR (24)	counts Unavailable Seconds (UAS)
CIBESR (25)	counts Bursty Errored Seconds (BES)
CISESR (26)	counts Severely Errored Seconds (SES)
CICSLFR (27)	counts Controlled Slip Seconds (CSS) and Loss Of Frame Counts (LOFC)

Each of these current interval registers is 16 bits in length. Please see “54016 Definitions” for definitions of ES, UAS, BES, SES, CSS, and LOFC.

Interval Count Registers

The interval count registers are a set of 96 separate 16–bit registers that contain the number of events that have occurred in each of the previous 96, individual 15 minute periods. Or in other words, the interval count registers contain the performance of the T1 line for the previous 24 hours broken into 15 minute periods. There are five separate interval count registers. They are:

ESICR (28)	contains Errored Seconds (ES)
UASICR (29)	contains Unavailable Seconds (UAS)
BESICR (2A)	contains Bursty Errored Seconds (BES)
SESICR (2B)	contains Severely Errored Seconds (SES)
CSLFICR (2C)	contains Controlled Slip Seconds (CSS) and Loss Of Frame Counts (LOFC)

Please see “54016 Definitions” for definitions of ES, UAS, BES, SES, CSS, and LOFC.

Day Count Registers

The day count registers count the number of events that have occurred in the previous 24 hour period. There are five separate day count registers. They are:

ESDCR (2D)	counts Errored Seconds (ES)
UASDCR (2E)	counts Unavailable Seconds (UAS)
BESDCR (2F)	counts Bursty Errored Seconds (BES)
SESDCR (30)	counts Severely Errored Seconds (SES)
CSLFDCR (31)	counts Controlled Slip Seconds (CSS) and Loss Of Frame Counts (LOFC)

Each of these current interval registers are 16 bits in length. Please see "54016 Definitions" for definitions of ES, UAS, BES, SES, CSS, and LOFC.

VITR: Valid Interval Total Register (32). An 8–bit register that counts the number of 15 minute intervals since the last reset. Hence, it has a maximum count of 96.

RMSR: Request Message Status Register (33). An 8–bit register that indicates which (if any) request maintenance message has been received. If a request maintenance message is received, the $\overline{INT}$ pin will be asserted (transitions low). The RMSR will be cleared when read. This indicates to an external controller that a request has been received and is being processed. The $\overline{INT}$ pin will return high as soon as the RMSR is accessed. There are currently 15 request messages defined.

(MSB)							(LSB)
RM7	RM6	RM5	RM4	RM3	RM2	RM1	RM0

RM7	MSB of the request message
RM0	LSB of the request message

CR: Control Register (34). An 8–bit register that selects whether the DS2282 will respond to address A (or Z) or address B (or Y). The default is for the DS2282 to respond only to address A (or Z). The user can set the DS2282 to respond address B (or Y) by setting the AD bit to a one. In addition, CR allows the user to send an all one's sequence FFh or LAPD idel code 7Eh.

(MSB)							(LSB)
0	0	0	0	0	0	ICS	AD

AD	Address Select Bit. Set to a one to respond to address B (or Y)
ICS	Idle Code Select 0 = FFh 1 = 7Eh

54016 DEFINITIONS

Errored Seconds (ES): A one–second period with either:

a. one or more CRC–6 error events or
b. one or more OOF events or
c. one or more controlled slips.

Severely Errored Seconds (SES): A one–second period with either:

a. 320 or more CRC–6 error events or
b. one or more OOF events.

Unavailable Seconds (UAS): A one–second period in which an unavailable signal state is present. In counting UAS, the initial period of 10 consecutive SES's is included in the count whereas the final 10 seconds of 10 consecutive non–SES's which removes the unavailable signal state is not included in the count. During UAS's, neither ES, or SES, or BES, are counted. Refer to "Monitor Registers" for a more detailed description of UAS.

Unavailable Signal State: An unavailable signal state is declared when 10 consecutive SESs have been received. An unavailable signal state is considered cleared when 10 consecutive non–SES events have occurred.

Controlled Slip Seconds (CSS): A one–second period with one or more controlled slips. A controlled slip is the deletion or replication of a DS1 frame. Indications of controlled slips are input to the DS2282 via the $\overline{SLIP}$ pin. If indications of controlled slips are not available, the $\overline{SLIP}$ pin should be tied low.

Loss Of Frame Count (LOFC): A count of the number of times Loss Of Frame (LOF) has been declared. An LOF is declared by the following method. Each superframe (3 ms) will be examined for a LOF event. If an event is present, then an internal counter (which is not available to the user) will be incremented by five, if no event is present, then the counter will be decremented by one. When the counter crosses a boundary of 4166 (2.5 sec x 333.3 SF/sec x 5 counts/SF) then a LOF will be declared and the LOFC will be incremented by one. At this point, the counter will be reset to zero when for at least one full second, a LOF has not occured.

Bursty Errored Seconds (BES): A one–second period with more than one but less than 320 CRC–6 error events.

ESF Error Event: Each ESF is checked for either a CRC–6 event or an OOF event.

INITIALIZING THE ADDRESS OF THE SERIAL PORT

The serial port on the DS2282 can be assigned an address from 0 to 30 decimal. Address location 31 decimal will set the serial port into a mode where the Extra Bit is not needed in the communications over the serial port (see “Serial Port Operation”). The default address is 0 decimal. The DS2282 is shipped from the factory with the default value in place. The address can be programmed in the following manner:

1. Power down the DS2282.
2. Set the Program Address Select pin to be pulled high when power is applied.
3. Configure the User Bits 1 to 5 with the desired address; UB1 is the LSB, UB5 is the MSB.
4. Leave all other pins open.
5. Apply power to the DS2282 for at least 1 second.
6. Power down the DS2282.
7. Set the Program Address Select pin to remain low when power is reapplied.

At this point, the DS2282 will be programmed to the proper value. Assigning a new address value can be performed with the same procedure. The address value is stored in nonvolatile memory.

NONVOLATILE STORAGE

The DS2282 can retain its onboard program and the contents of the nonvolatile registers for at least ten years in the absence of power at room temperature. If power is applied to the DS2282 at least 50% of the time, the nonvolatile storage will last at least 20 years.

SINGLE IN–LINE CONNECTOR

The DS2282 is designed to connect directly into a 30–position Single In–Line connector. These connectors are available from a number of vendors.

LOOPBACK CONTROL REGISTER

The Loopback Control Register (LBCR) allows the user to determine the action of the Payload Loopback (PLB) and Line Loopback (LLB) pins. The user has the option to either allow the DS2282 to respond normally to loopbacks, as described in “Receive Unscheduled Message Operation,” or to force the PLB or LLB pins high or low. The default value for the LBCR is 00 hex. In addition, the LCR allows the user to automatically interrupt the transmission of the yellow alarm to either send a PRM (T1.403) or a Response Message–RM (54016) by setting the IYA bit. The yellow alarm interrupt routine transmits 27 opening flags to insure synchronization by the far end receiver prior to transmitting a PRM or RM. Within the T1.403 mode, an Unscheduled Message enabled by the TUMR register will override the transmission of the interruptable yellow alarm. Also, the LBCR allows a software method of disabling local slip indications by setting the DS bit. This enables the Enhanced Configuration Data Response (model #3) to be sent in 54016 mode, when local slip indication is disabled.

(MSB) (LSB)

0	DS	IYA	0	DLLB	FLLB	DPLB	FPLB

DS — Disable Local $\overline{\text{SLIP}}$ Indications.
0 = follow the $\overline{\text{SLIP}}$ pin for SLIP indications (this includes disabling slip counts by permanently tying the $\overline{\text{SLIP}}$ pin low)
1 = force the disabling of local slip indications regardless of the $\overline{\text{SLIP}}$ pin

IYA — Interruptable Yellow Alarm Enable.
0 = do not transmit an interruptable yellow

alarm
1 = transmit an interruptable yellow alarm

DLLB Disable Automatic LLB Action.
0 = allow the LLB pin to act normally
1 = force the LLB pin to the value in FLLB

FLLB Force LLB.
0 = force the LLB pin low
1 = force the LLB pin high

DPLB Disable Automatic PLB Action.
0 = allow the PLB pin to act normally
1 = force the PLB pin to the value in FPLB

FPLB Force PLB.
0 = force the PLB pin low
1 = force the PLB pin high

HARDWARE MODE

The DS2282 provides an optional hardware mode for operation without an external controller. The external UB5 pin allows the user to select between the hardware and software operating modes. The hardware mode is provisioned by connecting the UB5 pin to GND. If the UB5 pin is left floating, the software mode is enabled for serial port operations. In the hardware mode, the DS2282 will continue to monitor and supply the FDL data stream messages automatically without any interaction by the user. B8ZS, T1.403, and 54016 operating modes are configured by external pin connections, along with the PRM C/R bit control, address, and idle code selects indicated by the hardware mode table. The external UB pins (1–6) are read during power up or reset events. After power up or reset occurs, the defined hardware operating mode can be changed in software via the corresponding register bits.

HARDWARE MODE Table 7

PIN	SYMBOL	REGISTER BIT	DESCRIPTION
24	UB5	N/A	0 (GND) = Hardware Select, N/C (Floating) = Software Select
20	B8ZS	UBR–B8ZS	**B8ZS Select Pin**. 1 = enabled, 0 = disabled
19	UB4	UBR–54016	**Mode Select Pin**. 0 (GND) = T1.403, N/C (Floating) = TR54016
16	UB1	PAR–RC/R	**Receive PRM C/R Bit Control Pin for T1.403 Mode**. 0 (GND) = only respond to PRM with C/R bit set to one. N/C (Floating) = only respond to PRM with C/R bit set to zero.
		CR–AD	**Address Select Bit Control Pin for TR54016**. 0 (GND) = respond to address B (or Y). N/C (Floating) = respond to address A (or Z).
16	UB2	PAR–TC/R	**Transmit PRM C/R Bit Control Pin for T1.403 Mode**. 0 (GND) = force C/R bit to one in outgoing PRM. N/C (Floating) = force C/R bit to zero in outgoing PRM.
		CR–ICS	**Idle Code Select Bit Control Pin for TR54016**. 0 (GND) = 7E (h) N/C (Floating) = FF (h).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to V_{CC}
Operating Temperature	0°C to +70°C
Storage Temperature	0°C to 70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	3
Logic 1 for RST	V_{IH}	3.5		V_{CC}+0.3	V	
Logic 0	V_{IL}	–0.3		+0.8	V	
Supply	V_{DD}	4.75		5.25	V	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		30		pF	
Output Capacitance	C_{OUT}		50		pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		30		mA	1
Static Input Leakage	I_I	–50		+50	µA	2, 3
Output Voltage (80 µA)	V_{OH}	2.4	4.8		V	
Output Voltage (1.6 mA)	V_{OL}		0.15	0.45	V	
RST Pull–down Resistance	R_{PD}	40		125	KΩ	

NOTES:

1. RCLK=1.544 MHz; V_{DD}=5.25V; outputs open; inputs tied low
2. V_{IN}=.45 volts
3. Does not apply to RST

AC ELECTRICAL CHARACTERISTICS

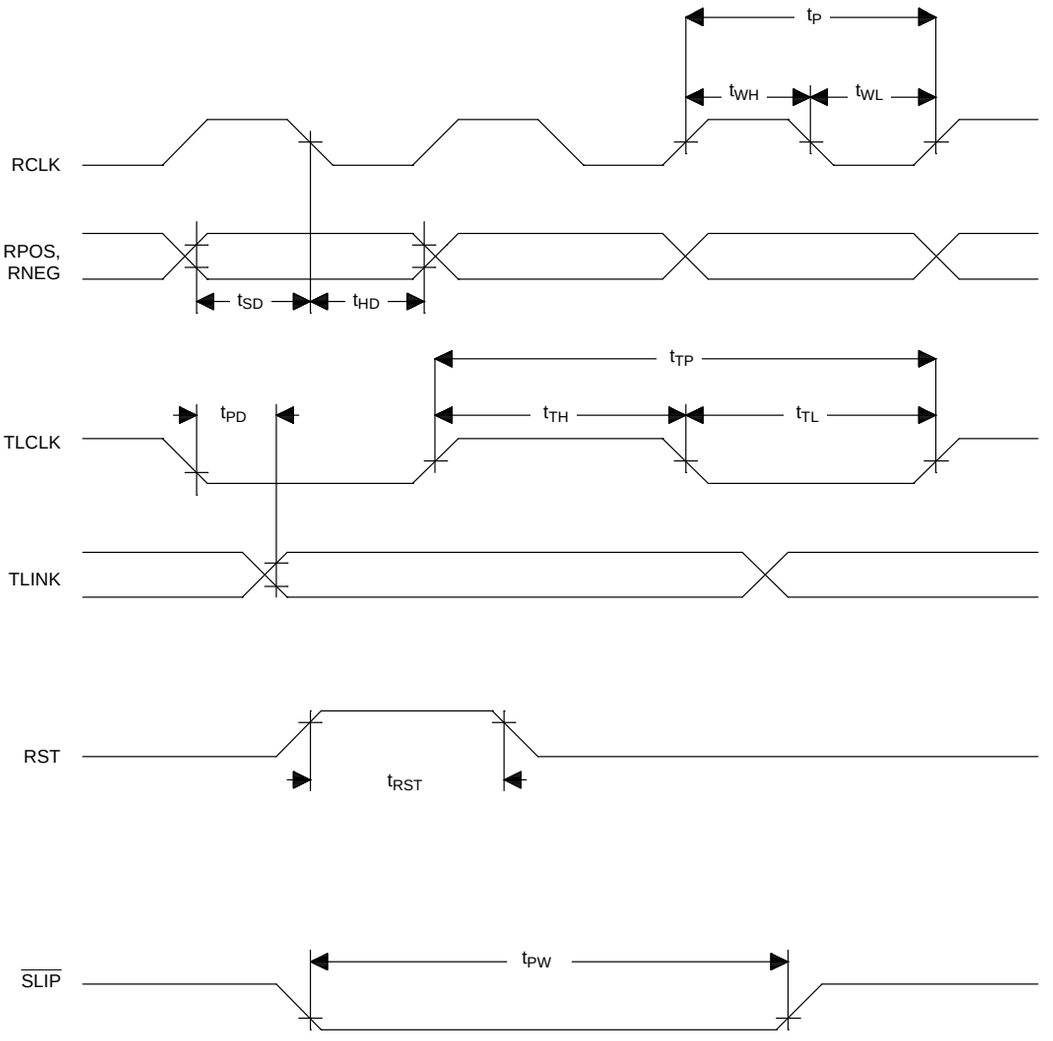
(0°C to 70°C; V_{DD}=5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_P		648		ns	1
RCLK Pulse Width	t_{WH}, t_{WL}	100			ns	
RPOS, RNEG Setup to RCLK Falling	t_{SD}	50			ns	
RPOS, RNEG Hold from RCLK Falling	t_{HD}	50			ns	
Propagation Delay from TLCLK Falling to TLINK Valid	t_{PD}			120	µs	
TLCLK Period	t_{TP}		250		µs	1
TLCLK Pulse Width	t_{TH}, t_{TL}	50			µs	
RST Pulse Width	t_{RST}	10			µs	
$\overline{SLIP}$ Pulse Width	t_{PW}	10			µs	
Sync/Reframe Time				30	ms	2

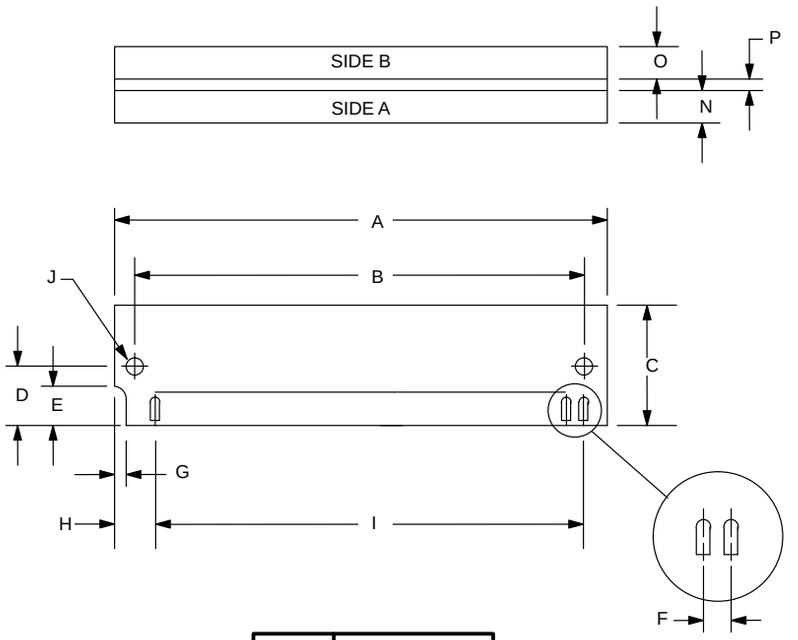
NOTES:

1. Must be accurate to ±32 ppm for precise one second interval measurements.
2. Time necessary to sync to an error–free signal.

AC TIMING DIAGRAM Figure 5



DS2282 T1 FDL CONTROLLER/MONITOR



PKG	30-PIN	
DIM	MIN	MAX
A IN.	3.455	3.505
B IN.	3.229	3.239
C IN.	0.845	0.855
D IN.	0.395	0.405
E IN.	0.245	0.255
F IN.	0.100 BSC	
G IN.	0.075	0.085
H IN.	0.295	0.305
I IN.	2.900 BSC	
J IN.	0.120	0.130
N IN.		0.200
O IN.		0.145
P IN.		0.054