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National Semiconductor

June 1999

DS1651/DS3651
Quad High Speed MOS Sense Amplifiers

General Description

The DS1651/DS3651 is TTL compatible high speed circuits intended for sensing in a broad range of MOS memory system applications. Switching speeds have been enhanced over conventional sense amplifiers by application of Schottky technology, and TRI-STATE® strobing is incorporated, offering a high impedance output state for bused organization.

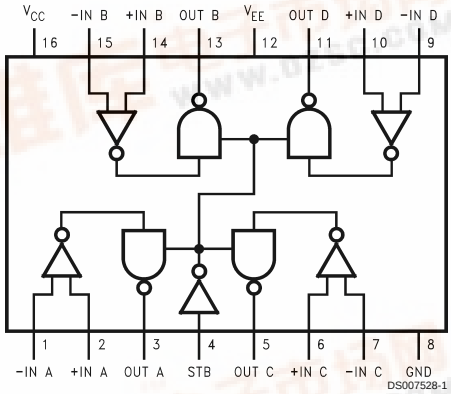
The DS1651/DS3651 has active pull-up outputs and offers open collector outputs providing implied "AND" operations.

Features

- High speed
- TTL compatible
- Input sensitivity — ±7 mV
- TRI-STATE outputs for high speed buses
- Standard supply voltages — ±5V
- Pin and function compatible with MC3430

Connection Diagram

Dual-in-Line Package



Top View
Order Number DS1651J, DS3651J or DS3651N
See NS Package Number J16A or N16A

Truth Table

Input	Strobe	Output
		DS3651
$V_{ID} \geq 7$ mW $T_A = 0^\circ C$ to $+70^\circ C$	L H	H Open
-7 mV $\leq V_{ID} \leq +7$ mV $T_A = 0^\circ C$ to $+70^\circ C$	L H	X Open
$V_{ID} \leq -7$ mV $T_A = 0^\circ C$ to $+70^\circ C$	L H	L Open

L = Low logic state
H = High logic state
Open = TRI-STATE
X = Indeterminate state

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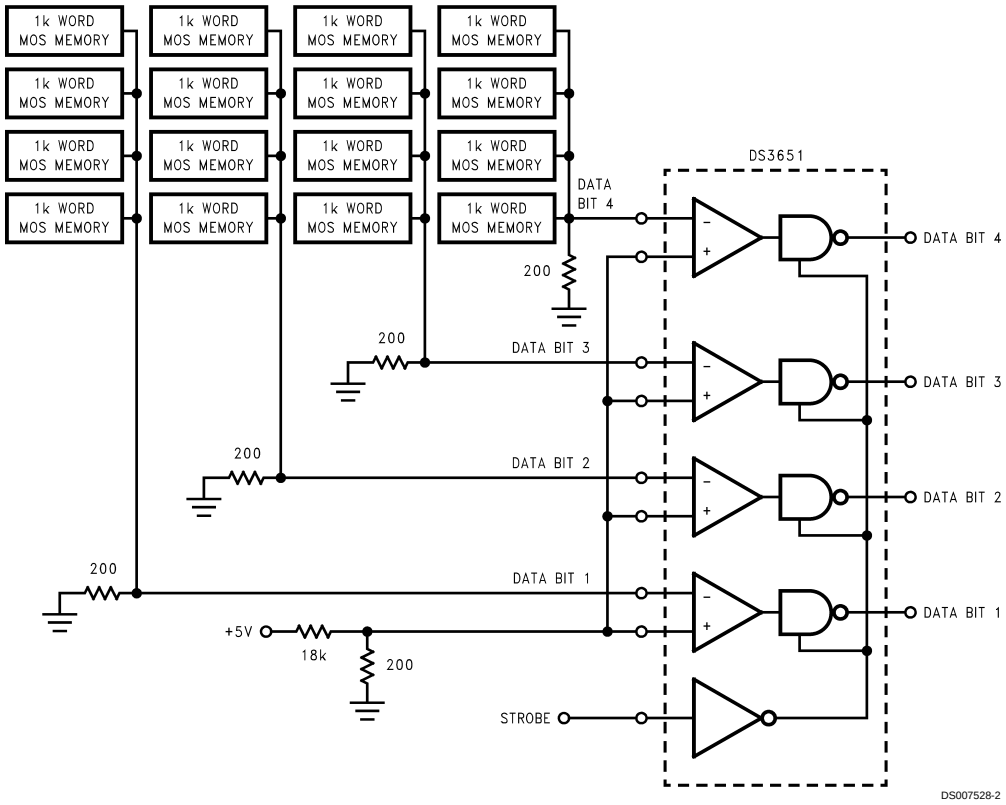
Typical Applications

A Typical MOS Memory Sensing Application for a 4k work by 4-bit Memory Arrangement Employing 1103 Type Memory Devices



Note: Only 4 devices are required for a 4k word by 16-bit memory system.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltages	
V_{CC}	+7 V_{DC}
V_{EE}	−7 V_{DC}
Differential-Mode Input Signal Voltage Range, V_{IDR}	±6 V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	±5 V_{DC}
Strobe Input Voltage, $V_{I(S)}$	5.5 V_{DC}
Strobe Temperature Range	−65˚C to +150˚C
Maximum Power Dissipation (Note 1) at 25˚C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temp. (Soldering, 10 seconds)	300˚C

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})			
DS1651	4.5	5.5	V
DS3651	4.75	5.25	V
Supply Voltage (V_{EE})			
DS1651	−4.5	−5.5	V
DS3651	−4.75	−5.25	V
Operating Temperature (T_A)			
DS1651	−55	+125	˚C
DS3651	0	+70	˚C
Output Load Current, (I_{OL})		16	mA
Differential Mode Input Voltage Range, (V_{IDR})	−5.0	+5.0	V
Common-Mode Input Voltage Range, (V_{ICR})	−3.0	+3.0	V
Input Voltage Range (Any Input to GND), (V_{IR})	−5.0	+3.0	V

Electrical Characteristics

V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted (Notes 3, 4)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{IS}	Input Sensitivity (Note 6) (Common-Mode Voltage Range) V_{ICR} = −3V ≤ V_{IN} ≤ +3V	Min ≤ V_{CC} ≤ Max Min ≥ V_{EE} ≥ Max					±7.0	mV
V_{IO}	Input Offset Voltage					2		mV
I_{IB}	Input Bias Current	V_{CC} = Max, V_{EE} = Max					20	µA
I_{IO}	Input Offset Current					0.5		µA
$V_{IL(S)}$	Strobe Input Voltage (Low State)						0.8	V
$V_{IH(S)}$	Strobe Input Voltage (High State)				2			V
$I_{IL(S)}$	Strobe Current (Low State)	V_{CC} = Max, V_{EE} = Max, V_{IN} = 0.4V					−1.6	mA
$I_{IL(S)}$	Strobe Current (High State)	V_{CC} = Max, V_{EE} = Max	V_{IN} = 2.4V	DS3651			40	µA
			V_{IN} = V_{CC}				1	mA
			V_{IN} = 2.4V	DS1651			100	µA
			V_{IN} = V_{CC}				1	mA
V_{OH}	Output Voltage (High States)	V_{CC} = Min, V_{EE} = Min	I_O = −400 µA	DS1651/DS3651	2.4			V
V_{OL}	Output Voltage (Low State)	V_{CC} = Min, V_{EE} = Min	I_O = 16 mA	DS3651			0.45	V
				DS1651			0.50	
I_{OS}	Output Current Short Circuit	V_{CC} = Max, V_{EE} = Max, (Note 5)		DS1651/DS3651	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	V_{CC} = Max, V_{EE} = Max		DS3651			40	µA
				DS1651			100	µA
I_{CC}	High Logic Level Supply Current	V_{CC} = Max, V_{EE} = Max				45	60	mA
I_{EE}	High Logic Level Supply Current	V_{CC} = Max, V_{EE} = Max				−17	−30	mA

Switching Characteristics

V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, T_A = 25˚C unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	5 mV + V_{IS}, (*Figure 2*)	DS1651/ DS3651		23	45	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)	5 mV + V_{IS}, (*Figure 2*)	DS1651/ DS3651		22	55	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)	(*Figure 1*)	DS1651/ DS3651		14	29	ns

Note 1: Derate cavity package 10.1 mW/˚C above 25˚C; derate molded package 11.8 mW/˚C above 25˚C.

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

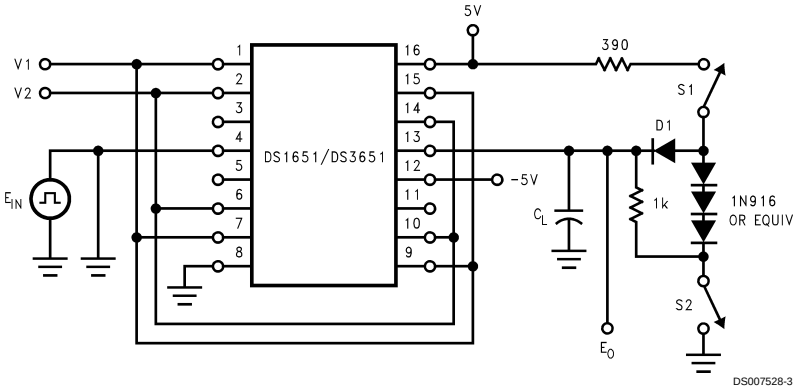
Note 3: Unless otherwise specified min/max limits apply across the 0˚C to +70˚C range for the DS3651 and across the −55˚C to +125˚C range for the DS1651. All typical values are for T_A = 25˚C, V_{CC} = 5V and V_{EE} = −5V.

Note 4: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 5: Only one output at a time should be shorted.

Note 6: A parameter which is of primary concern when designing with sense amplifiers is, what is the minimum differential input voltage required at the sense amplifier input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS1651 and DS3651 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents, and guarantees a minimum input differential voltage to cause a given output logic state with respect to a maximum source impedance of 200Ω at each input.

Switching Time Waveform



Note: Output of channel B shown under test, other channels are tested similarly.

Delay	V1	V2	S1	S2	C_L
$t_{PLO(S)}$)	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz
Duty cycle = 50%

AC Test Circuits

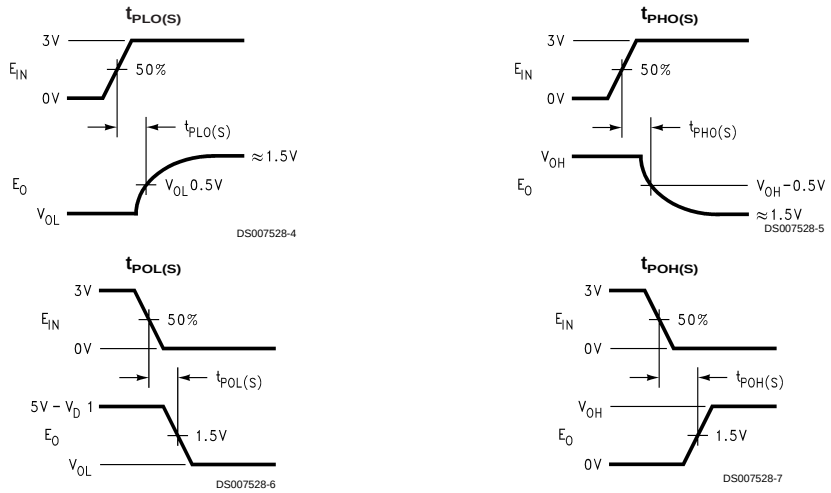
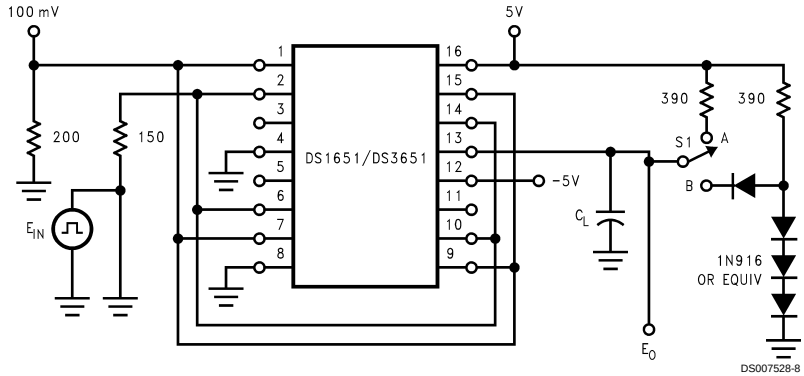
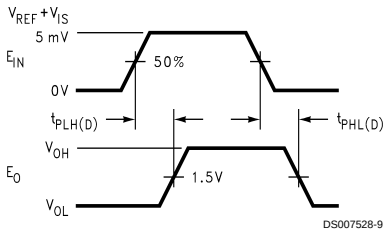


FIGURE 1. Strobe Propagation Delay $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHL(S)}$ and $t_{POH(S)}$



Note: Output of channel B shown under test, other channels are tested similarly.
S1 at "B" for DS1651/DS3651, C_L = 50 pF total for DS1651/DS3651.

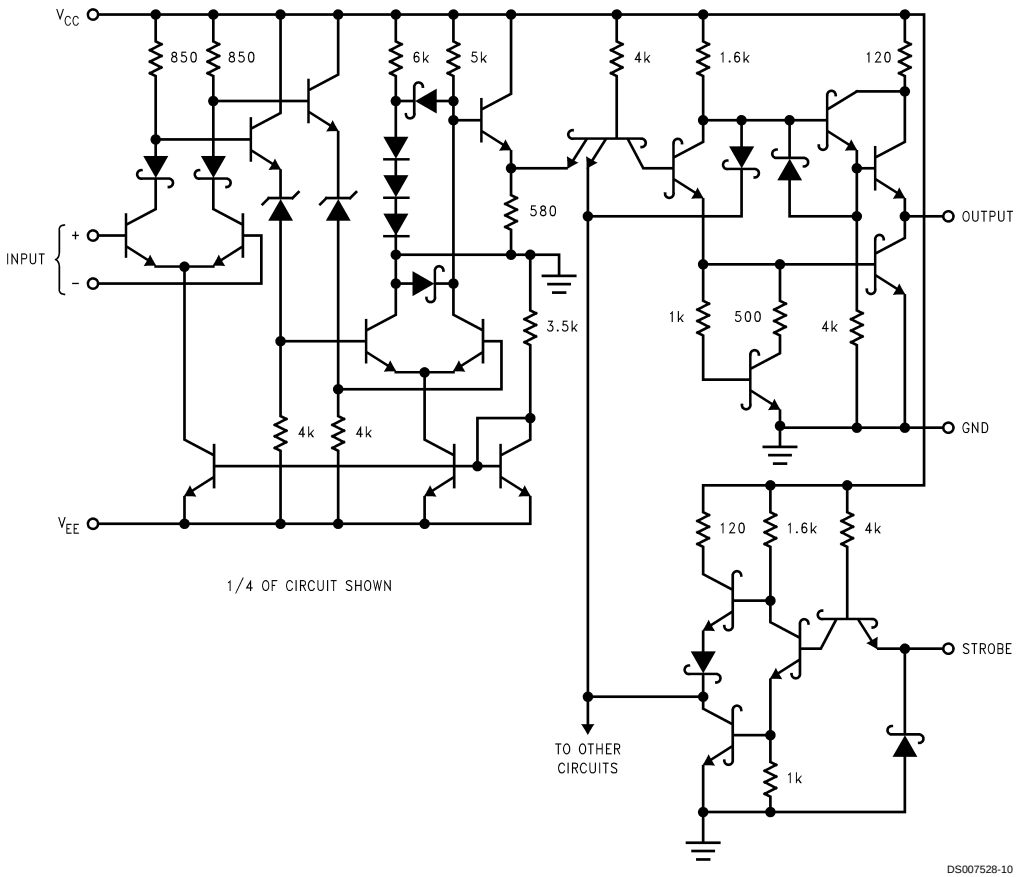


E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq$ 10 ns measured 10% to 90%
PRR = 1 MHz, duty cycle = 500 ns

FIGURE 2. Differential Input Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$

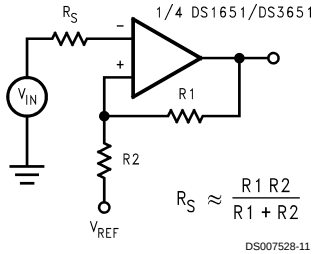
Schematic Diagrams

DS1651/DS3651



Typical Applications

Level Detector with Hysteresis



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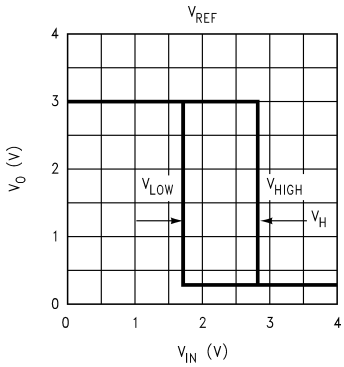
Transfer Characteristics and Equations for Level Detector with Hysteresis



DS007528-12

$$V_{HIGH} = V_{REF} + \frac{R2\,[V_{O(MAX)} - V_{REF}]}{R1 + R2}$$

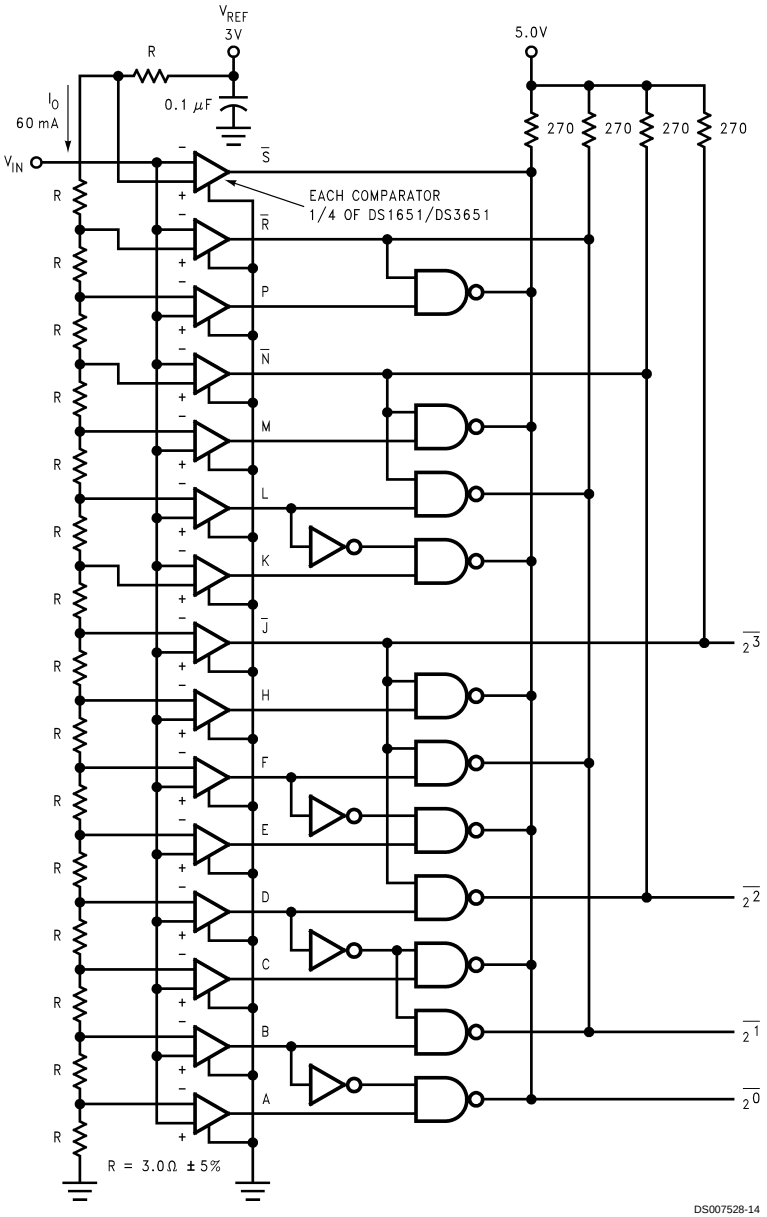
$$V_{LOW} = V_{REF} + \frac{R2\,[V_{O(MIN)} - V_{REF}]}{R1 + R2}$$

Hysteresis Loop (V_H)

$$V_H = V_{HIGH} - V_{LOW} = \frac{R2}{R1 + R2}\,[V_{O(MAX)} - V_{O(MIN)}]$$

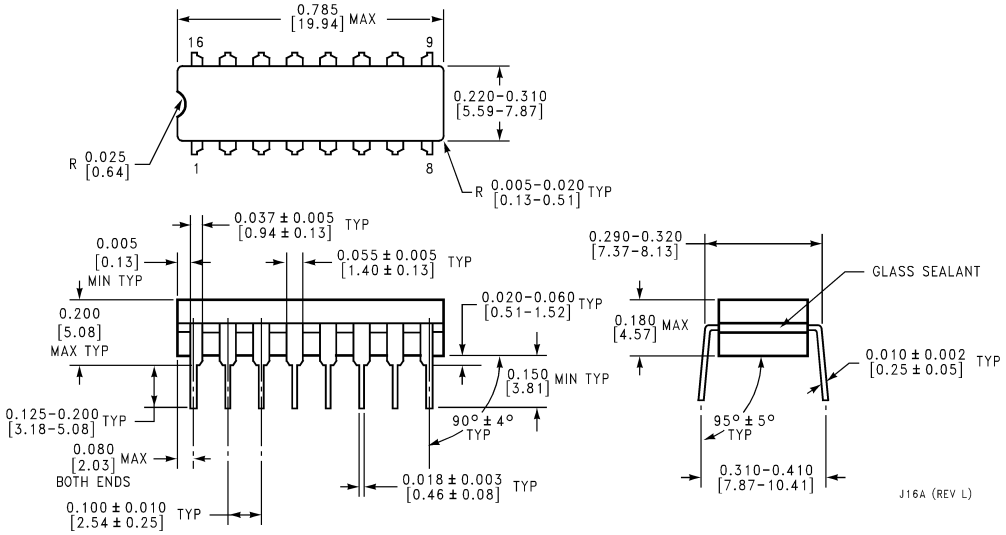
Typical Applications (Continued)

4-Bit Parallel A/D Converter

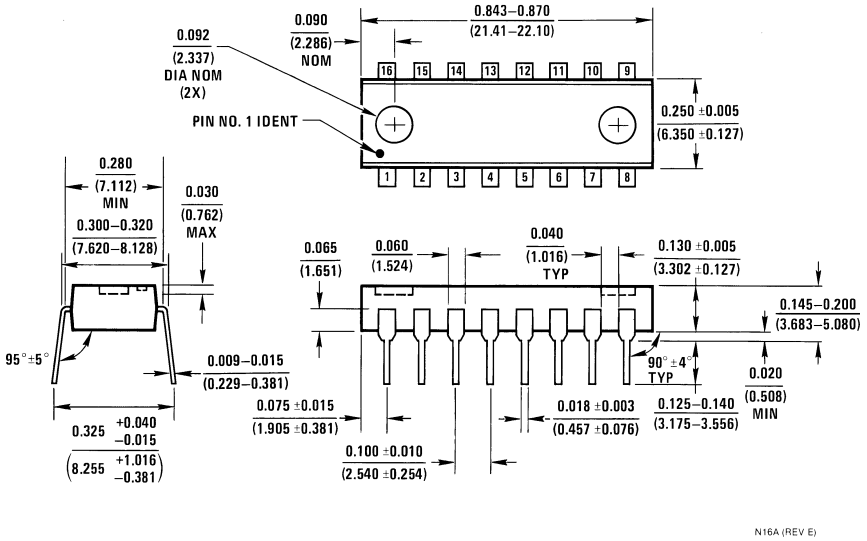


$\overline{2^0}$ = ($\overline{A}$ + B) ($\overline{C}$ + D) ($\overline{E}$ + F) ($\overline{H}$ + J) ($\overline{K}$ + L) ($\overline{M}$ + N) ($\overline{P}$ + R) ($\overline{S}$)
$\overline{2^1}$ = ($\overline{B}$ + D) ($\overline{F}$ + J) ($\overline{L}$ + N) ($\overline{R}$)
$\overline{2^2}$ = ($\overline{D}$ + J) ($\overline{N}$)
$\overline{2^3}$ = $\overline{J}$
Conversion time ≅ 50 ns

Physical Dimensions inches (millimeters) unless otherwise noted



Ceramic Dual-in-Line Package (J)
Order Number DS1651J, DS1653J, DS3651J or DS3653J
NS Package Number J16A



Molded Dual-in-Line Package (N)
Order Number DS3651N or DS3653N
NS Package Number N16A

Notes

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

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