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February 2000



DS75451/2/3 Series Dual Peripheral Drivers

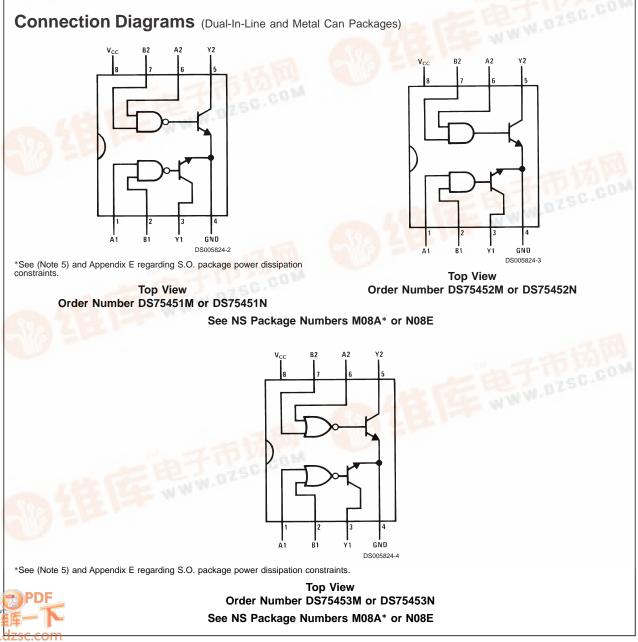
General Description

The DS7545X series of dual peripheral drivers is a family of versatile devices designed for use in systems that use TTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

The DS75451, DS75452 and DS75453 are dual peripheral AND, NAND and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

Features

- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI "A" and "B" series



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, (V _{CC}) (Note 2)	7.0V
Input Voltage	5.5V
Inter-Emitter Voltage (Note 3)	5.5V
Output Voltage (Note 4)	30V
Output Current (Note 5)	300 mA
Maximum Power (Note 5)	
Dissipation [†] at 25°C	

Molded DIP Package	957 mW
SO Package	632 mW
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, (V _{CC})	4.75	5.25	V
Temperature, (T _A)	0	+70	°C
†Derate molded package 7.7 mW/°(mW/°C above 25°C.	C above 25°C, c	lerate SO pac	kage 7.56

Electrical Characteristics

(Notes 6, 7)

Symbol	Parameter			Conditions		Min	Тур	Max	Units
	High-Level Input Voltage	(Figure 7)		Contaitions		2	1.76	max	V
	Low-Level Input Voltage							0.8	V
V _{IL}	· · ·								<u> </u>
VI	Input Clamp Voltage	$V_{CC} = Min$, I _I = –12 mA					-1.5	V
V _{OL}	Low-Level Output Voltage		V _{IL} = 0.8V	I _{OL} = 100 mA	DS75451, DS75453		0.25	0.4	V
		Min,		I _{OL} = 300 mA	DS75451, DS75453		0.5	0.7	V
		(Figure 7)	V _{IH} = 2V	I _{OL} = 100 mA	DS75452		0.25	0.4	V
				I _{OL} = 300 mA	DS75452		0.5	0.7	V
I _{он}	High-Level Output Current	V _{CC} = Min.	V _{OH} = 30V	$V_{IH} = 2V$	DS75451, DS75453			100	μA
		(<i>Figure 7</i>)		$V_{IL} = 0.8V$	DS75452			100	μA
I,	Input Current at Maximum Input Voltage	V _{CC} = Max	$V_{CC} = Max, V_1 = 5.5V, (Figure 9)$					1	mA
I _{IH}	High-Level Input Current	V _{CC} = Max	$k_{\rm I} = 2.4 V_{\rm I} (F)$	-igure 9)				40	μA
IIL	Low-Level Input Current	V _{CC} = Max	$k_{\rm I} = 0.4 V_{\rm I} (R)$	-igure 8)			-1	-1.6	mA
I _{CCH}	Supply Current, Outputs	00	V ₁ = 5V		DS75451		7	11	mA
	High	Max, (<i>Figure</i>	$V_{I} = 0V$		DS75452		11	14	mA
		10)	V ₁ = 5V		DS75453		8	11	mA
I _{CCL}	Supply Current, Outputs	V _{CC} =				52	65	mA	
	Low	Max, (<i>Figure</i>	V ₁ = 5V		DS75452		56	71	mA
		(<i>i</i> iguie 10)	$V_{I} = 0V$		DS75453		54	68	mA

Switching Characteristics

 $(V_{CC} = 5V, T_A = 25^{\circ}C)$

Symbol	Parameter	Conditions		Min	Тур	Max	Units
t _{PLH}	Propagation Delay Time, Low-to-High	$C_{L} = 15 \text{ pF}, R_{L} = 50\Omega,$	DS75451		18	25	ns
	Level Output	I _O ≈ 200 mA, (<i>Figure 14</i>)	DS75452		26	35	ns
			DS75453		18	25	ns
t _{PHL}	Propagation Delay Time, High-to-Low	$C_{L} = 15 \text{ pF}, R_{L} = 50\Omega,$	DS75451		18	25	ns
	Level Output	I _O ≈ 200 mA, (<i>Figure 14</i>)	DS75452		24	35	ns
			DS75453		16	25	ns
t _{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R _L = 50Ω, I _O ≈ 200 mA, (<i>Figure 14</i>)			5	8	ns
t _{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 50 Ω , $I_O \approx$ 200 mA, (Figure 14)			7	12	ns

Swite	Switching Characteristics (Continued)								
Symbol	Parameter	Conditions		Min	Тур	Max	Units		
V _{OH}	High-Level Output Voltage after Switching	$V_{\rm S}$ = 20V, $I_{\rm O}$ \approx 300 mA, (Fi	igure 15)	V _S – 6.5			mV		

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: The voltage between two emitters of a multiple-emitter transistor.

Note 4: The maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 5: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 6: Unless otherwise specified min/max limits apply across 0°C to +70°C range. All typicals are given for V_{CC} = +5V and T_A = 25°C.

Note 7: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Truth Tables (H = high level, L = low level)

DS75451

Α	В	Y		
L	L	L (ON State)		
L	Н	L (ON State)		
н	L	L (ON State)		
н	Н	H (OFF State)		

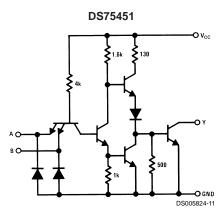
DS75452

Α	В	Y	
L	L	H (OFF State)	
L	Н	H (OFF State)	
н	L	H (OFF State)	
Н	Н	L (ON State)	

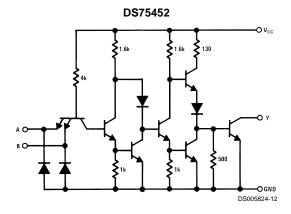
DS75453

Α	В	Y
L	L	L (ON State)
L	Н	H (OFF State)
Н	L	H (OFF State)
н	н	H (OFF State)

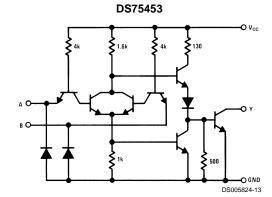
Schematic Diagrams



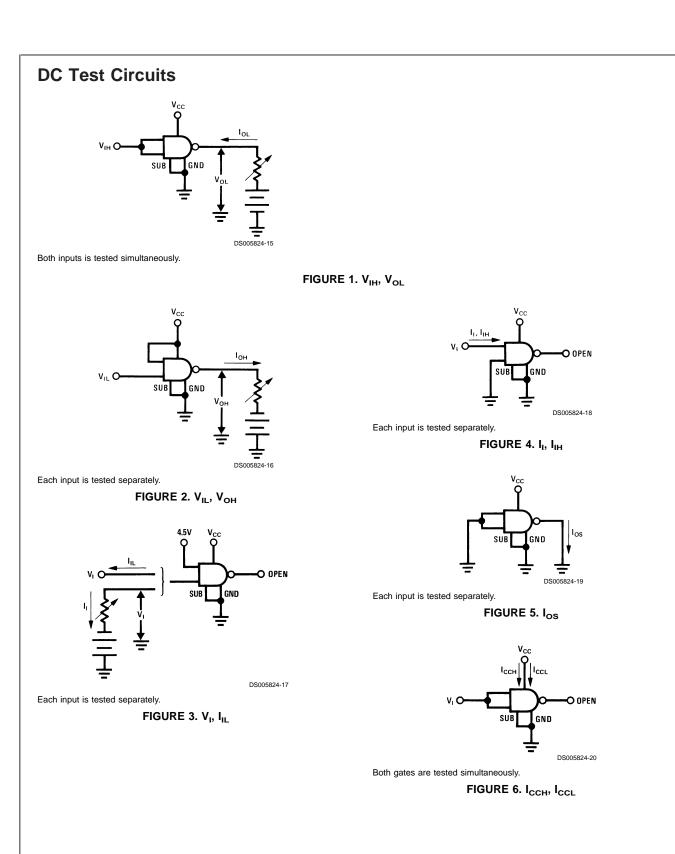
Resistor values shown are nominal.



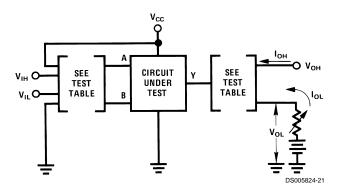
Resistor values shown are nominal.



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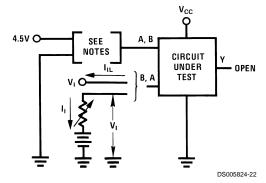






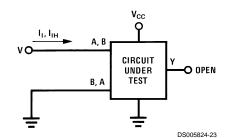
Circuit	Input Circuit Under		Οι	ıtput
Circuit	Test	Input	Apply	Measure
DS75451	V _{IH}	V _{IH}	V _{он}	I _{OL}
	V _{IL}	V _{cc}	I _{OL}	V _{OL}
DS75452	V _{IH}	V _{IH}	I _{OL}	V _{OL}
	V _{IL}	V _{cc}	V _{он}	I _{он}
DS75453	V _{IH}	Gnd	V _{он}	I _{он}
	V _{IL}	V _{IL}	I _{OL}	V _{он}

FIGURE 7. V_{IH} , V_{IL} , I_{OH} , V_{OL}



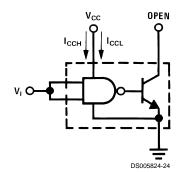
Note A: Each input is tested separately. **Note B:** When testing DS75453 input not under test is grounded. For all other circuits it is at 4.5V.





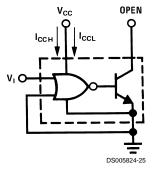
Each input is tested separately.





Both gates are tested simultaneously.

FIGURE 10. $I_{\rm CCH},\,I_{\rm CCL}$ for AND, NAND Circuits



Both gates are tested simultaneously.

FIGURE 11. I_{CCH}, I_{CCL} for OR, NOR Circuits

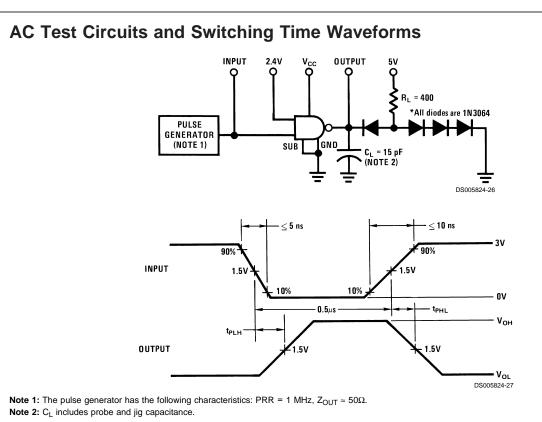
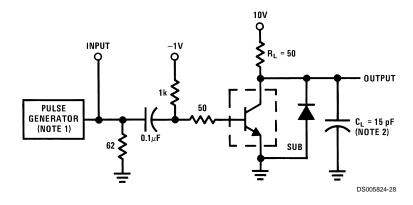
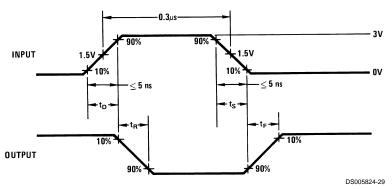


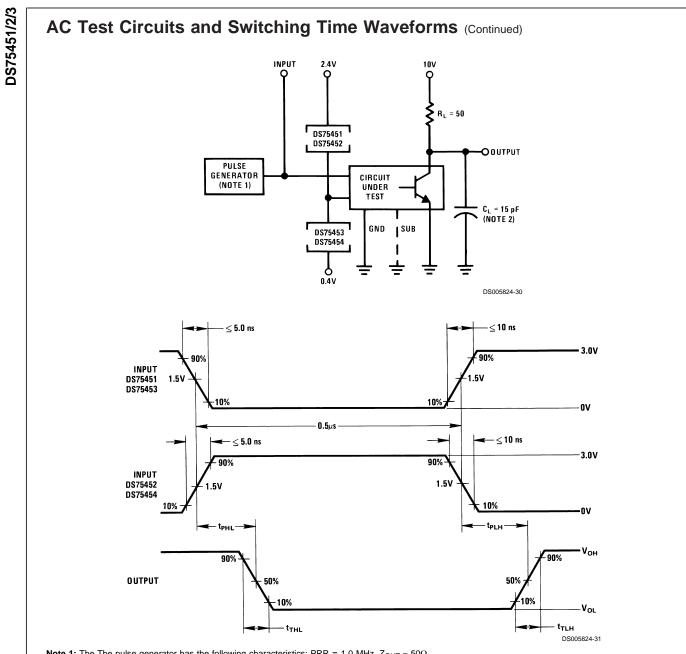
FIGURE 12. Propagation Delay Times, Each Gate





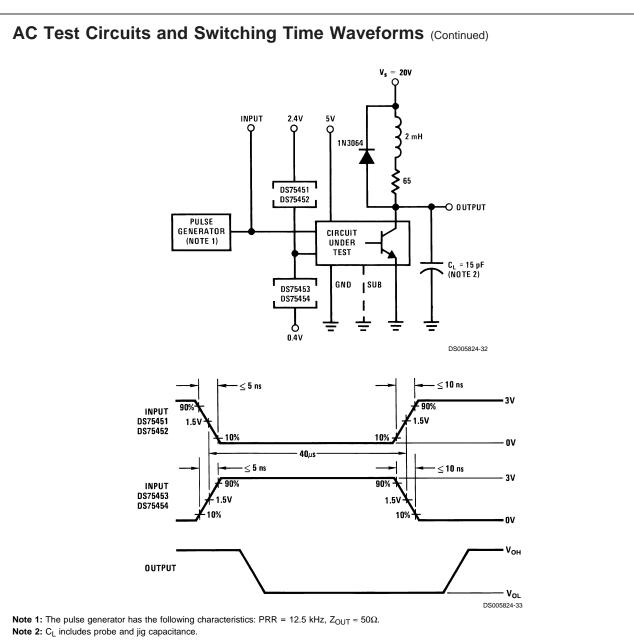
Note 1: The pulse generator has the following characteristics: duty cycle \leq 1%, $Z_{OUT} \approx 50\Omega$. **Note 2:** C_L includes probe and jig capacitance.





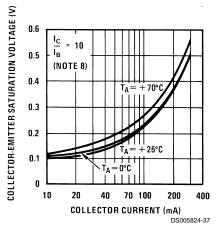
Note 1: The The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$. **Note 2:** C_L includes probe and jig capacitance.

FIGURE 14. Switching Times of Complete Drivers





Typical Performance Characteristics

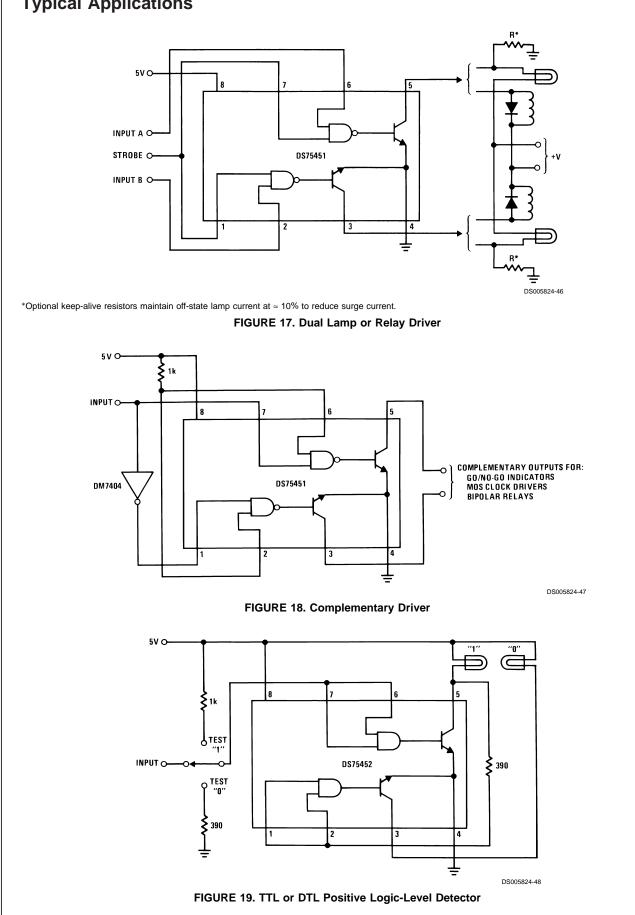


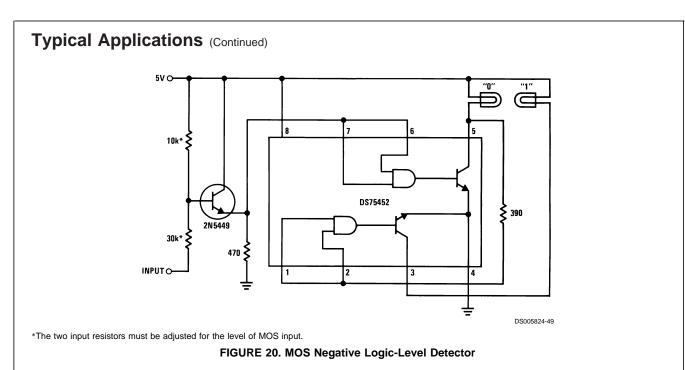


DS75451/2/3

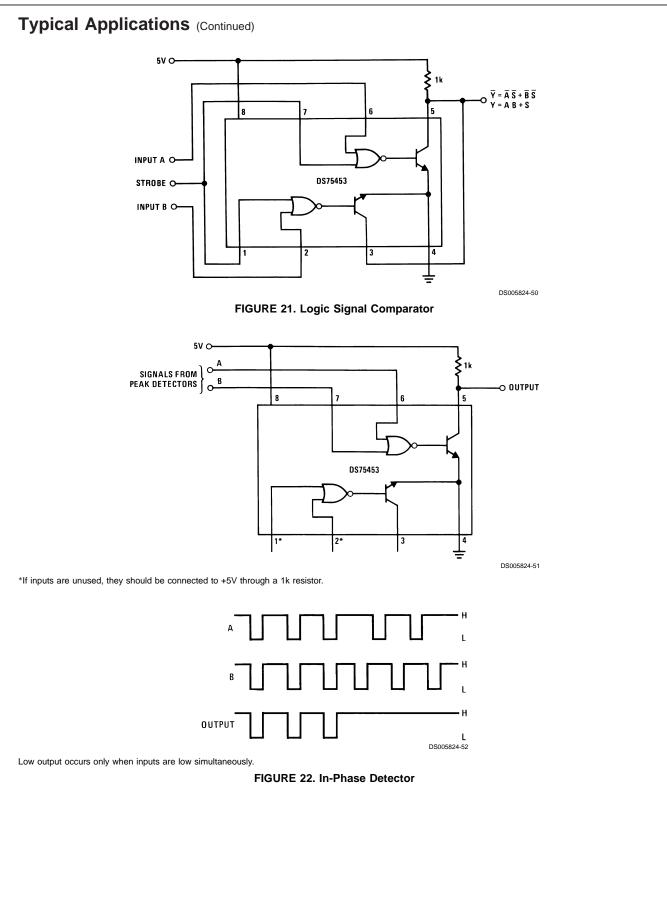


Typical Applications

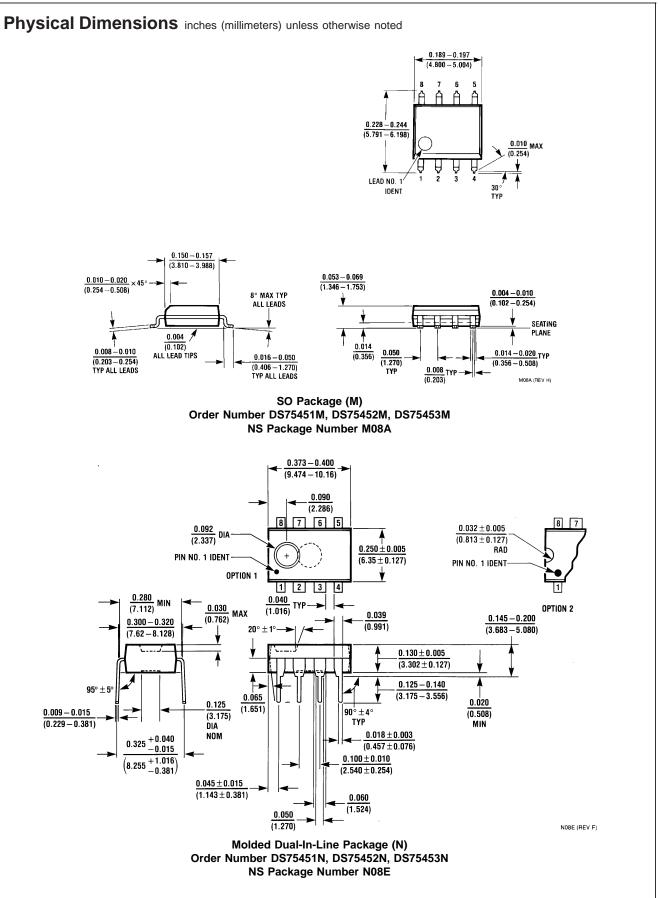












Notes

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