

June 1999

DS90CR286A/DS90CR216A

+3.3V Rising Edge Data Strobe LVDS Receiver 28-Bit Channel Link—66 MHz, +3.3V Rising Edge Strobe LVDS Receiver 21-Bit Channel Link—66 MHz

General Description

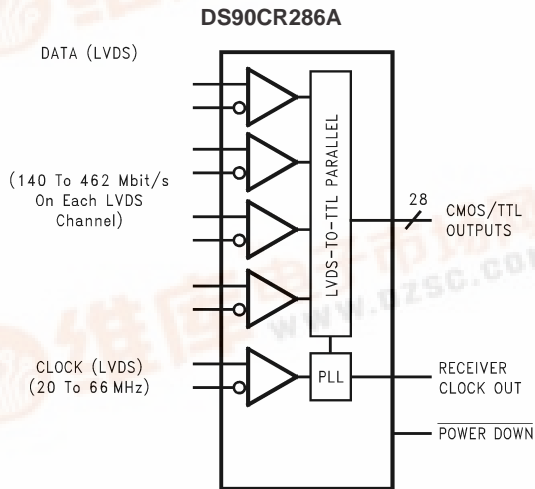
The DS90CR286A receiver converts the four LVDS data streams (Up to 1.848 Gbps throughput or 231 Megabytes/sec bandwidth) back into parallel 28 bits of CMOS/TTL data. Also available is the DS90CR216A that converts the three LVDS data streams (Up to 1.386 Gbps throughput or 173 Megabytes/sec bandwidth) back into parallel 21 bits of CMOS/TTL data. Both Receivers' outputs are Rising edge strobe.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

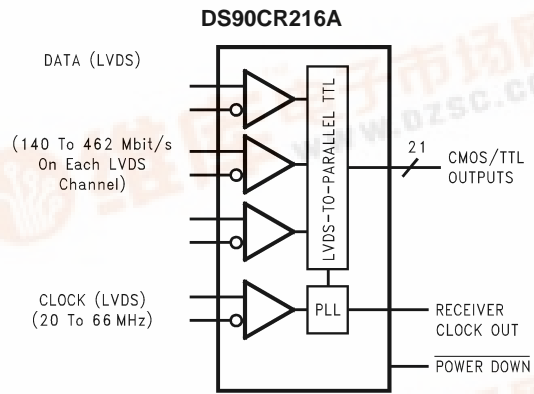
Features

- 20 to 66 MHz shift clock support
- 50% duty cycle on receiver output clock
- Best-in-Class Set & Hold Times on RxOUTPUTS
- Rx power consumption <270 mW (typ) @66MHz Worst Case
- Rx Power-down mode <200µW (max)
- ESD rating >7 kV (HBM), >700V (EIAJ)
- PLL requires no external components
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 56-lead or 48-lead TSSOP package
- Operating Temperature: -40°C to +85°C

Block Diagrams



Order Number DS90CR286AMTD
See NS Package Number MTD56



Order Number DS90CR216AMTD
See NS Package Number MTD48

DS90CR286A/DS90CR216A +3.3V Rising Edge Data Strobe LVDS Receiver 28-Bit Channel Link—66 MHz, +3.3V Rising Edge Data Strobe LVDS Receiver 21-Bit Channel Link—66 MHz



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-----------------------------|------------------------------|
| Supply Voltage (V_{CC}) | -0.3V to +4V |
| CMOS/TTL Output Voltage | -0.3V to ($V_{CC} + 0.3V$) |
| LVDS Receiver Input Voltage | -0.3V to ($V_{CC} + 0.3V$) |
| Junction Temperature | +150°C |
| Storage Temperature | -65°C to +150°C |

| | |
|-------------------------------------|--------|
| Lead Temperature (Soldering, 4 sec) | +260°C |
|-------------------------------------|--------|

Maximum Package Power Dissipation Capacity @ 25°C

| | |
|------------------------|--------|
| MTD56 (TSSOP) Package: | |
| DS90CR286A | 1.61 W |
| MTD48 (TSSOP) Package: | |
| DS90CR216A | 1.89 W |

Package Derating:

| | |
|------------|------------------------|
| DS90CR286A | 12.4 mW/°C above +25°C |
| DS90CR216A | 15 mW/°C above +25°C |

ESD Rating

| | |
|--------------------------------|--------|
| (HBM, 1.5 k Ω , 100 pF) | > 7 kV |
| (EIAJ, 0 Ω , 200 pF) | > 700V |

Recommended Operating Conditions

| | Min | Nom | Max | Units |
|--|-----|-----|-----|------------------|
| Supply Voltage (V_{CC}) | 3.0 | 3.3 | 3.6 | V |
| Operating Free Air Temperature (T_A) | -40 | +25 | +85 | °C |
| Receiver Input Range | 0 | | 2.4 | V |
| Supply Noise Voltage (V_{CC}) | | | 100 | mV _{PP} |

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|--|------------------------------------|---|----------------|------|----------|---------|----|
| CMOS/TTL DC SPECIFICATIONS | | | | | | | |
| V_{OH} | High Level Output Voltage | $I_{OH} = -0.4$ mA | 2.7 | 3.3 | | V | |
| V_{OL} | Low Level Output Voltage | $I_{OL} = 2$ mA | | 0.06 | 0.3 | V | |
| I_{OS} | Output Short Circuit Current | $V_{OUT} = 0V$ | | -60 | -120 | mA | |
| LVDS RECEIVER DC SPECIFICATIONS | | | | | | | |
| V_{TH} | Differential Input High Threshold | $V_{CM} = +1.2V$ | | | +100 | mV | |
| V_{TL} | Differential Input Low Threshold | | -100 | | | mV | |
| I_{IN} | Input Current | $V_{IN} = +2.4V, V_{CC} = 3.6V$ | | | ± 10 | μA | |
| | | $V_{IN} = 0V, V_{CC} = 3.6V$ | | | ± 10 | μA | |
| RECEIVER SUPPLY CURRENT | | | | | | | |
| ICCRW | Receiver Supply Current Worst Case | $C_L = 8$ pF, Worst Case Pattern, DS90CR286A (Figures 1, 2), $T_A = -10^\circ C$ to $+70^\circ C$ | $f = 33$ MHz | | 49 | 65 | mA |
| | | | $f = 37.5$ MHz | | 53 | 70 | mA |
| | | | $f = 66$ MHz | | 81 | 105 | mA |
| ICCRW | Receiver Supply Current Worst Case | $C_L = 8$ pF, Worst Case Pattern, DS90CR286A (Figures 1, 2), $T_A = -40^\circ C$ to $+85^\circ C$ | $f = 40$ MHz | | 53 | 70 | mA |
| | | | $f = 66$ MHz | | 81 | 105 | mA |
| ICCRW | Receiver Supply Current Worst Case | $C_L = 8$ pF, Worst Case Pattern, DS90CR216A (Figures 1, 2), $T_A = -10^\circ C$ to $+70^\circ C$ | $f = 33$ MHz | | 49 | 55 | mA |
| | | | $f = 37.5$ MHz | | 53 | 60 | mA |
| | | | $f = 66$ MHz | | 78 | 90 | mA |
| ICCRW | Receiver Supply Current Worst Case | $C_L = 8$ pF, Worst Case Pattern, DS90CR216A (Figures 1, 2), $T_A = -40^\circ C$ to $+85^\circ C$ | $f = 40$ MHz | | 53 | 60 | mA |
| | | | $f = 66$ MHz | | 78 | 90 | mA |
| ICCRZ | Receiver Supply Current Power Down | Power Down = Low Receiver Outputs Stay Low during Power Down Mode | | 10 | 55 | μA | |

Electrical Characteristics (Continued)

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for $V_{CC} = 3.3V$ and $T_A = +25C$.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Receiver Switching Characteristics

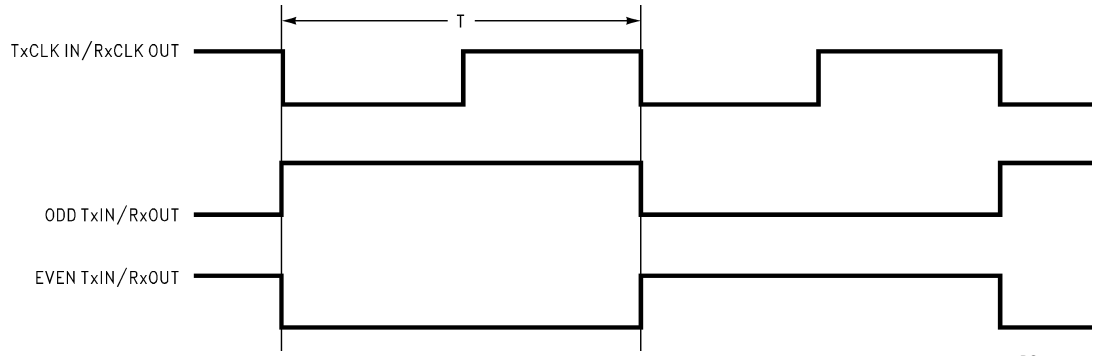
Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | Min | Typ | Max | Units | |
|--------|--|------------|------|------|-------|----|
| CLHT | CMOS/TTL Low-to-High Transition Time (Figure 2) | | 2 | 5 | ns | |
| CHLT | CMOS/TTL High-to-Low Transition Time (Figure 2) | | 1.8 | 5 | ns | |
| RSPos0 | Receiver Input Strobe Position for Bit 0 (Figure 9, Figure 10) | f = 40 MHz | 1.0 | 1.4 | 2.15 | ns |
| RSPos1 | Receiver Input Strobe Position for Bit 1 | | 4.5 | 5.0 | 5.8 | ns |
| RSPos2 | Receiver Input Strobe Position for Bit 2 | | 8.1 | 8.5 | 9.15 | ns |
| RSPos3 | Receiver Input Strobe Position for Bit 3 | | 11.6 | 11.9 | 12.6 | ns |
| RSPos4 | Receiver Input Strobe Position for Bit 4 | | 15.1 | 15.6 | 16.3 | ns |
| RSPos5 | Receiver Input Strobe Position for Bit 5 | | 18.8 | 19.2 | 19.9 | ns |
| RSPos6 | Receiver Input Strobe Position for Bit 6 | | 22.5 | 22.9 | 23.6 | ns |
| RSPos0 | Receiver Input Strobe Position for Bit 0 (Figure 9, Figure 10) | f = 66 MHz | 0.7 | 1.1 | 1.4 | ns |
| RSPos1 | Receiver Input Strobe Position for Bit 1 | | 2.9 | 3.3 | 3.6 | ns |
| RSPos2 | Receiver Input Strobe Position for Bit 2 | | 5.1 | 5.5 | 5.8 | ns |
| RSPos3 | Receiver Input Strobe Position for Bit 3 | | 7.3 | 7.7 | 8.0 | ns |
| RSPos4 | Receiver Input Strobe Position for Bit 4 | | 9.5 | 9.9 | 10.2 | ns |
| RSPos5 | Receiver Input Strobe Position for Bit 5 | | 11.7 | 12.1 | 12.4 | ns |
| RSPos6 | Receiver Input Strobe Position for Bit 6 | | 13.9 | 14.3 | 14.6 | ns |
| RSKM | RxIN Skew Margin (Note 4) (Figure 11) | f = 40 MHz | 490 | | | ps |
| | | f = 66 MHz | 400 | | | ps |
| RCOP | RxCLK OUT Period (Figure 3) | | 15 | T | 50 | ns |
| RCOH | RxCLK OUT High Time (Figure 3) | f = 40 MHz | 10.0 | 12.2 | | ns |
| RCOL | RxCLK OUT Low Time (Figure 3) | | 10.0 | 11.0 | | ns |
| RSRC | RxOUT Setup to RxCLK OUT (Figure 3) | | 6.5 | 11.6 | | ns |
| RHRC | RxOUT Hold to RxCLK OUT (Figure 3) | | 6.0 | 11.6 | | ns |
| RCOH | RxCLK OUT High Time (Figure 3) | f = 66 MHz | 5.0 | 7.6 | | ns |
| RCOL | RxCLK OUT Low Time (Figure 3) | | 5.0 | 6.3 | | ns |
| RSRC | RxOUT Setup to RxCLK OUT (Figure 3) | | 4.5 | 7.3 | | ns |
| RHRC | RxOUT Hold to RxCLK OUT (Figure 3) | | 4.0 | 6.3 | | ns |
| RCCD | RxCLK IN to RxCLK OUT Delay 25°C, $V_{CC} = 3.3V$ (Note 5)(Figure 4) | | 3.5 | 5.0 | 7.5 | ns |
| RPLLS | Receiver Phase Lock Loop Set (Figure 5) | | | 10 | | ms |
| RPDD | Receiver Power Down Delay (Figure 8) | | | 1 | | µs |

Note 4: Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPos). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 250 ps).

Note 5: Total latency for the channel link chipset is a function of clock period and gate delays through the transmitter (TCCD) and receiver (RCCD). The total latency for the 215/285 transmitter and 216A/286A receiver is: $(T + TCCD) + (2 * T + RCCD)$, where T = Clock period.

AC Timing Diagrams



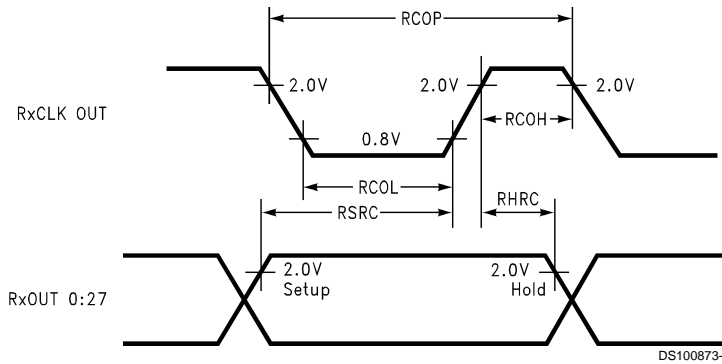
DS100873-2

FIGURE 1. "Worst Case" Test Pattern



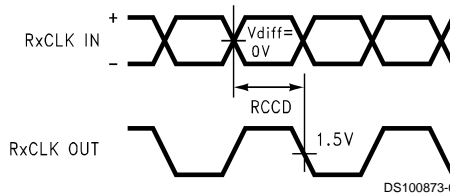
DS100873-4

FIGURE 2. DS90CR286A/DS90CR216A (Receiver) CMOS/TTL Output Load and Transition Times



DS100873-5

FIGURE 3. DS90CR286A/DS90CR216A (Receiver) Setup/Hold and High/Low Times



DS100873-6

FIGURE 4. DS90CR286A/DS90CR216A (Receiver) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

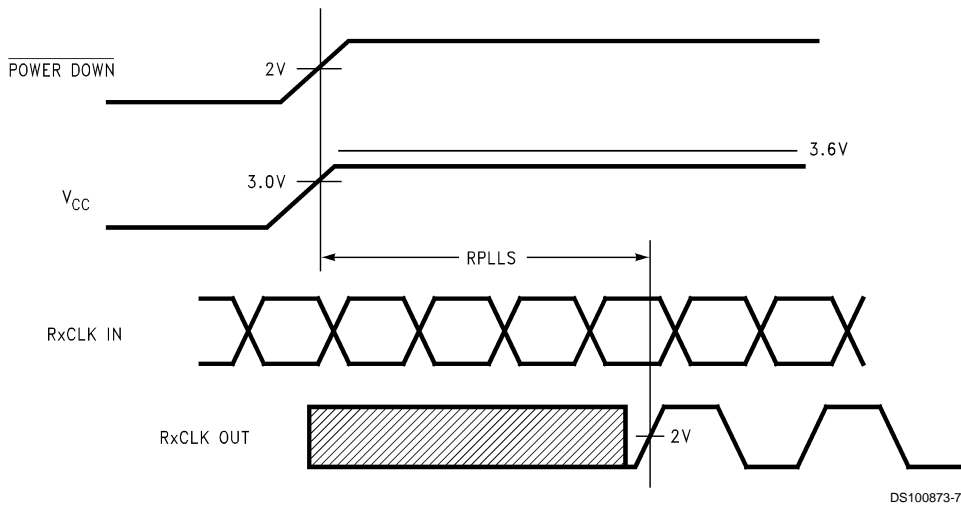


FIGURE 5. DS90CR286A/DS90CR216A (Receiver) Phase Lock Loop Set Time

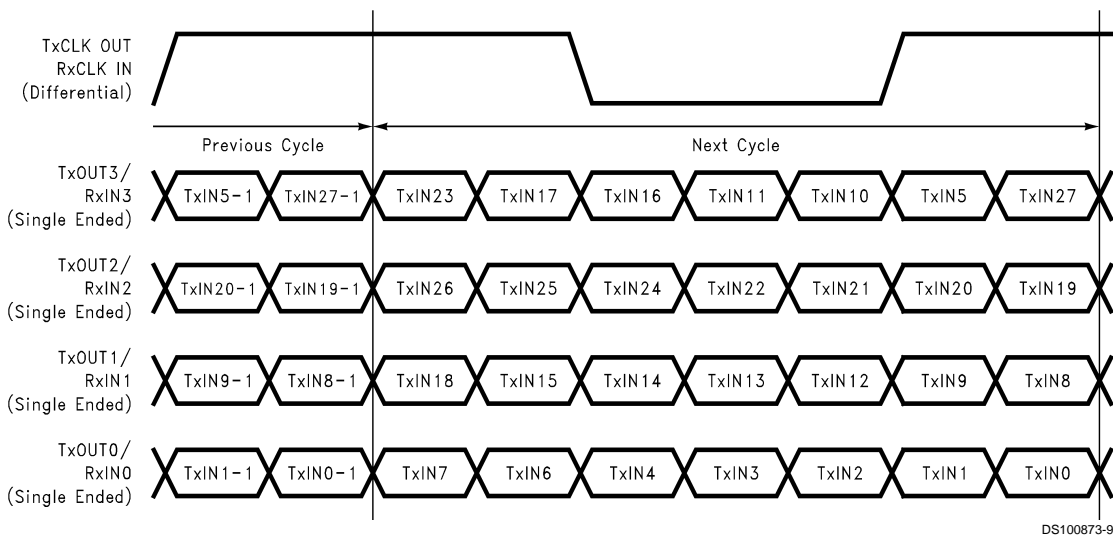


FIGURE 6. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90CR286A

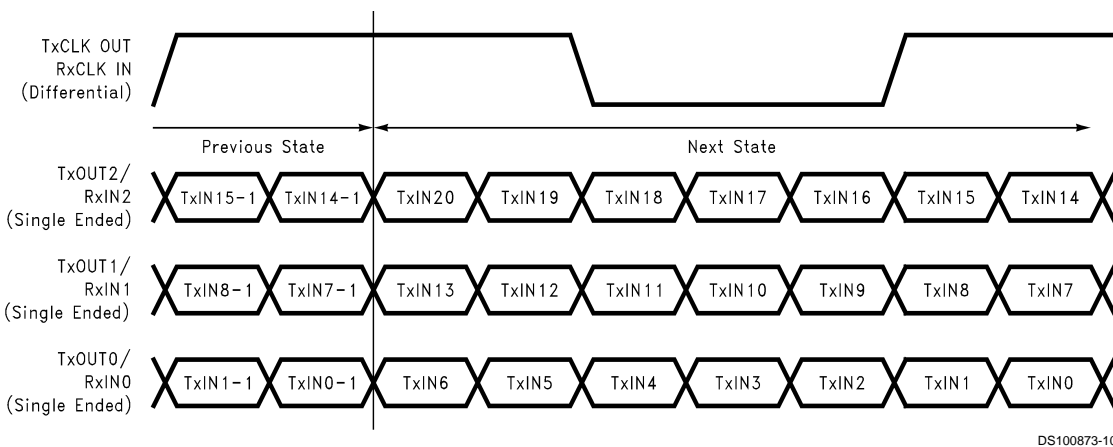


FIGURE 7. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90CR216A

AC Timing Diagrams (Continued)

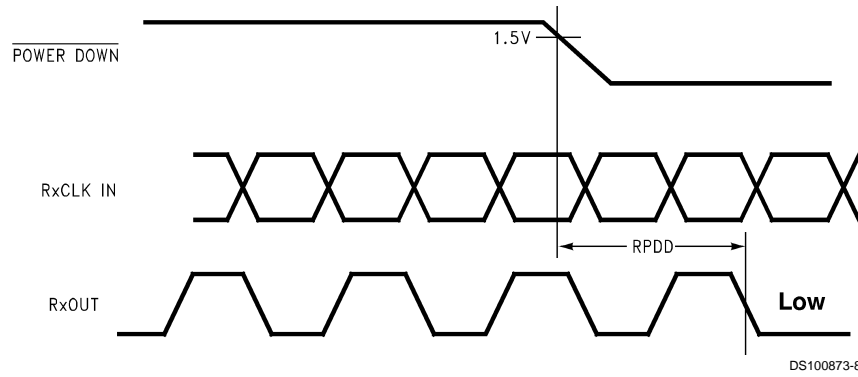


FIGURE 8. DS90CR286A/DS90CR216A (Receiver) Power Down Delay

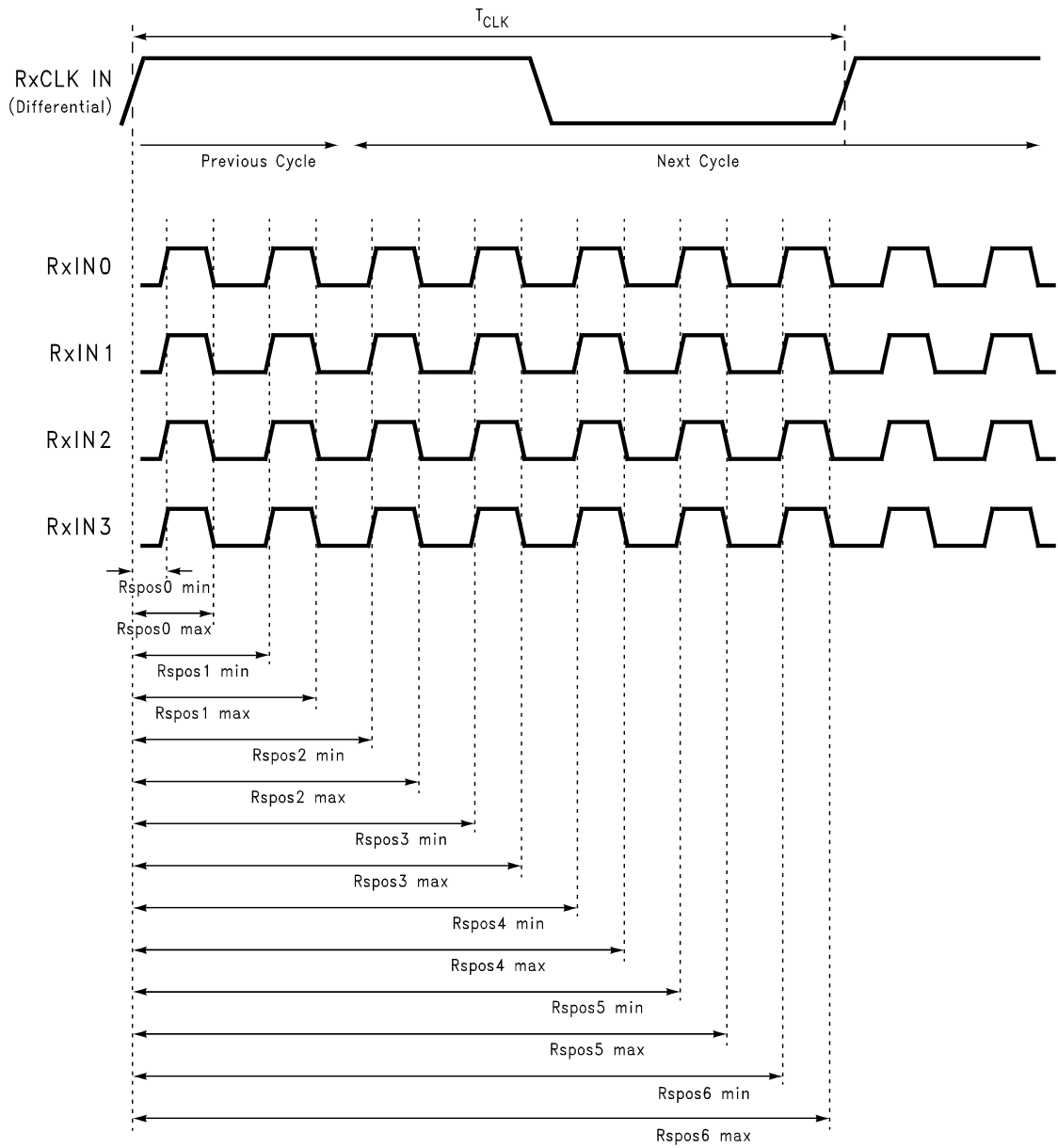
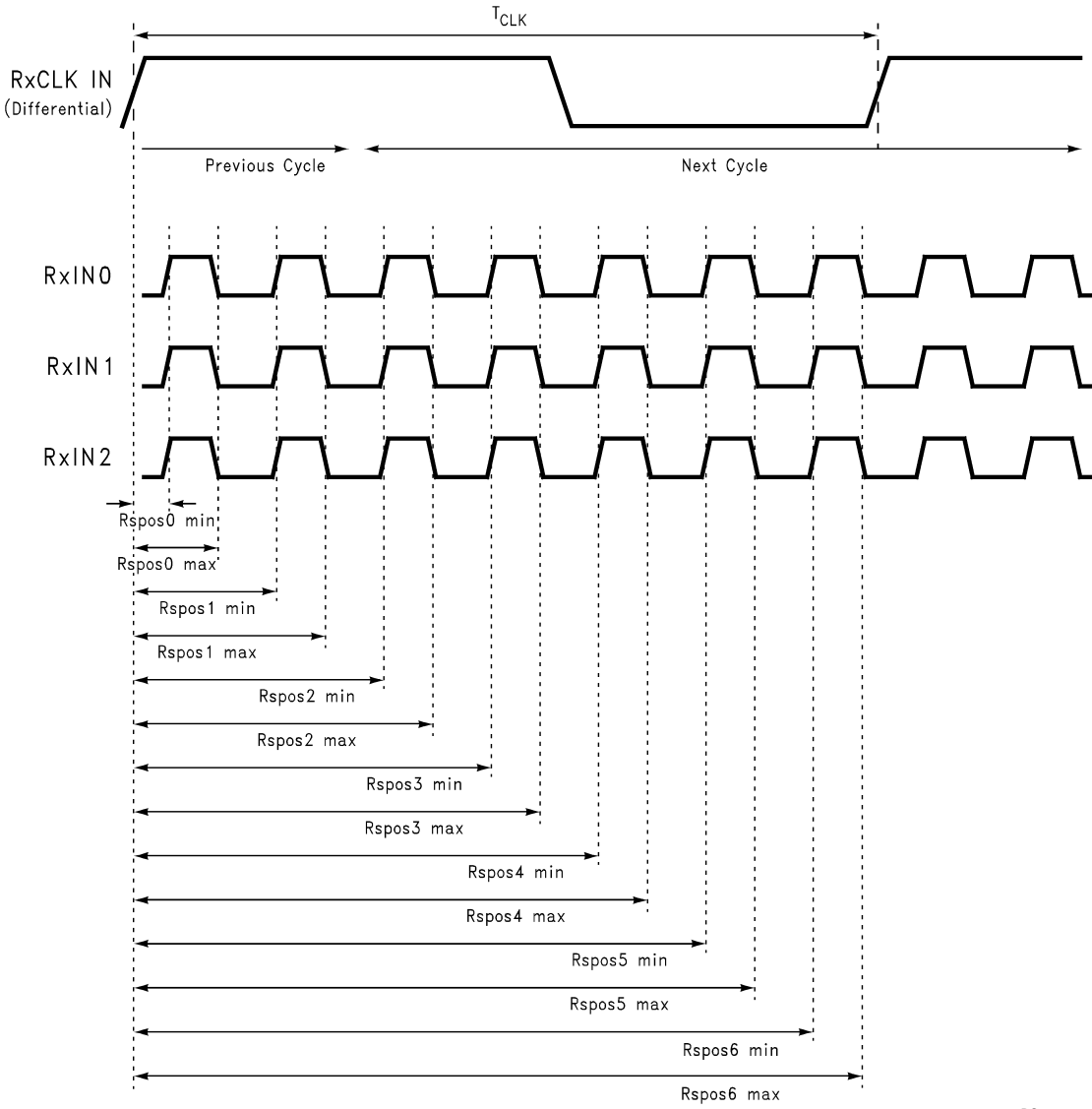


FIGURE 9. DS90CR286A (Receiver) LVDS Input Strobe Position

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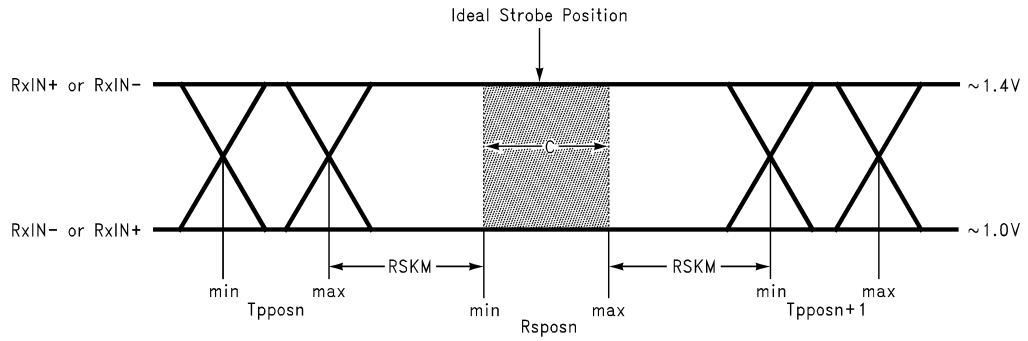
AC Timing Diagrams (Continued)



DS100873-26

FIGURE 10. DS90CR216A (Receiver) LVDS Input Strobe Position

AC Timing Diagrams (Continued)



DS100873-11

C — Setup and Hold Time (Internal data sampling window) defined by Rspostn (receiver input strobe position) min and max
 Tpposn — Transmitter output pulse position (min and max)
 RSKM = Cable Skew (type, length) + Source Clock Jitter (cycle to cycle) (Note 6) + ISI (Inter-symbol interference) (Note 7)
 Cable Skew — typically 10 ps–40 ps per foot, media dependent

Note 6: Cycle-to-cycle jitter is less than TBD ps at 66 MHz.
Note 7: ISI is dependent on interconnect length; may be zero.

FIGURE 11. Receiver LVDS Input Skew Margin

DS90CR286A Pin Description— 28-Bit Channel Link Receiver

| Pin Name | I/O | No. | Description |
|----------------------|-----|-----|--|
| RxIN+ | I | 4 | Positive LVDS differential data inputs. |
| RxIN- | I | 4 | Negative LVDS differential data inputs. |
| RxOUT | O | 28 | TTL level data outputs. |
| RxCLK IN+ | I | 1 | Positive LVDS differential clock input. |
| RxCLK IN- | I | 1 | Negative LVDS differential clock input. |
| RxCLK OUT | O | 1 | TTL level clock output. The rising edge acts as data strobe. |
| PWR DOWN | I | 1 | TTL level input. When asserted (low input) the receiver outputs are low. |
| V _{CC} | I | 4 | Power supply pins for TTL outputs. |
| GND | I | 5 | Ground pins for TTL outputs. |
| PLL V _{CC} | I | 1 | Power supply for PLL. |
| PLL GND | I | 2 | Ground pin for PLL. |
| LVDS V _{CC} | I | 1 | Power supply pin for LVDS inputs. |
| LVDS GND | I | 3 | Ground pins for LVDS inputs. |

DS90CR216A Pin Description— 21-Bit Channel Link Receiver

| Pin Name | I/O | No. | Description |
|----------------------|-----|-----|--|
| RxIN+ | I | 3 | Positive LVDS differential data inputs. (Note 8) |
| RxIN- | I | 3 | Negative LVDS differential data inputs. (Note 8) |
| RxOUT | O | 21 | TTL level data outputs. |
| RxCLK IN+ | I | 1 | Positive LVDS differential clock input. |
| RxCLK IN- | I | 1 | Negative LVDS differential clock input. |
| RxCLK OUT | O | 1 | TTL level clock output. The rising edge acts as data strobe. |
| PWR DOWN | I | 1 | TTL level input. When asserted (low input) the receiver outputs are low. |
| V _{CC} | I | 4 | Power supply pins for TTL outputs. |
| GND | I | 5 | Ground pins for TTL outputs. |
| PLL V _{CC} | I | 1 | Power supply for PLL. |
| PLL GND | I | 2 | Ground pin for PLL. |
| LVDS V _{CC} | I | 1 | Power supply pin for LVDS inputs. |
| LVDS GND | I | 3 | Ground pins for LVDS inputs. |

Note 8: These receivers have input failsafe bias circuitry to guarantee a stable receiver output for floating or terminated receiver inputs. Under these conditions receiver inputs will be in a HIGH state. If a clock signal is present, outputs will all be HIGH; if the clock input is also floating/terminated outputs will remain in the last valid state. A floating/terminated clock input will result in a LOW clock output.

Pin Diagram

DS90CR286A

| | | | |
|----------------------|----|----|-----------------|
| RxOUT22 | 1 | 56 | V _{CC} |
| RxOUT23 | 2 | 55 | RxOUT21 |
| RxOUT24 | 3 | 54 | RxOUT20 |
| GND | 4 | 53 | RxOUT19 |
| RxOUT25 | 5 | 52 | GND |
| RxOUT26 | 6 | 51 | RxOUT18 |
| RxOUT27 | 7 | 50 | RxOUT17 |
| LVDS GND | 8 | 49 | RxOUT16 |
| RxIN0- | 9 | 48 | V _{CC} |
| RxIN0+ | 10 | 47 | RxOUT15 |
| RxIN1- | 11 | 46 | RxOUT14 |
| RxIN1+ | 12 | 45 | RxOUT13 |
| LVDS V _{CC} | 13 | 44 | GND |
| LVDS GND | 14 | 43 | RxOUT12 |
| RxIN2- | 15 | 42 | RxOUT11 |
| RxIN2+ | 16 | 41 | RxOUT10 |
| RxCLKIN- | 17 | 40 | V _{CC} |
| RxCLKIN+ | 18 | 39 | RxOUT9 |
| RxIN3- | 19 | 38 | RxOUT8 |
| RxIN3+ | 20 | 37 | RxOUT7 |
| LVDS GND | 21 | 36 | GND |
| PLL GND | 22 | 35 | RxOUT6 |
| PLL V _{CC} | 23 | 34 | RxOUT5 |
| PLL GND | 24 | 33 | RxOUT4 |
| PWR DWN | 25 | 32 | RxOUT3 |
| RxCLK OUT | 26 | 31 | V _{CC} |
| RxOUT0 | 27 | 30 | RxOUT2 |
| GND | 28 | 29 | RxOUT1 |

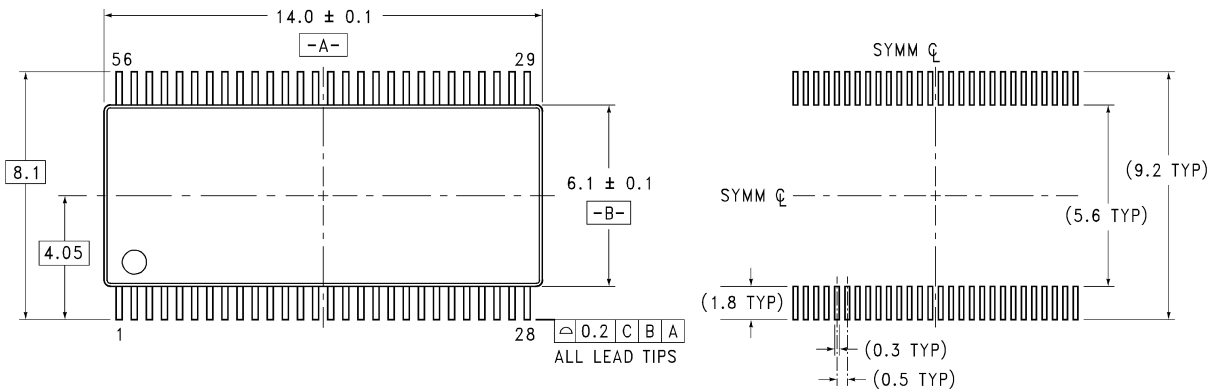
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DS90CR216A

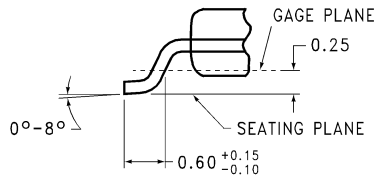
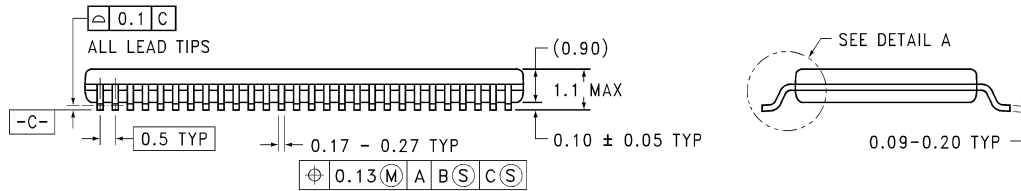
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|----------------------|----|----|-----------------|
| RxOUT17 | 1 | 48 | V _{CC} |
| RxOUT18 | 2 | 47 | RxOUT16 |
| GND | 3 | 46 | RxOUT15 |
| RxOUT19 | 4 | 45 | RxOUT14 |
| RxOUT20 | 5 | 44 | GND |
| N/C | 6 | 43 | RxOUT13 |
| LVDS GND | 7 | 42 | V _{CC} |
| RxIN0- | 8 | 41 | RxOUT12 |
| RxIN0+ | 9 | 40 | RxOUT11 |
| RxIN1- | 10 | 39 | RxOUT10 |
| RxIN1+ | 11 | 38 | GND |
| LVDS V _{CC} | 12 | 37 | RxOUT9 |
| LVDS GND | 13 | 36 | V _{CC} |
| RxIN2- | 14 | 35 | RxOUT8 |
| RxIN2+ | 15 | 34 | RxOUT7 |
| RxCLK IN- | 16 | 33 | RxOUT6 |
| RxCLK IN+ | 17 | 32 | GND |
| LVDS GND | 18 | 31 | RxOUT5 |
| PLL GND | 19 | 30 | RxOUT4 |
| PLL V _{CC} | 20 | 29 | RxOUT3 |
| PLL GND | 21 | 28 | V _{CC} |
| PWR DWN | 22 | 27 | RxOUT2 |
| RxCLK OUT | 23 | 26 | RxOUT1 |
| RxOUT0 | 24 | 25 | GND |

DS100873-13

Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



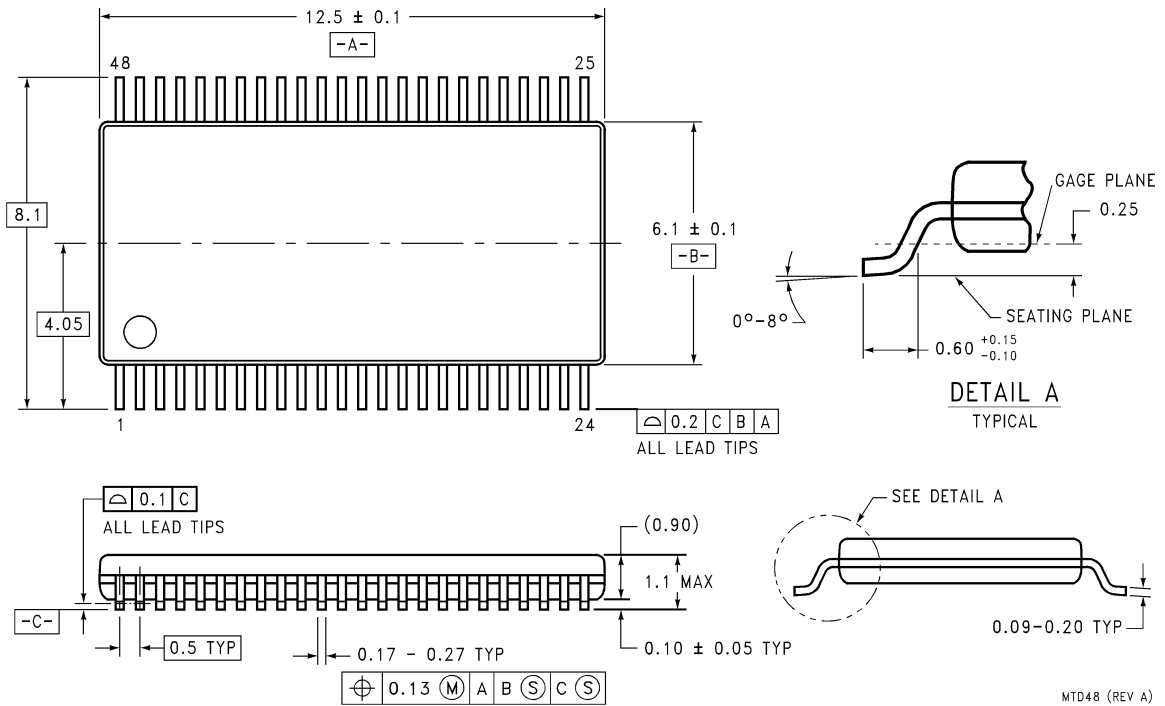
DETAIL A
TYPICAL

MTD56 (REV B)

56-Lead Molded Thin Shrink Small Outline Package, JEDEC
Order Number DS90CR286AMTD
NS Package Number MTD56

DS90CR286A/DS90CR216A +3.3V Rising Edge Data Strobe LVDS Receiver 28-Bit Channel Link — 66 MHz
DS90CR286A/DS90CR216A +3.3V Rising Edge Data Strobe LVDS Receiver 21-Bit Channel Link — 66 MHz

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Molded Thin Shrink Small Outline Package, JEDEC
Order Number DS90CR216AMTD
NS Package Number MTD48

MTD48 (REV A)

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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