National Semiconductor

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DS90CR486
133MHz 48-Bit Channel Link Deserializer (6.384 Gbps)

General Description

The DS90CR486 receiver converts eight Low Voltage Differential Signaling (LVDS) data streams back into 48 bits of LVCMOS/LVTTL data. Using a 133MHz clock, the data throughput is 6.384Gbit/s (798Mbytes/s).

The multiplexing of data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 48-bit wide data and one clock, up to 98 conductors are required. With this Channel Link chipset as few as 19 conductors (8 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides an 80% reduction in interconnect width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cables' smaller form factor.

The DS90CR486 deserializer is improved over prior generations of Channel Link devices and offers higher bandwidth support and longer cable drive with three areas of enhancement. To increase bandwidth, the maximum clock rate is increased to 133 MHz and 8 serialized LVDS outputs are provided. Cable drive is enhanced with a user selectable pre-emphasis (on DS90CR485) feature that provides additional output current during transitions to counteract cable loading effects. Optional DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference). With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable. A cable deskew capability has been added to deskew long cables of pair-to-pair skew. These three enhancements allow long cables to be driven.

The DS90CR486 is intended to be used with the DS90CR485 Channel Link Serializer. It is also backward compatible with serializers DS90CR481 and DS90CR483. The DS90CR486 is footprint compatible with the DS90CR484.

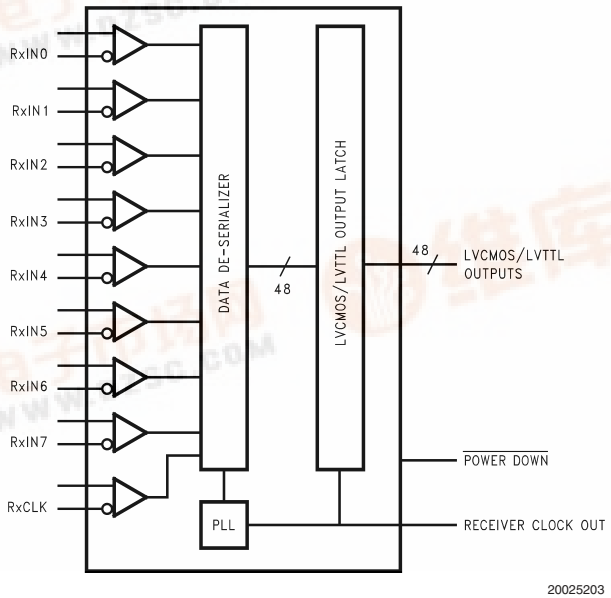
The chipset is an ideal solution to solve EMI and interconnect size problems for high-throughput point-to-point applications.

For more details, please refer to the "Applications Information" section of this datasheet.

Features

- Up to 6.384 Gbps throughput
- 66MHz to 133MHz input clock support
- Reduces cable and connector size and cost
- Cable Deskew function
- DC balance reduces ISI distortion
- For point-to-point backplane or cable applications
- Low power, 890 mW typ at 133MHz
- Flow through pinout for easy PCB design
- +3.3V supply voltage
- 100-pin TQFP package
- Conforms to TIA/EIA-644-A-2001 LVDS Standard

Generalized Block Diagram



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Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +3.6V
LVCMOS/LVTTL Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to +3.6V
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec.)	+260˚C
Maximum Package Power Dissipation Capacity @ 25˚C	
100 TQFP Package:	2.9 W
Package Derating:	23.8 mW/˚C above +25˚C
ESD Rating:	
(HBM, 1.5kΩ, 100pF)	> 2 kV
(EIAJ, 0Ω, 200pF)	> 200 V

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.14	3.3	3.46	V
Operating Free Air Temperature (T_A)	−10	+25	+70	˚C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{p-p}
Clock Rate	66		133	MHz

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage	All LVCMOS/LVTTL inputs except $\overline{PD}$.		2.0		V_{CC}	V
		For $\overline{PD}$ input only.		2.5		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V, or V_{CC} (Note 1)			+1.8	+15	µA
		V_{IN} = GND		−15	0		µA
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA		2.0			V
V_{OL}	Low Level Output Voltage	I_{OL} = +2 mA				0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.8	−1.5	V
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V				±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V				±10	µA
RECEIVER SUPPLY CURRENT							
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, BAL = Low, Worst Case Pattern (*Figures 1, 2*)	f = 66 MHz		190	245	mA
			f = 100 MHz		230	325	mA
			f = 133 MHz		270	340	mA
ICCRZ	Receiver Supply Current Power Down	$\overline{PD}$ = Low Receiver Outputs stay low during Power down mode.			60	110	µA

Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
CLHT	LVCMOS/LVTTL Low-to-High Transition Time, (*Figure 2*), Rx data out, (Note 5)			0.8	1.3	ns
	LVCMOS/LVTTL Low-to-High Transition Time, (*Figure 2*), Rx clock out, (Note 5)			0.7	1.0	ns
CHLT	LVCMOS/LVTTL High-to-Low Transition Time, (*Figure 2*), Rx data out, (Note 5)			0.9	1.3	ns
	LVCMOS/LVTTL High-to-Low Transition Time, (*Figure 2*), Rx clock out, (Note 5)			0.8	1.0	ns
RCOP	RxCLK OUT Period, (*Figure 3*)		7.518	T	15.152	ns
RCOH	RxCLK OUT High Time, (*Figure 3*)	f = 133 MHz	2.7			ns
		f = 100 MHz	3.8			ns
		f = 66 MHz	6.0			ns
RCOL	RxCLK OUT Low Time, (*Figure 3*)	f = 133 MHz	2.7			ns
		f = 100 MHz	3.8			ns
		f = 66 MHz	6.0			ns
RSRC	RxOUT Data valid before RxCLK OUT, (*Figure 3*)	f = 133 MHz	2.0	3.5		ns
		f = 100 MHz	3.0	4.7		ns
		f = 66 MHz	5.0	7.0		ns
RHRC	RxOUT Data valid after RxCLK OUT, (*Figure 3*)	f = 133 MHz	2.5	4.1		ns
		f = 100 MHz	3.5	5.0		ns
		f = 66 MHz	6.0	8.0		ns
RPDL	Receiver Propagation Delay - Latency, (*Figure 4*)		2(TCIP)+5	2(TCIP)+10	2(TCIP)+15	ns
RPLLS	Receiver Phase Lock Loop Set ,(*Figure 5*)				10	ms
RPDD	Receiver Powerdown Delay, (*Figure 6*)				1	µs
RSKMD	Receiver Skew Margin with Deskew, BAL=Low (*Figure 7*), (Note 6)	f = 133 MHz	275			ps
		f = 100 MHz	400			ps
		f = 66 MHz	500			ps
RDR	Receiver Deskew Range	f = 133 MHz	−150		+150	ps
		f = 100 MHz	−200		+200	ps
		f = 66 MHz	−200		+200	ps

Note 1: The I_{IN} parameter for the $\overline{PD}$ pin is not tested at 2.5V.

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 3: Typical values are given for V_{CC} = 3.3V and T_A = +25˚C.

Note 4: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{TH}, V_{TL} and ΔV_{ID}).

Note 5: CLHT and CHLT are measurements of the receiver data outputs low-to-high and high-to-low time over the recommended frequency range. The limits are based on bench characterization and Guaranteed By Design (GBD) using statistical analysis.

Note 6: Receiver Skew Margin with Deskew (RSKMD) is defined as the valid data sampling region at the receiver inputs. The DESKEW function will constrain the receiver's sampling strobes to the middle half of the LVDS bit and removes (adjusts for) fixed interconnect skew. This margin (RSKMD) allows for inter-symbol interference (dependent on type/length of cable), Transmitter Pulse Position (TPPOS) variance, and LVDS clock jitter (TJCC).

RSKMD ≥ ISI + TPPOS(variance) + LVDS Source Clock Jitter (cycle to cycle). See Applications Information section for more details.

AC Timing Diagrams

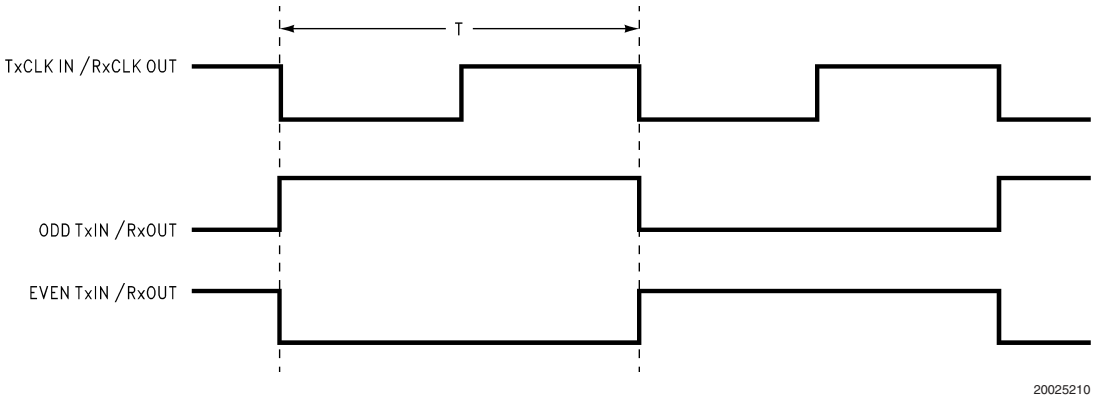


FIGURE 1. "Worst Case" Test Pattern

Note 7: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVCMOS/LVTTL I/O.

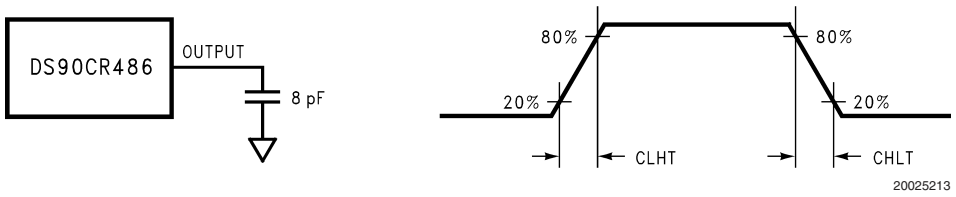


FIGURE 2. DS90CR486 LVCMOS/LVTTL Output Load and Transition Times

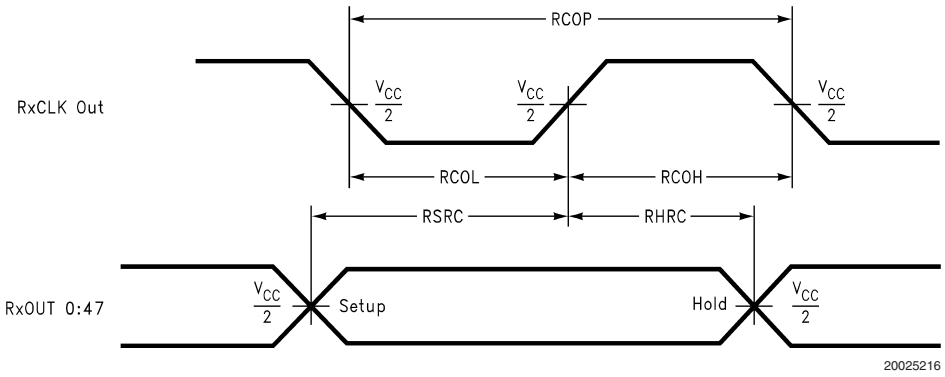


FIGURE 3. DS90CR486 Setup/Hold and High/Low Times

AC Timing Diagrams (Continued)

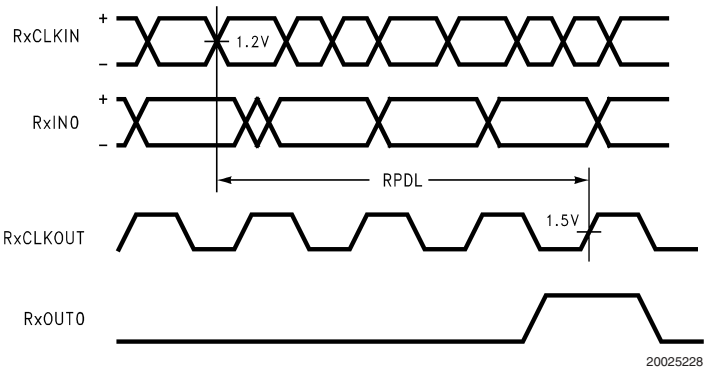


FIGURE 4. DS90CR486 Propagation Delay - Latency

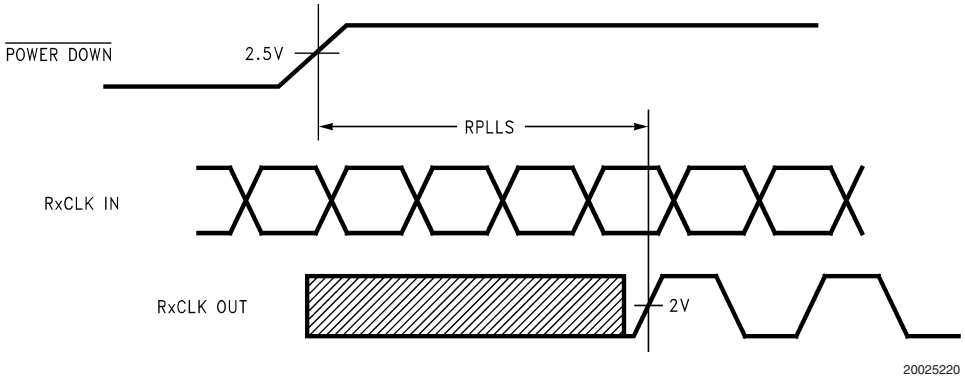


FIGURE 5. DS90CR486 Phase Lock Loop Set Time (V_{CC} > 3.0V)

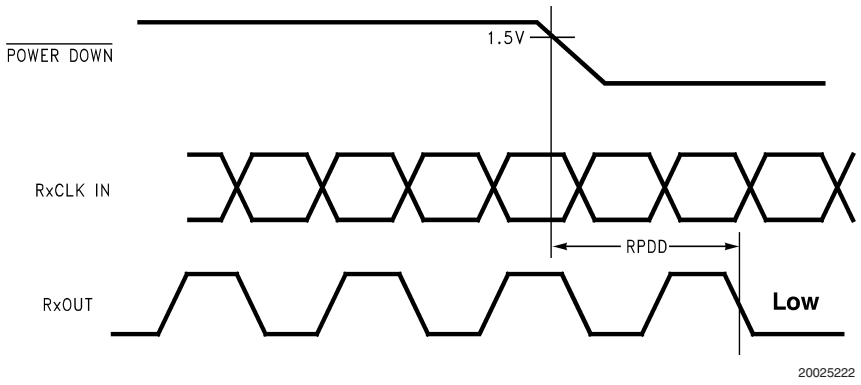
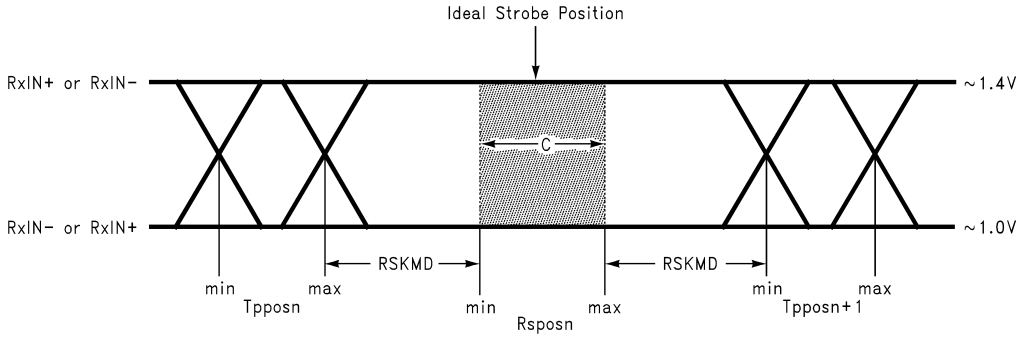


FIGURE 6. DS90CR486 Power Down Delay

AC Timing Diagrams (Continued)



C — Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max

Tppos — Transmitter output pulse position (min and max)

RSKMD = ISI (Inter-symbol interference) + TPPOS(variance) + LVDS Source Clock Jitter (cycle to cycle)

Cable Skew — typically 10 ps–40 ps per foot, media dependent

Note 8: Refer to transmitter datasheet for Cycle-to-cycle LVDS Output jitter specification.

Note 9: ISI is dependent on interconnect length; may be zero. Pre-emphasis in the transimitter is used to reduce the ISI. Refer to transmitter datasheet for more information.

FIGURE 7. Receiver Skew Margin with DESKEW (RSKMD)

LVDS Interface

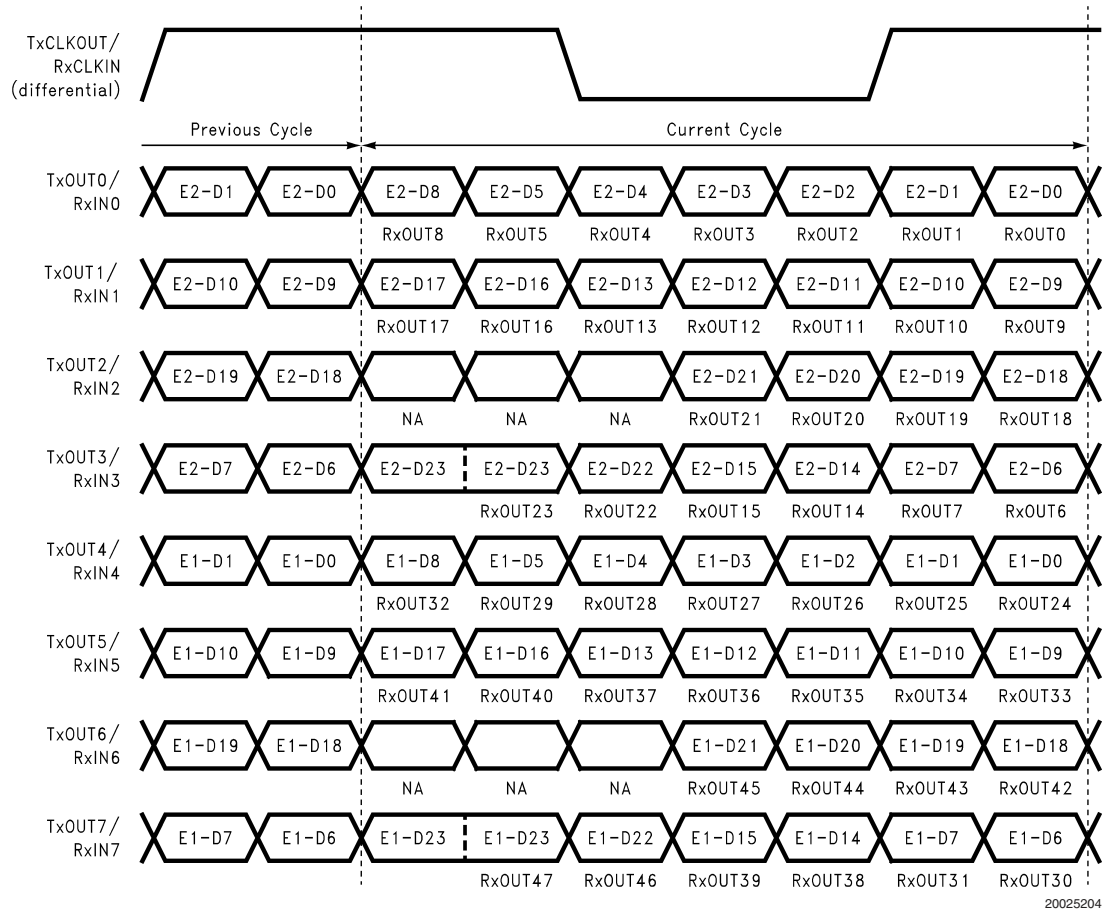


FIGURE 8. 48 LVCMOS/LVTTL Outputs Mapped to 8 LVDS Inputs (DC Balance Mode- Disable, BAL = Low) (E1 - Falling Edge; E2 - Rising Edge)

LVDS Interface (Continued)

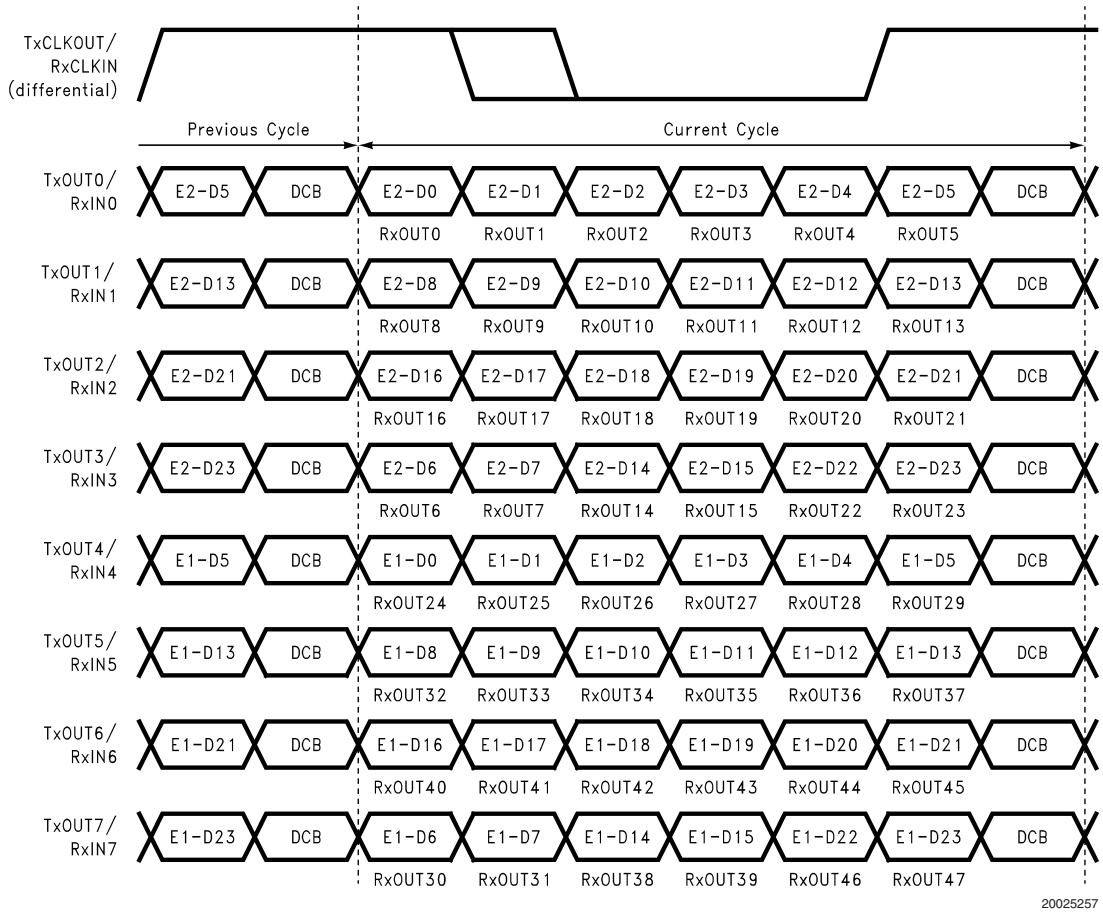


FIGURE 9. 48 LVCMOS/LVTTL Outputs Mapped to 8 LVDS Inputs(DC Balance Mode - Enable, BAL = High) (E1 - Falling Edge; E2 - Rising Edge)

DS90CR486 Outputs Mapped to DS90CR485 Outputs/DS90CR483 Inputs

DS90CR486 Receiver Output	DS90CR485 Transmitter Input *	DS90CR483 Transmitter Input
RxOUT0	E2-D0	TxIN0
RxOUT1	E2-D1	TxIN1
RxOUT2	E2-D2	TxIN2
RxOUT3	E2-D3	TxIN3
RxOUT4	E2-D4	TxIN4
RxOUT5	E2-D5	TxIN5
RxOUT6	E2-D6	TxIN6
RxOUT7	E2-D7	TxIN7
RxOUT8	E2-D8	TxIN8
RxOUT9	E2-D9	TxIN9
RxOUT10	E2-D10	TxIN10
RxOUT11	E2-D11	TxIN11
RxOUT12	E2-D12	TxIN12
RxOUT13	E2-D13	TxIN13
RxOUT14	E2-D14	TxIN14
RxOUT15	E2-D15	TxIN15
RxOUT16	E2-D16	TxIN16
RxOUT17	E2-D17	TxIN17
RxOUT18	E2-D18	TxIN18
RxOUT19	E2-D19	TxIN19
RxOUT20	E2-D20	TxIN20
RxOUT21	E2-D21	TxIN21
RxOUT22	E2-D22	TxIN22
RxOUT23	E2-D23	TxIN23
RxOUT24	E1-D0	TxIN24
RxOUT25	E1-D1	TxIN25
RxOUT26	E1-D2	TxIN26
RxOUT27	E1-D3	TxIN27
RxOUT28	E1-D4	TxIN28
RxOUT29	E1-D5	TxIN29
RxOUT30	E1-D6	TxIN30
RxOUT31	E1-D7	TxIN31
RxOUT32	E1-D8	TxIN32
RxOUT33	E1-D9	TxIN33
RxOUT34	E1-D10	TxIN34
RxOUT35	E1-D11	TxIN35
RxOUT36	E1-D12	TxIN36
RxOUT37	E1-D13	TxIN37
RxOUT38	E1-D14	TxIN38
RxOUT39	E1-D15	TxIN39
RxOUT40	E1-D16	TxIN40
RxOUT41	E1-D17	TxIN41
RxOUT42	E1-D18	TxIN42
RxOUT43	E1-D19	TxIN43
RxOUT44	E1-D20	TxIN44
RxOUT45	E1-D21	TxIN45
RxOUT46	E1-D22	TxIN46
RxOUT47	E1-D23	TxIN47

* E1 = Falling Edge and E2 = Rising Edge of RxCLK P/M Input Clock Edge

DS90CR486 Pin Description—Channel Link Receiver

Pin Name	I/O	No.	Description
RxINP	I	8	Positive LVDS differential data inputs.
RxINM	I	8	Negative LVDS differential data inputs.
RxOUT	O	48	LVCMOS/LVTTL level data outputs. In PowerDown ($\overline{PD}$ = Low) mode, receiver outputs are forced to a **Low state**.
RxCLKP	I	1	Positive LVDS differential clock input.
RxCLKM	I	1	Negative LVDS differential clock input.
RxCLKOUT	O	1	LVCMOS/LVTTL level clock output. The rising edge acts as data strobe.
PLLSEL	I	1	Control input for PLL range select. **This pin must be tied to V_{CC}**. No connect or tied to GND is reserved for future use.
$\overline{PD}$	I	1	Power Down pin. This pin must be tied to input level of 2.5V to Vcc for normal operation. When de-asserted (low input) the receiver outputs are **Low**. Please refer to the Applications Information on the back for more information.
DESKEW	I	1	This pin must be tied to logic High or Vcc for normal operation of Deskew function. De-asserting a pulse of duration greater than one clock will restart the deskew initialization. **Do NOT tie this pin to LOW**. Please refer to the Applications Information on the back for more information.
BAL	I	1	LVCMOS/LVTTL level input. This pin must be tied to logic High or Vcc to enable DC Balance function(*Figure 9*). When tied low or left open, the DC Balance function is disabled(*Figure 8*). Please refer to the Applications Information on the back for more infomation.
CON1	I	1	Control Pin. **This pin must be tied to logic High or Vcc.**
V_{CC}	I	6	Power supply pins for LVCMOS/LVTTL outputs and digital circuitry.
GND	I	8	Ground pins for LVCMOS/LVTTL outputs and digital circuitry.
$PLLV_{CC}$	I	1	Power supply for PLL circuitry.
PLLGND	I	2	Ground pin for PLL circuitry.
$LVDSV_{CC}$	I	2	Power supply pin for LVDS inputs.
LVDSGND	I	3	Ground pins for LVDS inputs.
NC		6	No Connect. Make NO Connection to these pins - leave open.

Note 10: These receivers have input fail-safe bias circuitry to guarantee a stable receiver output for floating or terminated receiver inputs. Under these conditions receiver inputs will be in a HIGH state. If a clock signal is present, outputs will all be HIGH; if the cable inter-connects are disconnected which results in floating/terminated inputs, the outputs will remain in the last valid state. A floating/terminated clock input will result in a LOW clock output.

Applications Information

DC BALANCE

In addition to data information an additional bit is transmitted on every LVDS data signal line during each cycle as shown in *Figure 9*. This bit is the DC balance bit (DCB). The purpose of the DC Balance bit is to minimize the short- and long-term DC bias on the signal lines. This is achieved by selectively sending the data either unmodified or inverted.

The value of the DC balance bit is calculated from the running word disparity and the data disparity of the current word to be sent. The data disparity of the current word shall be calculated by subtracting the number of bits of value 0 from the number of bits value 1 in the current word. Initially, the running word disparity may be any value between +7 and –6. The running word disparity shall be calculated as a continuous sum of all the modified data disparity values, where the unmodified data disparity value is the calculated data disparity minus 1 if the data is sent unmodified and 1 plus the inverse of the calculated data disparity if the data is sent inverted. The value of the running word disparity shall saturate at +7 and –6.

The value of the DC balance bit (DCB) shall be 0 when the data is sent unmodified and 1 when the data is sent inverted. To determine whether to send data unmodified or inverted, the running word disparity and the current data disparity are used. If the running word disparity is positive and the current data disparity is positive, the data shall be sent inverted. If the running word disparity is positive and the current data disparity is zero or negative, the data shall be sent unmodified. If the running word disparity is negative and the current data disparity is positive, the data shall be sent unmodified. If the running word disparity is negative and the current data disparity is zero or negative, the data shall be sent inverted. If the running word disparity is zero, the data shall be sent inverted.

DC Balance mode is set when the BAL pin on the transmitter and receiver are tied HIGH - see pin descriptions.

DESKEW

The "DESKEW" function on this receiver will deskew or compensate fixed interconnect skew between data signals, with respect to the rising edge of the LVDS clock, on each of the independent differential pairs (pair-to-pair skew). The deskew initialization or calibration is done automatically when the device is powered up. The control pin CON1 must set High and the Deskew pin must set to High on the DS90CR486. However, the Deskew calibration can also be performed after the device is powered up. De-asserting with a pulse of duration greater than one clock cycle to the Deskew pin to restart the calibration of deskew. The calibration takes 4096 clock cycles to complete after the TX and RX PLLs lock (20ms). No RxIN data is sampled during this period. The data outputs during this period will be Low. For normal operation, deskew pin must set to High. Setting the deskew pin to Low or No Connect will continuously re-calibrate the sampling strobes. Data outputs are Low during this period.

In order for the deskew function to work properly, it must be intialized. The DS90CR486 deskew can be initialized with any data pattern with a transition over a period of three clock cycles. Therefore, there are mulitiple ways to initialize the deskew function depending on the setup configuration (Please refer to *Figure 10*). For example, to initialize the operation of deskew using DS90CR485 and DS90CR486 in DC balance mode, the DS_OPT pin at the input of the transmitter DS90CR485 can be set High OR Low when powered up. The period of this input to the DS_OPT pin must be at least 20ms (TX and RX PLLs lock time) plus 4096 clock cycles in order for the receiver to complete the deskew operation. For other configuration setup with DS90CR483 and DS90CR484, please refer to the flow chart on *Figure 10*.

The DS_OPT pin at the input of the transmitter (DS90CR485) can be used to initiate the deskew calibration pattern. Depends on the configuration, it can be set High or applied Low when power up in order for the receiver to complete the deskew operation. For this reason, the LVDS clock signal with DS_OPT applied high (active data sampling) shall be 1111000 or 1110000 pattern and the LVDS data lines (TxOUT 0-7) shall be High for one clock cycle and Low for the next clock cycle. During the deskew operation with DS_OPT applied low, the LVDS clock signal shall be 1111100 or 1100000 pattern. The transmitter will also output a series of 1111000 or 1110000 onto the LVDS data lines (TxOUT 0-7) during deskew so that the receiver can automatically calibrated the data sampling strobes at the receiver inputs. Each data channel is deskewed independently and is tuned over a specific range. Please refer to corresponding receiver datasheet for a list of deskew ranges.

Note that the deskew initialization must be performed at least once after the PLL has locked to the input clock frequency, and it must be done at the time when the receiver is powered up and PLL has locked. If power is lost, or if the cable has been swithcd or disconnected, the initialization procedure must be repeated or else the receiver may not sample the incoming LVDS data correctly.

POWER DOWN

The receiver provides a power down feature. When de-asserted current draw through the supply pins is minimized and the PLLs are shut down. The receiver outputs are forced to an active LOW state when in the power down mode. (See Pin Description Tables). This is not a LVCMOS/LVTTL input pin and has a high input threshold. For normal operation, this pin must be tied to an input level of 2.5V to Vcc.

CONFIGURATIONS

The chipset is designed to be connected typically to a single receiver load. This is known as a point-to-point configuration. It is also possible to drive multiple receiver loads if certain restrictions are made(i.e. low data rate). Only the final receiver at the end of the interconnect should provide termination across the pair. In this case, the driver still sees the intended DC load of 100 Ohms. Receivers connected to the cable between the transmitter and the final receiver must not load down the signal. To meet this system requirement, stub lengths from the line to the receiver inputs must be kept very short.

CABLE TERMINATION

A termination resistor is required for proper operation to be obtained. The termination resistor should be equal to the differential impedance of the media being driven. This should be in the range of 90 to 132 Ohms. 100 Ohms is a typical value common used with standard 100 Ohm twisted pair cables. This resistor is required for control of reflections and also to complete the current loop. It should be placed as close to the receiver inputs to minimize the stub length from the resistor to the receiver input pins.

Applications Information (Continued)

HOW TO CONFIGURE FOR BACKPLANE APPLICATIONS

In a backplane application with differential line impedance of 100Ω the differential line pair-to-pair skew can controlled by trace layout. The transmitter-DS90CR485 "DS_OPT" pin may be set high. In a backplane application with short PCB distance traces, pre-emphasis from the transmitter is typically not required. The "PRE" pin should be left open (do not tie to ground). A resistor pad provision for a pull up resistor to Vcc can be implemented in case pre-emphasis is needed to counteract heavy capacitive loading effects.

SUPPLY BYPASS RECOMMENDATIONS

Bypass capacitors must be used on the power supply pins. Different pins supply different portions of the circuit, therefore capacitors should be nearby all power supply pins except as noted in the pin description table. Use high frequency ceramic (surface mount recommended) 0.1µF capacitors close to each supply pin. If space allows, a 0.01µF capacitor should be used in parallel, with the smallest value closest to the device pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple (large) via should be used to connect the decoupling capacitors to the power plane. A 4.7 to 10µF bulk cap is recommended near the PLLVCC pins and also the LVDSVCC pins. Connections between the caps and the pin should use wide traces.

RECEIVER OUTPUT DRIVE STRENGTH

The DS90CR486 output specifies a 8pF load, V_{OH} and V_{OL} are tested at ± 2mA, which is intended for only 1 or maybe 2 loads. The DS90CR486 reciever's output driving capability has improved over prior generation of Channel Link devices. Additional buffering at the reciver output is not necessary. If high fan-out is required or long transmission line driving capability, buffering the receiver output is recommended. Receiver outputs do not support / provide a TRI-STATE function.

LVDS INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - — S = space between the pair
  - — 2S = space between pairs
  - — 3S = space to TTL signal
- Minimize the number of VIA
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Minimize skew between pairs
- Terminate as close to the RXinputs as possible

For more information:

Channel Link Applications Notes currently available:

- AN-1041 Introduction to Channel Link
- AN-1108 PCB and Interconnect Guidelines
- AN-905 Differential Impedance
- National's LVDS Owner's Manual

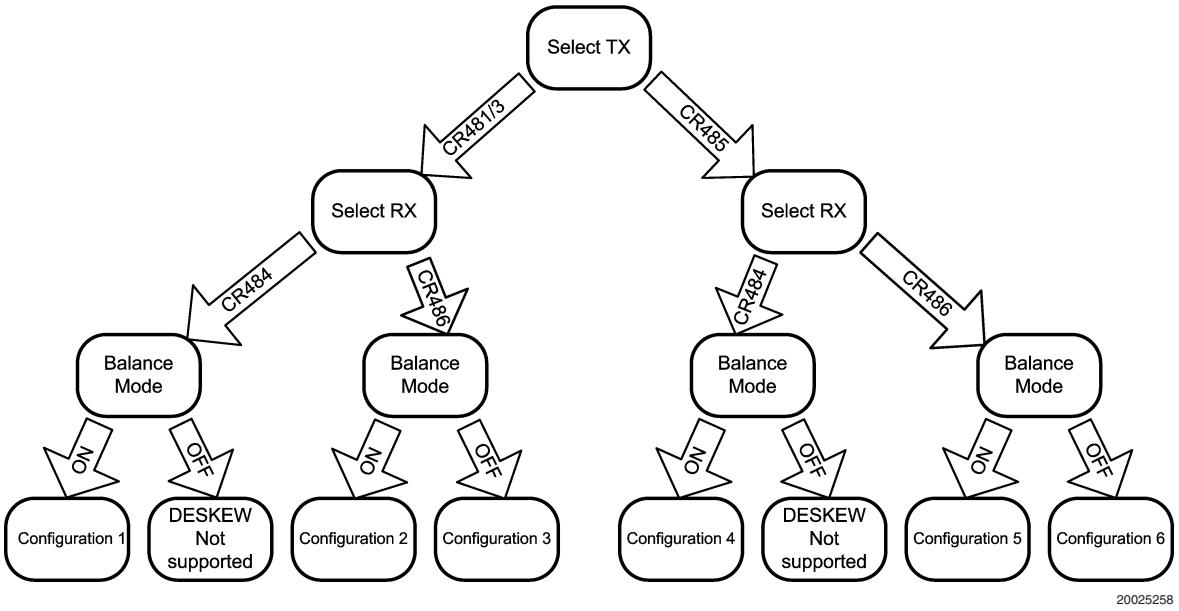


FIGURE 10. Deskew Configuration Setup Chart

CONFIGURATION 1

DS90CR481/483 and DS90CR484 with DC Balance ON (BAL=High, 33MHz to 80MHz) – The DS_OPT pin at the input of the transmitter DS90CR481/483 must be applied low for a minimum of four clock cycles in order for the receiver to complete the deskew operation. The input to the DS_OPT pin can be applied at any time after the PLL has locked to the input clock frequency. In this particular setup, the "DESKEW" pin on the receiver DS90CR484 must set High.

CONFIGURATION 2

DS90CR481/483 and DS90CR486 with DC Balance ON (BAL=High, CON1=High, 66MHz to 112MHz) – The DS_OPT pin at the input of the transmitter DS90CR481/483 can be set to High OR Low when power up. The period of this input to the DS_OPT pin must be at least 20ms (TX and RX PLLs lock time) plus 4096 clock cycles in order for the receiver to complete the deskew operation. The "DESKEW" and CON1 pins on the receiver DS90CR486 must be tied to High for this setup.

CONFIGURATION 3

DS90CR481/483 and DS90CR486 with DC Balance OFF (BAL=Low, CON1=High, 66MHz to 112MHz) – The input to the DS_OPT pin of the transmitter DS90CR481/483 in this configuration is completely ignored by the transimitters. In order to initialize the deskew operation on the receiver DS90CR486, data and clcok must be applied to the transimitter when power up. The "DESKEW" and CON1 pins on the receiver DS90CR486 must be tied to High for this setup.

CONFIGURATION 4

DS90CR485 and DS90CR484 with DC Balance ON (BAL=High, 66MHz to 80MHz) – The DS_OPT pin at the input of the transmitter DS90CR485 must be applied low for a minimum of four clock cycles in order for the receiver to complete the deskew operation. The input to the DS_OPT pin can be applied at any time after the PLL has locked to the input clock frequency. In this setup, the "DESKEW" pin on the receiver DS90CR484 must set High.

CONFIGURATION 5

DS90CR485 and DS90CR486 with DC Balance ON (BAL=Hiigh, CON1=High, 66MHz to 133MHz) – The DS_OPT pin at the input of the transmitter DS90CR485 can be set to High OR Low when power up. The period of this input to the DS_OPT pin must be at least 20ms (TX and RX PLLs lock time) plus 4096 clock cycles in order for the receiver to complete the deskew operation. The "DESKEW" and CON1 pins on the receiver DS90CR486 must set High.

CONFIGURATION 6

DS90CR485 and DS90CR486 with DC Balance OFF (BAL=Low, CON1=High, 66MHz to 133MHz) –The input to the DS_OPT pin of the transmitter DS90CR485 in this configuration is completely ignored. In order to initialize the deskew operation on the receiver DS90CR486, data and clcok must be applied to the transimitter when power up. The "DESKEW" and CON1 pins on the receiver DS90CR486 must set High.

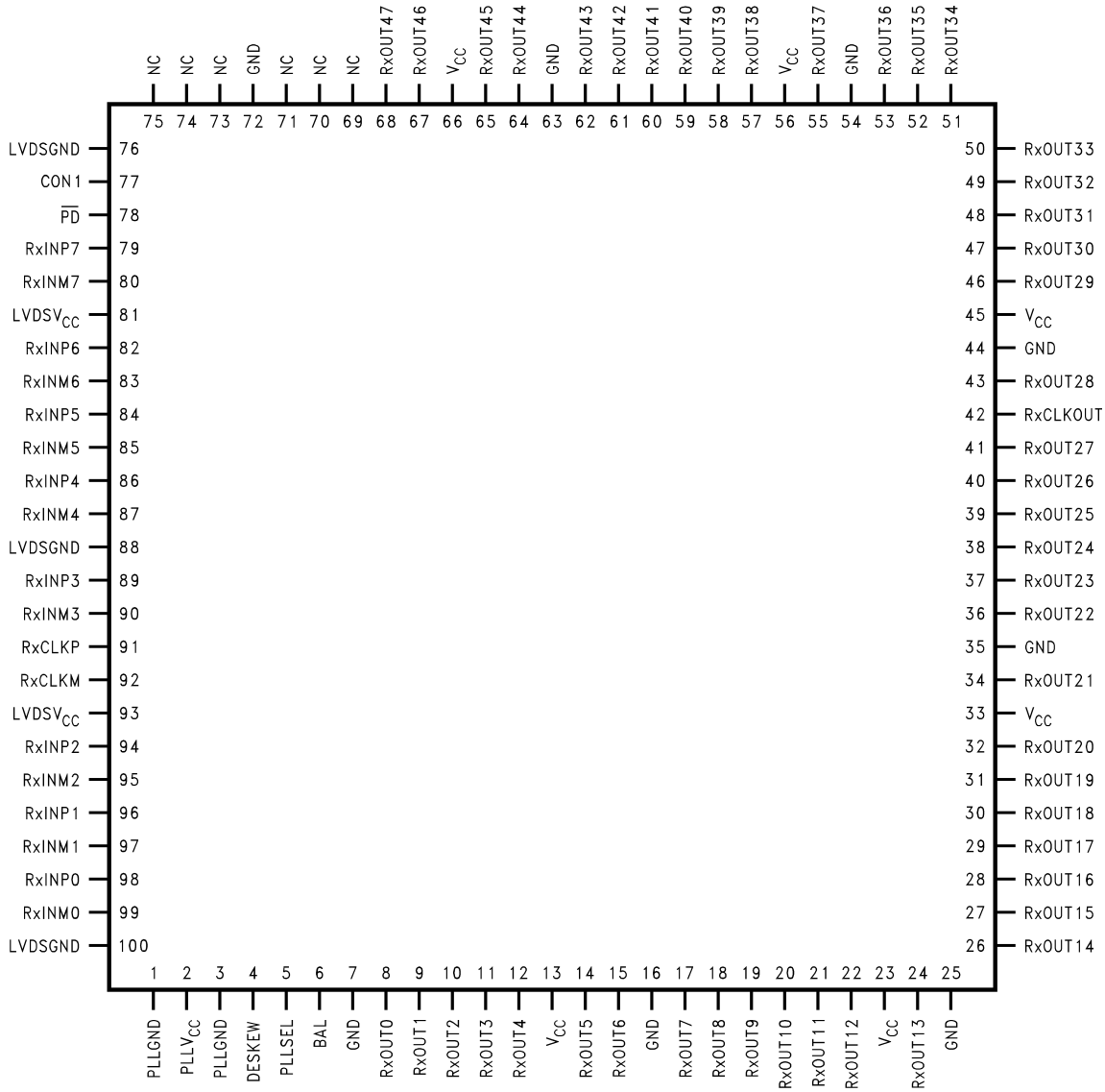
DESKEW NOT SUPPORTED

Deskew function is NOT supported in these configuration setups. The deskew feature is only supported with DC Balance ON (BAL=High) for DS90CR484. Note that the deskew function in the DS90CR486 works in both DC Balance and NON-DC Balance modes.

Note 11: For more details on Deskew operation, please refer to the "Application Information" section.

Pin Diagram

Receiver - DS90CR486
(Top View)



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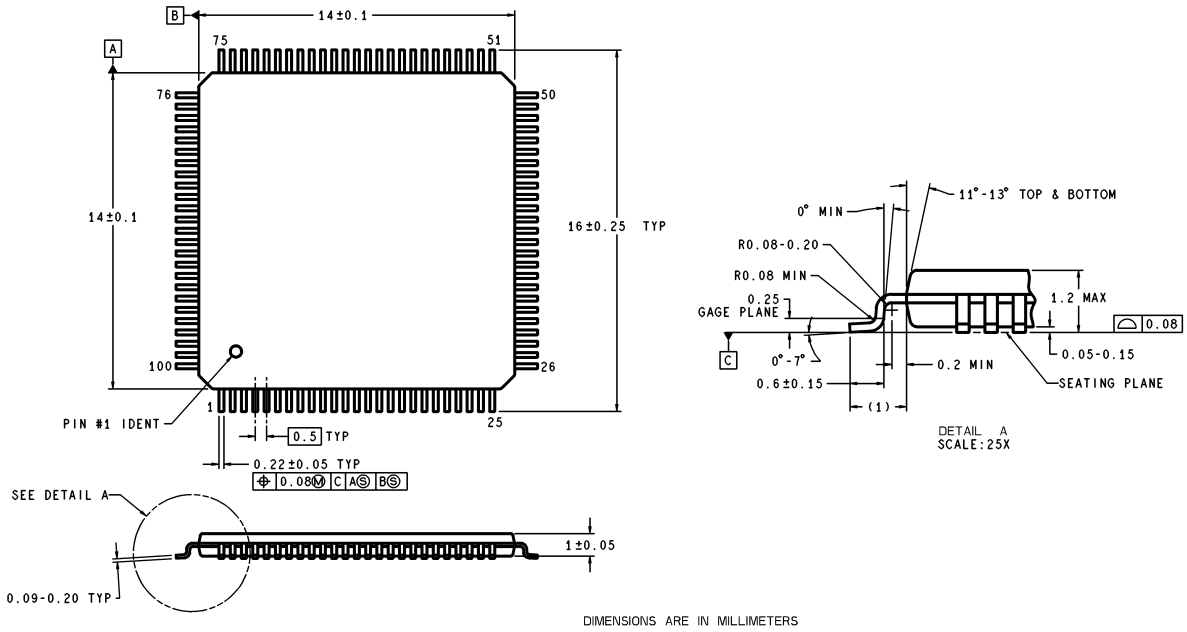
Physical Dimensions inches (millimeters) unless otherwise noted



VJD100A (Rev B)

Dimensions show in millimeters
Order Number DS90CR486VS
NS Package Number VS100A

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