National Semiconductor

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DS92001
3.3V B/LVDS-BLVDS Buffer

General Description

The DS92001 B/LVDS-BLVDS Buffer takes a BLVDS input signal and provides an BLVDS output signal. In many large systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the 'stub length' or the distance between the transmission line and the unterminated receivers on individual cards. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns often make it difficult to make the stubs as short as the designer would like.

The DS92001 has edge transitions optimized for multidrop backplanes where the switching frequency is in the 200 MHz range or less. The output edge rate is critical in some systems where long stubs may be present, and utilizing a slow transition allows for longer stub lengths.

The DS92001, available in the LLP (Leadless Leadframe Package) package, will allow the receiver inputs to be placed very close to the main transmission line, thus improving system performance.

A wide input dynamic range allows the DS92001 to receive differential signals from LVPECL as well as LVDS sources. This will allow the device to also fill the role of an LVPECL-BLVDS translator.

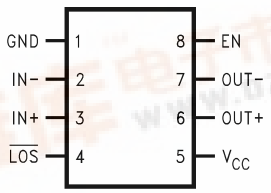
The $\overline{LOS}$ pin detects a non-driven B/LVDS bus state at the input and provides an active LOW output. The $\overline{LOS}$ pin can be tied to the device's output enable pin (EN) to generate a TRI-STATE output state when the input is un-driven. The $\overline{LOS}$ pin can also be used locally to inform the system of the bus state.

Features

- Single +3.3 V Supply
- B/LVDS receiver inputs accept LVPECL signals
- TRI-STATE outputs
- Loss of Signal ($\overline{LOS}$) pin detects a non-driven bus
- Receiver input threshold < ±100 mV
- Fast propagation delay of 1.4 ns (typ)
- Low jitter 400 Mbps fully differential data path
- Compatible with BLVDS 10-bit SerDes (40MHz)
- Compatible with ANSI/TIA/EIA-644-A LVDS standard
- Available in SOIC and space saving LLP package
- Industrial Temperature Range

Connection and Block Diagrams

SOIC - Top View



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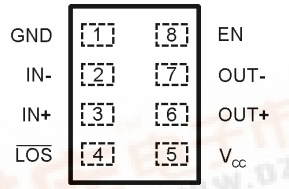
LLP - Top View



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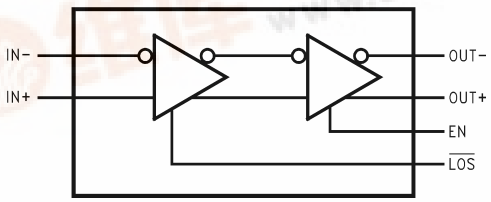
DAP (GND) Pad Not Shown



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Functional Operation

BLVDS Inputs	BLVDS Outputs	
[IN+] – [IN–]	OUT+	OUT–
VID ≥ 0.1V	H	L
VID ≤ –0.1V	L	H
Full Fail-safe OPEN/SHORTor Terminated	H	L

Ordering Information

Order Number	NS Pkg. No.	Pkg. Type
DS92001TM	M08A	SOIC
DS92001TLD	LDA08A	LLP

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
LVCMOS/LVTTL Input Voltage (EN)	−0.3V to (V_{CC} + 0.3V)
LVCMOS/LVTTL Output Voltage ($\overline{LOS}$)	−0.3V to (V_{CC} + 0.3V)
B/LVDS Receiver Input Voltage (IN+, IN−)	−0.3V to +4V
BLVDS Driver Output Voltage (OUT+, OUT−)	−0.3V to +4V
BLVDS Output Short Circuit Current	Continuous
Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature Range	
Soldering (4 sec.)	+260˚C
Maximum Package Power Dissipation at 25˚C	
M Package	726 mW
Derate M Package	5.8 mW/˚C above +25˚C
LDA Package	2.44 W
Derate LDA Package	19.49 mW/˚C above +25˚C
ESD Ratings	
(HBM, 1.5kΩ, 100pF)	≥2.5kV
(EIAJ, 0Ω, 200pF)	≥250V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID}) with V_{CM}=1.2V	0.1		2.4	|V|
Operating Free Air Temperature	−40	+25	+85	˚C
B/LVDS Input Rise/Fall 20% to 80%		2	20	ns

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS (EN)						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC} or 2.0V		+7	+20	µA
I_{IL}	Low Level Input Current	V_{IN} = GND or 0.8V	−10	±1	+10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.6	−1.5	V
LVCMOS/LVTTL DC SPECIFICATIONS ($\overline{LOS}$)						
V_{OH}	Output High Voltage	I_{OH} = −4mA, V_{ID} ≥ |200mV|, V_{CM} = 1.2V	V_{CC} −0.4V	3.1	V_{CC}	V
V_{OL}	Output Low Voltage (Note 5)	I_{OL} = 4mA, V_{ID} = 0V, V_{CM} = 1.2V		0.15	0.4	V
I_{OSHLOS}	Output Short Circuit Current (output high)(Note 4)	V_{OUT} = 0V, 200mV ≤ V_{ID} ≤ 2V, V_{CM} = 1.5V		−35	−60	mA
BLVDS OUTPUT DC SPECIFICATIONS (OUT)						
$\|V_{OD}\|$	Differential Output Voltage (Note 2)	R_L = 27Ω	250	350	500	mV
		R_L = 50Ω	350	450	600	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States	RL = 27Ω or 50Ω *Figure 1, Figure 2*			20	mV
V_{OS}	Offset Voltage	R_L = 27Ω or R_L = 50Ω	1.1	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States	*Figure 1*		2	20	mV
I_{OZ}	Output TRI-STATE Current	EN = 0V, V_{OUT} = V_{CC} or GND	−20	±5	+20	µA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
BLVDS OUTPUT DC SPECIFICATIONS (OUT)							
I_{OFF}	Power-Off Leakage Current	V_{CC} = 0V or Open Circuit, V_{OUT} = 3.6V		–20	±5	+20	µA
I_{OS1}	Output Short Circuit Current (Note 4)	EN = V_{CC}, V_{CM} = 1.2V,V_{ID} = 200mV, V_{OUT+} = 0V, or V_{ID} = –200mV, V_{CM} = 1.2V, V_{OUT-} = 0V			–30	–60	mA
		V_{ID} = –200mV, V_{CM} = 1.2V, V_{OUT+} = V_{CC} , or V_{ID} = 200mV, V_{CM} =1.2V, V_{OUT-} = V_{CC}			53	80	mA
I_{OSD}	Differential Output Short Circuit Current (Note 4)	EN = V_{CC}, V_{ID} = |200mV|, V_{CM}. = 1.2V, V_{OD} = 0V (connect true and complement outputs through a current meter)			|30|	|42|	mA
B/LVDS RECEIVER DC SPECIFICATIONS (IN)							
V_{TH}	Differential Input High Threshold (Note 5)	V_{CM} = +0.05V, +1.2V or +3.25V			–30	–5	mV
V_{TL}	Differential Input Low Threshold (Note 5)			–70	–30		mV
V_{CMR}	Common Mode Voltage Range (Note 5)			|V_{ID}|/2		V_{CC} –|V_{ID}|/2	V
I_{IN}	Input Current	V_{IN} = V_{CC}	V_{CC} = 3.6V or 0V		|1.5|	|20|	µA
		V_{IN} = 0V			|1.5|	|20|	µA
ΔI_{IN}	Change in Magnitude of I_{IN}	V_{IN} = V_{CC}			1	6	µA
		V_{IN} = 0V			1	6	µA
V_{FSOD}	Fail-safe BLVDS Outputs (OUT+ is a more positive voltage than OUT–) (Note 5)	Inputs open, shorted, or terminated	R_L = 27Ω	250	350	500	mV
			R_L = 50Ω	350	450	600	mV
SUPPLY CURRENT							
I_{CCD}	Total Dynamic Supply Current (includes load current)	EN = V_{CC}, R_L = 27Ω or 50Ω, C_L = 15 pF, Freq. = 200MHz 50% duty cycle, V_{ID} = 200mV, V_{CM} = 1.2V			50	65	mA
I_{CCZ}	TRI-STATE Supply Current	EN = 0V,Freq. = 200MHz 50% duty cycle, V_{ID} = 200mV, V_{CM}= 1.2V			36	46	mA

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS (OUT)						
t_{PHLD}	Differential Propagation Delay High to Low (Note 10)	V_{ID} = 200mV, V_{CM} = 1.2V, R_L = 27Ω or 50Ω, C_L = 15pF *Figure 3* and *Figure 4*	1.0	1.4	2.0	ns
t_{PLHD}	Differential Propagation Delay Low to High (Note 10)		1.0	1.4	2.0	ns
t_{SKD1}	Pulse Skew |t_{PLHD} – t_{PHLD}| (measure of duty cycle) (Notes 5, 6)		0	20	200	ps
t_{SKD3}	Part-to-Part Skew (Note 5) (Note 7)		0	200	300	ps
t_{SKD4}	Part-to-Part Skew (Note 5) (Note 8)		0		1	ns

AC Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS (OUT)						
t_{LHT}	Rise Time (Notes 5, 10) 20% to 80% points	R_L = 50Ω or 27Ω, C_L = 15pF *Figure 3* and *Figure 5*	0.350	0.6	1.0	ns
t_{HLT}	Fall Time (Notes 5, 10) 80% to 20% points		0.350	0.6	1.0	ns
t_{PHZ}	Disable Time (Active High to Z)	R_L = 50Ω, C_L = 15pF *Figure 6* and *Figure 7*		3	25	ns
t_{PLZ}	Disable Time (Active Low to Z)			3	25	ns
t_{PZH}	Enable Time (Z to Active High)			100	120	ns
t_{PZL}	Enable Time (Z to Active Low)			100	120	ns
t_{DJ}	LVDS Data Jitter, Deterministic (Peak-to-Peak) (Note 9)	V_{ID} = 300mV; PRBS = 2^{23} – 1 data; V_{CM} = 1.2V at 400Mbps (NRZ)			78	ps
t_{RJ}	LVDS Clock Jitter, Random (Note 9)	V_{ID} = 300mV; V_{CM} = 1.2V at 200MHz clock			36	ps
f_{MAX}	Maximum guaranteed frequency (Note 11)	V_{ID} = 200mV, V_{CM} = 1.2V	200	300		MHz
LVCMOS/LVTTL AC SPECIFICATIONS ($\overline{LOS}$)						
t_{PHLLOS}	LVTTL Propagation Delay High to Low (Note 5)	CL = 10pF, IN– = 1V, 1V ≤ IN+ ≤ 1.3V, Freq. = 10MHz, 50% Duty Cycle *Figures 8, 9*	10	15	20	ns
t_{PLHLOS}	LVTTL Propagation Delay Low to High (Note 5)		2	5	10	ns
t_{LHLOS}	Rise Time 20% to 80% (Note 5)		1	2	3	ns
t_{HLLOS}	Fall Time 80% to 20% (Note 5)		1	1.3	3	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{ID}, V_{OD}, V_{TH}, V_{TL}, and ΔV_{OD}. V_{OD} has a value and direction. Positive direction means OUT+ is a more positive voltage than OUT–.

Note 3: All typical are given for V_{CC} = +3.3V and T_A = +25˚C, unless otherwise stated.

Note 4: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Note 5: The parameters are guaranteed by design. The limits are based on statistical analysis of the device performance over the PVT (process, voltage and temperature) range.

Note 6: t_{SKD1}, $|t_{PLHD} - t_{PHLD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel (a measure of duty cycle).

Note 7: t_{SKD3}, Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5˚C of each other within the operating temperature range. This parameter guaranteed by design and characterization.

Note 8: t_{SKD4}, Part to Part Skew, is the differential channel-to- channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max – Min| differential propagation delay.

Note 9: The parameters are guaranteed by design. The limits are based on statistical analysis of the device performance over the PVT range with the following test equipment setup: Agilent 86130A used as stimulus, 5 feet of RG142B cable with DUT test board and Agilent 86100A (digital scope mainframe) with Agilent 86122A (20GHz scope module). Data input jitter pk to pk = 22 picoseconds; Clock input jitter = 24 picoseconds; t_{DJ} measured 100 picoseconds, t_{RJ} measured 60 picoseconds.

Note 10: Propagation delay, rise and fall times are guaranteed by design and characterization to 200MHz. Generator for these tests: 50MHz ≤ f ≤ 200MHz, Zo = 50Ω, tr, tf ≤ 0.5ns. Generator used was HP8130A (300MHz capability).

Note 11: f_{MAX} test: Generator (HP8133A or equivalent), Input duty cycle = 50%. Output criteria: VOD ≥ 200mV, Duty Cycle better than 45/55%. This specification is guaranteed by design and characterization. A minimum is specified, which means that the device will operate to specified conditions from DC to the minimum guaranteed AC frequency. The typical value is always greater than the minimum guarantee.

DC Test Circuits

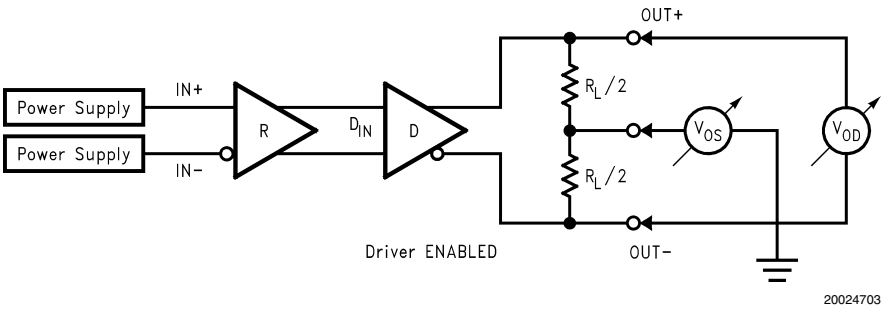

FIGURE 1. Differential Driver DC Test Circuit

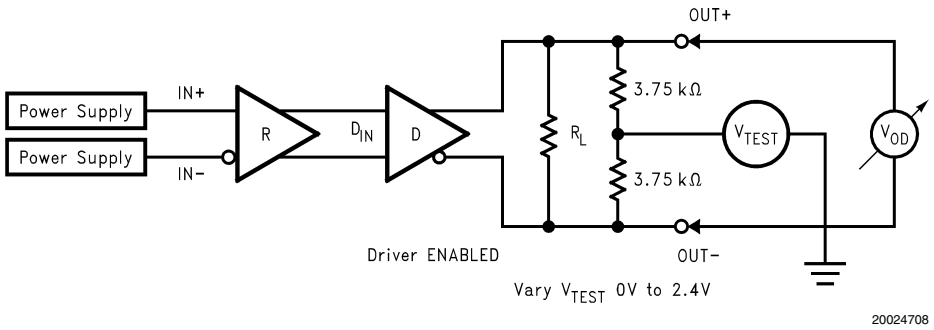

FIGURE 2. Differential Driver Full Load DC Test Circuit

AC Test Circuits and Timing Diagrams

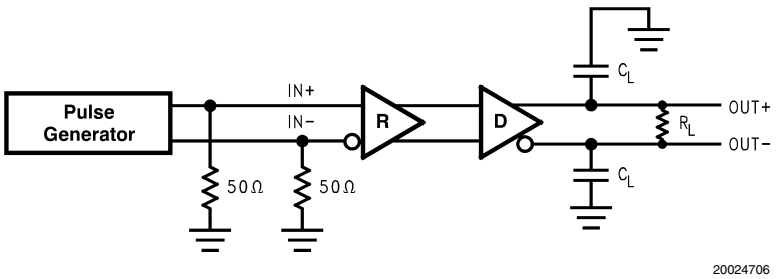

FIGURE 3. BLVDS Output Load

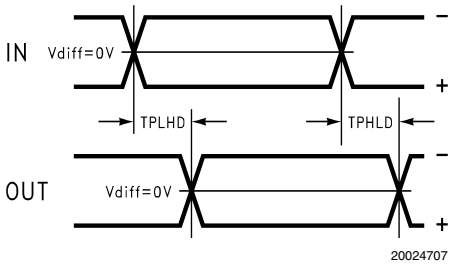

FIGURE 4. Propagation Delay Low-to-High and High-to-Low

AC Test Circuits and Timing Diagrams (Continued)

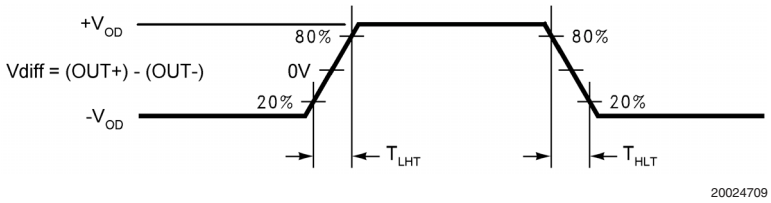

FIGURE 5. BLVDS Output Transition Time

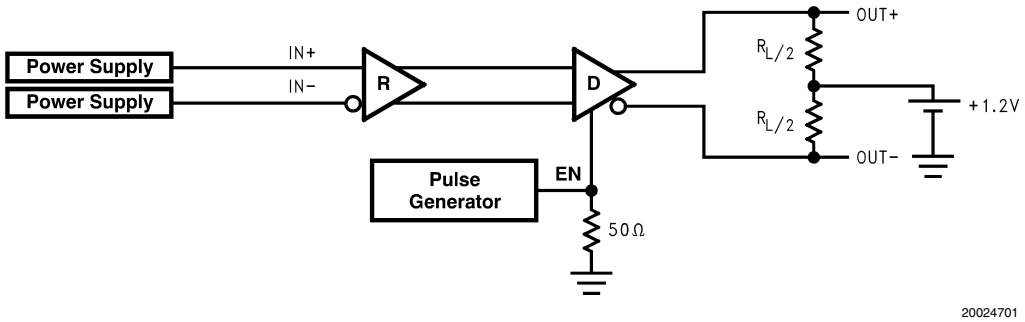

FIGURE 6. TRI-STATE Delay Test Circuit

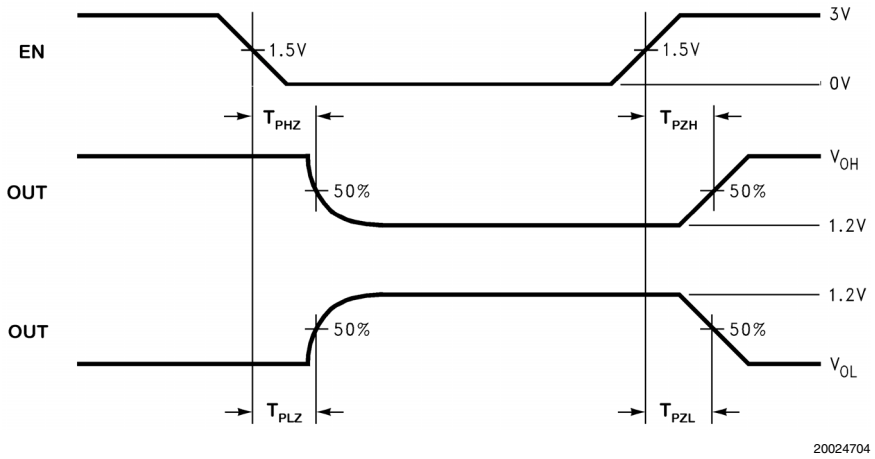

FIGURE 7. Output active to TRI-STATE and TRI-STATE to active output time

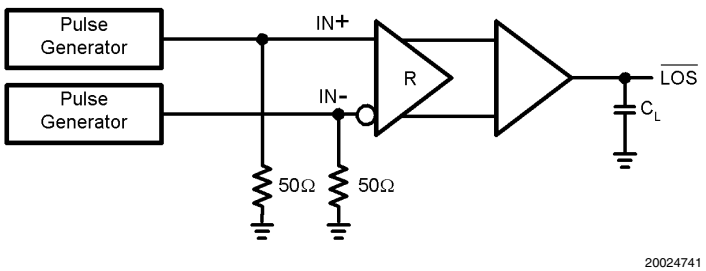

FIGURE 8. $\overline{\text{LOS}}$ Output Load for Propagation Delay, and Rise/Fall Times

AC Test Circuits and Timing Diagrams (Continued)

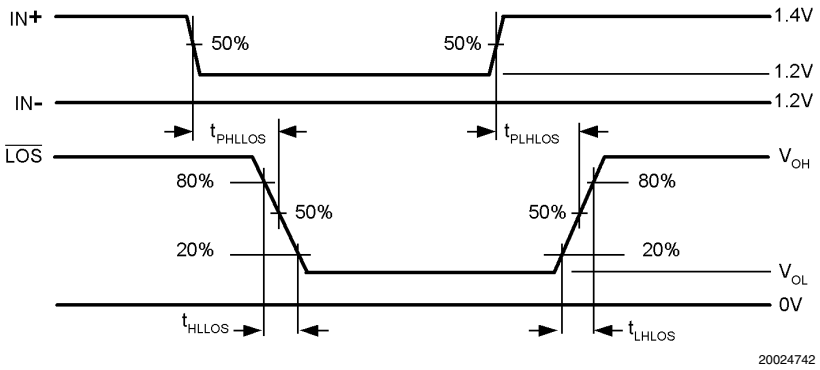

FIGURE 9. LOS Output Waveforms for Propagation Delay, and Rise/Fall Times

DS92001 Pin Description (SOIC and LLP)

Pin Name	Pin #	Input/Output	Description
GND	1	P	Ground
IN –	2	I	Inverting receiver B/LVDS input pin
IN+	3	I	Non-inverting receiver B/LVDS input pin
$\overline{LOS}$	4	O	Loss of Signal output pin. $\overline{LOS}$ is asserted low while signal is invalid. See Applications Information section.
V_{CC}	5	P	Power Supply, 3.3V ± 0.3V.
OUT+	6	O	Non-inverting driver BLVDS output pin
OUT -	7	O	Inverting driver BLVDS output pin
EN	8	I	Enable pin. When EN is LOW, the driver is disabled and the BLVDS outputs are in TRI-STATE. When EN is HIGH, the driver is enabled. LVCMOS/LVTTL levels.
GND	DAP	P	LLP Package Ground

Typical Applications

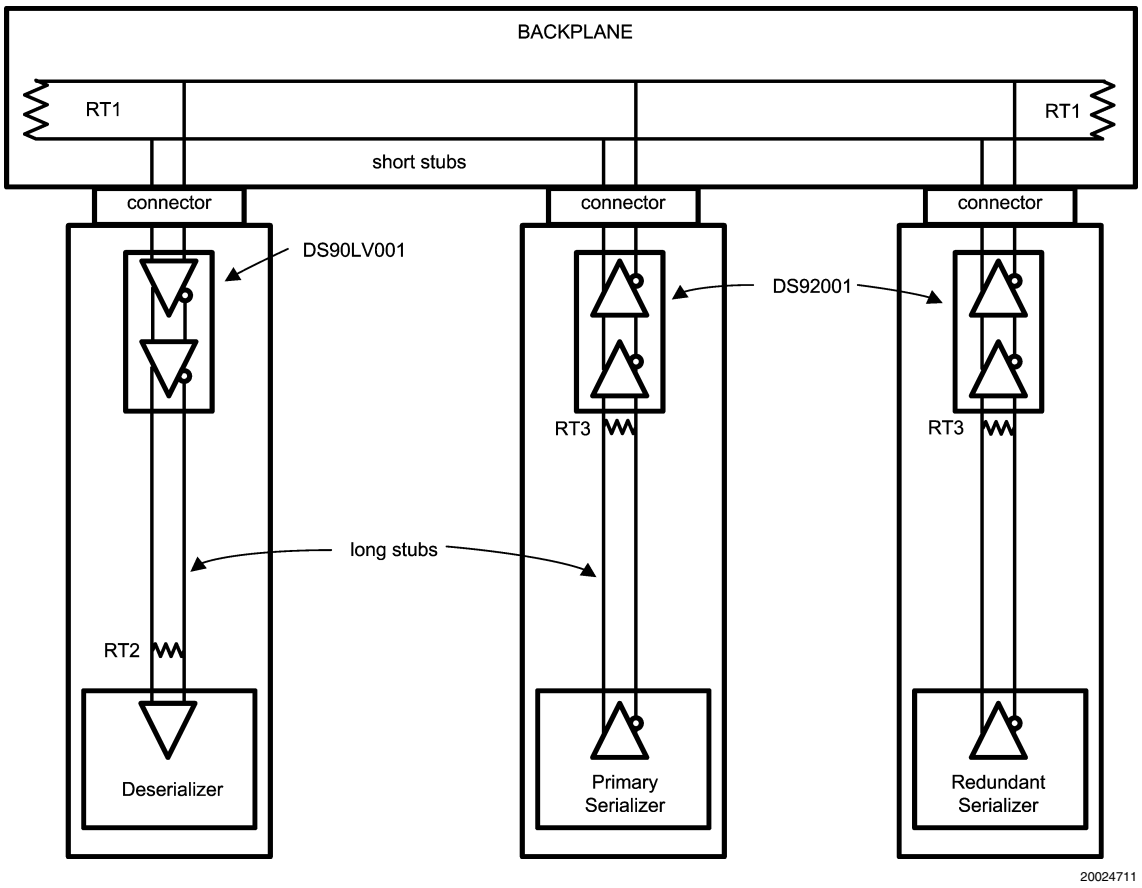

FIGURE 10. Backplane Stub-Hider Application

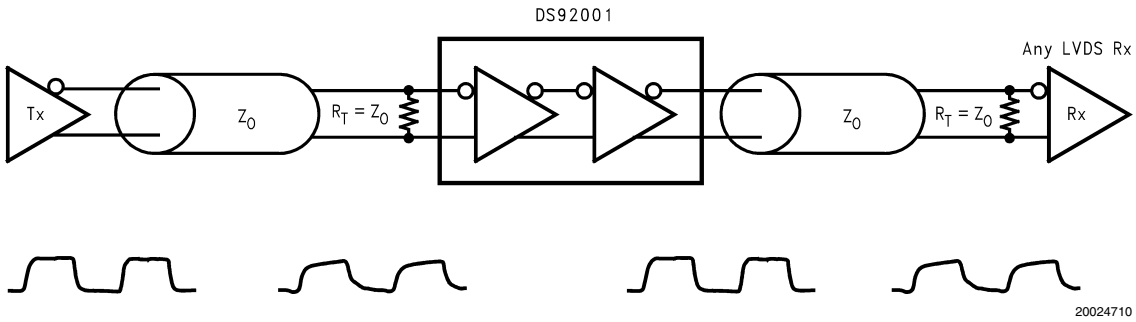

FIGURE 11. Cable Repeater Application

Application Information

The DS92001 can be used as a 'stub-hider.' In many systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the 'stub length' or the distance between the transmission line and the unterminated receivers on the individual cards. See *Figure 10*. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns and PCB designs often make it difficult to make the stubs as short as the designer would like. The DS92001, available in the LLP (Leadless Leadframe Package) package, can improve system performance by allowing the receiver to be placed very close to the main transmission line either on the backplane itself or very close to the connector on the card. Longer traces to the LVDS receiver may be placed after the DS92001. This very small LLP package is a 75% space savings over the SOIC package.

The DS92001 may also be used as a repeater as shown in *Figure 11*. The signal is recovered and redriven at full strength down the following segment. The DS92001 may also be used as a level translator, as it accepts LVDS, BLVDS, and LVPECL inputs.

$\overline{\text{LOS}}$ Detection:

The $\overline{\text{LOS}}$ pin presents a logic High level during normal operation ($|100|mV \leq V_{ID} \leq |2|V$, of the device. When normal transmission stops the $\overline{\text{LOS}}$ pin is asserted low. This occurs when the signal's source is removed, or turned-off (TRI-STATE). When the input signal voltage (V_{ID}) is less than |10| millivolts the $\overline{\text{LOS}}$ pin is asserted Low. For normal operation, Rise and Fall times presented to the B/LVDS inputs must be faster than 20 nanoseconds (20% to 80%) to avoid a loss of signal detection. Typical input transitions are in the 1-3 nanosecond range. In the case of a decaying signal (such as valid signal to TRI-STATE), the slope should be monotonic to avoid glitches in the $\overline{\text{LOS}}$ detection.

$\overline{\text{LOS}}$ Detection - Output Low

Power Decoupling Recommendations:

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1µF and 0.01µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple vias should be used to connect the decoupling capacitors to the power planes. A 10µF (35V) or greater solid tantalum capacitor should be connected at the power entry point on the printed circuit board between the supply and ground.

PC Board considerations:

Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals.

Isolate TTL signals from LVDS signals, otherwise the TTL signals may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).

Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

For PC board considerations for the LLP package, please refer to application note AN-1187 "Leadless Leadframe Package." It is important to note that to optimize signal integrity (minimize jitter and noise coupling), the LLP thermal land pad, which is a metal (normally copper) rectangular region located under the package as seen in *Figure 12*, should be attached to ground and match the dimensions of the exposed pad on the PCB (1:1 ratio).

Top View

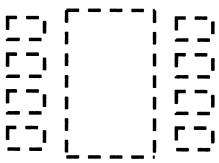

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FIGURE 12. LLP Thermal Land Pad and Pin Pads - Top View

Differential Traces:

Use controlled impedance traces which match the differential impedance of your transmission medium (ie. cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs should be < 10mm long). This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Application Information (Continued)

Avoid 90˚ turns (these cause impedance discontinuities). Use arcs or 45˚ bevels.

Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

Termination:

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor should be between 90Ω and 130Ω for point-to-point links. Multidrop (driver in the middle) or multipoint configurations are typically terminated at both ends. The termination value may be lower than 100Ω due to loading effects and in the 50Ω to 100Ω range. Remember that the current mode outputs need the termination resistor to generate the differential voltage.

Surface mount 1% - 2% resistors are the best. PCB stubs, component lead, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be < 10mm (12mm MAX).

Probing LVDS Transmission Lines:

Always use high impedance (> 100kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing will give deceiving results.

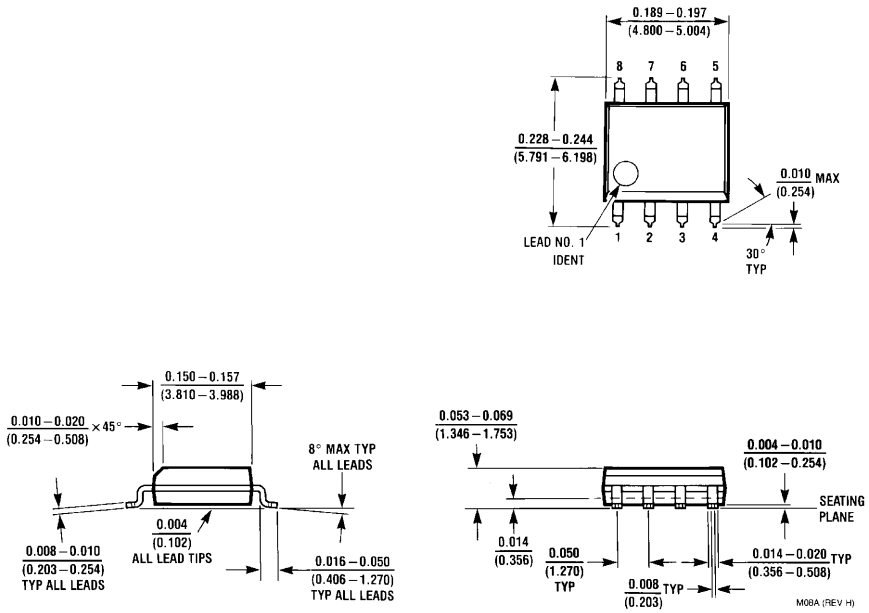
FailSafe Feature:

The BLVDS receiver is a high gain, high speed device that amplifies a small differential signal (30mV) to BLVDS ouput drive levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

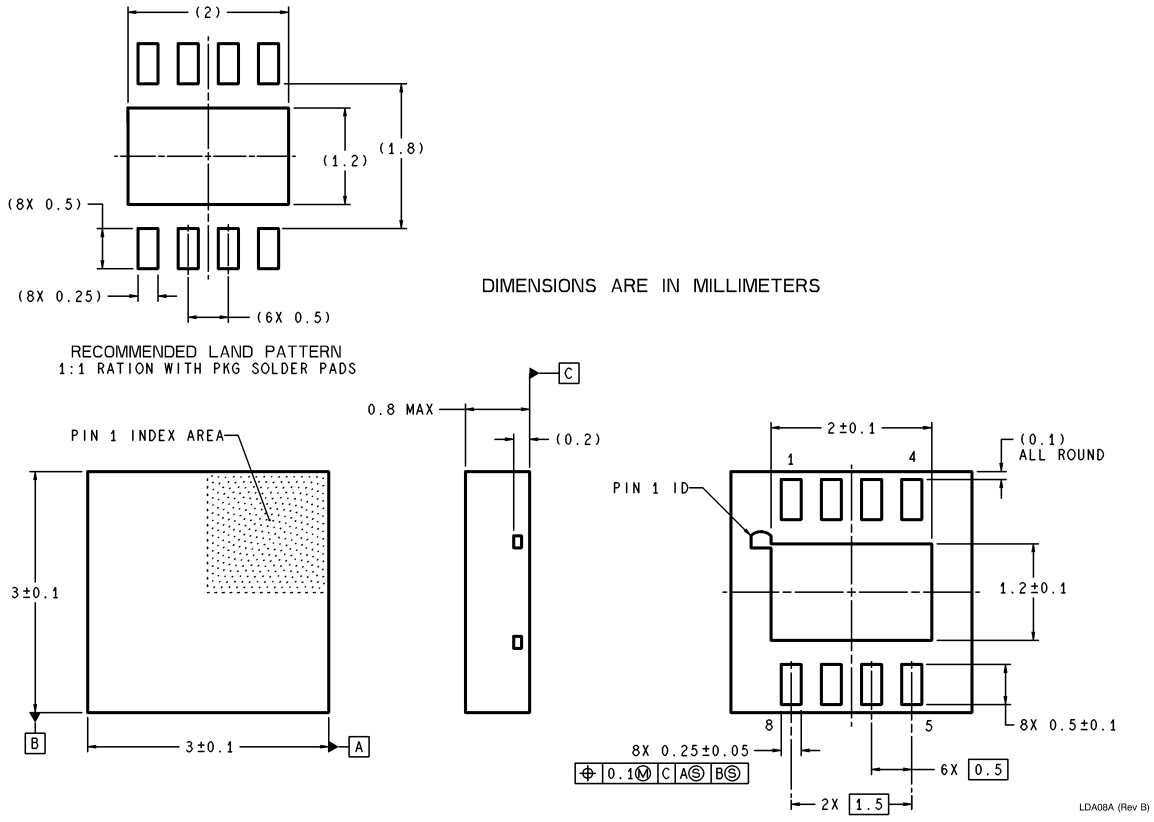
The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a high level output voltage) for floating, terminated or shorted receiver inputs.

1. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a power-off condition, the BLVDS outputs will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.
2. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the BLVDS outputs will remain in a HIGH state. Shorted input fail-safe voltage range is 0V to 2.4V.
3. **External Biasing.** External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry. Please refer to application note AN-1194 "Failsafe Biasing of LVDS Interfaces" for more information.

Physical Dimensions inches (millimeters)
unless otherwise noted



Order Number DS92001TM
See NS Package Number M08A



Order Number DS92001TLD
See NS Package Number LDA08A

Notes

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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