Burr-Brown Products
from Texas Instruments

SLES005A – JUNE 2001 – REVISED FEBRUARY 2002

ENHANCED MULTIFORMAT, DELTA-SIGMA, AUDIO DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Supports DSD and PCM Format**
- **Accepts 16-, 18-, 20- and 24-Bit Audio Data for PCM Format**
- **Accepts Direct Stream Digital (1 bit)**
- **Analog Performance (V_{CC} = 5 V):**
  - **Dynamic Range: 106 dB Typ**
  - **SNR: 106 dB Typ**
  - **THD+N: 0.0015% Typ**
  - **Full–Scale Output: 3.1 V(pp) Typ**
- **Includes 8x Oversampling Digital Filter for PCM Format:**
  - **Stopband Attenuation: –60 dB**
  - **Passband Ripple: ±0.02 dB**
- **Including Digital DSD Filter For DSD Format:**
  - **Passband Choices: 50 kHz, 70 kHz or 60 kHz at –3 dB**
- **Sampling Frequency:**
  - **PCM Mode: 10 kHz to 200 kHz**
  - **DSD Mode: 64 × 44.1 kHz**
- **System Clock:**
  - **$128f_S$ $192f_S$, $256f_S$, $384f_S$ $512f_S$, $768f_S$**
- **Data Formats:**
  - **Standard, I^2S, and Left-Justified for PCM Direct Stream Digital**
- **User-Programmable Mode Controls:**
  - **Digital Attenuation**
  - **Digital De-Emphasis**
  - **Digital Filter Roll-Off: Sharp or Slow Soft Mute**
  - **Zero Detect Mute**
  - **Zero Flags for Each Output**
- **Dual Supply Operation: 5-V Analog, 3.3-V Digital**
- **5-V Tolerant Digital Inputs**
- **Small 20-Lead QSOP Package**

APPLICATIONS

- **Universal A/V Players**
- **SACD Players**
- **Car Audio Systems**
- **Other Applications Requiring 24-Bit Audio**

DESCRIPTION

The DSD1702 is a CMOS, monolithic, stereo digital-to-analog converter that supports both PCM audio data format and direct stream digital (DSD) audio data format.

The device includes an 8x digital interpolation filter for PCM signals. A digital DSD filter provides three different selectable frequency response options, followed by Burr-Brown's enhanced multilevel delta-sigma modulator employing 4th-order noise shaping and 8-level amplitude quantization. This design achieves excellent dynamic performance and improved tolerance to clock jitter.

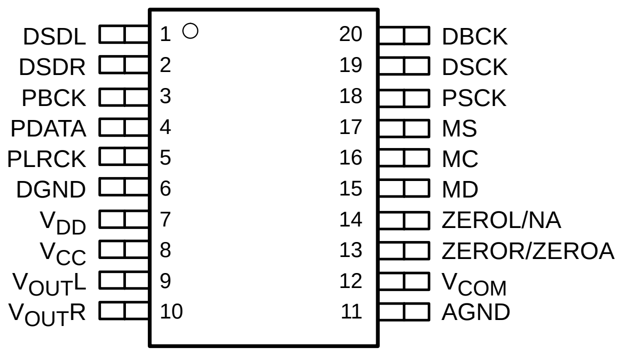
DSD1702 sampling rates of up to 192 kHz for PCM mode and 44.1 kHz × 64 for DSD mode are supported. A full set of user-programmable functions is accessible through a 3-wire serial control port, supporting register write functions.

The DSD1702 is available in a 20-lead QSOP package.

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precaustions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DSD1702
(TOP VIEW)

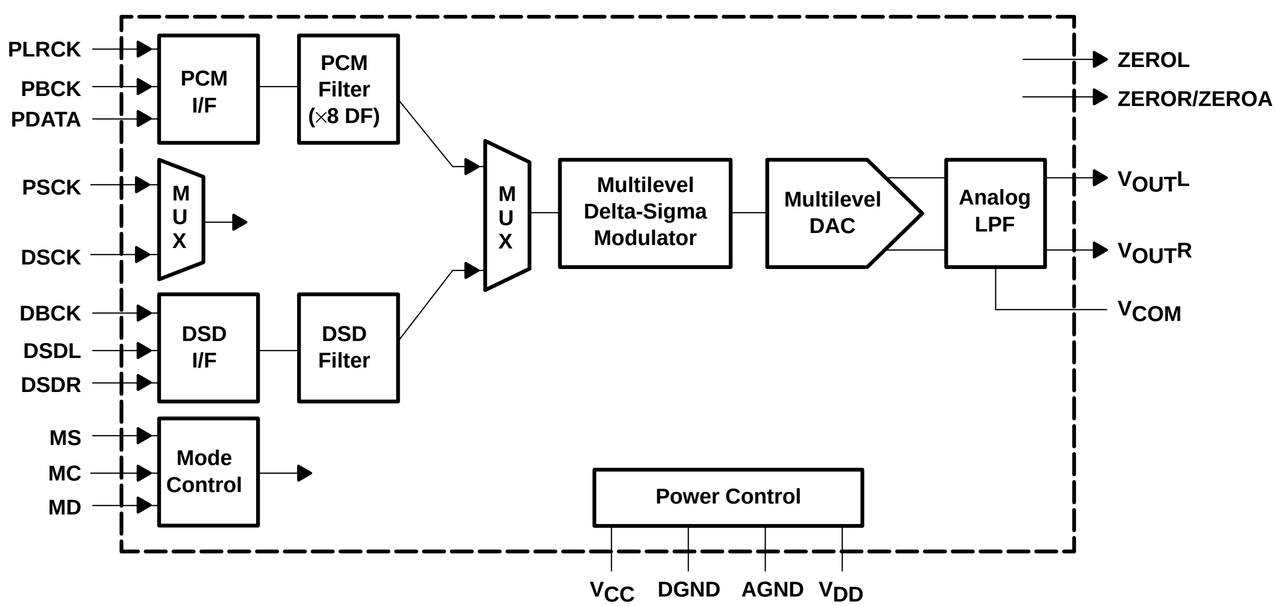


PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER†	TRANSPORT MEDIA
DSD1702E	QSOP–20	4073301	–25°C to 85°C	DSD1702E	DSD1702E	Rails
					DSD1702E/2K	Tape and Reel

† Models with a slash (/) are available only in tape and reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of DSD1702E/2K will get a single 2000-piece tape and reel.

block diagram



Terminal Functions

TERMINAL NAME	PIN	I/O	DESCRIPTIONS
DSDL	1	I	Audio data digital input (DSD L–channel) (see Note 1)
DSDR	2	I	Audio data digital input (DSD R–channel) (see Note 1)
PBCK	3	I	Audio data bit clock input. (PCM) (see Note 1)
PDATA	4	I	Audio data digital input. (PCM) (see Note 1)
PLRCK	5	I	Audio data latch enable input. (PCM) (see Note 1)
DGND	6	–	Digital ground
V_{DD}	7	–	Digital power supply, 3.3 V
V_{CC}	8	–	Analog power supply, 5 V
$V_{OUT}L$	9	O	Analog output for L–channel
$V_{OUT}R$	10	O	Analog output for R–channel
AGND	11	–	Analog ground
V_{COM}	12	–	Common voltage decoupling
ZEROR/ZEROA	13	O	Zero flag output for R–channel/zero flag output for L/R–channel. (see Note 3)
ZEROL/NA	14	O	Zero flag output for L–channel/no assignment (see Note 3)
MD	15	I	Mode control data Input. (see Note 2)
MC	16	I	Mode control clock input. (see Note 2)
MS	17	I	Chip Select for Mode control. (see Note 2)
PSCK	18	I	System clock input. (PCM) (see Note 1)
DSCK	19	I	System clock input. (DSD) (see Note 1)
DBCK	20	I	Audio data bit clock input. (DSD) (see Note 1)

NOTES: 1. Schmitt trigger input, 5-V tolerant.
2. Schmitt trigger input with internal pulldown, 5-V tolerant.
3. Usage depending on AZRO register setting.

absolute maximum ratings†

Supply voltage, V_{DD} . . . . 6.5 V
Supply voltage, V_{CC} . . . . 4 V
Ground voltage differences, AGND, DGND . . . . ±0.1 V
Digital input voltage . . . . –0.3 V to (6.5 V + 0.3 V)
Input current (Any pins except supplies) . . . . ±10 mA
Ambient temperature under bias . . . . –40°C to 125°C
Storage temperature . . . . –55°C to 125°C
Junction temperature . . . . 150°C
Lead temperature (soldering) . . . . 260°C, 5 sec
Package temperature (IR reflow, peak) . . . . 235°C, 10 sec

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics, $T_A = 25°C$, $V_{DD} = 3.3$ V, $V_{CC} = 5$ V (unless otherwise noted)

In PCM mode, $f_S = 44.1$ kHz, system clock = 256 f_S, 24-bit data
In DSD mode, $f_S = 2.8224$ MHz (= 64 × 44.1 kHz), system clock = 256 × 44.1 kHz, 1-bit data

PARAMETERS		TEST CONDITIONS	DSD1702E MIN	DSD1702E TYP	DSD1702E MAX	UNITS
Resolution				24		Bits
DATA FORMAT						kHz
PCM MODE						
	Audio data interface format		Standard, I^2S, left justified			
	Audio data bit length		16-, 18-, 20-, 24-bits selectable			
	Audio data format		MSB First, 2s Complement			
f_S	Sampling frequency		10		200	
	System clock frequency		$128f_S$, $192f_S$, $256f_S$, $384f_S$, $512f_S$, $768f_S$			
DSD MODE						
	Audio data interface format		Direct stream digital (DSD)			
	Audio data bit length		1-Bit			
f_S	Sampling frequency	$f_S = 44.1$ kHz		$64f_S$		Hz
	System clock frequency	$f_S = 44.1$ kHz	$256f_S$, $384f_S$, $512f_S$, $768f_S$			kHz
Digital Input/OUTPUT						
Logic Family			TTL Compatible			
V_{IH}	Input logic level		2.0			VDC
V_{IL}	Input logic level				0.8	VDC
I_{IH}(4)	Input logic current	$V_{IN} = V_{DD}$			10	µA
I_{IL}(4)	Input logic current	$V_{IN} = 0$ V			–10	µA
I_{IH}(5)	Input logic current	$V_{IN} = V_{DD}$		65	100	µA
I_{IL}(5)	Input logic current	$V_{IN} = 0$ V			–10	µA
V_{OH} (6)	Output logic level	$I_{OH} = –2$ mA	2.4			VDC
V_{OL} (6)	Output logic level	$I_{OL} = 2$ mA			1.0	VDC

NOTES: 4. Pins 1, 2, 3, 4, 5, 18, 19, 20: DSDL, DSDR, PBCK, PDATA, PLRCK, PSCK, DSCK, DBCK.
5. Pins 15, 16, 17: MD, MC, MS.
6. Pins 13, 14: ZEROR, ZEROL.

electrical characteristics, T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V (unless otherwise noted) (continued)

In PCM mode, f_S = 44.1 kHz, system clock = 256f_S, 24-bit data
In DSD mode, f_S = 2.8224 MHz (= 64 × 44.1 kHz), system clock = 256 × 44.1 kHz, 1-bit data

PARAMETERS	TEST CONDITIONS	DSD1702E MIN	DSD1702E TYP	DSD1702E MAX	UNITS
Dynamic Performance[7]					
PCM MODE					
THD+N at V_{OUT} = 0 dB	f_S = 44.1 kHz		0.0015%	0.002%	
	f_S = 96 kHz		0.0020%		
	f_S = 192 kHz		0.0025%		
Dynamic range	EIAJ, A-Weighted, f_S = 44.1 kHz	103	106		dB
	A-Weighted, f_S = 96 kHz		106		dB
	f_S = 192 kHz		105		dB
Signal-to-noise ratio[8]	EIAJ, A-Weighted, f_S = 44.1 kHz	103	106		dB
	A-Weighted, f_S = 96 kHz		106		dB
	f_S = 192 kHz		105		dB
Channel separation	f_S = 44.1 kHz	100	103		dB
	f_S = 96 kHz		103		dB
	f_S = 192 kHz		102		dB
Level linearity error	V_{OUT} = –90 dB		±0.5		dB
DSD MODE (at f_S = 64 × 44.1 kHz)					
THD+N	V_{OUT} = 0 dB, EIAJ		0.0015%		
Dynamic range	EIAJ, A-Weighted		106		dB
Signal–to–noise ratio	EIAJ, A-Weighted		106		dB
Channel separation			103		dB
Level linearity error	V_{OUT} = –90 dB		±0.5		dB
DC Accuracy					
Gain error			±1.0	±6.0	%/FSR
Gain mismatch, channel-to-channel			±1.0	±3.0	%/FSR
Bipolar zero error	V_{OUT} = 0.5 V_{CC} at BPZ		±30	±60	mV
Analog Output					
Output voltage	Full scale (–0dB)		62%/V_{CC}		$V_{(PP)}$
Center voltage			50%/V_{CC}		VDC
Load impedance	AC load	5			kΩ
Digital Filter Performance					
8x Interpolation Filter					
Sharp roll off Filter					
Passband	±0.02 dB			0.454f_S	
Passband	–3 dB			0.487f_S	
Stopband		0.546f_S			
Passband ripple				± 0.02	dB
Stopband Attenuation	Stopband = 0.546f_S	– 60			dB

NOTES: 7. Analog performance specs are measured by audio precision system 2 under averaging mode.
8. SNR is tested at infinite zero detection OFF.

electrical characteristics, T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V (unless otherwise noted) (continued)

In PCM mode, f_S = 44.1 kHz, system clock = 256f_S, 24-bit data
In DSD mode, f_S = 2.8224 MHz (= 64 × 44.1 kHz), system clock = 256 × 44.1 kHz, 1-bit data

PARAMETERS		TEST CONDITIONS	DSD1702E MIN	DSD1702E TYP	DSD1702E MAX	UNITS
Digital Filter Performance						
Slow Rolloff Filter						
	Passband	–0.5 dB			0.308f_S	
		–3 dB			0.432f_S	
	Stopband		0.832f_S			
	Passband ripple	0.308 f_S			±0.5	dB
	Stopband attenuation	0.832 f_S	–58			dB
	Delay time			23/f_S		s
De-Emphasis Filter		PCM mode only				
	De-Emphasis error	At f_S = 32, 44.1 or 48 kHz		±0.1		dB
DSD Filter						
Filter–1						
	Passband	At –3 dB		50		kHz
	Stopband attenuation	At 100 kHz		–18		dB
Filter–2						
	Passband	At –3 dB		70		kHz
	Stopband attenuation	At 100 kHz		–9.8		dB
Filter–3						
	Passband	At –3 dB		60		kHz
	Stopband attenuation	At 100 kHz		–17		dB
Internal Analog Filter Performance						
	Frequency response	At 20 kHz		–0.02		dB
		At 44 kHz		–0.1		
		At 50 kHz		–0.12		
		At 100 kHz		–0.5		
Power Supply Requirements						
V_{DD}	Voltage range		3.0	3.3	3.6	VDC
V_{CC}			4.5	5	5.5	
I_{DD}	Supply current	f_S = 44.1 kHz		10	14	mA
		f_S = 192 kHz		23		
		DSD mode		17		
I_{CC}		f_S = 44.1 kHz		8.5	13	
		f_S = 192 kHz		9		
	Power dissipation	f_S = 44.1 kHz		76	111	mW
		f_S = 192 kHz		120		
Temperature Range						
	Operation temperature		–25		85	°C
θ_{JA}	Thermal resistance	20-pin QSOP		98		°C/W

system clock and reset functions

system clock input

The DSD1702 requires a system clock for operating the digital interpolation filter, digital DSD filter and multilevel delta-sigma modulator. The system clock is applied to PSCK (pin 18) in PCM mode and to DSCK (pin 19) in DSD mode. When CKCE (control register 20, B7) is not set to 1, the system clock is also applied to PSCK in DSD mode. The DSD1702 has a system clock detection circuit. Table I shows examples of system clock frequencies for common audio sampling rates.

Figure 1 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. Burr-Brown's PLL1700 multiclock generator is an excellent choice for providing the DSD1702 system clock.

In PCM mode, the over sampling rate of digital filter is 4 times when a $128f_S$ and $192f_s$ system clock is applied to DSD1702. When a $256f_S$, $384f_S$, $512f_S$ and $768f_S$ is applied, the over sampling rate is eight times.

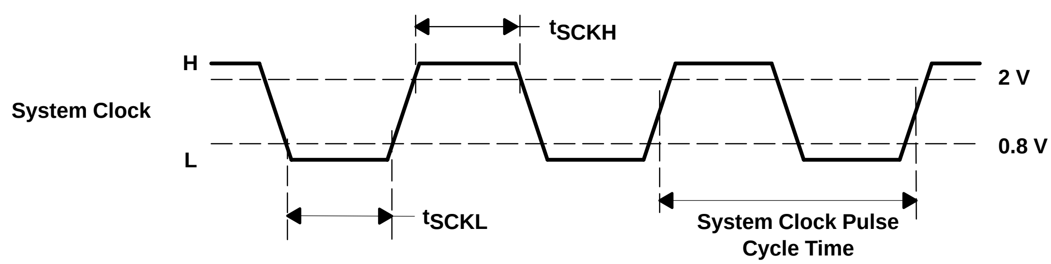
power-on reset functions

The DSD1702 includes a power-on reset function. Figure 1 shows the operation of this function. With V_{DD} > 2 V, the power-on reset function will be enabled. The initialization sequence requires 1024 system clocks from the time V_{DD} > 2 V as shown in Figure 2. After the initialization period, the DSD1702 will be set to its reset default state, as described in the mode control register section of this data sheet.

Table 1. System Clock Rates for Common Audio Sampling Frequencies

MODE	SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)					
		$128f_S$	$192f_S$	$256f_S$	$384f_S$	$512f_S$	$768f_S$
PCM	16kHz	2.048	3.072	4.096	6.144	8.192	12.288
	32kHz	4.096	6.144	8.192	12.288	16.384	24.576
	44.1kHz	5.6488	8.4672	11.2896	16.9344	22.5792	33.8688
	48kHz	6.144	9.216	12.288	18.432	24.576	36.864
	88.2kHz	11.2896	16.9344	22.5792	33.8688	45.1584	67.7376
	96kHz	12.288	16.84	24.576	36.864	49.152	73.728
	192kHz	24.576	36.864	See Note 9	See Note 9	See Note 9	See Note 9
DSD	64x44.1kHz	—	—	11.2896	16.9344	22.5792	33.8688

NOTE 9: This system clock is not supported for the given sampling frequency.



System Clock Pulse Width High	t_{SCKH}	**5 ns (min)**
System Clock Pulse Width Low	t_{SCKL}	**5 ns (min)**

Figure 1. System Clock Input Timing

system clock and reset functions (continued)

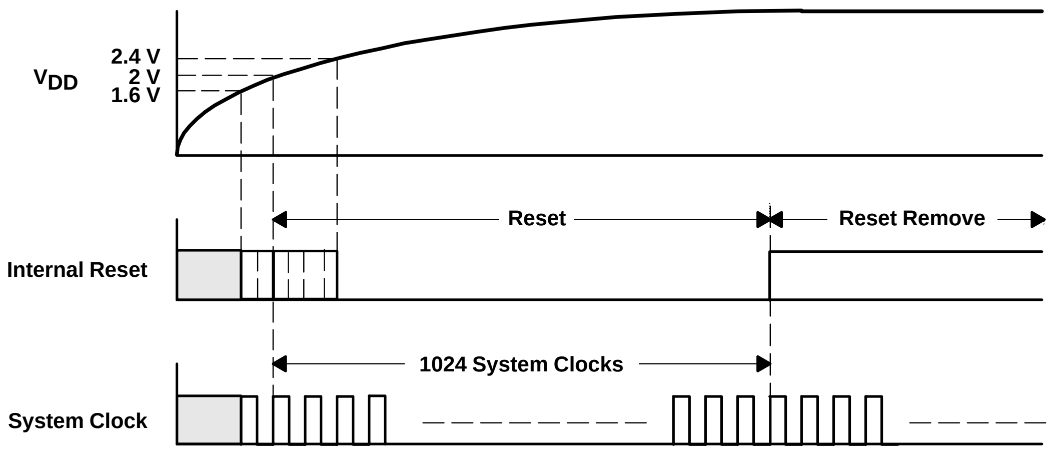


Figure 2. Power-On Reset Timing

audio serial interface

The DSD1702 has two audio serial interface ports: PCM audio interface port and DSD audio interface port.

In PCM mode, the audio interface is a 3-wire serial port. It includes PLRCK (pin 5), PBCK (pin 3), and PDATA (pin 4). PBCK is the serial audio bit clock, and it is used to clock the serial data present on PDATA into the serial shift register of the audio interface. Serial data is clocked into the DSD1702 on the rising edge of PBCK. PLRCK is the serial audio left/right word clock. It is used to latch serial data into the internal registers of the serial audio interface.

DSD1702 requires the synchronization of PLRCK and system clock, but does not need a specific phase relation between PLRCK and system clock.

If the relationship between PLRCK and system clock changes more than ±6 PBCK, internal operation is initialized within $1/f_S$ and analog outputs are forced into 0.5 V_{CC} until re-synchronization between PLRCK and system clock is completed.

In DSD mode, the audio interface port is also a 3-wire serial connection. DBCK (pin 20) is the serial audio bit clock, and it is used to clock the individual direct stream digital (= DSD) audio data on DSDL (pin 1) and DSDR (pin 2). DSD data is clocked into the DSD1702 on the rising edge of DBCK. DBCK must be synchronous with the system clock, but does not require a specific phase relation to it. DBCK is operated at the DSD sampling frequency, nominally 64 × 44.1kHz.

audio data formats and timing

In PCM mode, the DSD1702 supports industry-standard audio data formats, including standard, I^2S, and left-justified. The data formats are shown in Figures 3 and 4. Data formats are selected using the format bits, FMT[2:0], in control register 20. The default data format is 24-bit standard format. All formats require binary 2s complement, MSB-first audio data. Figure 5 shows a detailed timing diagram for the serial audio interface.

In DSD mode, the DSD1702 supports a DSD audio data format. The data formats are shown in FIGURE 5. The data formats are selected automatically when DSD bit in control register 22 is set. Figure 6 shows a detailed timing diagram for the DSD audio data interface.

serial control interface

The serial control interface is a 3-wire serial port which operates completely asynchronously to the serial audio interface. The serial control interface is utilized to program the on-chip mode registers. The control interface includes MD (pin 15), MC (pin 16), and MS (pin 17). MD is the serial data input, used to program the mode registers. MC is the serial bit clock, used to shift data into the control port. MS is the chip select for control port.

system clock and reset functions (continued)

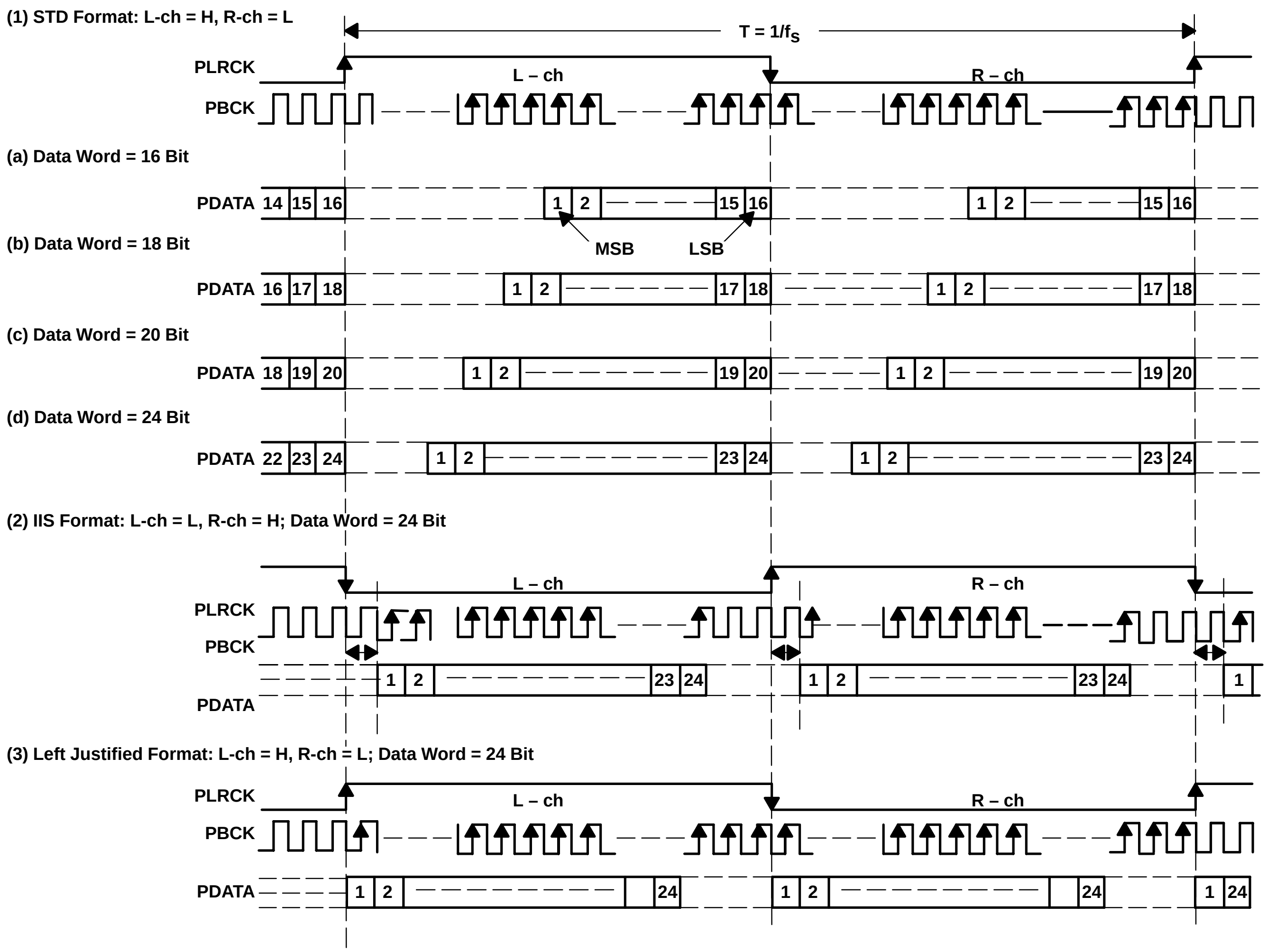


Figure 3. PCM Data Format

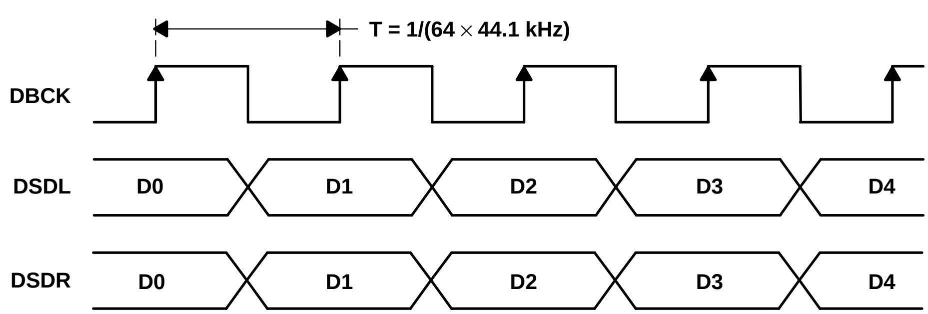


Figure 4. Normal Data Output Form From DSD Decoder

system clock and reset functions (continued)

PARAMETERS		MIN	MAX	UNIT
t_{BCY}	BCK pulse cycle time	70		ns
t_{BCH}	BCK high level time	30		ns
t_{BCL}	BCK low level time	30		ns
t_{BL}	BCK rising edge to LRCK edge	10		ns
t_{LB}	LRCK falling edge to BCK	10		ns
t_{DS}	Rising edge DIN set up time	10		ns
t_{DH}	DIN hold time	10		ns

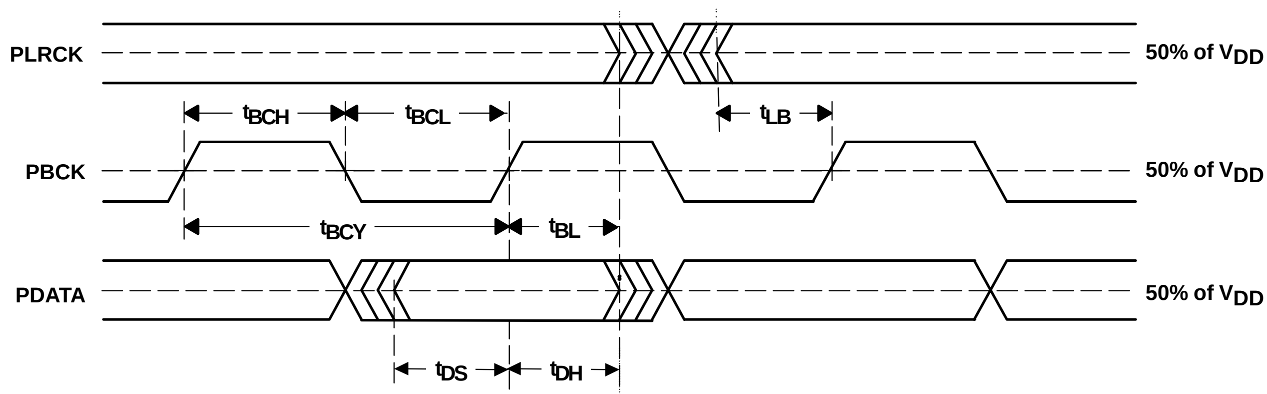


Figure 5. Timing for PCM Audio Interface

PARAMETERS		MIN	MAX	UNIT
t_{BCY}	BCK pulse cycle time		2.8224†	MHz
t_{BCH}	BCK high level time	30		ns
t_{BCL}	BCK low level time	30		ns
t_{DS}	DIN set up time	10		ns
t_{DH}	DIN hold time	10		ns

† 2.8224 MHz = 64 x 44.1 kHz, This value is specified as a sampling rate of DSD.

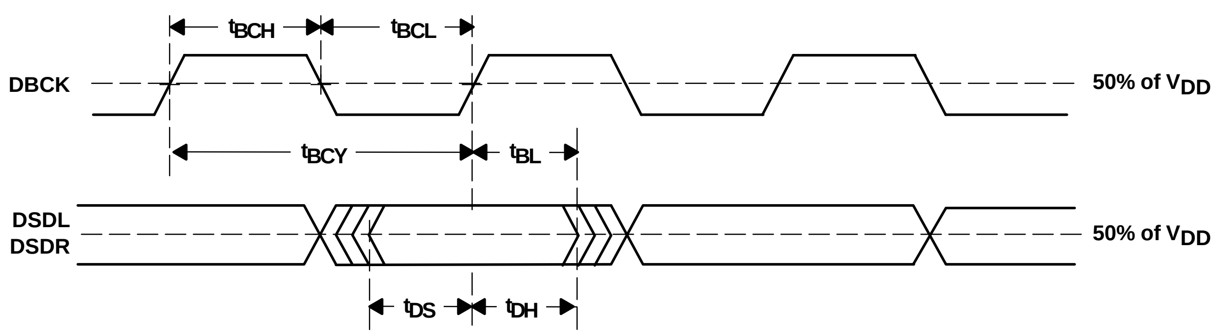


Figure 6. Timing for DSD Audio Interface

register write operation

All write operations for the serial control port use 16-bit data words. Figure 7 shows the control data word format. The most significant bit must be a 0. There are seven bits, labeled IDX[6:0], that set the register index (or address). The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 8 shows the functional timing diagram for the serial control port. MS is held at a logic 1 state until a register needs to be written. To start the register write cycle, MS is set to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MD. After the sixteenth clock cycle has completed, the data is latched into the indexed mode control register. To write the next data, MS must be set to 1 once.

control interface timing requirements

Figure 9 shows a detailed timing diagram for the serial control interface. These timing parameters are critical for proper control port operation.

MSB															LSB
0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	D7	D6	D5	D4	D3	D2	D1	D0
	Register Index (or Address)							Register Data							

Figure 7. Control Data Word Format MD

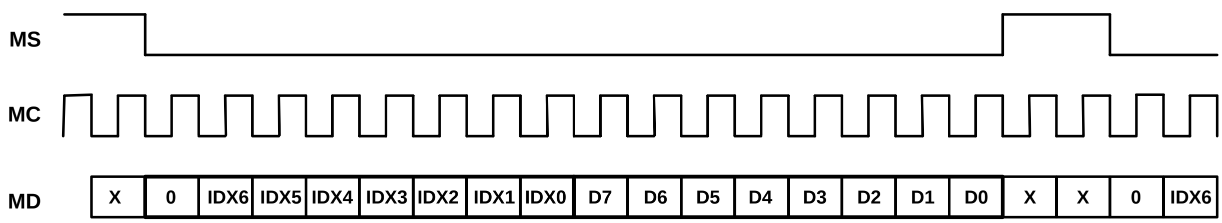
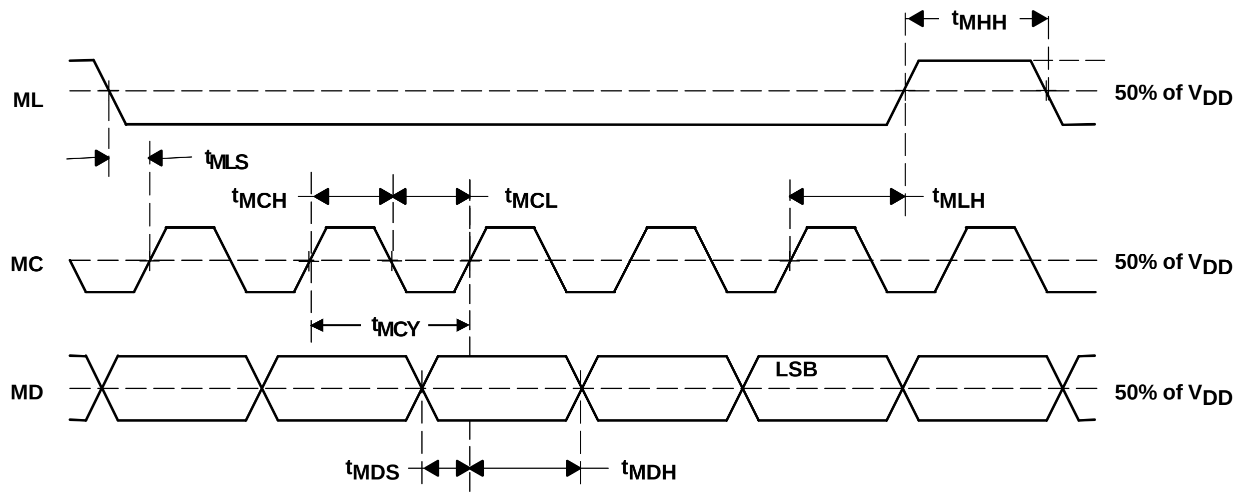


Figure 8. Register Write Operation

control interface timing requirements (continued)



PARAMETERS		MIN	MAX	UNIT
t_{MCY}	MC pulse cycle time	100		ns
t_{MCL}	MC low level time	40		ns
t_{MCH}	MC high level time	40		ns
t_{MHH}	MS high level time	80		ns
t_{MSS}	MS fall edge to MC rise edge	15		ns
t_{MSH}	MS hold time†	15		ns
t_{MDH}	MD hold time	15		ns
t_{MDS}	MD set-up time	15		ns

† MC rise edge for LSB to MS rise edge

Figure 9. Control Interface Timing

mode control registers

user-programmable mode controls

The DSD1702 includes a number of user programmable functions that are accessed via control registers. The registers are programmed using the serial control Interface as previously discussed in this data sheet. Table 2 lists the available mode control functions, along with their reset default conditions and associated register index.

Table 2. User-Programmable Mode Controls

FUNCTION	RESET DEFAULT	REGISTER	BIT(S)	PCM	DSD
Digital attenuation control, 0dB to –infinity in 0.5dB steps	0 dB, no attenuation	16 and 17	AT1[7:0], AT2[7:0]	√	√
Soft mute control	Mute disabled	18	MUT[2:0]	√	√
Infinite zero detect mute	Disabled	18	INZD	√	
Oversampling rate control ($64f_S$ or $128f_S$)	$64f_S$ oversampling	18	OVER	√	
DAC operation control	DAC1 and DAC2 enabled	19	DAC[2:1]	√	√
De-emphasis function control	De-emphasis disabled	19	DEM	√	
De-emphasis sample rate select	44.1 kHz	19	DMF[1:0]	√	
Audio data format control	24-Bit standard format	20	FMT[2:0]	√	
Roll-off control for 8x digital filter	Sharp roll-off	20	FLT	√	
Clock select control	Disabled	20	CKCE	√	√
System reset	Not operated	22	SRST	√	√
DSD mode control	PCM mode	22	DSD		√
DSD filter select	Filter-1	22	DFLT[1:0]		√
Zero flag output pin select	L/R flags separately	22	AZRO	√	
Output phase select	Normal phase	22	DREV	√	√
Zero flag polarity select	High	22	ZREV	√	

register map

The mode control register map is shown in Table 3. Each register includes an index (or address) indicated by the IDX[6:0] bits.

Table 3. Mode Control Register Map

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register 16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
Register 17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
Register 18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	OVER	RSV	INZD	RSV	RSV	MUT2	MUT1
Register 19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	DMF1	DMF0	DEM	RSV	RSV	DAC2	DAC1
Register 20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	CKCE	FLT	REV	RSV	RSV	FMT2	FMT1	FMT0
Register 21	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
Register 22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	RSV	DSD	DFLT1	DFLT0	AZRO	ZREV	DREV

mode control registers (continued)

register definitions

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
Register 17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20

ATx[7:0] Digital Attenuation Level Setting **:PCM/DSD Mode**

Where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

In PCM mode, default value : $1111\ 1111_B$, 0 dB.

Each DAC channel ($V_{OUT}L$ and $V_{OUT}R$) includes a digital attenuation function. The attenuation level may be set from 0 dB to –119.5 dB and –infinity in 0.5 dB steps in PCM mode and 6 dB to –113.5 dB and –infinity in DSD mode. Alternatively, the attenuation level may be set to infinite attenuation (or mute). A 6dB gain difference is applied between PCM mode and DSD mode to compensate for the 0.5 maximum modulation index of DSD signals.

The following table shows attenuation levels for various settings:

ATx[7:0]	DECIMAL VALUE	ATTENUATION LEVEL SETTING	
		PCM Mode	DSD Mode
$1111\ 1111_B$	255	0 dB, No Attenuation. (default)	6 dB
$1111\ 1110_B$	254	–0.5 dB	5.5 dB
$1111\ 1101_B$	253	–1 dB	5 dB
:	:	:	:
$1111\ 0011_B$	243	–6 dB	0 dB
$1111\ 0010_B$	242	–6.5 dB	–0.5 dB
:	:	:	:
$1000\ 0011_B$	131	–62 dB	–56 dB
$1000\ 0010_B$	130	–62.5 dB	–56.5 dB
$1000\ 0001_B$	129	–63 dB	–57 dB
$1000\ 0000_B$	128	–63.5 dB	–57.5 dB
:	:	:	:
$0111\ 0101_B$	117	–69 dB	–63 dB
:	:	:	:
$0001\ 0000_B$	16	–119.5 dB	–113.5 dB
$0000\ 1111_B$	15	–infinity	–infinity
:	:	:	:
$0000\ 0000_B$	0	–infinity	–infinity

IDX[6:0] Register Index
Register 16: 10000_B
Register 17: 10001_B

register definitions (continued)

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	OVER	RSV	INZD	RSV	RSV	MUT2	MUT1

MUTx Soft Mute Control **:PCM/DSD Mode**

Where, x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

Default value: 0

MUTx = 0	Mute disabled (default)
MUTx = 1	Mute enabled

The mute bits, MUT1 and MUT2, are used to enable or disable the soft mute function for the corresponding DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. The soft mute function is incorporated into the digital attenuators. When mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output will be decreased from the current setting to infinite attenuation, one attenuator step (0.5 dB) at a time. This provides *pop-free* muting of the DAC output.

By setting MUTx = 0, the attenuator will be incremented one step at a time to the previously programmed attenuation level.

INZD Infinite Zero Detect Mute Control **:PCM Mode**

Default value: 0

INZD = 0	Infinite zero detect mute disabled (default)
INZD = 1	Infinite zero detect mute disabled (default)

The INZD bit is used to enable or disable the zero detect mute function described in the zero flag and infinite zero detect mute section in this data sheet. The zero detect mute function is independent of the zero flag output operation, so enabling or disabling the INZD bit has no effect on the zero flag outputs (ZEROL and ZEROR).

OVER Oversampling Rate Control **:PCM Mode**

Default value: 0

OVER = 0	64x Oversampling for system clock ≥ $256f_S$, and 32x Oversampling for system clock < 256 f_S. (default)
OVER = 1	128x Oversampling for system clock ≥ $256f_S$, and 64x Oversampling for system clock < 256 f_S.

Sets the oversampling rate of the delta-sigma D/A converters. The OVER = 1 setting is recommended when the system clock is 128 f_S or 192 f_S.

RSV Reserved Bit

The RSV should be set to 0.

IDX[6:0] Register Index

Register 18: 10010_B

register definitions (continued)

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 19	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	DMF1	DMF0	DEM	RSV	RSV	DAC2	DAC1

DACx DAC Operation Control **:PCM/DSD Mode**

Where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) or $V_{OUT}R$ (x = 2).

Default value: 0

DACx = 0	DAC operation enabled (default)
DACx = 0	DAC operation disabled

The DAC operation controls are used to enable and disable the DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. When DACx = 0, the corresponding output will generate the audio waveform dictated by the data present on the DATA pin. When DACx = 1, the corresponding output will be set to the bipolar zero level, or $V_{CC}/2$.

DME De-emphasis Function Control **:PCM Mode**

Default value: 0

DME = 0	De-emphasis disabled (default)
DME = 1	De-emphasis enabled

The DME bit is used to enable or disable the digital de-emphasis function. Refer to the plots shown in the Typical Characteristics section of this data sheet.

DMF[1:0] Sampling Frequency Select for the De-emphasis Function **:PCM Mode**

Default value: 00

The DMF[1:0] bits are used to select the sampling frequency used for the digital de-emphasis function when it is enabled.

DMF[1:0]	De-emphasis Sample Rate Select
00	44.1 kHz (default)
01	48 kHz
10	32 kHz
11	Reserved

RSV Reserved Bit

The RSV should be set to 0.

IDX[6:0] Register Index

Register 19: 10011_B

register definitions (continued)

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	CKCE	FLT	RSV	RSV	RSV	FMT2	FMT1	FMT0

FMT[2:0] Audio Interface Data Format :PCM Mode

Default value: 00

The FMT[2:0] bits are used to select the data format for the serial audio interface. The table below shows the available format options.

FMT[2:0]	Audio Data Format Select
000	24-Bit standard format, right-justified data (default)
001	20-Bit standard format, right-justified data
010	18-Bit standard format, right-justified data
011	16-Bit standard format, right-justified data
100	I^2S format, 24 bits
101	Left-justified format, 24 bits
110	Reserved
111	Reserved

FLT Digital Filter Roll-Off Control :PCM Mode

Default value: 0

FLT = 0	Sharp rolloff (default)
FLT = 1	Slow rolloff

The FLT bit allows the user to select the digital filter rolloff that is best suited to their application. Sharp and slow filter rolloffs are available. The response curves for filter selections are shown in the Typical Characteristics section of this data sheet.

CKCE Clock Select Control :DSD Mode

Default value: 0

CKCE = 0	System clock is applied to PSCK in DSD mode(default)
CKCE = 1	System clock is applied to DSCK in DSD mode

The CKCE bit selects system clock source in DSD mode. (PSCK or DSCK)

The CKCE bit must be set before to set DSD to 1.

RSV Reserved Bit

The RSV should be set to 0.

IDX[6:0] Register Index

Register 20: 10100_B

register definitions (continued)

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 21	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV

User cannot write register 21. All RSV bits [B7:B0] must be set to 0.

IDX[6:0] Register Index

Register 21: 10101_B

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	RSV	DSD	DFLT1	DFLT0	AZRO	ZREV	DREV

DREV Output Phase Select **:PCM/DSD Mode**

Default value: 0

DREV = 0	Normal output (default)
DREV = 1	Inverted output

The DREV bit is output analog signal phase control.

ZREV Zero Flag Polarity Select **:PCM Mode**

Default value: 0

ZREV = 0	Zero flag pins HIGH at a zero detect (default)
ZREV = 1	Zero flag pins LOW at a zero detect

The ZREV bit allows the user to select the polarity of zero flag pins.

AZRO Zero Flag Output Pin Select **:PCM Mode**

Default value: 0

AZRO = 0	When ZREV=0, ZEROL and ZEROR pin of each channel goes to HIGH when each channel is continuously zero data. (default) When ZREV=1, ZEROL and ZEROR pin of each channel goes to LOW when each channel is continuously zero data.
AZRO = 1	When ZREV=0, ZEROR pin goes to HIGH when both L and R channels are continuously zero at the same time. ZEROL pin stays in LOW state. When ZREV=1, ZEROR pin goes to LOW when both L and R channels are continuously zero at the same time. ZEROL pin stays in LOW state.

The AZRO bit allows the user to select output form of zero flag pins.

DFLT[1:0] DSD Filter Select **:DSD Mode**

Default value: 0

DFLT[1:0]	DSD Filter Select
00	Filter-1 (default
01	Filter-2
10	Filter-3
11	Reserved

The DFLT[1:0] bits allow the user to select the DSD filter from three kind of filters.

register definitions (continued)

DSD DSD Mode Control **:PCM/DSD Mode**

Default value: 0

DSD = 0	PCM mode (default)
DSD = 1	DSD mode

The DSD bit allows the user to control the operation mode, PCM mode and DSD mode.

SRST System Reset **:PCM/DSD Mode**

Default value: 0

SRST = 0	Not operated (default)
SRST = 1	DAC system is reset once

The SRST bit allows the user to reset DAC system. This function is same as the power on reset.

RSV Reserved Bit

The RSV should be set to 0.

IDX[6:0] Register Index

Register 22: 10110_B

analog outputs

The DSD1702 includes two independent output channels, V_{OUT}L and V_{OUT}R. These are unbalanced outputs, each capable of driving 3.1 $V_{(pp)}$ typical into a 10-kΩ ac-coupled load. The internal output amplifiers for V_{OUT}L and V_{OUT}R are biased to the dc common-mode (or bipolar zero) voltage, equal to V_{CC} / 2.

The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise shaping characteristics of the delta-sigma D/A converters. The frequency response of this filter is shown in Figure 10. By itself, this filter may not be enough to attenuate the out-of-band noise to an acceptable level for many applications. An external low-pass filter is recommended to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the Applications Information section of this data sheet.

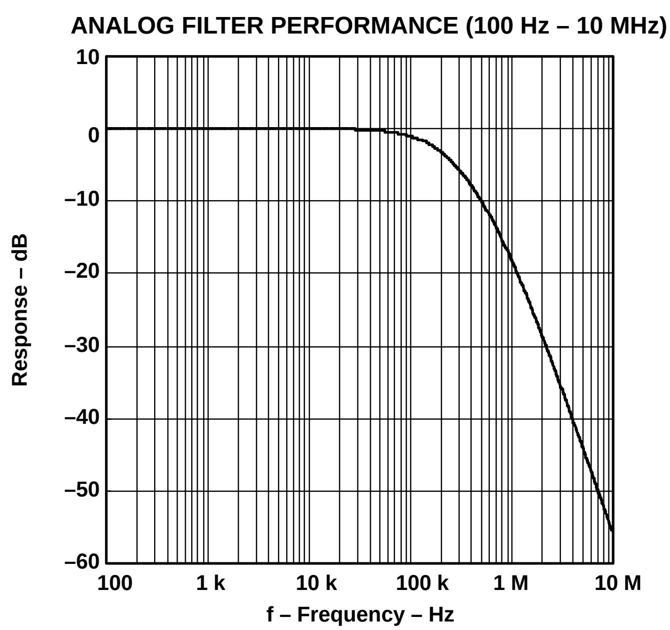


Figure 10. Output Filter Frequency Response

zero flags and zero detect mute functions

The DSD1702 includes circuitry for detecting an all 0 data condition for the PCM audio data input pin. This includes two independent functions: zero output flags and zero detect mute. Although the flag and mute functions are independent of one another, the zero detection mechanism is common to both functions.

zero detect condition

Zero detection for each output channel is independent from the other.

In PCM mode, if the data for a given channel remains at a 0 level for 1024 sample periods (or PLRCK clock periods), a zero detect condition exists for that channel.

In DSD mode, the zero detection is not available.

zero output flags

Given that a zero detect condition exists for one or more channels, the zero flag pins for those channels will be set to a logic 1 state. There are zero flag pins for each channel, ZEROL (pin 14) and ZEROR (pin 13). These pins can be used to operate external mute circuits, or used as status indicators for a microcontroller, audio signal processor, or other digitally-controlled circuit.

The active polarity of zero flag outputs can be inverted by setting the ZREV bit of control register 22 to 1. The reset default is active high output, or ZREV = 0.

infinite zero detect mute

Infinite zero detect mute is an internal logic function. This function is available in PCM mode only. The zero detect mute can be enabled or disabled using the INZD bit of control register 18. The reset default is zero detect mute disabled, INZD = 0. If the input data on L- and R-channels is countinuously and simultaneously zero for 1024 clocks of LRCK, the zero mute circuitry will immediately force the corresponding DAC output(s) to the bipolar zero level, or $0.5V_{CC}$.

APPLICATION INFORMATION

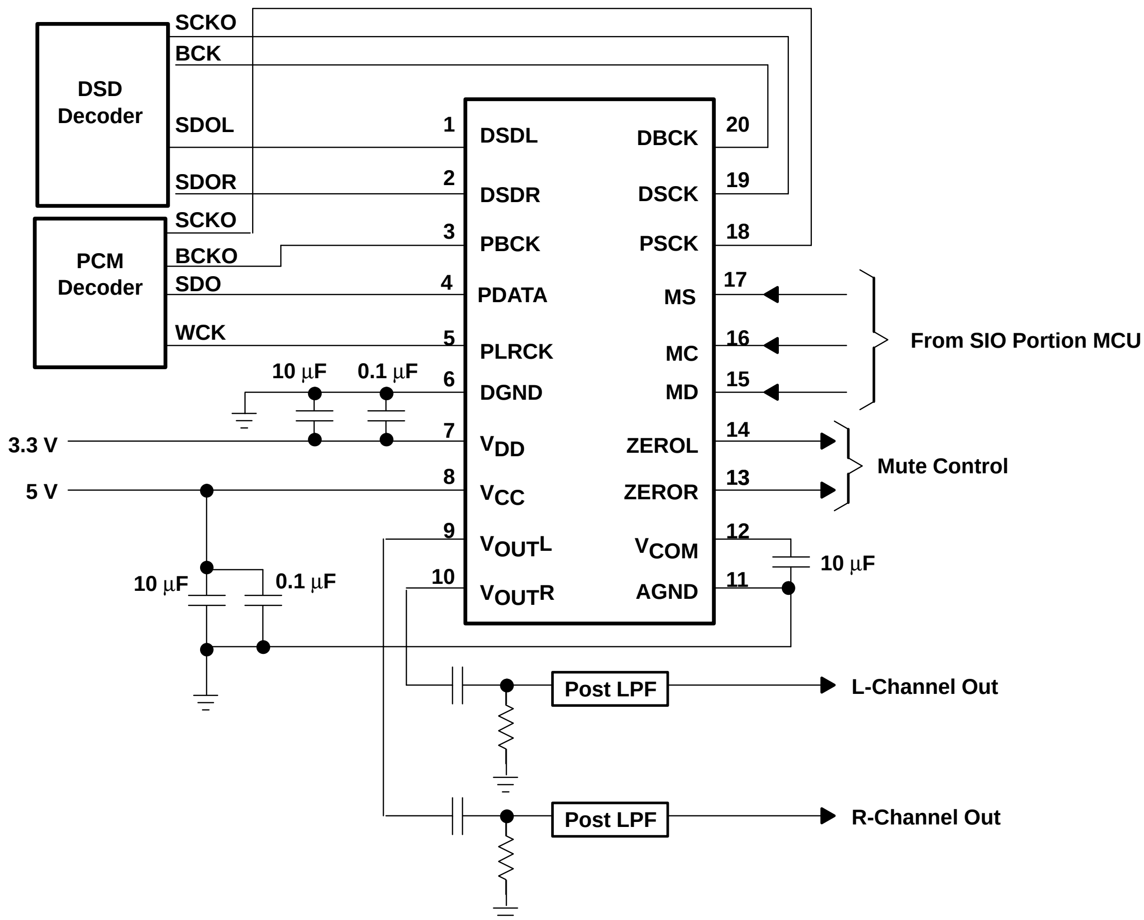


Figure 11. Basic Connection Diagram

connection diagrams

A basic connection diagram is shown in Figure 11, with the necessary power supply bypassing and decoupling components.

The use of series terminating resistors (22 Ω to 100 Ω) fitted close to the signal source is recommended for the xSCK, PLRCK, xBCK, DATA, DSDx inputs. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter which reduces high frequency noise emissions and helps to dampen glitches and ringing present on clock and data lines.

power supplies and grounding

The DSD1702 requires a 5-V analog supply and a 3.3-V digital supply. The 5-V supply is used to power the DAC analog and output filter circuitry, while the 3.3-V supply is used to power the digital filter and serial interface circuitry. For best performance, the 3.3-V digital supply should be derived from the 5-V supply by using a linear regulator. Burr-Brown’s REG1117-3.3 is an ideal choice for this application.

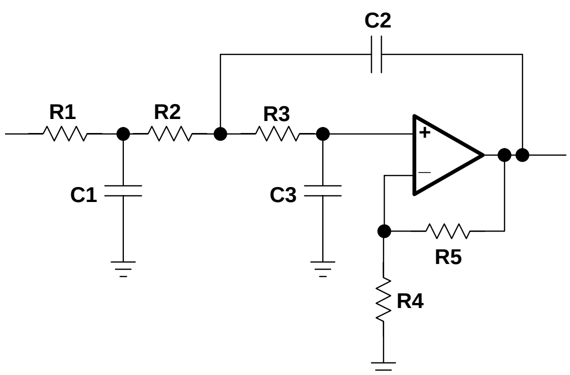
Proper power supply bypassing is shown in Figure 12. The 10-µF capacitors should be tantalum or aluminum electrolytic, while the 0.1-µF capacitors are ceramic (X7R type is recommended for surface-mount applications).

APPLICATION INFORMATION

D/A output filter circuits: post low-pass filter

The DSD1702 requires a third or second-order analog low-pass filter to achieve the frequency response recommended by SACD standard and reduce the out-of-band noise both produced by the DSD1702 delta-sigma modulator and inherent in the DSD modulated input signal.

Figure 12 shows the recommended external low-pass filter circuit. This circuit is a 3rd order Butterworth filter using the Sallen-Key circuit arrangement. The filter response and corner frequency are determined by the frequency response recommended by SACD standard. The table in Figure 12 lists the standard resistor and capacitor values corresponding with the DSD digital filter on DSD1702. This filter can be used in PCM and DSD modes.



	DSD Filter
R1	2.7 kΩ
R2	6.8 kΩ
R3	15 kΩ
R4	10 kΩ
R5	10 kΩ
C1	1500 pF
C2	680 pF
C3	100 pF

Figure 12. Post Low-Pass Filter Circuit

TYPICAL CHARACTERISTICS

digital filter—PCM mode

x8 interpolation filter (de-emphasis off)

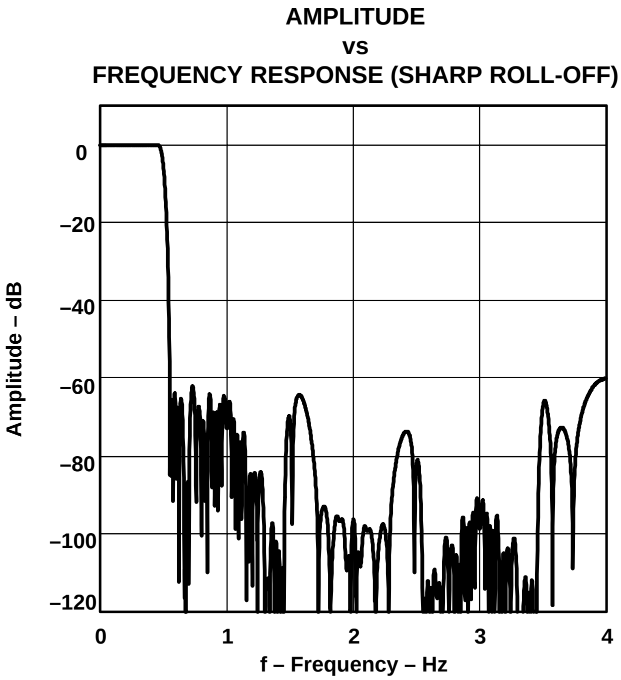


Figure 13

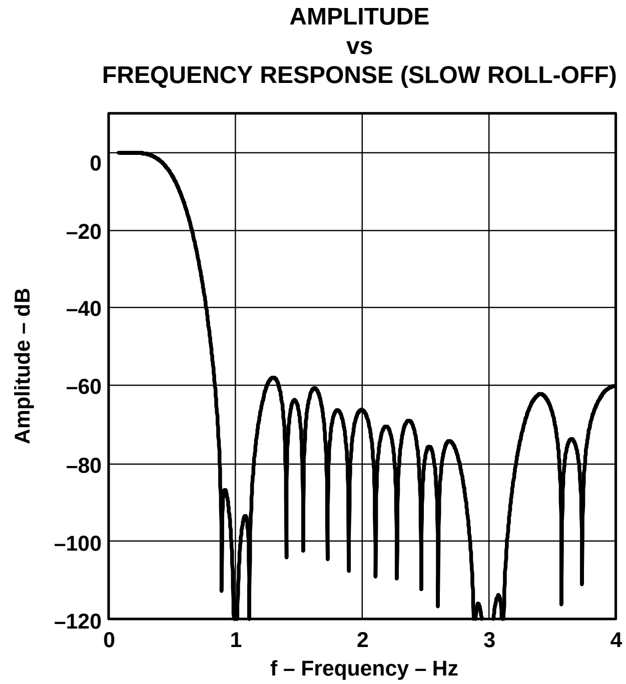


Figure 14

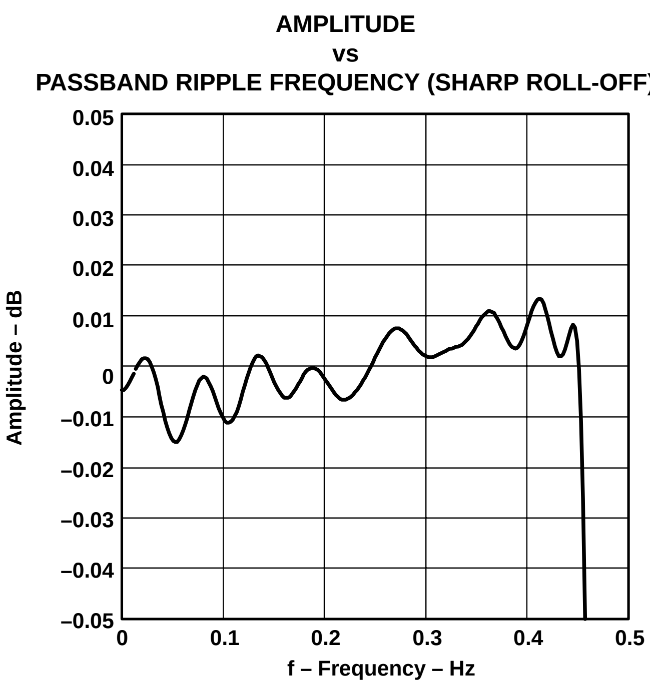


Figure 15

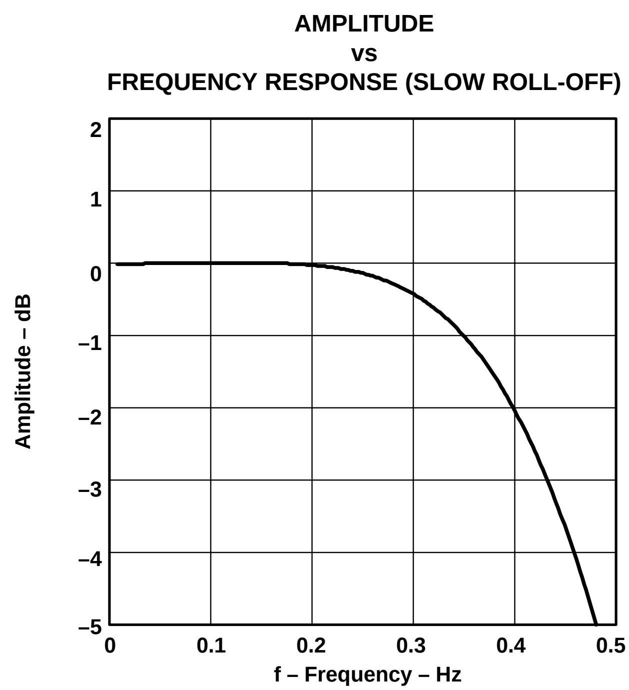


Figure 16

TYPICAL CHARACTERISTICS

digital filter—PCM mode (continued)

de-emphasis curves

LEVEL vs FREQUENCY DE-EMPHASIS (f_S = 32 kHz)

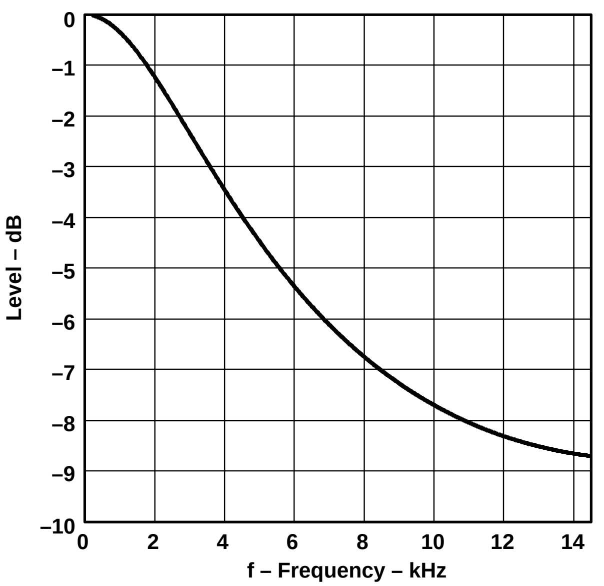


Figure 17

ERROR vs FREQUENCY DE-EMPHASIS (f_S = 32 kHz)

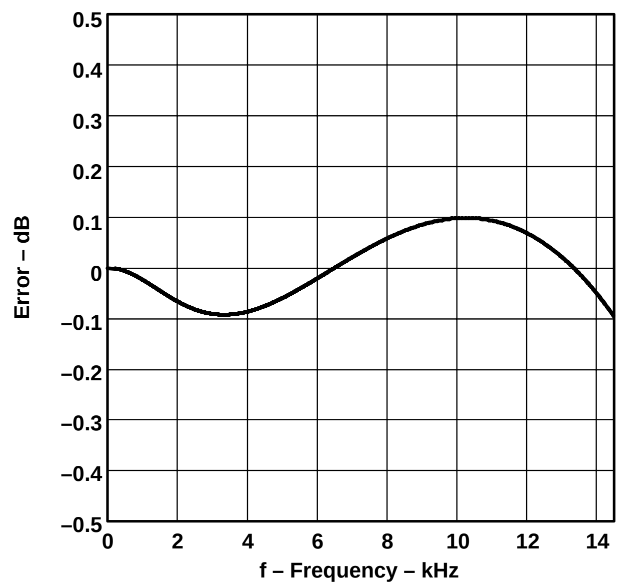


Figure 18

LEVEL vs FREQUENCY DE-EMPHASIS (f_S = 44.1 kHz)

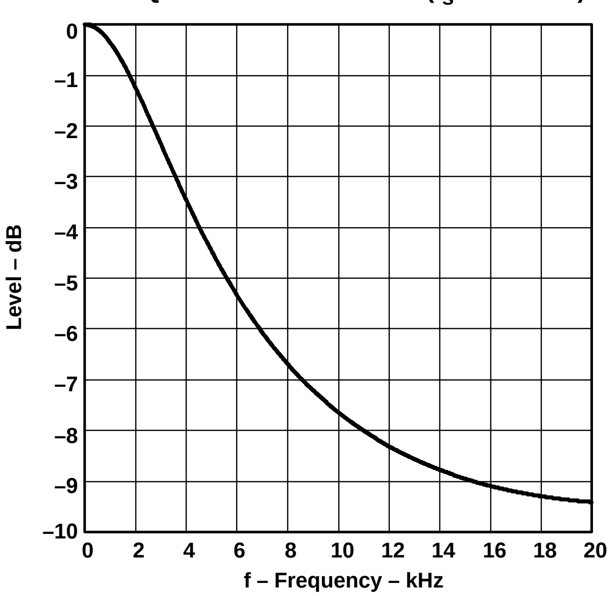


Figure 19

ERROR vs FREQUENCY DE-EMPHASIS (f_S = 44.1 kHz)

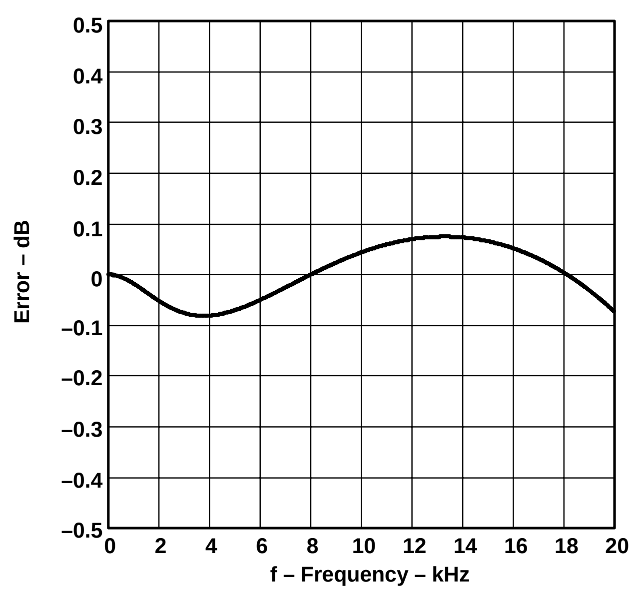


Figure 20

TYPICAL CHARACTERISTICS

digital filter—PCM mode (continued)

de-emphasis curves

LEVEL
vs
FREQUENCY DE-EMPHASIS (f_S = 48 kHz)

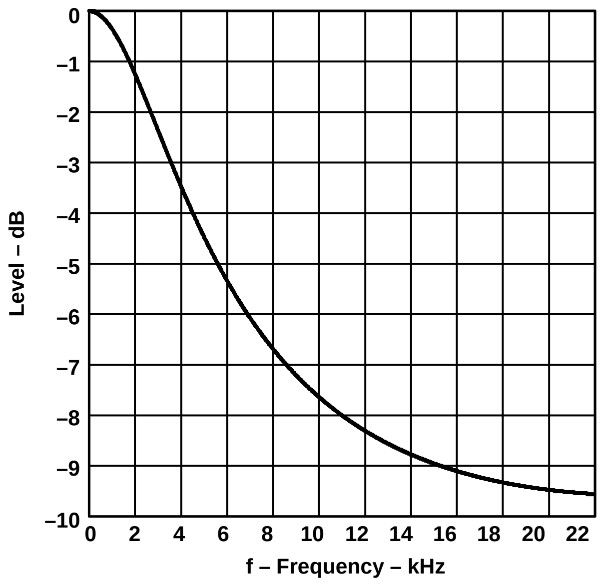


Figure 21

ERROR
vs
FREQUENCY DE-EMPHASIS (f_S = 48 kHz)

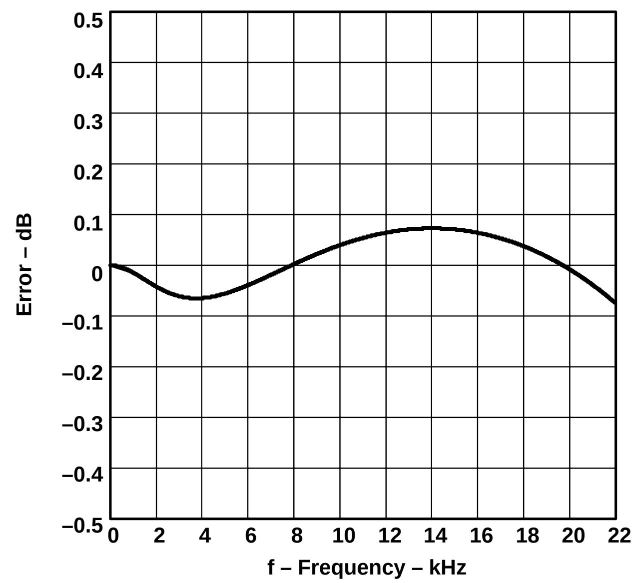


Figure 22

digital filter—DSD mode

DSD MODE AMPLITUDE
vs
INTERNAL DIGITAL FILTER FREQUENCY

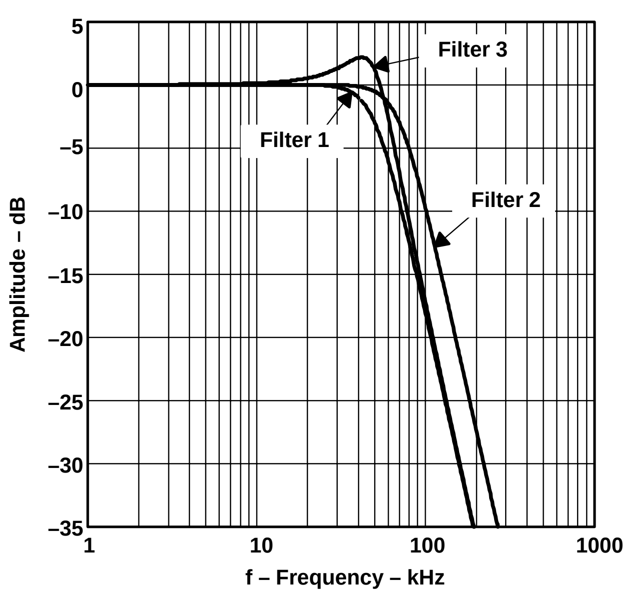


Figure 23

TYPICAL CHARACTERISTICS

analog dynamic performance

supply voltage characteristics

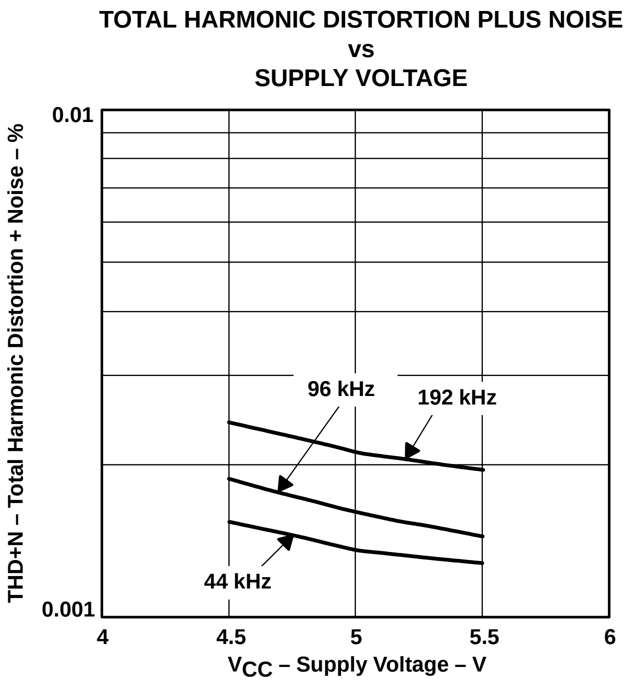


Figure 24

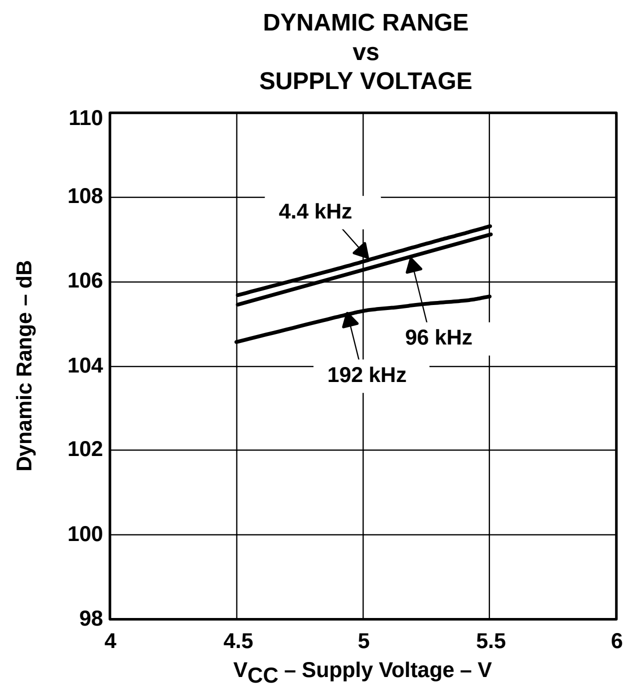


Figure 25

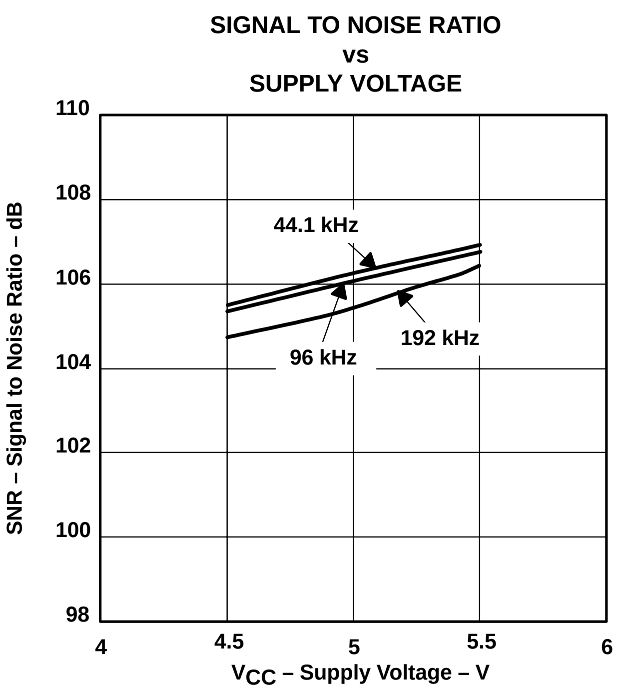


Figure 26

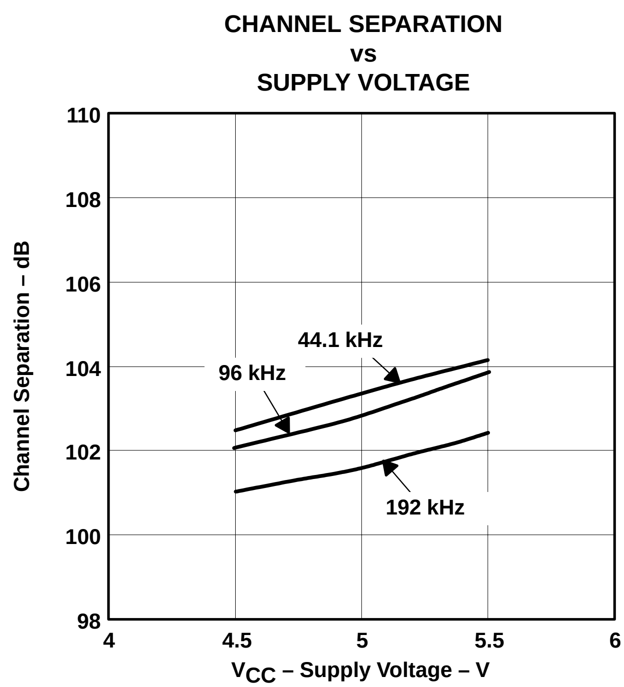


Figure 27

TYPICAL CHARACTERISTICS

analog dynamic performance (continued)

temperature characteristics

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREE-AIR TEMPERATURE

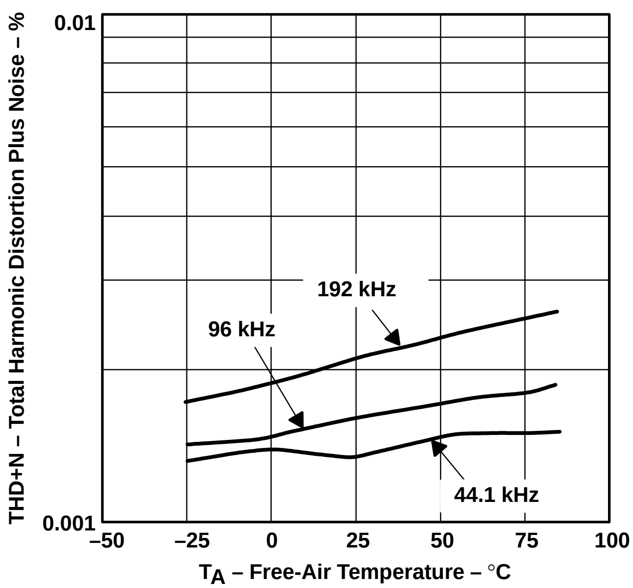


Figure 28

DYNAMIC RANGE
vs
FREE-AIR TEMPERATURE

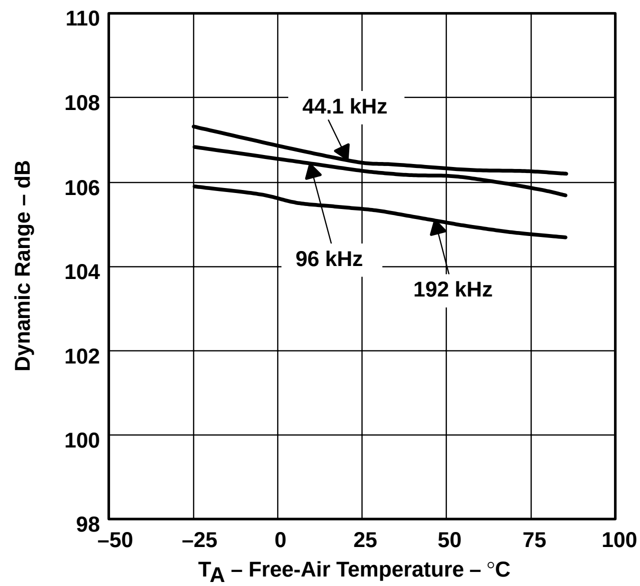


Figure 29

SIGNAL TO NOISE NOISE
vs
FREE-AIR TEMPERATURE

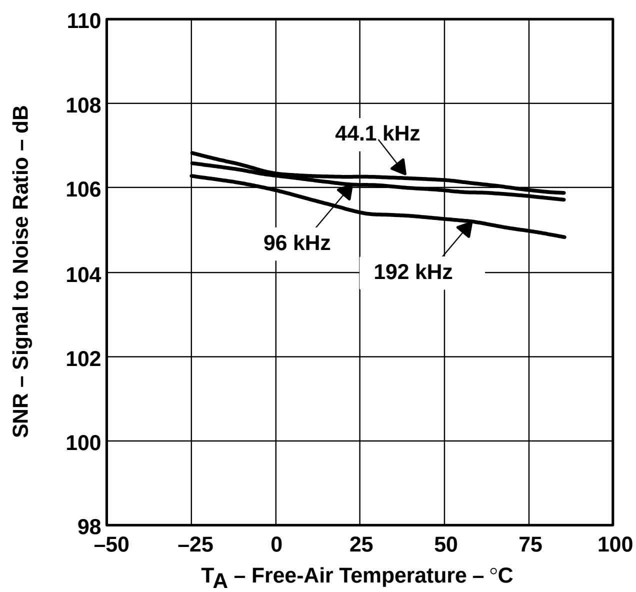


Figure 30

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265