Burr-Brown Products
from Texas Instruments

DSD1792

SLES067A − MARCH 2003 − REVISED AUGUST 2003

24-BIT, 192-kHz SAMPLING, ADVANCED SEGMENT, AUDIO STEREO DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Supports Both DSD and PCM Formats**
- **24-Bit Resolution**
- **Analog Performance:**
  - **Dynamic Range:**
    - **132 dB (9 V rms, Mono)**
    - **129 dB (4.5 V rms, Stereo)**
    - **127 dB (2 V rms, Stereo)**
  - **THD+N: 0.0004%**
- **Differential Current Output: 7.8 mA p-p**
- **8× Oversampling Digital Filter:**
  - **Stop-Band Attenuation: –130 dB**
  - **Pass-Band Ripple: ±0.00001 dB**
- **Sampling Frequency: 10 kHz to 200 kHz**
- **System Clock: 128, 192, 256, 384, 512, or 768 f_S With Autodetect**
- **Accepts 16-, 20-, and 24-Bit Audio Data**
- **PCM Data Formats: Standard, I^2S, and Left-Justified**
- **Optional Interface to External Digital Filter or DSP Available**
- **TDMCA Interface Available**
- **User-Programmable Mode Controls:**
  - **Digital Attenuation: 0 dB to –120 dB, 0.5 dB/Step**
  - **Digital De-Emphasis**
  - **Digital Filter Rolloff: Sharp or Slow**
  - **Soft Mute**
- **Dual Supply Operation:**
  - **5 V Analog, 3.3 V Digital**
- **5-V Tolerant Digital Inputs**
- **Small 28-Lead SSOP Package, Lead-Free Product**

APPLICATIONS

- **A/V Receivers**
- **SACD Player**
- **DVD Players**
- **HDTV Receivers**
- **Car Audio Systems**
- **Digital Multi-Track Recorders**
- **Other Applications Requiring 24-Bit Audio**

DESCRIPTION

The DSD1792 is a monolithic CMOS integrated circuit that includes stereo digital-to-analog converters and support circuitry in a small 28-lead SSOP package. The data converters use TI's advanced-segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The DSD1792 provides balanced current outputs, allowing the user to optimize analog performance externally. The DSD1792 accepts the PCM and DSD audio data formats, providing easy interfacing to audio DSP and decoder chips. The DSD1792 also interfaces with external digital filter devices (DF1704, DF1706, PMD200). Sampling rates up to 200 kHz are supported. A full set of user−programmable functions is accessible through a 4-wire serial control port, which supports register write and readback functions. The DSD1792 also supports the time-division-multiplexed command and audio (TDMCA) data format.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DSD1792DB	28-lead SSOP	28DB	−25°C to 85°C	DSD1792	DSD1792DB	Tube
					DSD1792DBR	Tape and reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[(1)]

		DSD1792
Supply voltage	$V_{CC}1$, $V_{CC}2L$, $V_{CC}2R$	−0.3 V to 6.5 V
	V_{DD}	−0.3 V to 4 V
Supply voltage differences: $V_{CC}1$, $V_{CC}2L$ and $V_{CC}2R$		±0.1 V
Ground voltage differences: AGND1, AGND2, AGND3L, AGND3R and DGND		±0.1 V
Digital input voltage	PLRCK, PDATA, PBCK, SCK, $\overline{RST}$, $\overline{MS}$[(2)], MDI, MC, DSDL[(2)], DSDR[(2)], DBCK	–0.3 V to 6.5 V
	DSDL[(3)], DSDR[(3)], $\overline{MS}$[(3)], MDO	–0.3 V to (V_{DD} + 0.3 V) < 4 V
Analog input voltage		–0.3 V to (V_{CC} + 0.3 V) < 6.5 V
Input current (any pins except supplies)		±10 mA
Ambient temperature under bias		–40°C to 125°C
Storage temperature		–55°C to 150°C
Junction temperature		150°C
Lead temperature (soldering)		260°C, 5 s
Package temperature (IR reflow, peak)		250°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input mode

(3) Output mode

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, $V_{CC}1$ = $V_{CC}2L$ = $V_{CC}2R$ = 5 V, f_S = 44.1 kHz, system clock = 256 f_S, and 24-bit data unless otherwise noted

PARAMETER		TEST CONDITIONS	DSD1792DB MIN	DSD1792DB TYP	DSD1792DB MAX	UNIT
RESOLUTION				24		Bits
DATA FORMAT (PCM Mode)						
	Audio data interface format			Standard, I^2S, left justified		
	Audio data bit length			16-, 20-, 24-bit selectable		
	Audio data format			MSB first, 2s complement		
f_S	Sampling frequency		10		200	kHz
	System clock frequency			128, 192, 256, 384, 512, 768 f_S		
DATA FORMAT (DSD Mode)						
	Audio data interface format			DSD (direct stream digital)		
	Audio data bit length			1 Bit		
f_S	Sampling frequency			2.8224		MHz
	System clock frequency		2.8224		11.2896	MHz

ELECTRICAL CHARACTERISTICS (Continued)

all specifications at T_A = 25°C, $V_{CC}1 = V_{CC}2L = V_{CC}2R$ = 5 V, f_S = 44.1 kHz, system clock = 256 f_S, and 24-bit data unless otherwise noted

PARAMETER		TEST CONDITIONS	DSD1792DB MIN	DSD1792DB TYP	DSD1792DB MAX	UNIT
DIGITAL INPUT/OUTPUT						
	Logic family			TTL compatible		
V_{IH}	Input logic level		2			VDC
V_{IL}	Input logic level				0.8	VDC
I_{IH}	Input logic current	$V_{IN} = V_{DD}$			10	µA
I_{IL}	Input logic current	V_{IN} = 0 V			–10	µA
V_{OH}	Output logic level	I_{OH} = −2 mA	2.4			VDC
V_{OL}	Output logic level	I_{OL} = 2 mA			0.4	VDC
I_{OHZ}	High-impedance output logic current(1)	$V_{OUT} = V_{DD}$			10	µA
I_{OLZ}	High-impedance output logic current(1)	V_{OUT} = 0 V			−10	µA
DYNAMIC PERFORMANCE (PCM MODE, 2-V RMS OUTPUT) (2)(3)						
	THD+N at V_{OUT} = 0 dB	f_S = 44.1 kHz		0.0004%	0.0008%	
		f_S = 96 kHz		0.0008%		
		f_S = 192 kHz		0.0015%		
	Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz	123	127		dB
		EIAJ, A-weighted, f_S = 96 kHz		127		dB
		EIAJ, A-weighted, f_S = 192 kHz		127		dB
	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz	123	127		dB
		EIAJ, A-weighted, f_S = 96 kHz		127		dB
		EIAJ, A-weighted, f_S = 192 kHz		127		dB
	Channel separation	f_S = 44.1 kHz	120	123		dB
		f_S = 96 kHz		122		dB
		f_S = 192 kHz		120		dB
	Level Linearity Error	V_{OUT} = –120 dB		±1		dB
DYNAMIC PERFORMANCE (PCM Mode, 4.5-V RMS Output) (2)(4)						
	THD+N at V_{OUT} = 0 dB	f_S = 44.1 kHz		0.0004%		
		f_S = 96 kHz		0.0008%		
		f_S = 192 kHz		0.0015%		
	Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz		129		dB
		EIAJ, A-weighted, f_S = 96 kHz		129		dB
		EIAJ, A-weighted, f_S = 192 kHz		129		dB
	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz		129		dB
		EIAJ, A-weighted, f_S = 96 kHz		129		dB
		EIAJ, A-weighted, f_S = 192 kHz		129		dB
	Channel separation	f_S = 44.1 kHz		124		dB
		f_S = 96 kHz		123		dB
		f_S = 192 kHz		121		dB

(1) Pin 13 (MDO)
(2) Filter condition:
THD+N: 20-Hz HPF, 20-kHz apogee LPF
Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
Signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
Channel separation: 20-Hz HPF, 20-kHz AES17 LPF
Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode.
(3) Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 33.
(4) Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 34.

ELECTRICAL CHARACTERISTICS (Continued)

all specifications at T_A = 25°C, $V_{CC}1$ = $V_{CC}2L$ = $V_{CC}2R$ = 5 V, f_S = 44.1 kHz, system clock = 256 f_S, and 24-bit data unless otherwise noted

PARAMETER	TEST CONDITIONS	DSD1792DB MIN	DSD1792DB TYP	DSD1792DB MAX	UNIT
DYNAMIC PERFORMANCE (MONO MODE) (1)(2)					
THD+N at V_{OUT} = 0 dB	f_S = 44.1 kHz		0.0004%		
	f_S = 96 kHz		0.0008%		
	f_S = 192 kHz		0.0015%		
Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz		132		dB
	EIAJ, A-weighted, f_S = 96 kHz		132		
	EIAJ, A-weighted, f_S = 192 kHz		132		
Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz		132		dB
	EIAJ, A-weighted, f_S = 96 kHz		132		
	EIAJ, A-weighted, f_S = 192 kHz		132		
DSD MODE DYNAMIC PERFORMANCE (1) (3) **(44.1 kHz, 64 F_S)**					
THD+N at FS	4.5 V rms		0.0005%		
Dynamic range	–60 dB, EIAJ, A-weighted		128		dB
Signal-to-noise ratio	EIAJ, A-weighted		128		dB
ANALOG OUTPUT					
Gain error		–6	±2	6	% of FSR
Gain mismatch, channel-to-channel		–3	±0.5	3	% of FSR
Bipolar zero error	At BPZ	–2	±0.5	2	% of FSR
Output current	Full scale (0 dB)		7.8		mA p-p
Center current	At BPZ		–6.2		mA
DIGITAL FILTER PERFORMANCE					
De-emphasis error				±0.004	dB
FILTER CHARACTERISTICS-1: SHARP ROLLOFF					
Pass band	±0.00001 dB			0.454 f_S	
	–3 dB			0.49 f_S	
Stop band		0.546 f_S			
Pass-band ripple				±0.00001	dB
Stop-band attenuation	Stop band = 0.546 f_S	–130			dB
Delay time			55/f_S		s
FILTER CHARACTERISTICS-2: SLOW ROLLOFF					
Pass band	±0.04 dB			0.254 f_S	
	–3 dB			0.46 f_S	
Stop band		0.732 f_S			
Pass-band ripple				±0.001	dB
Stop-band attenuation	Stop band = 0.732 f_S	–100			dB
Delay time			18/f_S		s

(1) Filter condition:
THD+N: 20-Hz HPF, 20-kHz apogee LPF
Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
Signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
Channel separation: 20-Hz HPF, 20-kHz AES17 LPF
Analog performance specifications are measured using the System Two Cascade audio measurement system by Audio Precision in the averaging mode.

(2) Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 34.

(3) Dynamic performance and dc accuracy are specified at the output of the postamplifier as shown in Figure 35.

ELECTRICAL CHARACTERISTICS (Continued)

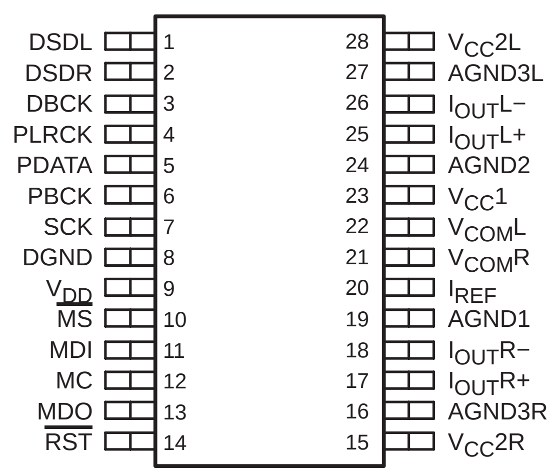
all specifications at T_A = 25°C, $V_{CC}1$ = $V_{CC}2L$ = $V_{CC}2R$ = 5 V, f_S = 44.1 kHz, system clock = 256 f_S, and 24-bit data unless otherwise noted

PARAMETER		TEST CONDITIONS	DSD1792DB			UNIT
			MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS						
V_{DD}	Voltage range		3	3.3	3.6	VDC
$V_{CC}1$, $V_{CC}2L$, $V_{CC}2R$	Voltage range		4.75	5	5.25	VDC
I_{DD}	Supply current (1)	f_S = 44.1 kHz		12	15	mA
		f_S = 96 kHz		23		
		f_S = 192 kHz		45		
I_{CC}	Supply current (1)	f_S = 44.1 kHz		33	40	mA
		f_S = 96 kHz		35		
		f_S = 192 kHz		37		
	Power dissipation (1)	f_S = 44.1 kHz		205	250	mW
		f_S = 96 kHz		250		
		f_S = 192 kHz		335		
TEMPERATURE RANGE						
	Operation temperature		–25		85	°C
θ_{JA}	Thermal resistance	28-pin SSOP		100		°C/W

(1) Input is BPZ data.

PIN ASSIGNMENTS

DSD1792
(TOP VIEW)

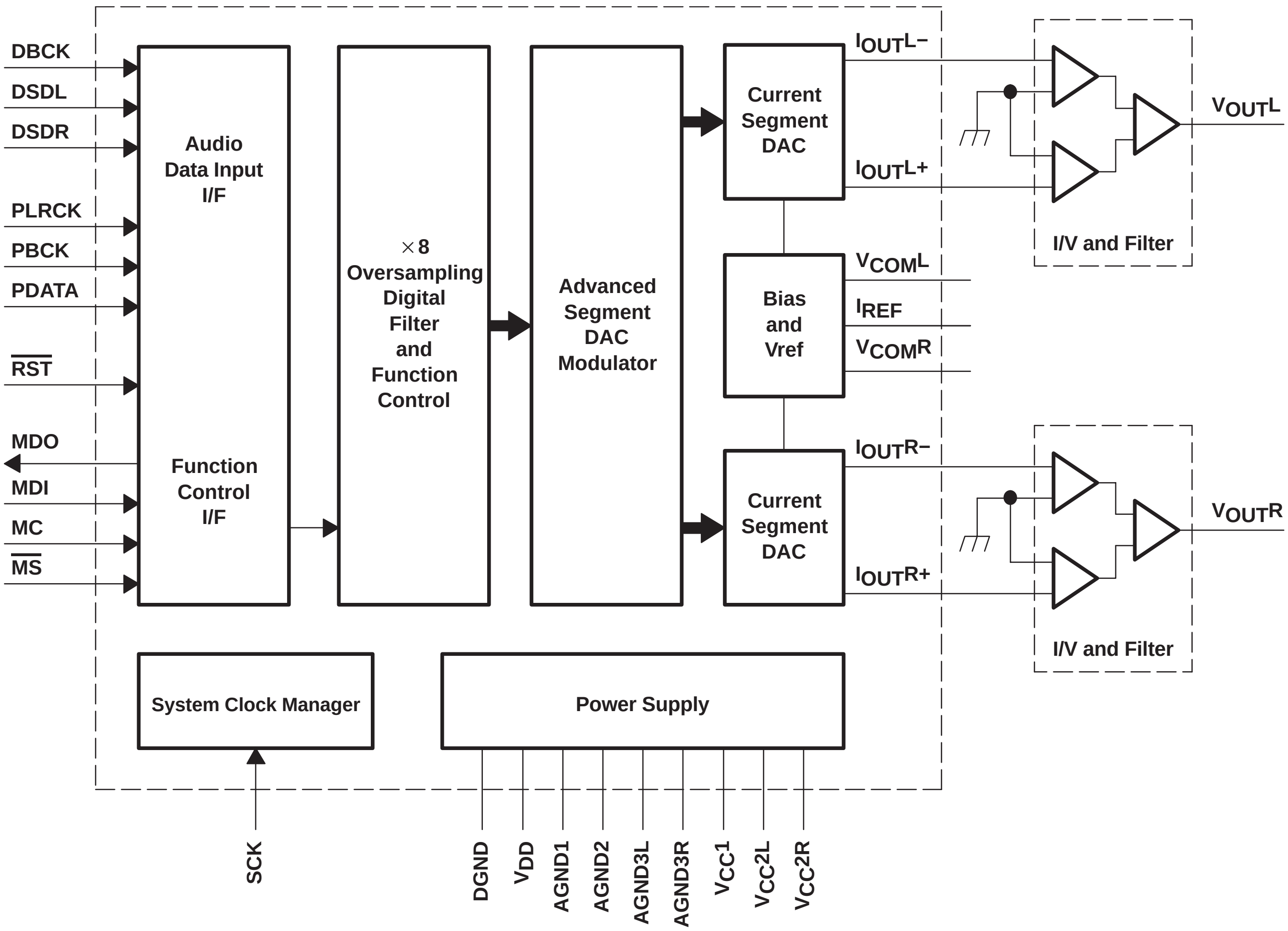


Terminal Functions

TERMINAL NAME	PIN	I/O	DESCRIPTIONS
AGND1	19	−	Analog ground (internal bias)
AGND2	24	−	Analog ground (internal bias)
AGND3L	27	−	Analog ground (L-channel DACFF)
AGND3R	16	−	Analog ground (R-channel DACFF)
DBCK	3	I	Bit clock input for DSD modes (1)
DGND	8	−	Digital ground
DSDL	1	I/O	L-channel audio data input when in DSD and external DF modes PCM-mode zero flag for L-channel when in zero-flag output mode(2)
DSDR	2	I/O	R-channel audio data input when in DSD and external DF modes PCM-mode zero flag for R−channel when in zero-flag output mode (2)
$I_{OUT}L+$	25	O	L-channel analog current output +
$I_{OUT}L–$	26	O	L-channel analog current output –
$I_{OUT}R+$	17	O	R-channel analog current output +
$I_{OUT}R–$	18	O	R-channel analog current output –
I_{REF}	20	−	Output current reference bias pin
MC	12	I	Mode control clock input(1)
MDI	11	I	Mode control data input (1)
MDO	13	O	Mode control readback data output (3)
$\overline{MS}$	10	I/O	Mode control chip-select input(2)
PBCK	6	I	Bit clock input. Connected to GND in DSD mode (1)
PDATA	5	I	Serial audio data input for PCM-format operation (1)
PLRCK	4	I	Left and right clock (f_S) input for PCM-format operation. WDCK clock input for external DF mode. Connected to GND for DSD mode (1)
$\overline{RST}$	14	I	Reset(1)
SCK	7	I	System clock input (1)
$V_{CC}1$	23	−	Analog power supply, 5 V
$V_{CC}2L$	28	−	Analog power supply (L-channel DACFF), 5 V
$V_{CC}2R$	15	−	Analog power supply (R-channel DACFF), 5 V
$V_{COM}L$	22	−	L-channel internal bias decoupling pin
$V_{COM}R$	21	−	R-channel internal bias decoupling pin
V_{DD}	9	−	Digital power supply, 3.3 V

(1) Schmitt-trigger input, 5-V tolerant
(2) Schmitt-trigger input and output. 5-V tolerant input, and CMOS output
(3) 3-state output

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE CURVES

DIGITAL FILTER

Digital Filter Response

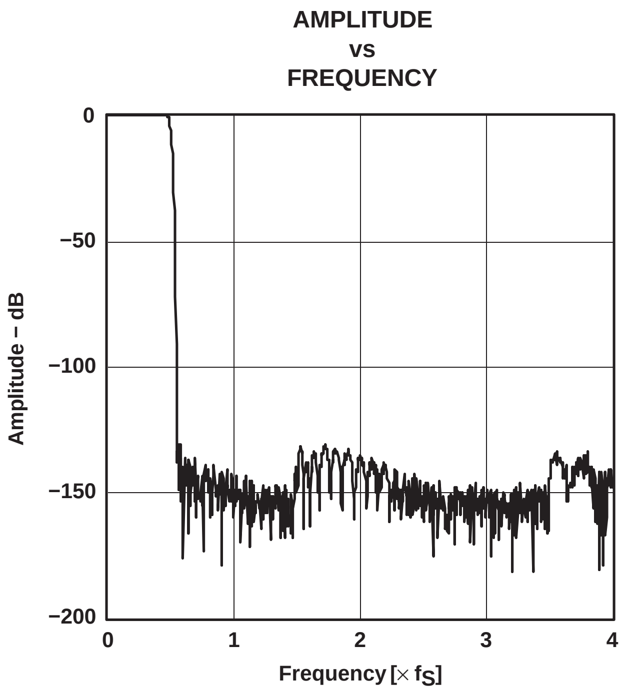


Figure 1. Frequency Response, Sharp Rolloff

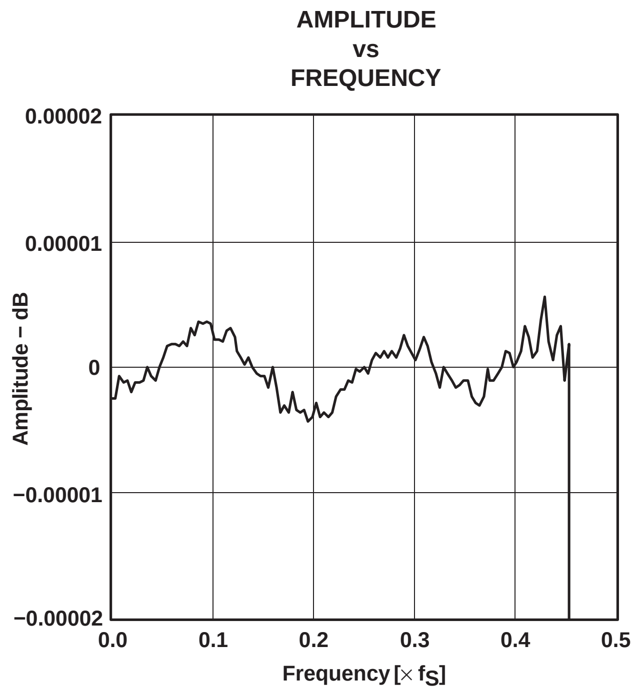


Figure 2. Pass-Band Ripple, Sharp Rolloff

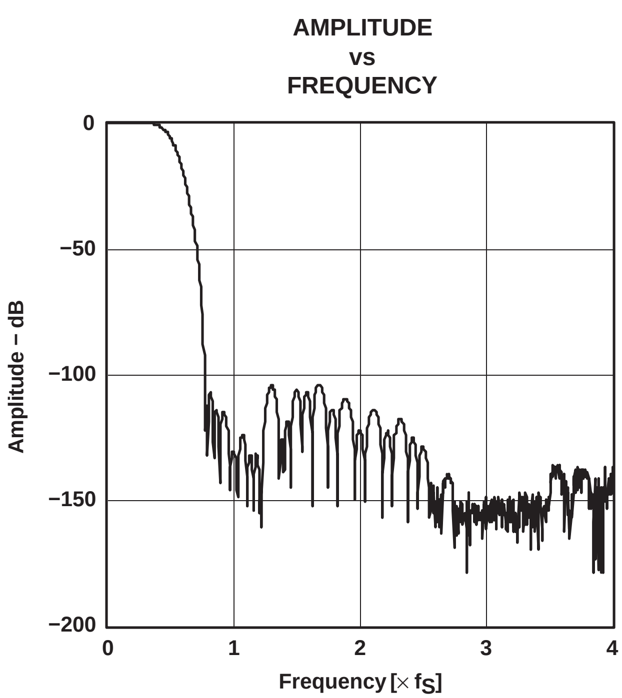


Figure 3. Frequency Response, Slow Rolloff

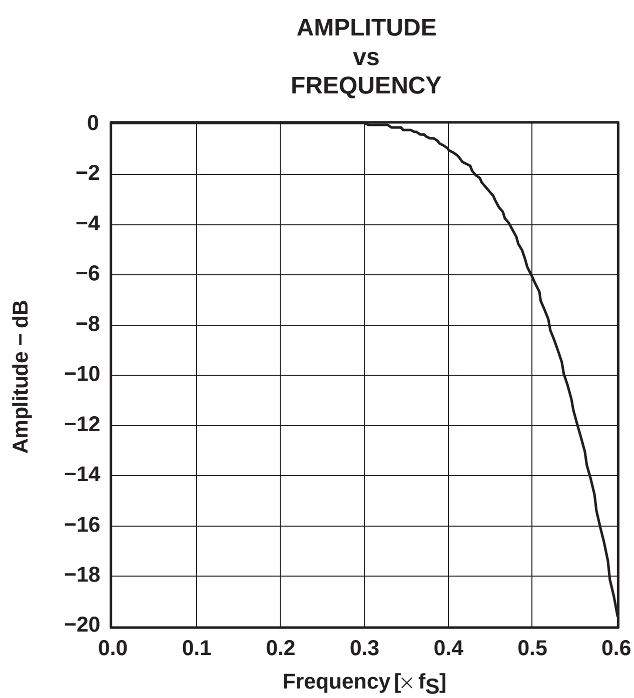


Figure 4. Transition Characteristics, Slow Rolloff

De-Emphasis Error

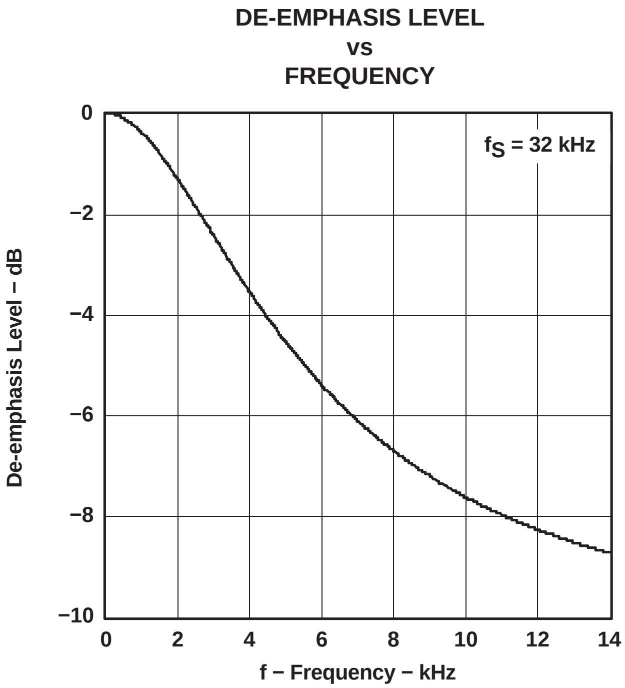


Figure 5

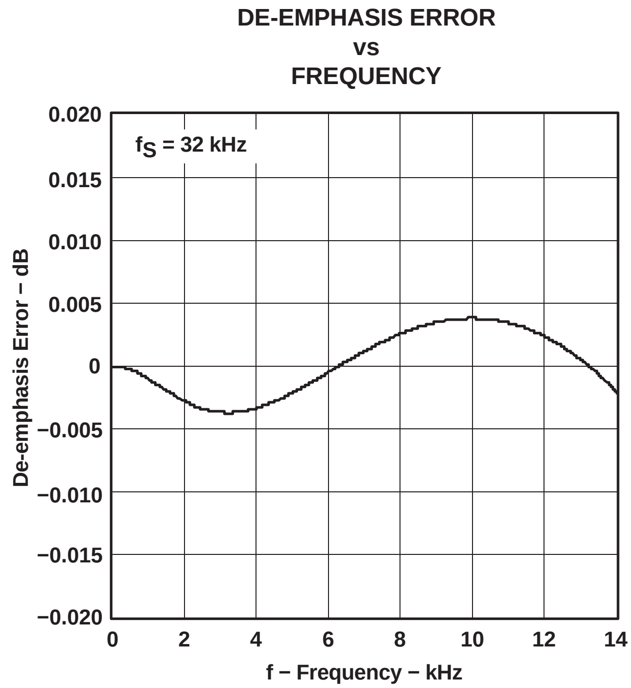


Figure 6

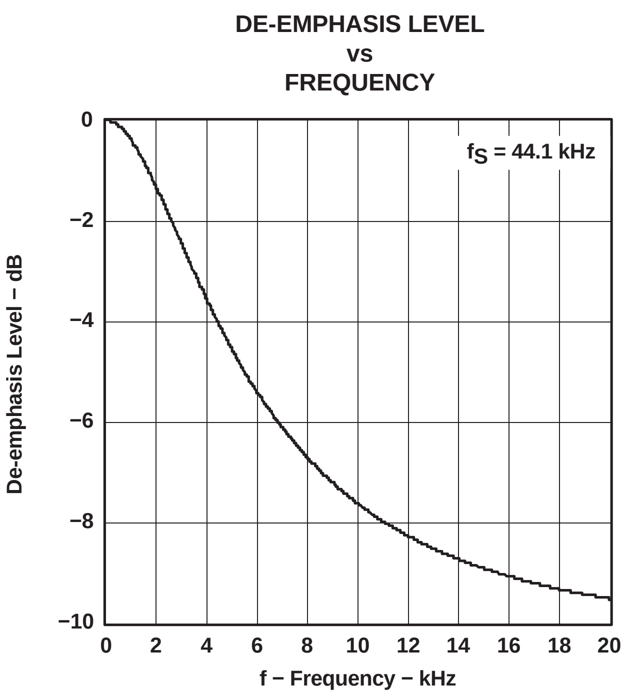


Figure 7

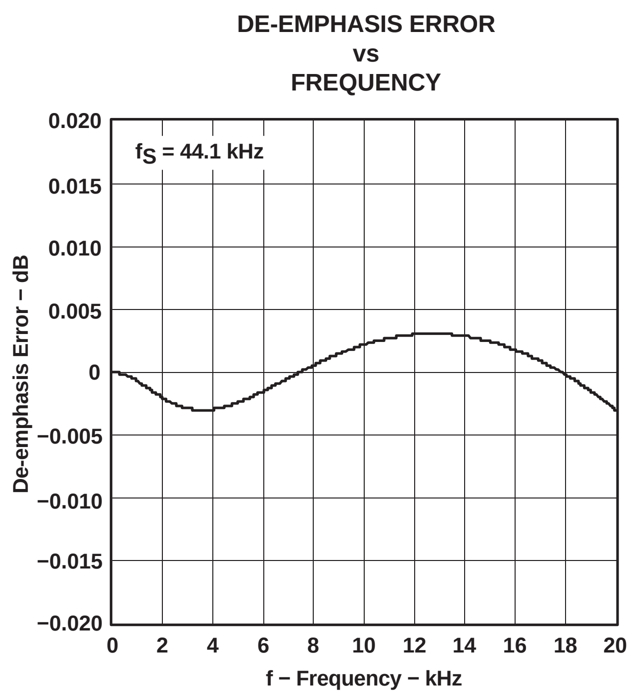


Figure 8

De-Emphasis Error (Continued)

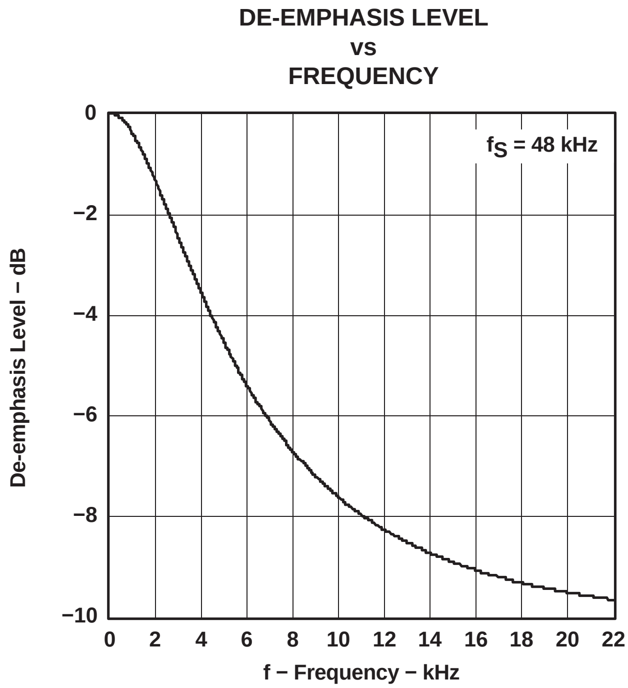


Figure 9

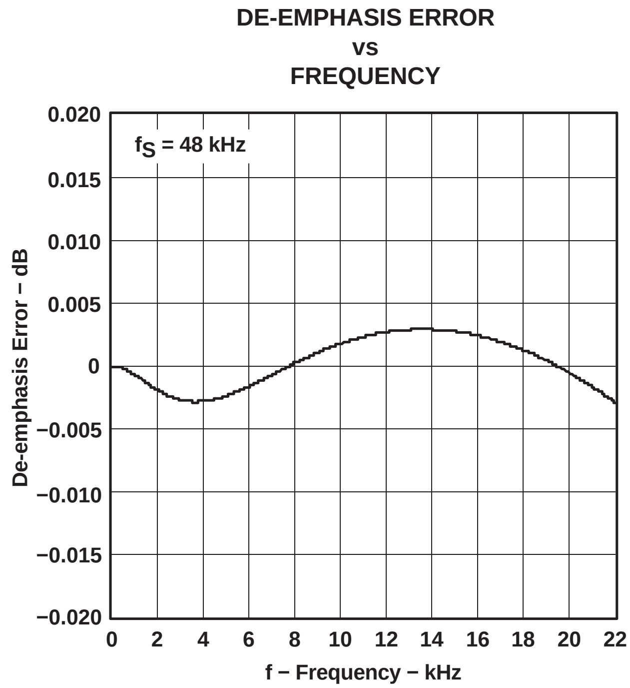


Figure 10

ANALOG DYNAMIC PERFORMANCE

Supply Voltage Characteristics

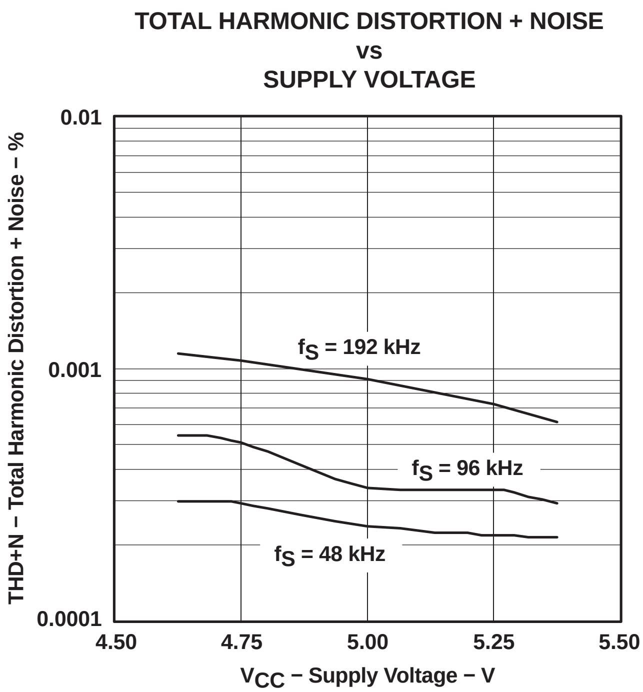


Figure 11

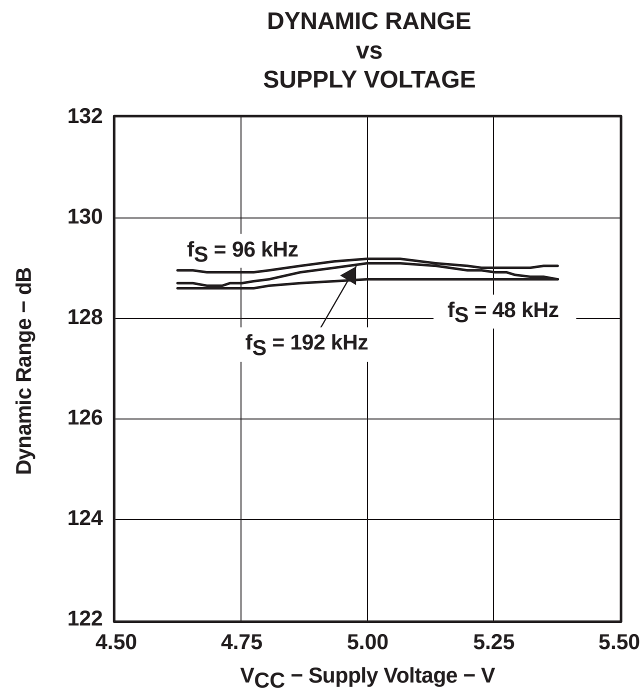


Figure 12

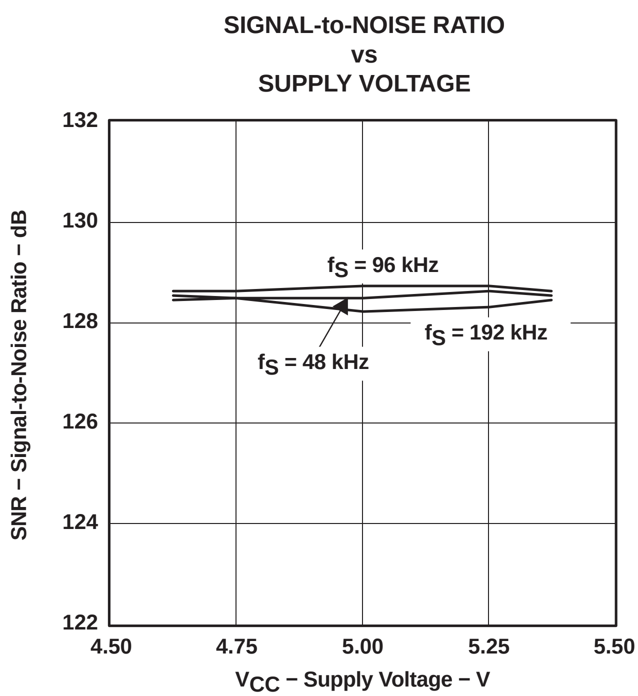


Figure 13

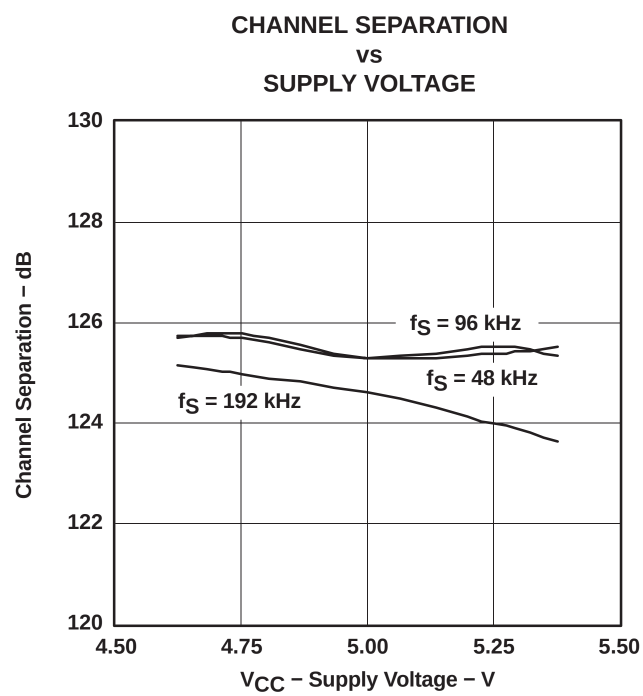


Figure 14

NOTE: PCM mode, T_A = 25°C, V_{DD} = 3.3 V, measurement circuit is Figure 34 (V_{OUT} = 4.5 V rms).

Temperature Characteristics

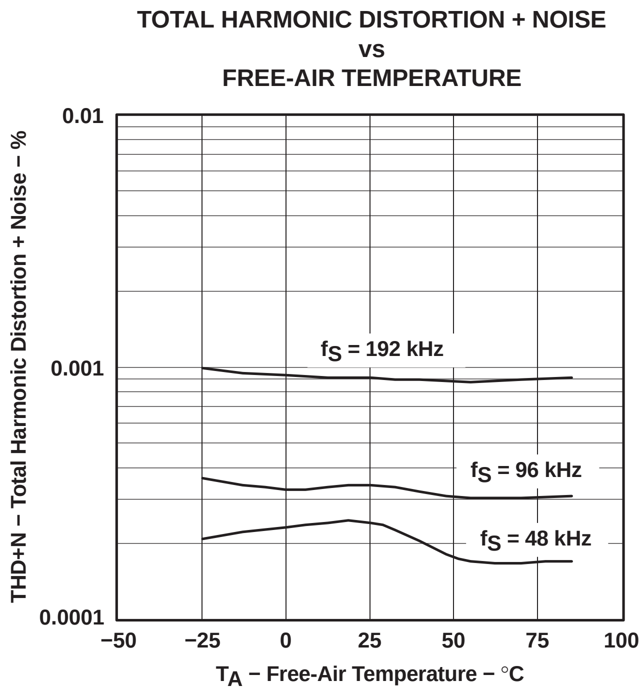


Figure 15

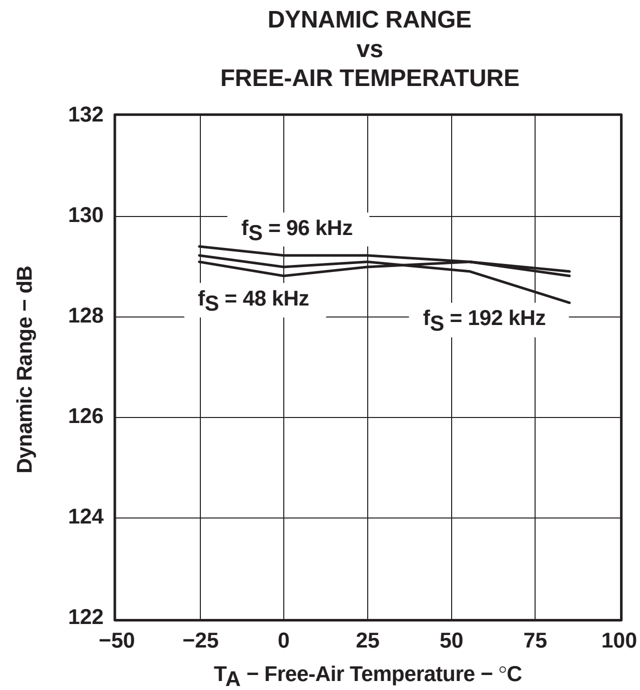


Figure 16

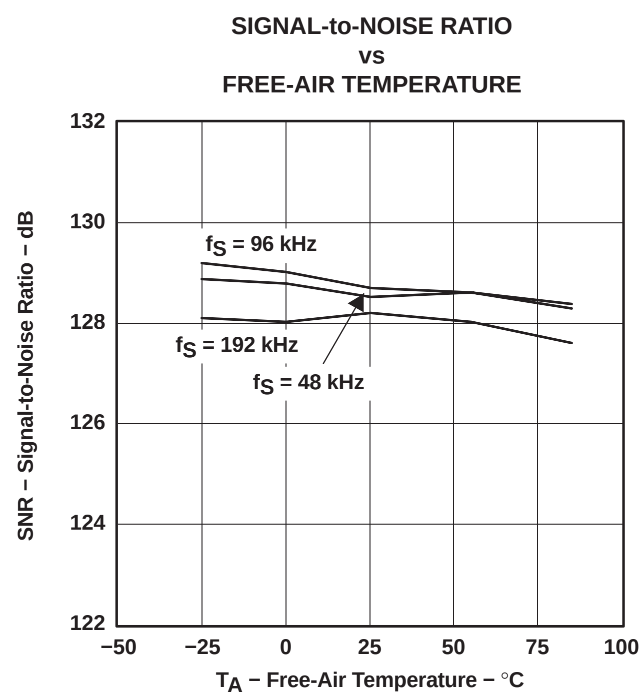


Figure 17

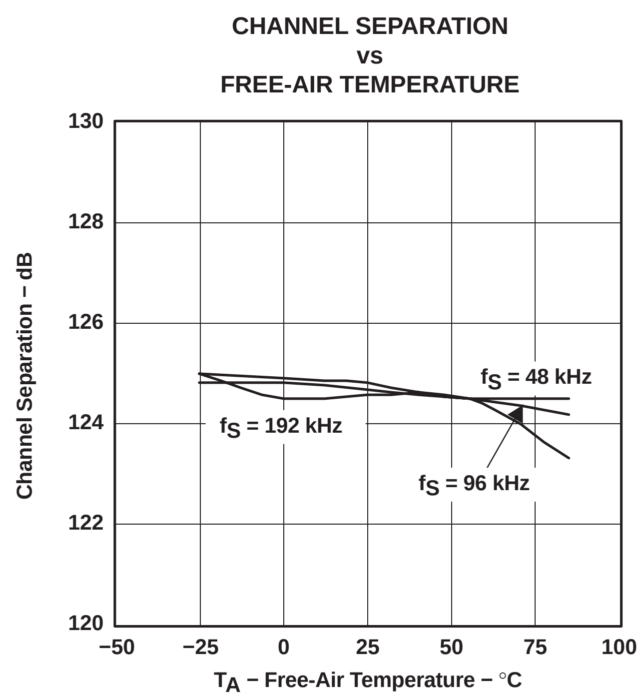


Figure 18

NOTE: PCM mode, V_{CC} = 5 V, V_{DD} = 3.3 V, measurement circuit is Figure 34 (V_{OUT} = 4.5 V rms).

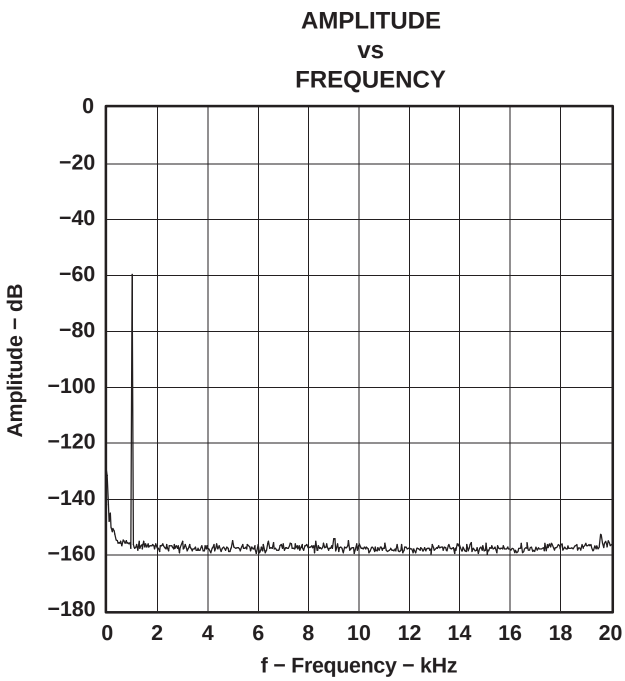


Figure 19. −60-db Output Spectrum, BW = 20 kHz

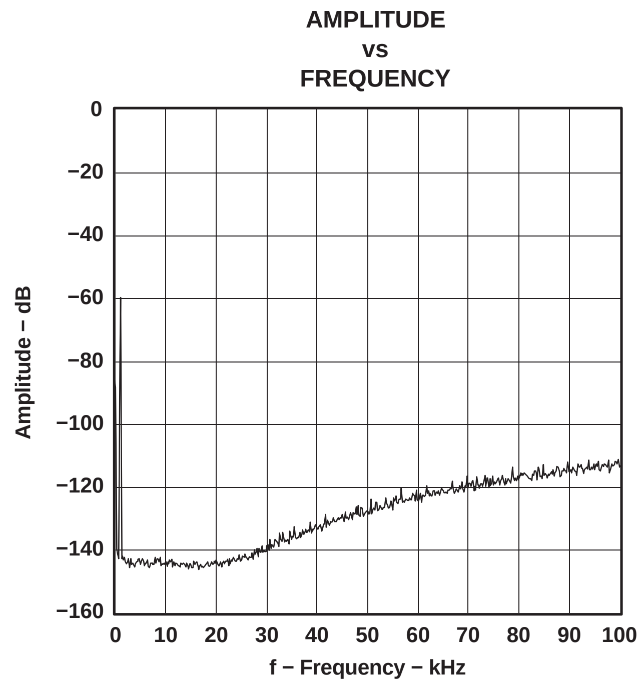


Figure 20. −60-db Output Spectrum, BW = 100 kHz

NOTE: PCM mode, f_S = 48 kHz, 32,768 point 8 average, T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 34.

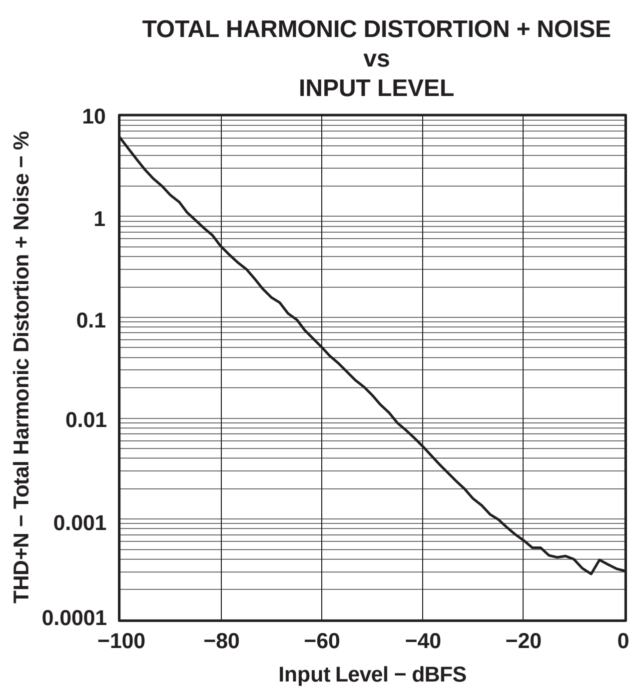


Figure 21. THD+N vs Input Level, PCM Mode

NOTE: PCM mode, f_S = 48 kHz, T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 34.

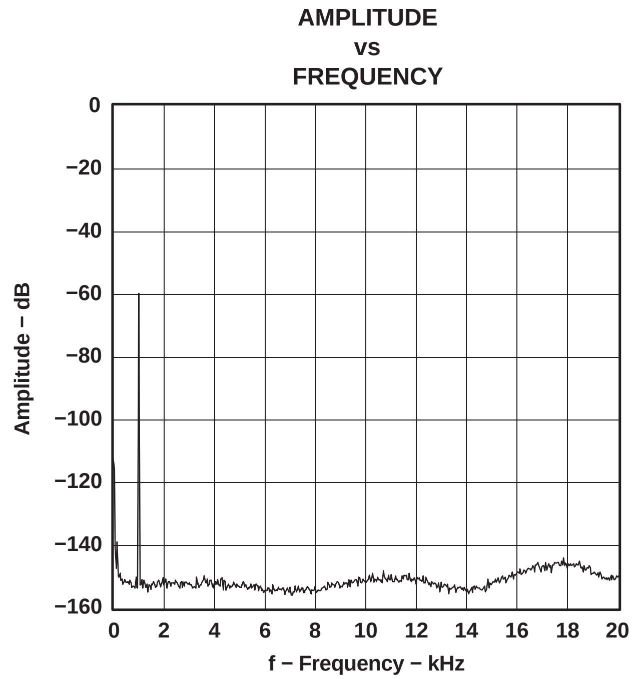


Figure 22. −60-dB Output Spectrum, DSD Mode

NOTE: DSD mode (FIR-4), 32,768 point 8 average, T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 35.

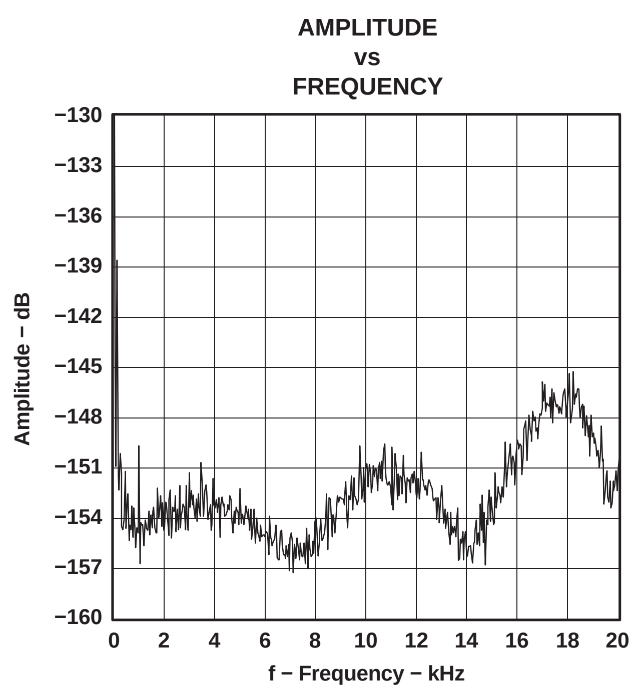


Figure 23. −150-dB Output Spectrum, DSD Mono Mode

NOTE: DSD mode (FIR-4), 32,768 point 8 average, T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, measurement circuit is Figure 35.

SYSTEM CLOCK AND RESET FUNCTIONS

System Clock Input

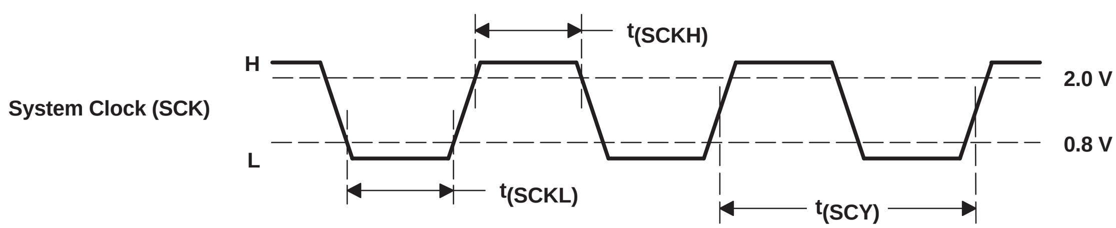
The DSD1792 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 7). The DSD1792 has a system clock detection circuit that automatically senses if the system clock is operating between 128 f_S and 768 f_S. Table 1 shows examples of system clock frequencies for common audio sampling rates. If the oversampling rate of the delta-sigma modulator is selected as 128 f_S, the system clock frequency is over 256 f_S.

Figure 24 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. One of the Texas Instruments' PLL1700 family of multiclock generators is an excellent choice for providing the DSD1792 system clock.

Table 1. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (F_{SCK}) (MHZ)					
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1 kHz	5.6488	8.4672	11.2896	16.9344	22.5792	33.8688
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864
96 kHz	12.288	18.432	24.576	36.864	49.152	73.728
192 kHz	24.576	36.864	49.152	73.728	(1)	(1)

(1) This system clock rate is not supported for the given sampling frequency.



PARAMETERS		MIN	MAX	UNITS
$t_{(SCY)}$	System clock pulse cycle time	13		ns
$t_{(SCKH)}$	System clock pulse duration, HIGH	$0.4t_{(SCY)}$		ns
$t_{(SCKL)}$	System clock pulse duration, LOW	$0.4t_{(SCY)}$		ns

Figure 24. System Clock Input Timing

Power-On and External Reset Functions

The DSD1792 includes a power-on reset function. Figure 25 shows the operation of this function. With V_{DD} > 2 V, the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time V_{DD} > 2 V. After the initialization period, the DSD1792 is set to its default reset state, as described in the *MODE CONTROL REGISTERS* section of this data sheet.

The DSD1792 also includes an external reset capability using the $\overline{RST}$ input (pin 14). This allows an external controller or master reset circuit to force the DSD1792 to initialize to its default reset state.

Figure 26 shows the external reset operation and timing. The $\overline{RST}$ pin is set to logic 0 for a minimum of 20 ns. The $\overline{RST}$ pin is then set to a logic 1 state, thus starting the initialization sequence, which requires 1024 system clock periods. Operation of the external reset is the same as that of the power-on reset. The external reset is especially useful in applications where there is a delay between the DSD1792 power up and system clock activation.

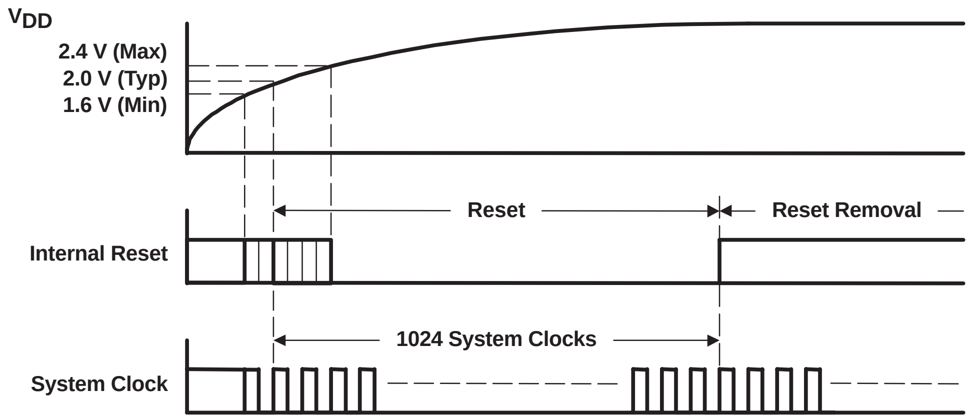
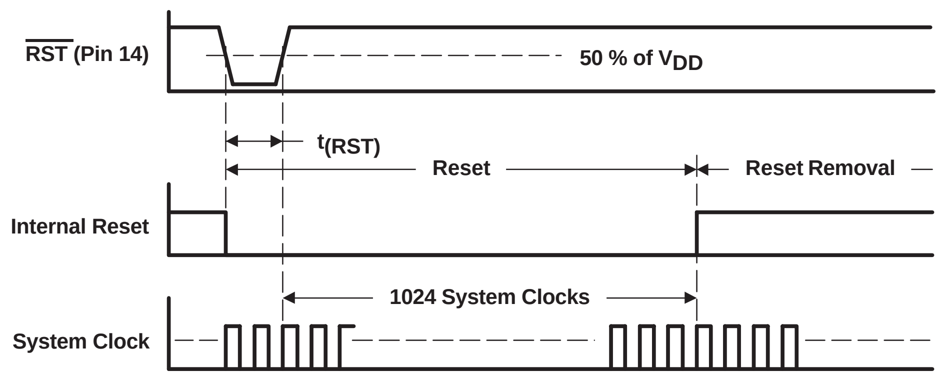


Figure 25. Power-On Reset Timing



PARAMETERS		MIN	MAX	UNITS
$t_{(RST)}$	Reset pulse duration, LOW	20		ns

Figure 26. External Reset Timing

AUDIO DATA INTERFACE

Audio Serial Interface

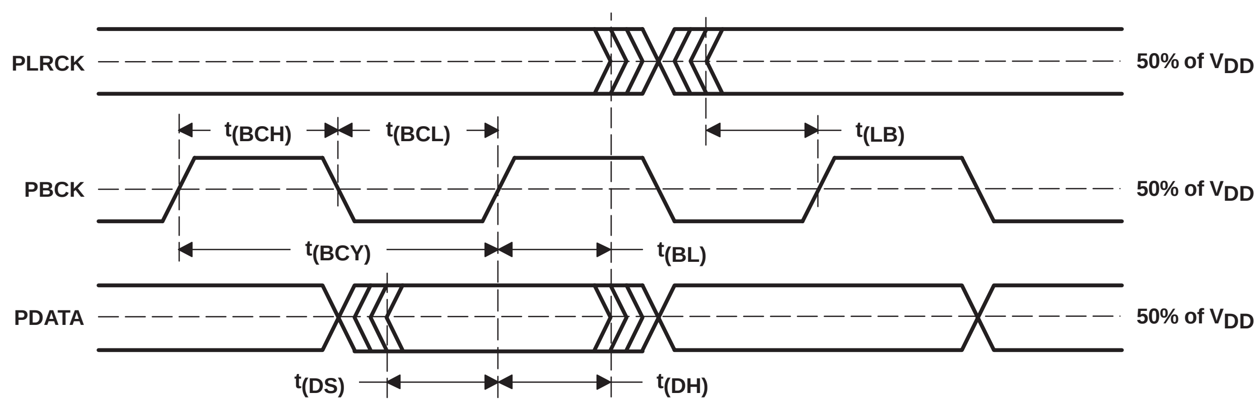
The audio interface port is a 3-wire serial port. It includes PLRCK (pin 4), PBCK (pin 6), and PDATA (pin 5). PBCK is the serial audio bit clock, and it is used to clock the serial data present on PDATA into the serial shift register of the audio interface. Serial data is clocked into the DSD1792 on the rising edge of PBCK. PLRCK is the serial audio left/right word clock.

The DSD1792 requires the synchronization of PLRCK and the system clock, but does not need a specific phase relation between PLRCK and the system clock.

If the relationship between PLRCK and the system clock changes more than ±6 PBCK, internal operation is initialized within $1/f_S$ and analog outputs are forced to the bipolar zero level until resynchronization between PLRCK and the system clock is completed.

PCM Audio Data Formats and Timing

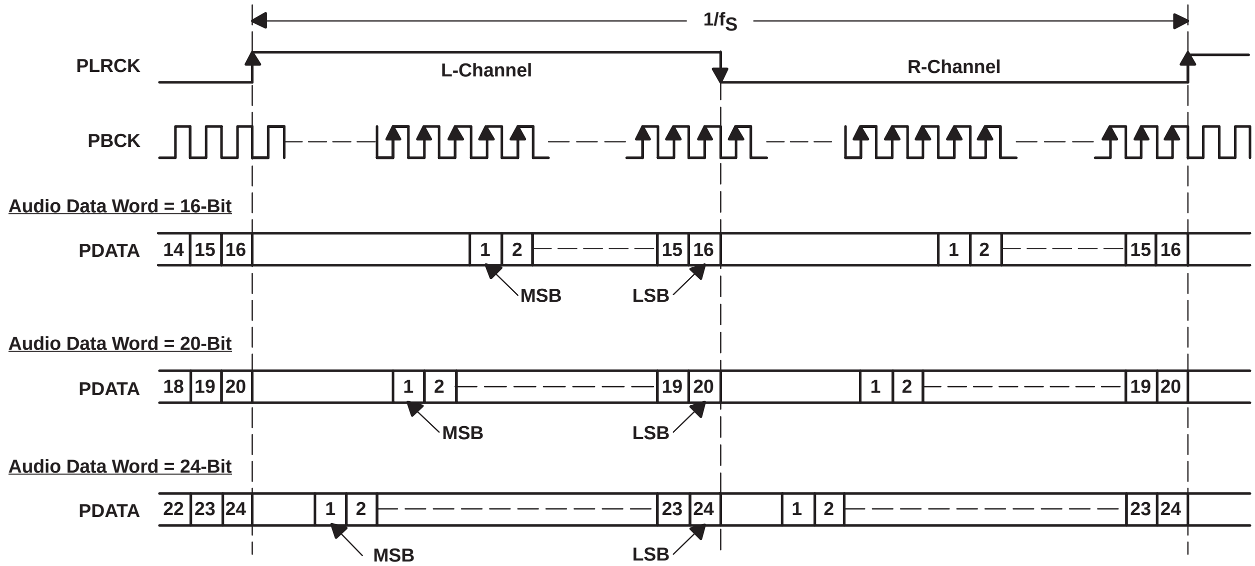
The DSD1792 supports industry-standard audio data formats, including standard right-justified, I^2S, and left-justified. The data formats are shown in Figure 28. Data formats are selected using the format bits, FMT[2:0], in control register 18. The default data format is 24-bit I^2S. All formats require binary 2s complement, MSB-first audio data. Figure 27 shows a detailed timing diagram for the serial audio interface.



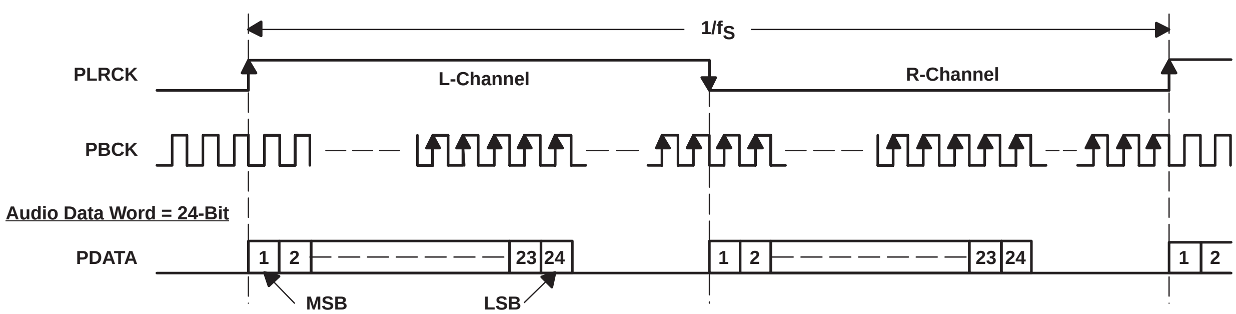
PARAMETERS		MIN	MAX	UNITS
$t_{(BCY)}$	PBCK pulse cycle time	70		ns
$t_{(BCL)}$	PBCK pulse duration, LOW	30		ns
$t_{(BCH)}$	PBCK pulse duration, HIGH	30		ns
$t_{(BL)}$	PBCK rising edge to PLRCK edge	10		ns
$t_{(LB)}$	PLRCK edge to PBCK rising edge	10		ns
$t_{(DS)}$	PDATA Setup time	10		ns
$t_{(DH)}$	PDATA hold time	10		ns
—	PLRCK clock data	50% ± 2 bit clocks		

Figure 27. Timing of Audio Interface

(1) Standard Data Format (Right Justified) ; L-Channel = HIGH, R-Channel = LOW



(2) Left Justified Data Format; L-Channel = HIGH, R-Channel = LOW



(3) I2S Data Format; L-Channel = LOW, R-Channel = HIGH

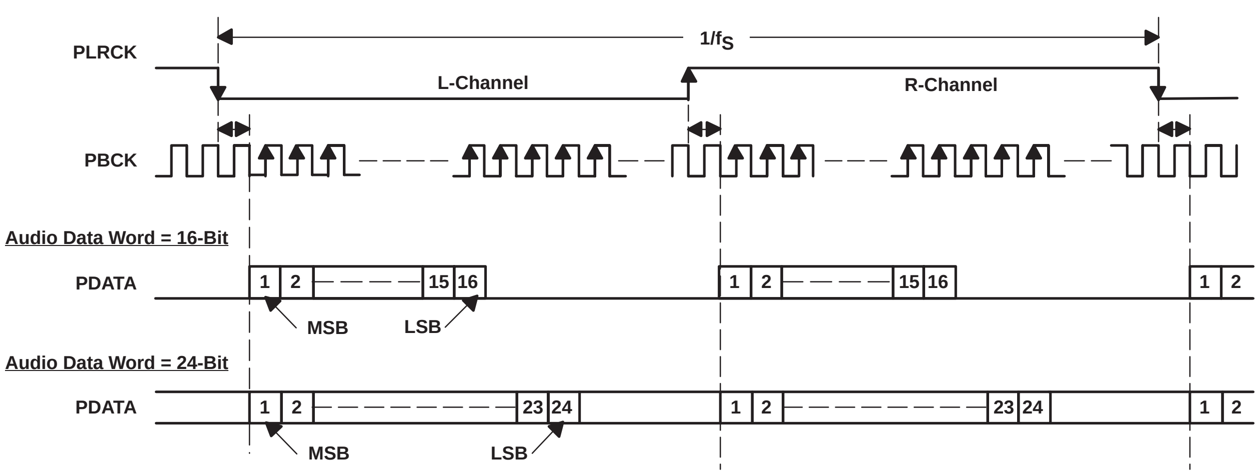


Figure 28. Audio Data Input Formats

External Digital Filter Interface and Timing

The DSD1792 supports an external digital filter interface comprising a 3- or 4-wire synchronous serial port, which allows the use of an external digital filter. External filters include the Texas Instruments' DF1704 and DF1706, the Pacific Microsonics PMD200, or a programmable digital signal processor.

In the external DF mode, PLRCK (pin 4), PBCK (pin 6) and PDATA (pin 5) are defined as WDCK, the word clock; BCK, the bit clock; and DATA, the monaural data, respectively. The external digital filter interface is selected by using the DFTH bit of control register 20, which functions to bypass the internal digital filter of the DSD1792.

When the DFMS bit of control register 19 is set, the DSD1792 can process stereo data. In this case, DSDL (pin 1) and DSDR (pin 2) are defined as L-channel data and R-channel data, respectively.

Detailed information for the external digital filter interface mode is provided in the *APPLICATION FOR EXTERNAL DIGITAL FILTER INTERFACE* section of this data sheet.

Direct Stream Digital (DSD) Format Interface and Timing

The DSD1792 supports the DSD-format interface operation, which includes out-of-band noise filtering using an internal analog FIR filter. The DSD-format interface consists of a 3-wire synchronous serial port, which includes DBCK (pin 3), DSDL (pin 1), and DSDR (pin 2). DBCK is the serial bit clock. DSDL and DSDR are L-channel and R-channel DSD data input, respectively. They are clocked into the DSD1792 on the rising edge of DBCK. PLRCK (pin 4) and PBCK (pin 6) should be connected to GND in the DSD mode. The DSD-(DSD mode) format interface is activated by setting the DSD bit of control register 20.

Detailed information for the DSD mode is provided in the *APPLICATION FOR DSD FORMAT (DSD MODE) INTERFACE* section of this data sheet.

TDMCA Interface

The DSD1792 supports the time-division-multiplexed command and audio (TDMCA) data format to enable control of and communication with a number of external devices over a single serial interface.

Detailed information for the TDMCA format is provided in the *TDMCA Format* section of this data sheet.

Serial Control Interface

The serial control interface is a 4-wire synchronous serial port, which operates asynchronously with the serial audio interface and the system clock (SCK). The serial control interface is used to program and read the on-chip mode registers. The control interface includes MDO (pin 13), MDI (pin 11), MC (pin 12), and $\overline{MS}$ (pin 10). MDO is the serial data output, used to read back the values of the mode registers; MDI is the serial data input, used to program the mode registers; MC is the bit clock, used to shift data in and out of the control port, and $\overline{MS}$ is the mode control enable, used to enable the internal mode register access.

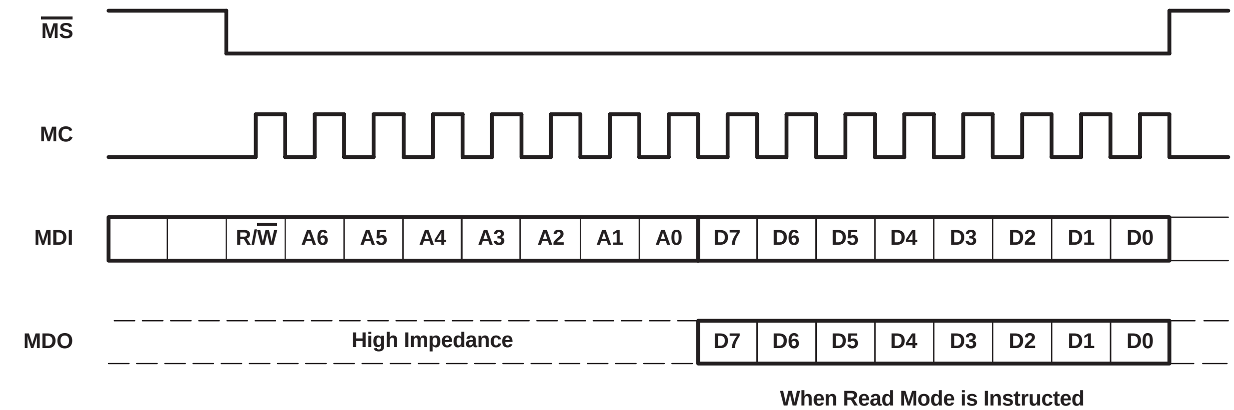
Register Read/Write Operation

All read/write operations for the serial control port use 16-bit data words. Figure 29 shows the control data word format. The most significant bit is the read/write (R/$\overline{W}$) bit. For write operations, the R/$\overline{W}$ bit must be set to 0. For read operations, the R/$\overline{W}$ bit must be set to 1. There are seven bits, labeled IDX[6:0], that set the register index (or address) for the read and write operations. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0] or to be read from, the register specified by IDX[6:0].

Figure 30 shows the functional timing diagram for writing or reading the serial control port. $\overline{MS}$ is held at a logic 1 state until a register needs to be written or read. To start the register write or read cycle, $\overline{MS}$ is set to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MDI and readback data on MDO. After the eighth clock cycle has completed, the data from the indexed-mode control register appears on MDO during the read operation. After the sixteenth clock cycle has completed, the data is latched into the indexed-mode control register during the write operation. To write or read subsequent data, $\overline{MS}$ must be set to 1 once.

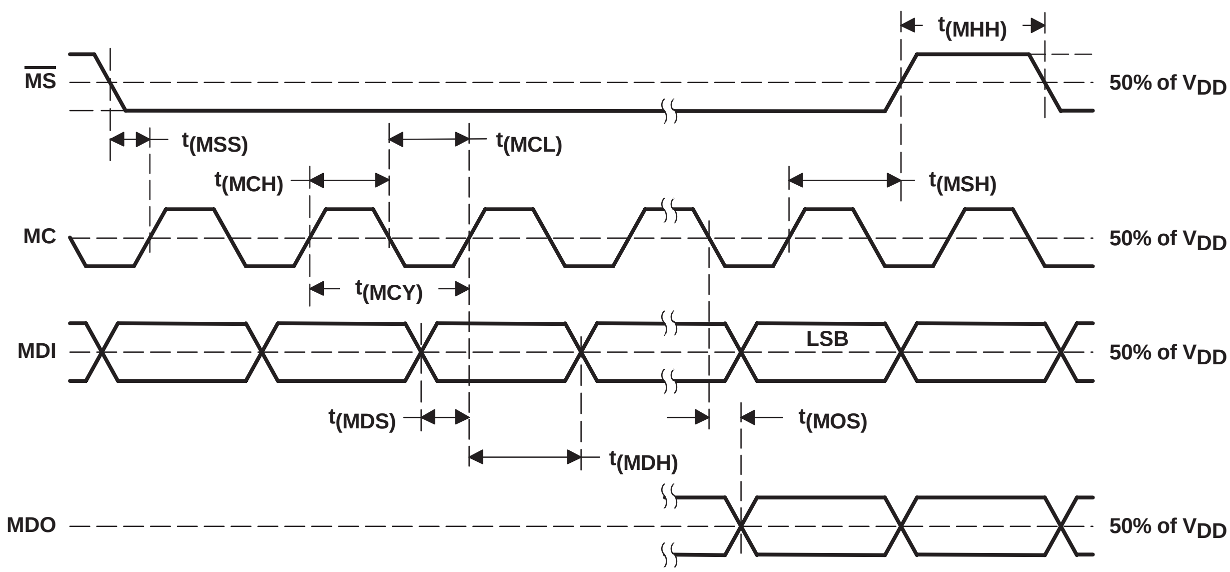
MSB															LSB
R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	D7	D6	D5	D4	D3	D2	D1	D0
Register Index (or Address)								Register Data							

Figure 29. Control Data Word Format for MDI



NOTE: Bit 15 is used for selection of write or read. Setting R/$\overline{\text{W}}$ = 0 indicates a write, while R/$\overline{\text{W}}$ = 1 indicates a read. Bits 14−8 are used for the register address. Bits 7–0 are used for register data.

Figure 30. Serial Control Format



PARAMETER		MIN	MAX	UNITS
$t_{(MCY)}$	MC pulse cycle time	100		ns
$t_{(MCL)}$	MC low-level time	40		ns
$t_{(MCH)}$	MC high-level time	40		ns
$t_{(MHH)}$	$\overline{\text{MS}}$ high-level time	80		ns
$t_{(MSS)}$	$\overline{\text{MS}}$ falling edge to MC rising edge	15		ns
$t_{(MSH)}$	$\overline{\text{MS}}$ hold time(1)	15		ns
$t_{(MDH)}$	MDI hold time	15		ns
$t_{(MDS)}$	MDI setup time	15		ns
$t_{(MOS)}$	MC falling edge to MDO stable		30	ns

(1) MC rising edge for LSB to $\overline{\text{MS}}$ rising edge

Figure 31. Control Interface Timing

MODE CONTROL REGISTERS

User-Programmable Mode Controls

The DSD1792 includes a number of user-programmable functions which are accessed via mode control registers. The registers are programmed using the serial control interface, which was previously discussed in this data sheet. Table 2 lists the available mode-control functions, along with their default reset conditions and associated register index.

Table 2. User-Programmable Function Controls

FUNCTION	DEFAULT	REGISTER	BIT	PCM	DSD	DF BYPASS
Digital attenuation control 0 dB to –120 dB and mute, 0.5 dB step	0 dB	Register 16 Register 17	ATL[7:0] (for L-ch) ATR[7:0] (for R-ch)	yes		
Attenuation load control—Disabled, enabled	Attenuation disabled	Register 18	ATLD	yes		
Input audio data format selection 16-, 20-, 24-bit standard (right-justified) format 24-bit MSB-first left-justified format 16-/24-bit I^2S format	24-bit I^2S format	Register 18	FMT[2:0]	yes		yes
Sampling rate selection for de-emphasis Disabled,44.1 kHz, 48 kHz, 32 kHz	De-emphasis disabled	Register 18	DMF[1:0]	yes	yes(1)	
De-emphasis control—Disabled, enabled	De-emphasis disabled	Register 18	DME	yes		
Soft mute control—Mute disabled, enabled	Mute disabled	Register 18	MUTE	yes		
Output phase reversal—Normal, reverse	Normal	Register 19	REV	yes	yes	yes
Attenuation speed selection $\times 1\ f_S$, $\times(1/2)f_S$, $\times(1/4)f_S$, $\times(1/8)f_S$	$\times 1\ f_S$	Register 19	ATS[1:0]	yes		
DAC operation control—Enabled, disabled	DAC operation enabled	Register 19	OPE	yes	yes	yes
Zero flag pin operation control DSD data input, zero flag output	DSD data input	Register 19	ZOE	yes		yes
Stereo DF bypass mode select Monaural, stereo	Monaural	Register 19	DFMS			yes
Digital filter rolloff selection Sharp rolloff, slow rolloff	Sharp rolloff	Register 19	FLT	yes		
Infinite zero mute control Disabled, enabled	Disabled	Register 19	INZD	yes		yes
System reset control Reset operation , normal operation	Normal operation	Register 20	SRST	yes	yes	yes
DSD interface mode control DSD enabled, disabled	Disabled	Register 20	DSD		yes	
Digital-filter bypass control DF enabled, DF bypass	DF enabled	Register 20	DFTH			yes
Monaural mode selection Stereo, monaural	Stereo	Register 20	MONO	yes	yes	yes
Channel selection for monaural mode data L-channel, R-channel	L-channel	Register 20	CHSL	yes	yes	yes
Delta-sigma oversampling rate selection $\times 64\ f_S$, $\times 128\ f_S$, $\times 32\ f_S$	$\times 64\ f_S$	Register 20	OS[1:0]	yes	yes(2)	yes
PCM zero output enable	Enabled	Register 21	PCMZ	yes		yes
DSD zero output enable	Disabled	Register 21	DZ[1:0]		yes	
Function available only for read						
Zero detection flag Not zero, zero detected	Not zero = 0 Zero detected = 1	Register 22	ZFGL (for L-ch) ZFGR (for R-ch)	yes	yes	yes
Device ID (at TDMCA)	−	Register 23	ID[4:0]	yes	yes	

(1) When in DSD mode, DMF[0:1] is defined as DSD filter (analog FIR) performance selection.
(2) When in DSD mode, OS[0:1] is defined as DSD filter (analog FIR) operation rate selection.

Register Map

The mode control register map is shown in Table 3. Registers 16–21 include an R/$\overline{W}$ bit, which determines whether a register read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation is performed. Registers 22 and 23 are read-only.

Table 3. Mode Control Register Map

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	R/$\overline{W}$	0	0	1	0	0	0	0	ATL7	ATL6	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 17	R/$\overline{W}$	0	0	1	0	0	0	1	ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0
Register 18	R/$\overline{W}$	0	0	1	0	0	1	0	ATLD	FMT2	FMT1	FMT0	DMF1	DMF0	DME	MUTE
Register 19	R/$\overline{W}$	0	0	1	0	0	1	1	REV	ATS1	ATS0	OPE	ZOE	DFMS	FLT	INZD
Register 20	R/$\overline{W}$	0	0	1	0	1	0	0	RSV	SRST	DSD	DFTH	MONO	CHSL	OS1	OS0
Register 21	R/$\overline{W}$	0	0	1	0	1	0	1	RSV	RSV	RSV	RSV	RSV	DZ1	DZ0	PCMZ
Register 22	R	0	0	1	0	1	1	0	RSV	RSV	RSV	RSV	RSV	RSV	ZFGR	ZFGL
Register 23	R	0	0	1	0	1	1	1	RSV	RSV	RSV	ID4	ID3	ID2	ID1	ID0

Register Definitions

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	R/$\overline{W}$	0	0	1	0	0	0	0	ATL7	ATL6	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 17	R/$\overline{W}$	0	0	1	0	0	0	1	ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

R/$\overline{W}$: Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

ATx[7:0]: Digital Attenuation Level Setting

These bits are available for read and write.

Default value: 1111 1111b

Each DAC output has a digital attenuator associated with it. The attenuator can be set from 0 dB to –120 dB, in 0.5-dB steps. Alternatively, the attenuator can be set to infinite attenuation (or mute).

The attenuation data for each channel can be set individually. However, the data load control (the ATLD bit of control register 18) is common to both attenuators. ATLD must be set to 1 in order to change an attenuator setting. The attenuation level can be set using the following formula:

$$\text{Attenuation level (dB)} = 0.5\text{ dB} \bullet (ATx[7:0]_{DEC} - 255)$$

where $ATx[7:0]_{DEC}$ = 0 through 255

For $ATx[7:0]_{DEC}$ = 0 through 14, the attenuator is set to infinite attenuation. The following table shows attenuation levels for various settings:

ATx[7:0]	Decimal Value	Attenuation Level Setting
1111 1111b	255	0 dB, no attenuation (default)
1111 1110b	254	–0.5 dB
1111 1101b	253	–1.0 dB
⋮	⋮	⋮
0001 0000b	16	–119.5 dB
0000 1111b	15	–120.0 dB
0000 1110b	14	Mute
⋮	⋮	⋮
0000 0000b	0	Mute

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 18	R/$\overline{W}$	0	0	1	0	0	1	0	ATLD	FMT2	FMT1	FMT0	DMF1	DMF0	DME	MUTE

R/$\overline{W}$: Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

ATLD: Attenuation Load Control

This bit is available for read and write.

Default value: 0

ATLD = 0	Attenuation control disabled (default)
ATLD = 1	Attenuation control enabled

The ATLD bit is used to enable loading of the attenuation data contained in registers 16 and 17. When ATLD = 0, the attenuation settings remain at the previously programmed levels, ignoring new data loaded from registers 16 and 17. When ATLD = 1, attenuation data written to registers 16 and 17 is loaded normally.

FMT[2:0]: Audio Interface Data Format

These bits are available for read and write.

Default value: 101

For the external digital filter interface mode (DFTH mode), this register is operated as shown in the *Application for Interfacing With an External Digital Filter* section of this data sheet.

FMT[2:0]	Audio Data Format Selection
000	16-bit standard format, right-justified data
001	20-bit standard format, right-justified data
010	24-bit standard format, right-justified data
011	24-bit MSB-first, left-justified data
100	16-bit I^2S-format data
101	24-bit I^2S-format data (default)
110	Reserved
111	Reserved

The FMT[2:0] bits are used to select the data format for the serial audio interface.

DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function

These bits are available for read and write.

Default value: 00

DMF[1:0]	De-Emphasis Sampling Frequency Selection
00	Disabled (default)
01	48 kHz
10	44.1 kHz
11	32 kHz

The DMF[1:0] bits are used to select the sampling frequency used by the digital de-emphasis function when it is enabled by setting the DME bit. The de-emphasis curves are shown in the *TYPICAL PERFORMANCE CURVES* section of this data sheet.

For the DSD mode, analog FIR filter performance can be selected using this register. Filter response plots are shown in the *TYPICAL PERFORMANCE CURVES* section of this data sheet. A register map is shown in the *Configuration for the DSD Interface Mode* section of this data sheet.

DME: Digital De-Emphasis Control

This bit is available for read and write.

Default value: 0

DME = 0	De-emphasis disabled (default)
DME = 1	De-emphasis enabled

The DME bit is used to enable or disable the de-emphasis function for both channels.

MUTE: Soft Mute Control

This bit is available for read and write.

Default value: 0

MUTE = 0	MUTE disabled (default)
MUTE = 1	MUTE enabled

The MUTE bit is used to enable or disable the soft mute function for both channels.

Soft mute is operated as a 256-step attenuator. The speed for each step to $-\infty$ dB (mute) is determined by the attenuation rate selected in the ATS register.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 19	R/$\overline{W}$	0	0	1	0	0	1	1	REV	ATS1	ATS0	OPE	ZOE	DFMS	FLT	INZD

R/$\overline{W}$: Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

REV: Output Phase Reversal

This bit is available for read and write.

Default value: 0

REV = 0	Normal output (default)
REV = 1	Inverted output

The REV bit is used to invert the output phase for both channels.

ATS[1:0]: Attenuation Rate Select

These bits are available for read and write.

Default value: 00

ATS[1:0]	Attenuation Rate Selection
00	PLRCK/2 (default)
01	PLRCK/4
10	PLRCK/8
11	PLRCK/16

The ATS[1:0] bits are used to select the rate at which the attenuator is decremented/incremented during level transitions.

OPE: DAC Operation Control

This bit is available for read and write.

Default value: 0

OPE = 0	DAC operation enabled (default)
OPE = 1	DAC operation disabled

The OPE bit is used to enable or disable the analog output for both channels. Disabling the analog outputs forces them to the bipolar zero level (BPZ) even if digital audio data is present on the input.

ZOE: Zero Flag Pin Operation Control

This bit is available for read and write.

Default value: 0

ZOE = 0	DSD data input (default)
ZOE = 1	Zero flag output

The ZOE bit is used to change the DSDL (pin 1) and DSDR (pin 2) pin assignments. When the ZOE bit is set to 0, DSDL and DSDR are inputs for L-channel and R-channel data. When the ZOE bit is set to 1, DSDL and DSDR become outputs for the L-channel and R-channel zero flags, respectively. See the PCMZ and DZ[1:0] bit descriptions of register 21.

DFMS: Stereo DF Bypass Mode Select

This bit is available for read and write.

Default value: 0

DFMS = 0	Monaural (default)
DFMS = 1	Stereo input enabled

The DFMS bit is used to enable stereo operation in DF bypass mode. In the DF bypass mode, when DFMS is set to 0, the pin for the input data is PDATA (pin 5) only, therefore the DSD1792 operates as a monaural DAC. When DFMS is set to 1, the DSD1792 can operate as a stereo DAC with inputs of input L-channel and R-channel data on DSDL (pin 1) and DSDR (pin 2), respectively.

FLT: Digital Filter Rolloff Control

This bit is available for read and write.

Default value: 0

FLT = 0	Sharp rolloff (default)
FLT = 1	Slow rolloff

The FLT bit is used to select the digital filter rolloff characteristic. The filter responses for these selections are shown in the *TYPICAL PERFORMANCE CURVES* section of this data sheet.

INZD: Infinite Zero Detect Mute Control

This bit is available for read and write.

Default value: 0

INZD = 0	Infinite zero detect mute disabled (default)
INZD = 1	Infinite zero detect mute enabled

The INZD bit is used to enable or disable the zero detect mute function. Setting INZD to 1 forces muted analog outputs to hold a bipolar zero level when the DSD1792 detects zero data in both channels continuously for 1024 sampling periods ($1/f_S$). The infinite zero detect mute function is not available in the DSD mode.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 20	R/$\overline{W}$	0	0	1	0	1	0	0	RSV	SRST	DSD	DFTH	MONO	CHSL	OS1	OS0

R/$\overline{W}$: Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

SRST: System Reset Control

This bit is available for write only.

Default value: 0

SRST = 0	Normal operation (default)
SRST = 1	System reset operation (generate one reset pulse)

The SRST bit is used to reset the DSD1792 to the initial system condition.

DSD: DSD Interface Mode Control

This bit is available for read and write.

Default value: 0

DSD = 0	DSD interface mode disabled (default)
DSD = 1	DSD interface mode enabled

The DSD bit is used to enable or disable the DSD interface mode.

DFTH: Digital Filter Bypass (or Through Mode) Control

This bit is available for read and write.

Default value: 0

DFTH = 0	Digital filter enabled (default)
DFTH = 1	Digital filter bypassed for external digital filter

The DFTH bit is used to enable or disable the external digital filter interface mode.

MONO: Monaural Mode Selection

This bit is available for read and write.

Default value: 0

MONO = 0	Stereo mode (default)
MONO = 1	Monaural mode

The MONO function is used to change the operation mode from the normal stereo mode to the monaural mode. When the monaural mode is selected, both DACs operate in a balanced mode for one channel of audio input data. Channel selection is available for L-channel or R-channel data, determined by the CHSL bit as described immediately following.

CHSL: Channel Selection for Monaural Mode

This bit is available for read and write.

Default value: 0

This bit is available when MONO = 1.

CHSL = 0	L-channel selected (default)
CHSL = 1	R-channel selected

The CHSL bit selects L-channel or R-channel data to be used in monaural mode.

OS[1:0]: Delta-Sigma Oversampling Rate Selection

These bits are available for read and write.

Default value: 00

OS[1:0]	Operation Speed Select
00	64 times f_S (default)
01	32 times f_S
10	128 times f_S
11	Reserved

The OS bits are used to change the oversampling rate of delta-sigma modulation. Use of this function enables the designer to stabilize the conditions at the post low-pass filter for different sampling rates. As an application example, programming to set 128 times in 44.1-kHz operation, 64 times in 96-kHz operation, and 32 times in 192-kHz operation allows the use of only a single type (cutoff frequency) of post low-pass filter. The 128 f_S oversampling rate is not available at sampling rates above 100 kHz. If the 128 f_S oversampling rate is selected, a system clock of more than 256 f_S is required.

In DSD mode, these bits are used to select the speed of the bit clock for DSD data coming into the analog FIR filter.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 21	$R/\overline{W}$	0	0	1	0	1	0	1	RSV	RSV	RSV	RSV	RSV	DZ1	DZ0	PCMZ

$R/\overline{W}$: Read/Write Mode Select

When $R/\overline{W}$ = 0, a write operation is performed.

When $R/\overline{W}$ = 1, a read operation is performed.

Default value: 0

DZ[1:0]: DSD Zero Output Enable

These bits are available for read and write.

Default value: 00

DZ[1:0]	Zero Output Enable
00	Disabled (default)
01	Even pattern detect
1x	96_H pattern detect

The DZ bits are used to enable or disable the output zero flags, and to select the zero pattern in the DSD mode. The DSD1792 sets zero flags when the 1 and 0 data are even in every 8 bits of DSD input data, or the DSD input data is 1001 0110 continuously for 200 ms.

PCMZ: PCM Zero Output Enable

These bits are available for read and write.

Default value: 1

PCMZ = 0	PCM zero output disabled
PCMZ = 1	PCM zero output enabled (default)

The PCMZ bit is used to enable or disable the output zero flags in the PCM mode and the external DF mode. The DSD1792 sets the zero flags when the input data is continuously zero for 1024 LRCKs in the PCM mode or 1024 × 8 WCKs in the external filter mode.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 22	R	0	0	1	0	1	1	0	RSV	RSV	RSV	RSV	RSV	RSV	ZFGR	ZFGL

R: Read Mode Select

Value is always 1, specifying the readback mode.

ZFGx: Zero-Detection Flag

Where x = L or R, corresponding to the DAC output channel. These bits are available only for readback.

Default value: 00

ZFGx = 0	Not zero
ZFGx = 1	Zero detected

When the DSD1792 detects that audio input data is continuously zero, the ZFGx bit is set to 1 for the corresponding channel(s).

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 23	R	0	0	1	0	1	1	1	RSV	RSV	RSV	ID4	ID3	ID2	ID1	ID0

R: Read Mode Select

Value is always 1, specifying the readback mode.

ID[4:0]: Device ID

The ID[4:0] bits show a device ID in the TDMCA mode.

TYPICAL CONNECTION DIAGRAM IN PCM MODE

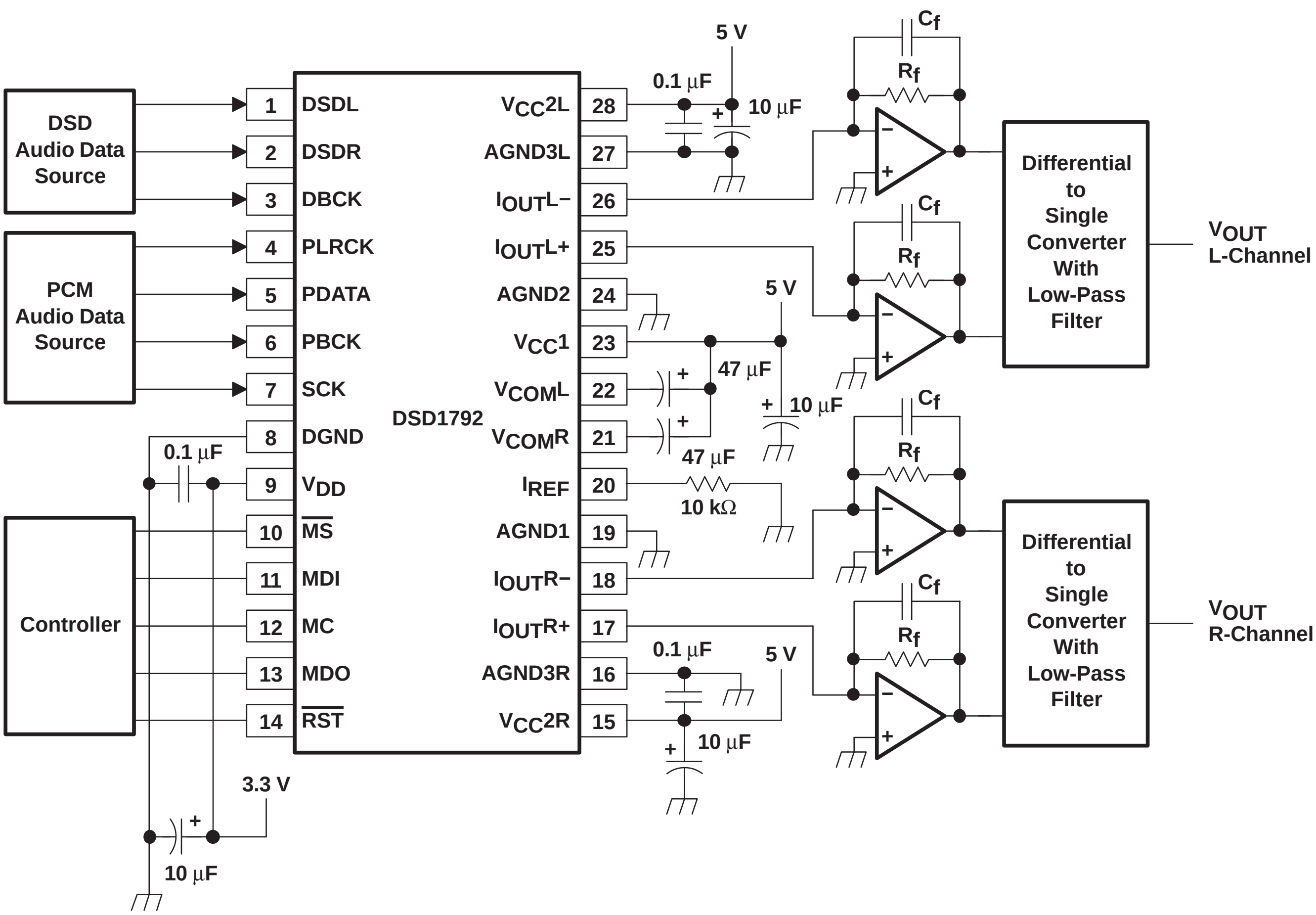


Figure 32. Typical Application Circuit for Standard PCM Audio Operation

APPLICATION INFORMATION

APPLICATION CIRCUIT

The design of the application circuit is very important in order to actually realize the high S/N ratio of which the DSD1792 is capable. This is because noise and distortion that are generated in an application circuit are not negligible.

In the circuit of Figure 33, the output level is 2 V rms and 127 dB S/N is achieved.

The circuit of Figure 34 can realize the highest performance. In this case the output level is set to 4.5 V rms and 129 dB S/N is achieved (stereo mode). In monaural mode, if the output of the L-channel and R-channel is used as a balanced output, 132 dB S/N is achieved (see Figure 36).

Figure 35 shows a circuit for the DSD mode, which is a 4^{th}-order LPF in order to reduce the out-of-band noise.

I/V Section

The current of the DSD1792 on each of the output pins (I_{OUT}L+, I_{OUT}L–, I_{OUT}R+, I_{OUT}R–) is 7.8 mA p-p at 0 dB (full scale). The voltage output level of the I/V converter (Vi) is given by following equation:

$$Vi = 7.8\ \text{mA p−p} \times R_f \quad (R_f : \text{feedback resistance of I/V converter})$$

An NE5534 op amp is recommended for the I/V circuit to obtain the specified performance. Dynamic performance such as the gain bandwidth, settling time, and slew rate of the op amp affects the audio dynamic performance of the I/V section.

Differential Section

The DSD1792 voltage outputs are followed by differential amplifier stages, which sum the differential signals for each channel, creating a single-ended I/V op-amp output. In addition, the differential amplifiers provide a low-pass filter function.

The op amp recommended for the IV circuit is the NE5534, and the op amp recommended for the differential circuit is the Linear Technology LT1028, because their input noise is low.

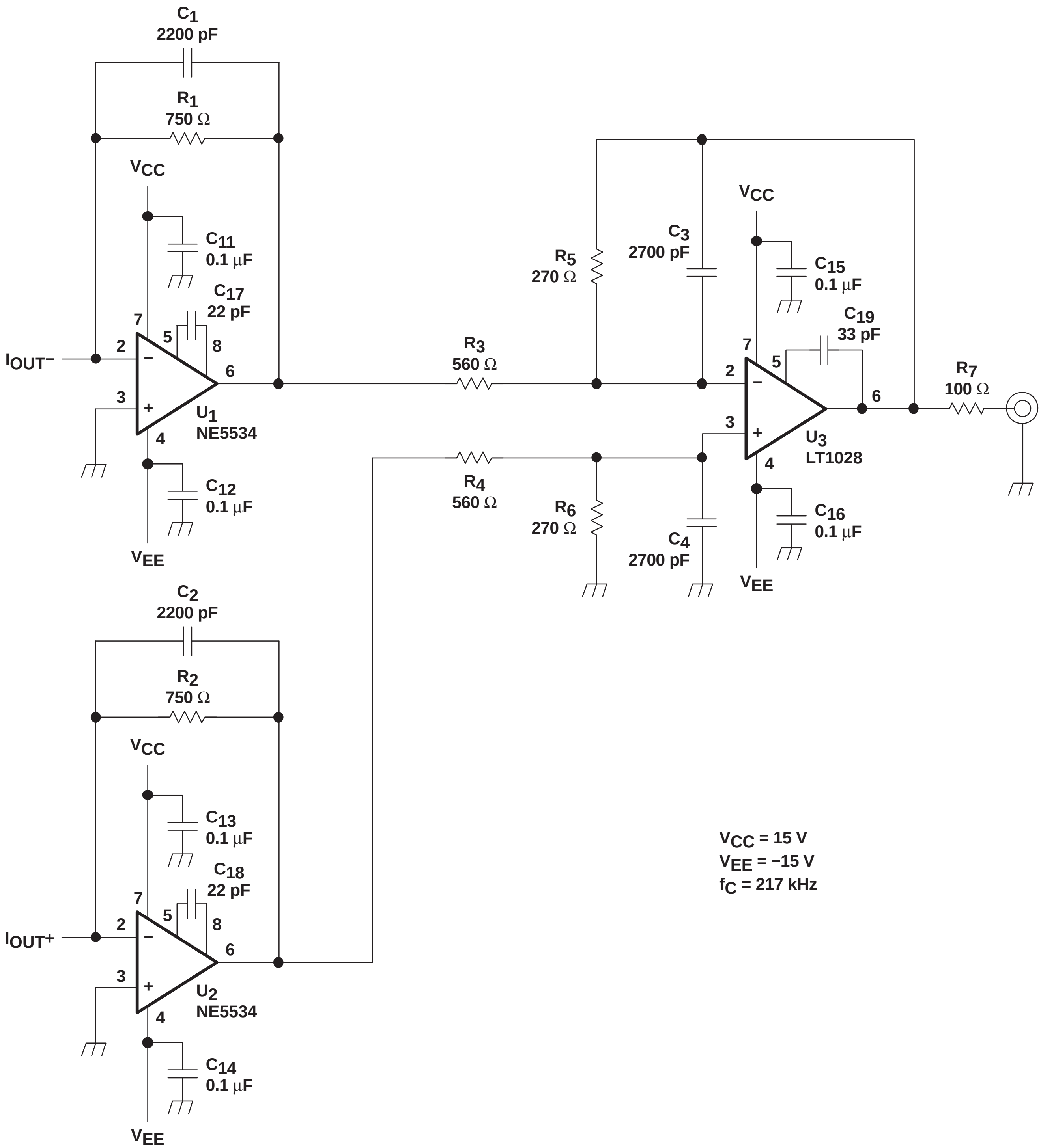


Figure 33. Measurement Circuit for PCM, V_{OUT} = 2.0 Vrms

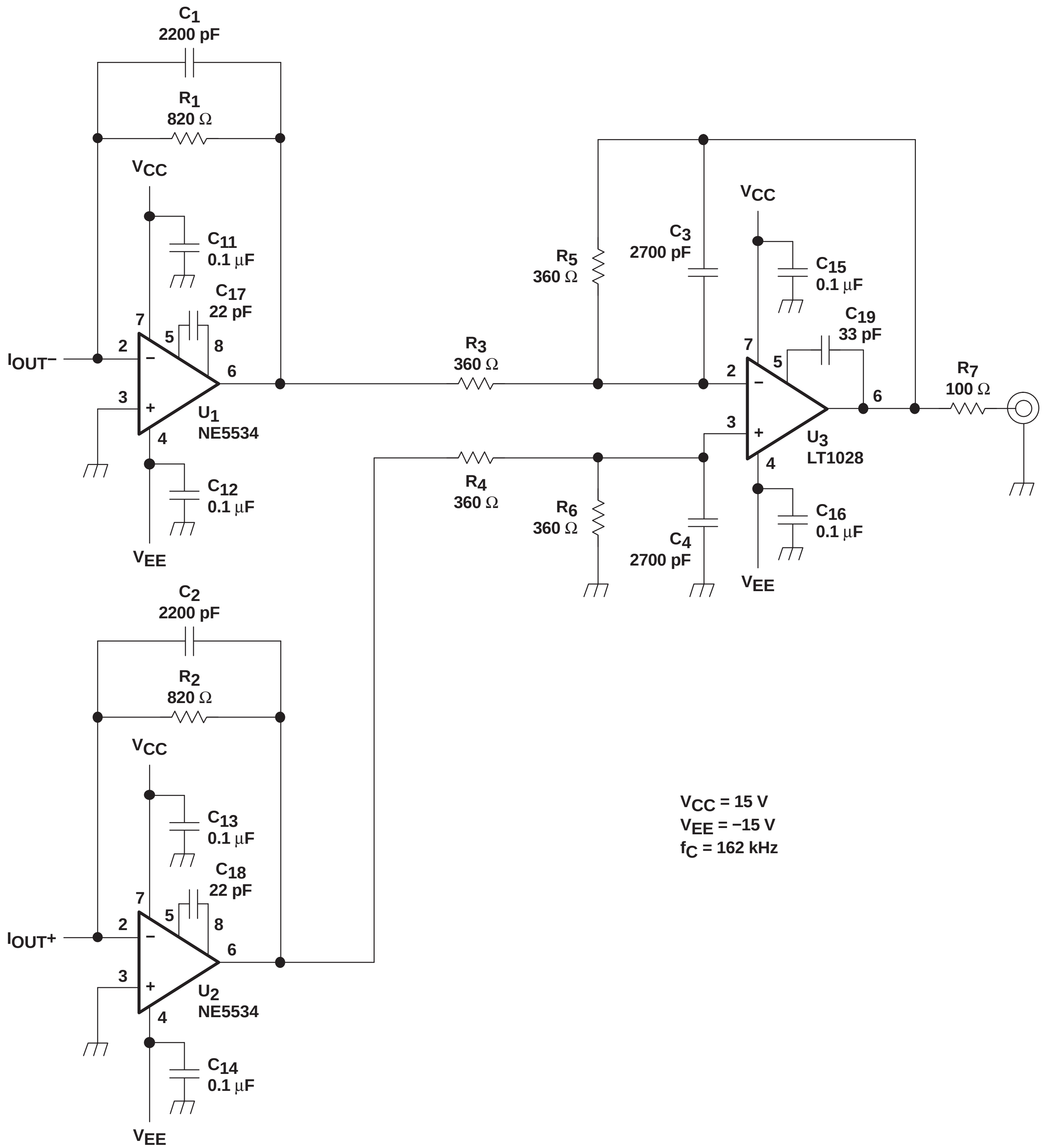


Figure 34. Measurement Circuit for PCM, V_{OUT} = 4.5 Vrms

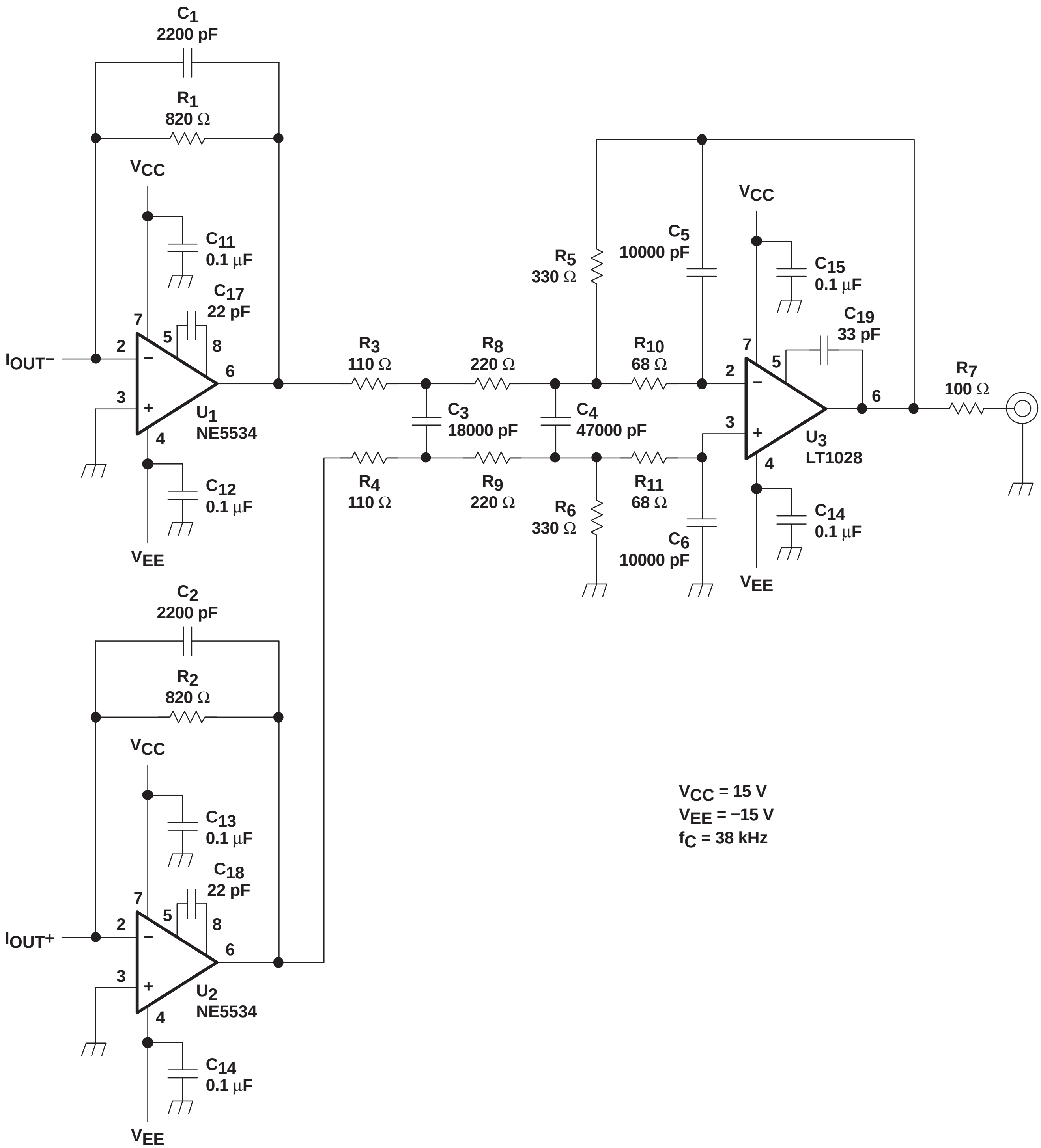


Figure 35. Measurement Circuit for DSD

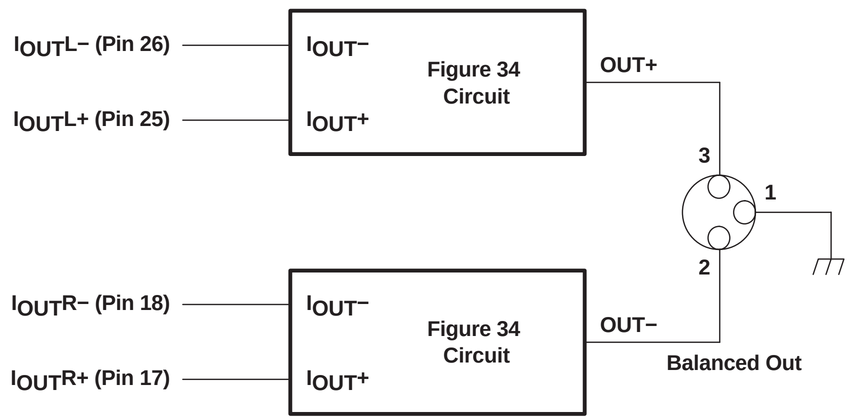


Figure 36. Measurement Circuit for Monaural Mode

APPLICATION FOR EXTERNAL DIGITAL FILTER INTERFACE

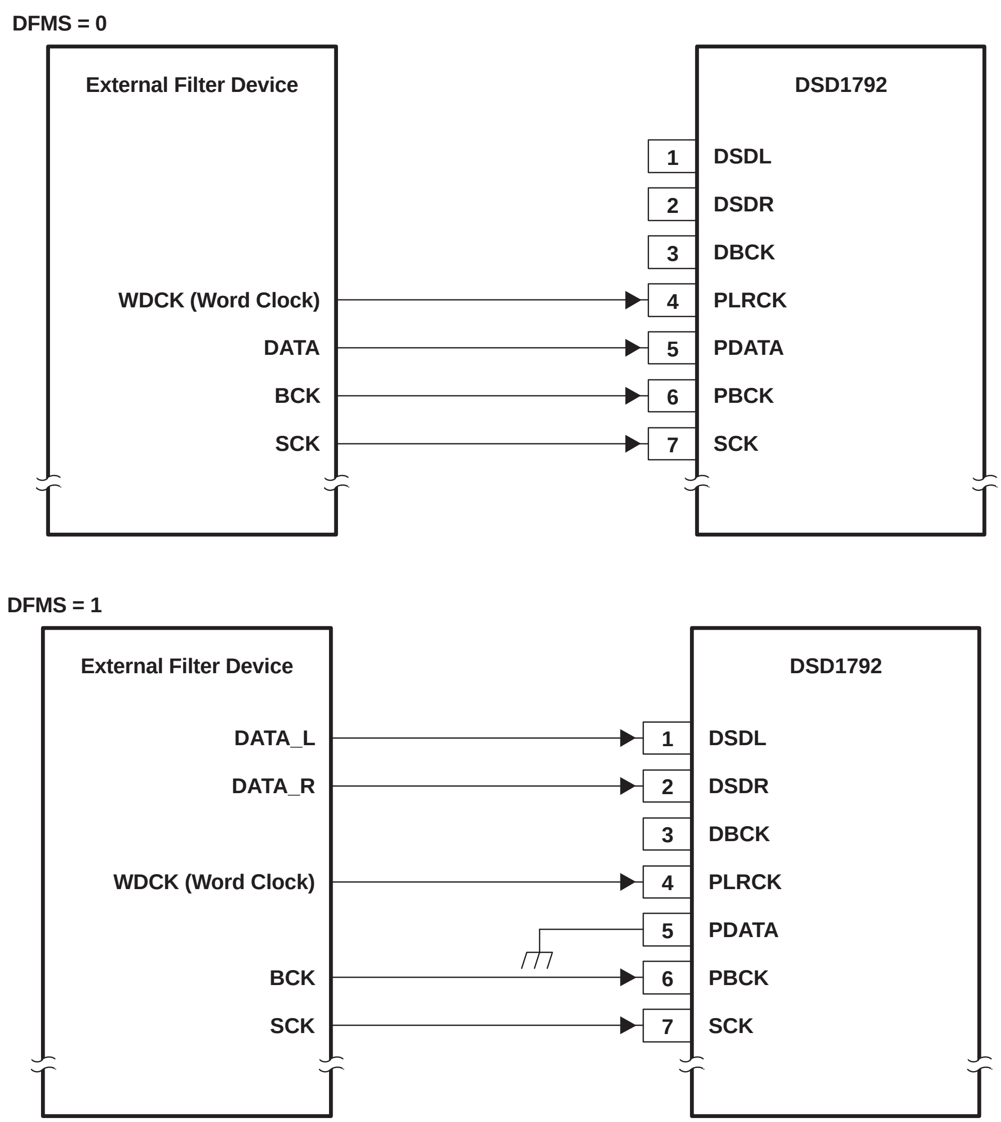


Figure 37. Connection Diagram for External DIgital Filter (Internal DF Bypass Mode) Application

Application for Interfacing With an External Digital Filter

For some applications, it may be desirable to use an external digital filter to perform the interpolation function, as it can provide improved stop-band attenuation when compared to the internal digital filter of the DSD1792.

The DSD1792 supports several external digital filters, including:

- Texas Instruments DF1704 and DF1706
- Pacific Microsonics PMD200 HDCD filter/decoder IC
- Programmable digital signal processors

The external digital filter application mode is accessed by programming the following bits in the corresponding control register:

- DFTH = 1 (register 20)

The pins used to provide the serial interface for the external digital filter are shown in the connection diagram of Figure 37. The word (WDCK) signal must be operated at 8× or 4× the desired sampling frequency, f_S.

System Clock (SCK) and Interface Timing

The DSD1792 in an application using an external digital filter requires the synchronization of WDCK and the system clock. The system clock is phase-free with respect to WDCK. Interface timing among WDCK, BCK, DATAL, and DATAR is shown in Figure 39.

Audio Format

The DSD1792 in the external digital filter interface mode supports right-justified audio formats including 16-bit, 20-bit, and 24-bit audio data, as shown in Figure 38. The audio format is selected by the FMT[2:0] bits of control register 18.

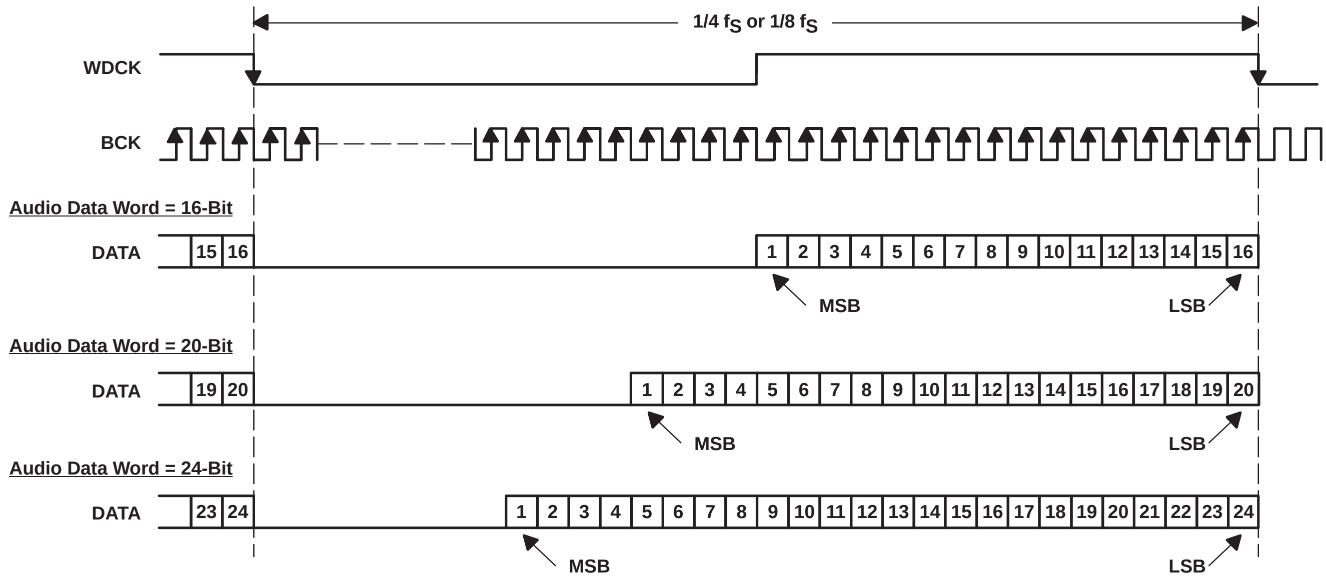
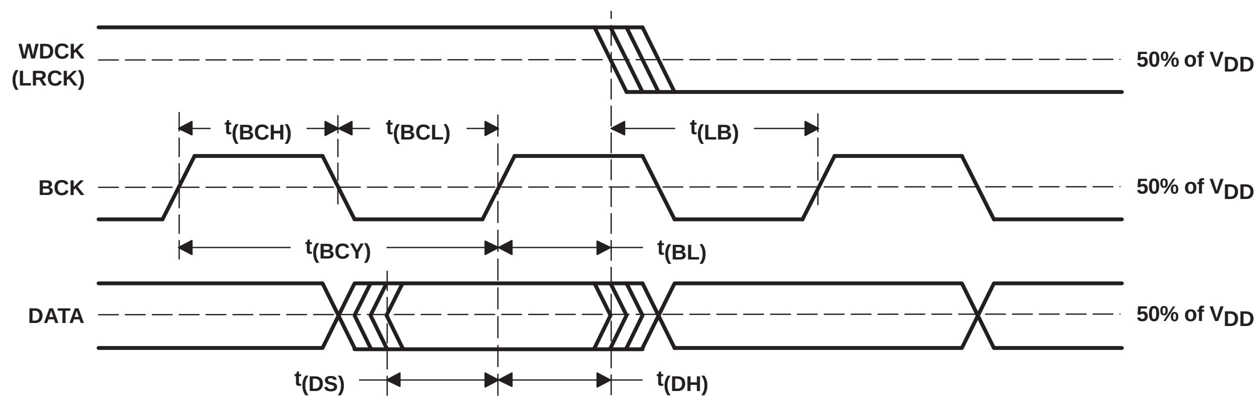


Figure 38. Audio Data Input Format for External Digital Filter (Internal DF Bypass Mode) Application



PARAMETER		MIN	MAX	UNITS
$t_{(BCY)}$	BCK pulse cycle time	20		ns
$t_{(BCL)}$	BCK pulse duration, LOW	7		ns
$t_{(BCH)}$	BCK pulse duration, HIGH	7		ns
$t_{(BL)}$	BCK rising edge to WDCK falling edge	5		ns
$t_{(LB)}$	WDCK falling edge to BCK rising edge	5		ns
$t_{(DS)}$	DATA setup time	5		ns
$t_{(DH)}$	DATA hold time	5		ns

Figure 39. Audio Interface Timing for External Digital Filter (Internal DF Bypass Mode) Application

Functions Available in the External Digital Filter Mode

The external digital filter mode allows access to the majority of the DSD1792 mode control functions.

The following table shows the register mapping available when the external digital filter mode is selected, along with descriptions of functions which are modified when using this mode selection.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	R/$\overline{W}$	0	0	1	0	0	0	0	−	−	−	−	−	−	−	−
Register 17	R/$\overline{W}$	0	0	1	0	0	0	1	−	−	−	−	−	−	−	−
Register 18	R/$\overline{W}$	0	0	1	0	0	1	0	−	FMT2	FMT1	FMT0	−	−	−	−
Register 19	R/$\overline{W}$	0	0	1	0	0	1	1	REV	−	−	OPE	−	DFMS	−	INZD
Register 20	R/$\overline{W}$	0	0	1	0	1	0	0	−	SRST	0	1	MONO	CHSL	OS1	OS0
Register 21	R/$\overline{W}$	0	0	1	0	1	0	1	−	−	−	−	−	−	−	PCMZ
Register 22	R	0	0	1	0	1	1	0	−	−	−	−	−	−	ZFGR	ZFGL

NOTE: 1: Bit is required for selection of external digital filter mode.
−: Function is disabled. No operation even if data bit is set

FMT[2:0]: Audio Data Format Selection

Default value: 000

FMT[2:0]	Audio Data Format Select
000	16-bit right-justified format (default)
001	20-bit right-justified format
010	24-bit right-justified format
Other	N/A

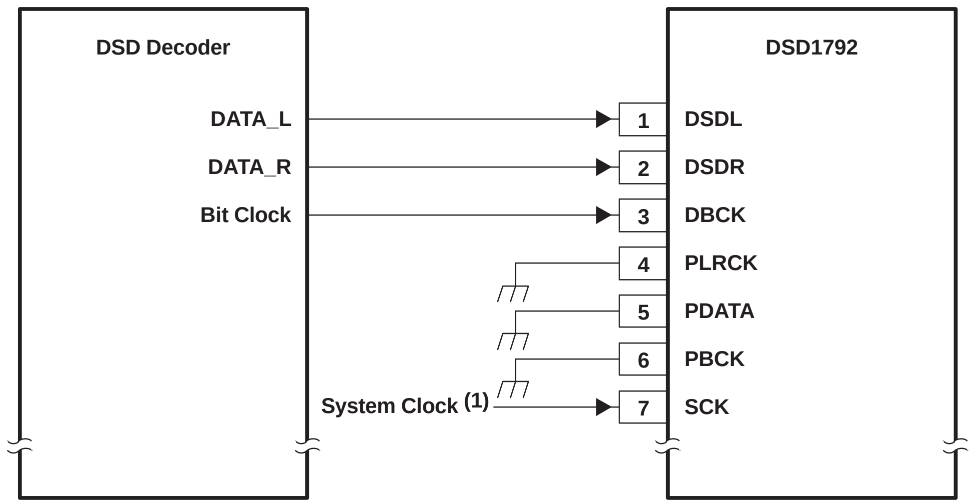
OS[1:0]: Delta-Sigma Modulator Oversampling Rate Selection

Default value: 00

OS[1:0]	Operation Speed Select
00	8 times WDCK (default)
01	4 times WDCK
10	16 times WDCK
11	Reserved

The effective oversampling rate is determined by the oversampling performed by both the external digital filter and the delta-sigma modulator. For example, if the external digital filter is 8× oversampling, and the user selects OS[1:0] = 00, then the delta-sigma modulator oversamples by 8×, resulting in an effective oversampling rate of 64×. The 16× WDCK oversampling rate is not available above a 100-kHz sampling rate. If the oversampling rate selected is 16× WDCK, the system clock frequency must be over 256 f_S.

APPLICATION FOR DSD FORMAT (DSD MODE) INTERFACE



(1) The system clock can be removed after setting the register to the DSD mode.

Figure 40. Connection Diagram in DSD Mode

Feature

This mode is used for interfacing directly to a DSD decoder, which is found in Super Audio CD™ (SACD) applications.

The DSD mode is accessed by programming the following bit in the corresponding control register.

DSD = 1 (register 20)

The DSD mode provides a low-pass filtering function. The filtering is provided using an analog FIR filter structure. Four FIR responses are available, and are selected by the DMF[1:0] bits of control register 18.

Super Audio CD is a trademark of Sony Kabushiki Kaisha TA Sony Corporation, Japan.

Pin Assignment When DSD Format Interface

Several pins are redefined for DSD mode operation. These include:

- DSDL (pin 1): DATAL as L-channel DSD data input
- DSDR (pin 2): DATAR as R-channel DSD data input
- DBCK (pin 3): Bit clock (BCK) for DSD data

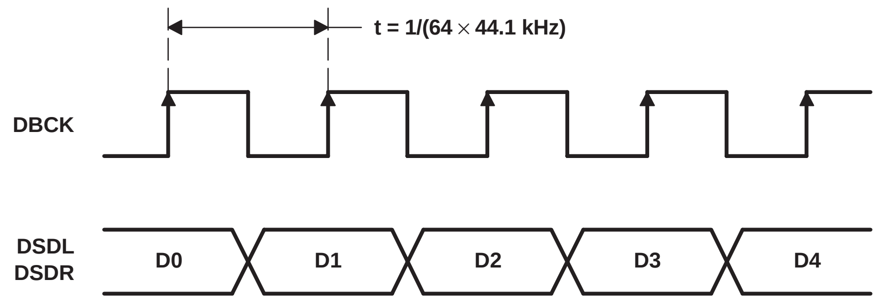
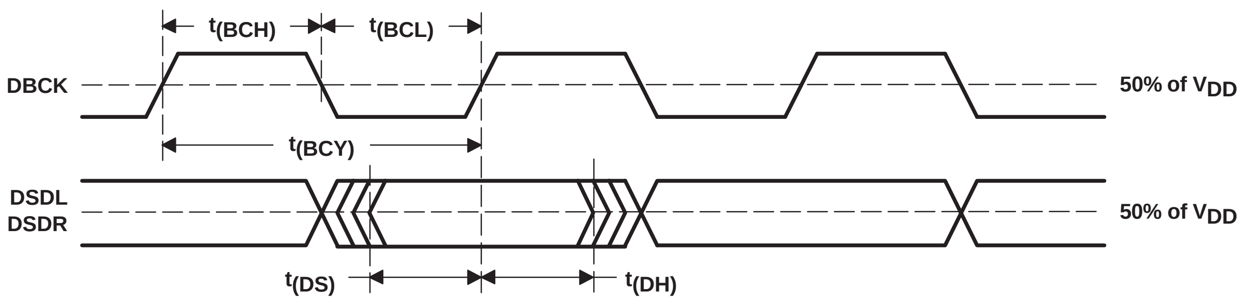


Figure 41. Normal Data Output Form From DSD Decoder



PARAMETER		MIN	MAX	UNITS
$t_{(BCY)}$	DBCK pulse cycle time	85(1)		ns
$t_{(BCH)}$	DBCK high-level time	30		ns
$t_{(BCL)}$	DBCK low-level time	30		ns
$t_{(DS)}$	DSDL, DSDR setup time	10		ns
$t_{(DH)}$	DSDL, DSDR hold time	10		ns

(1) 2.8224 MHz × 4. (2.8224 MHz = 64 × 44.1 kHz. This value is specified as a sampling rate of DSD.)

Figure 42. Timing for DSD Audio Interface

ANALOG FIR FILTER PERFORMANCE IN DSD MODE

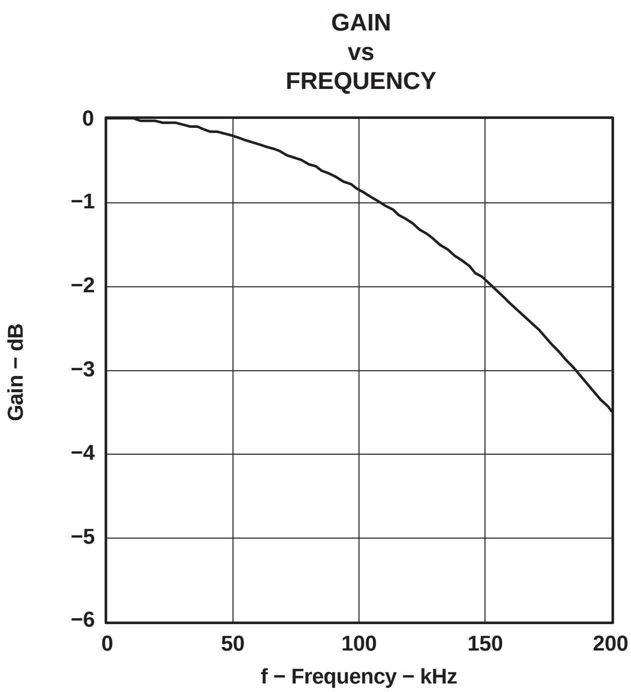


Figure 43. DSD Filter-1, Low BW

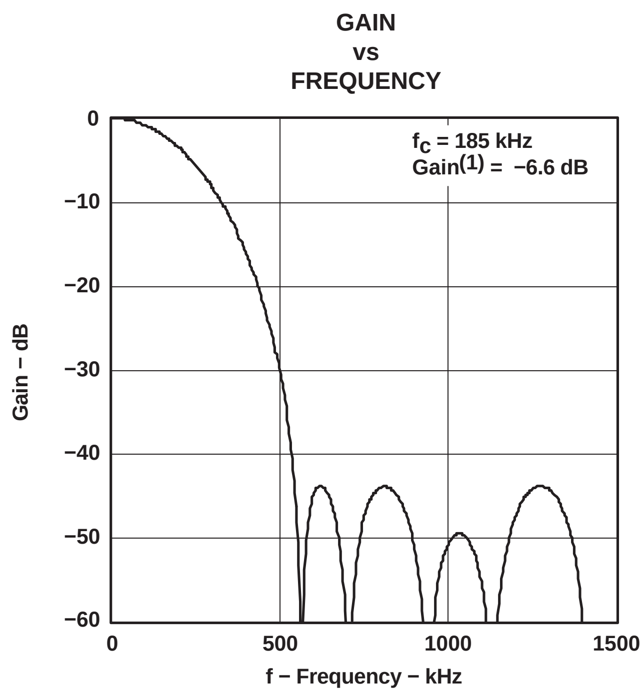


Figure 44. DSD Filter-1, High BW

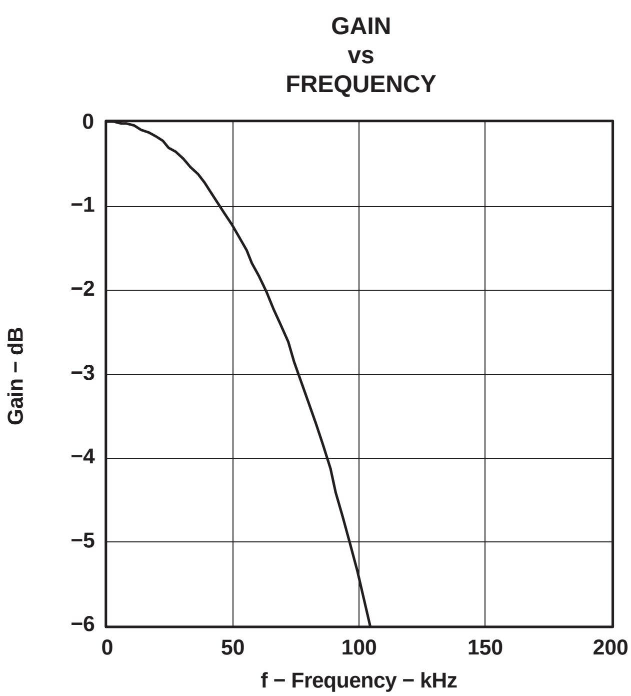


Figure 45. DSD Filter-2, Low BW

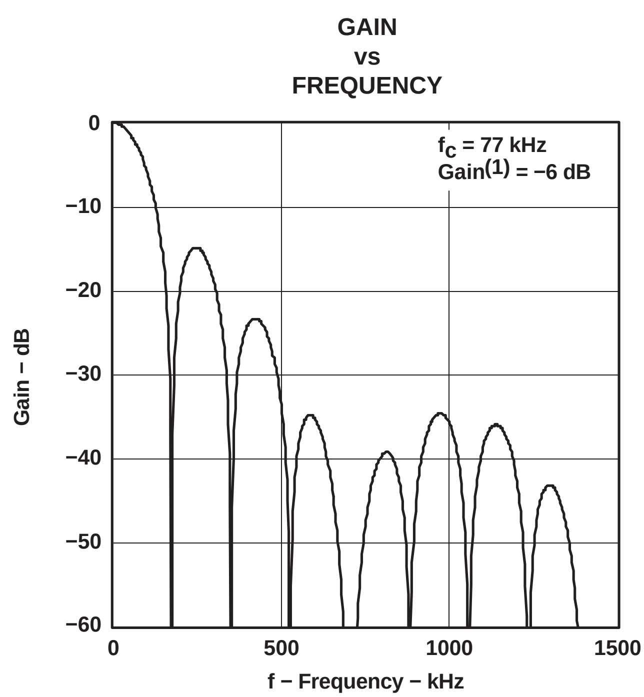


Figure 46. DSD Filter-2, High BW

(1) This gain is in comparison to PCM 0 dB, when the DSD input signal efficiency is 50%.

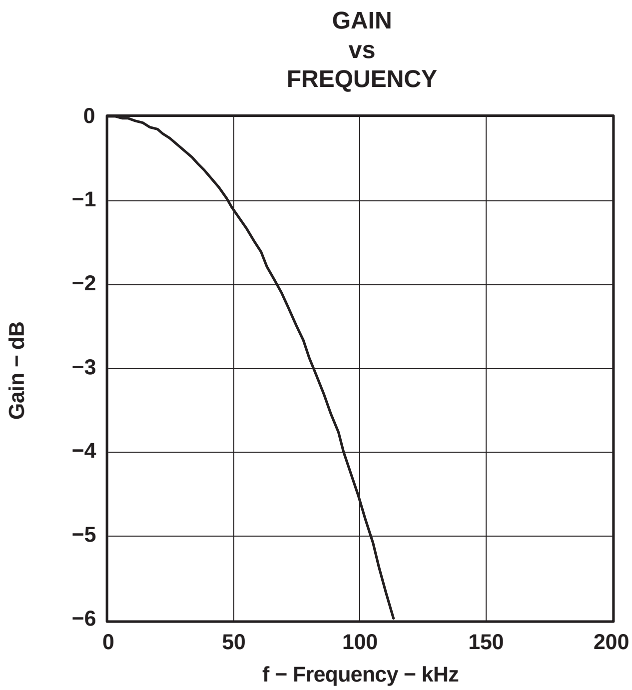


Figure 47. DSD Filter-3, Low BW

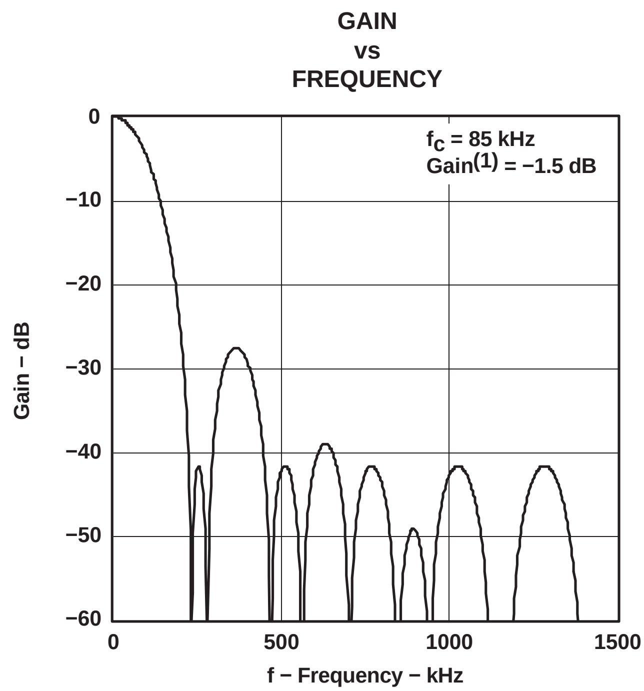


Figure 48. DSD Filter-3, High BW

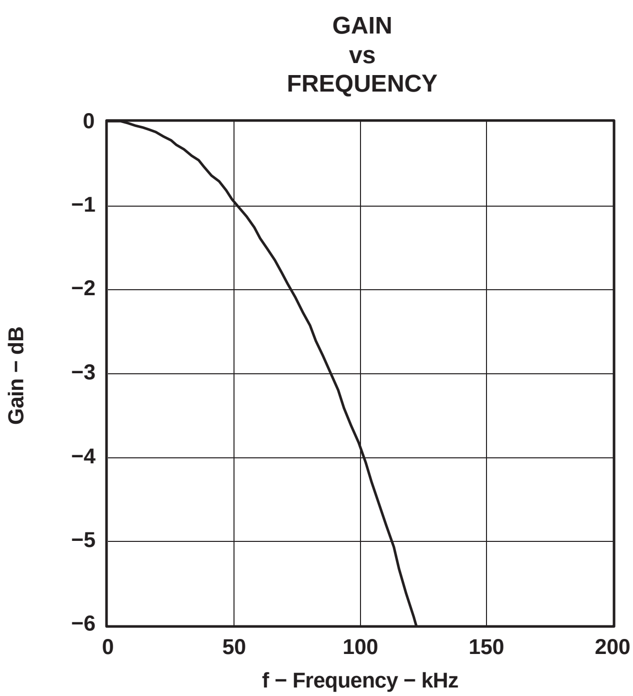


Figure 49. DSD Filter-4, Low BW

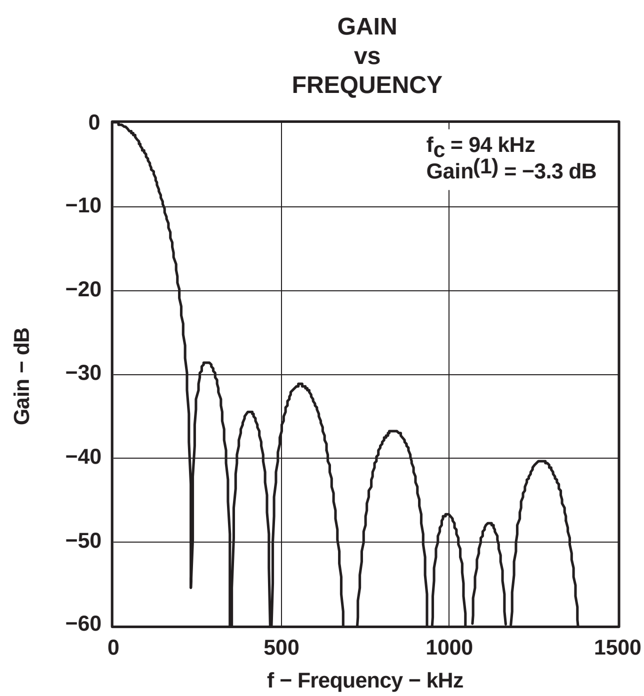


Figure 50. DSD Filter-4, High BW

(1) This gain is in comparison to PCM 0 dB, when the DSD input signal efficiency is 50%.

DSD MODE CONFIGURATION AND FUNCTION CONTROLS

Configuration for the DSD Interface Mode

DSD = 1 (Register 20, B5)

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	R/$\overline{W}$	0	0	1	0	0	0	0	−	−	−	−	−	−	−	−
Register 17	R/$\overline{W}$	0	0	1	0	0	0	1	−	−	−	−	−	−	−	−
Register 18	R/$\overline{W}$	0	0	1	0	0	1	0	−	−	−	−	DMF1	DMF0	−	−
Register 19	R/$\overline{W}$	0	0	1	0	0	1	1	REV	−	−	OPE	−	−	−	−
Register 20	R/$\overline{W}$	0	0	1	0	1	0	0	−	SRST	1	−	MONO	CHSL	OS1	OS0
Register 21	R	0	0	1	0	1	0	1	−	−	−	−	−	DZ1	DZ0	−
Register 22	R	0	0	1	0	1	1	0	−	−	−	−	−	−	ZFGR	ZFGL

NOTE: −: Function is disabled. No operation even if data bit is set

DMF[1:0]: Analog FIR Performance Selection

Default value: 00

DMF[1:0]	Analog-FIR Performance Select
00	FIR-1 (default)
01	FIR-2
10	FIR-3
11	FIR-4

Plots for the four analog FIR filter responses are shown in the *TYPICAL PERFORMANCE CURVES* section of this data sheet.

OS[1:0]: Analog-FIR Operation-Speed Selection

Default value: 00

OS[1:0]	Operation Speed Select
00	f_{DBCK} (default)
01	$f_{DBCK}/2$
10	Reserved
11	$f_{DBCK}/4$

The OS bit in the DSD mode is used to select the operating rate of the analog FIR. The OS bits must be set before setting the DSD bit to 1.

Requirements for System Clock

The bit clock (BCK) for the DSD mode is required at pin 3 of the DSD1792. The frequency of the bit clock can be N times the sampling frequency. Generally, N is 64 in DSD applications.

The interface timing between the bit clock and DATAL and DATAR is required to meet the same setup- and hold-time specifications as shown for the audio interface timing in Figure 42.

TDMCA Format

The DSD1792 supports the time-division-multiplexed command and audio (TDMCA) data format to simplify the host control serial interface. The TDMCA format is designed not only for the McBSP of TI DSPs but also for any programmable devices. The TDMCA format can transfer not only audio data but also command data, so that it can be used together with any kind of device that supports the TDMCA format. The TDMCA frame consists of command field, extended command field, and some audio data fields. Those audio data are transported to IN devices (such as a DAC) and/or from OUT devices (such as an ADC). The DSD1792 is an IN device. LRCK and BCK are used with both IN and OUT devices so that the sample frequency of all devices in a system must be the same. The TDMCA mode supports a maximum of 30 device IDs. The maximum number of audio channels depends on the BCK frequency.

TDMCA Mode Determination

The DSD1792 recognizes the TDMCA mode automatically when it receives an LRCK signal with a pulse duration of two BCK clocks. If the TDMCA mode operation is not needed, the duty cycle of LRCK must be 50%. Figure 51 shows the LRCK and BCK timing that determines the TDMCA mode. The DSD1792 enters the TDMCA mode after two continuous TDMCA frames. Any TDMCA commands can be issued during the next TDMCA frame after the TDMCA mode is entered.

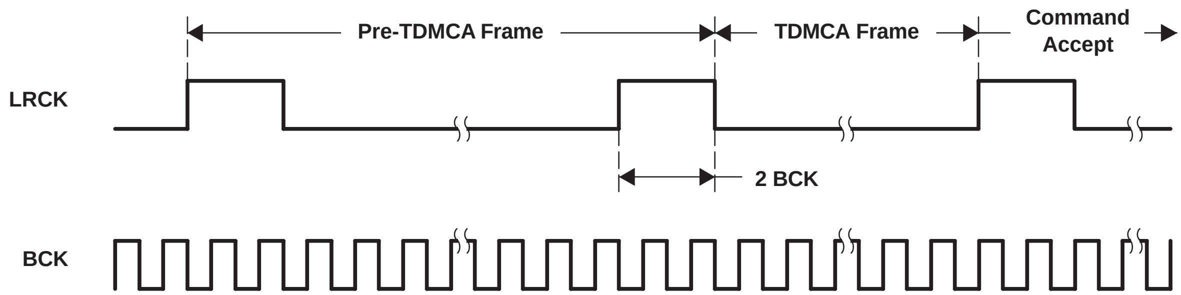


Figure 51. LRCK and BCK Timing of Determination TDMCA Mode

TDMCA Terminals

TDMCA requires six signals, of which four signals are for command and audio data interface, and two pairs of signals which are for daisy chaining. Those signals can be shared as in the following table. The DO signal has a 3-state output so that it can be connected directly to other devices.

TERMINAL NAME	TDMCA NAME	I/O	DESCRIPTION
PLRCK	LRCK	I	TDMCA frame start signal. It must be the same as the sampling frequency.
PBCK	BCK	I	TDMCA clock. Its frequency must be high enough to communicate a TDMCA frame within an LRCK cycle.
PDATA	DI	I	TDMCA command and audio data input signal
MDO	DO	O	TDMCA command data 3-state output signal
MC	DCI	I	TDMCA daisy-chain input signal
$\overline{MS}$	DCO	O	TDMCA daisy-chain output signal

Device ID Determination

The TDMCA mode also supports a multichip implementation in one system. This means a host controller (DSP) can simultaneously support several TDMCA devices, which can be of the same type or different types, including PCM devices. The PCM devices are categorized as IN device, OUT device, IN/OUT device, and NO device. The IN device has an input port to get audio data, the OUT device has an output port to supply audio data, the IN/OUT device has both input and output ports for audio data, and the NO device has no port for audio data but needs command data from the host. A DAC is an IN device, an ADC is an OUT device, a CODEC is an IN/OUT device, and a PLL is a NO device. The DSD1792 is an IN device. For the host controller to distinguish the devices, each device is assigned its own device ID by the daisy chain. The devices obtain their own device IDs automatically by connecting their DCI to the DCO of the preceding device and their DCO to the DCI of the following device in the daisy chain. The daisy chains are categorized as the IN chain and the OUT chain, which are completely independent and equivalent. Figure 52 shows an example daisy chain connection. If a system needs to chain the DSD1792 and a NO device in the same IN or OUT chain, the NO device should be chained at the back end of the chain because it does not require any audio data. Figure 53 shows an example of TDMCA system including an IN chain and an OUT chain with a TI DSP. For a device to get its own device ID, the DID signal must be set to 1 (see the *Command Field* section for details), and LRCK and BCK must be driven in the TDMCA mode for all PCM devices which are chained. The device at the top of the chain knows its device ID is 1 because its DCI is fixed HIGH. Other devices count the BCK pulses and observe their own DCI signal to determine their position and ID. Figure 54 shows the initialization of each device ID.

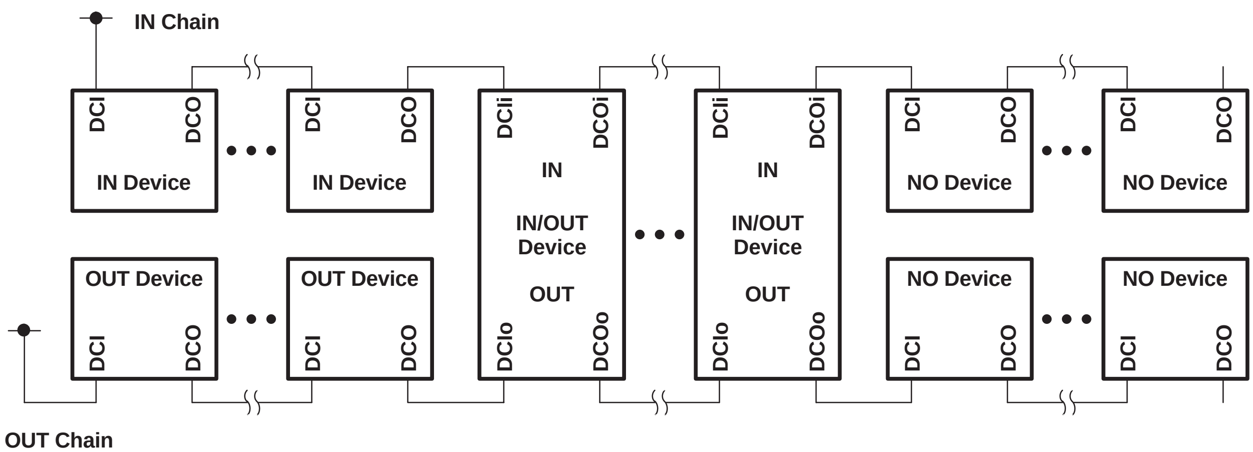


Figure 52. Daisy Chain Connection

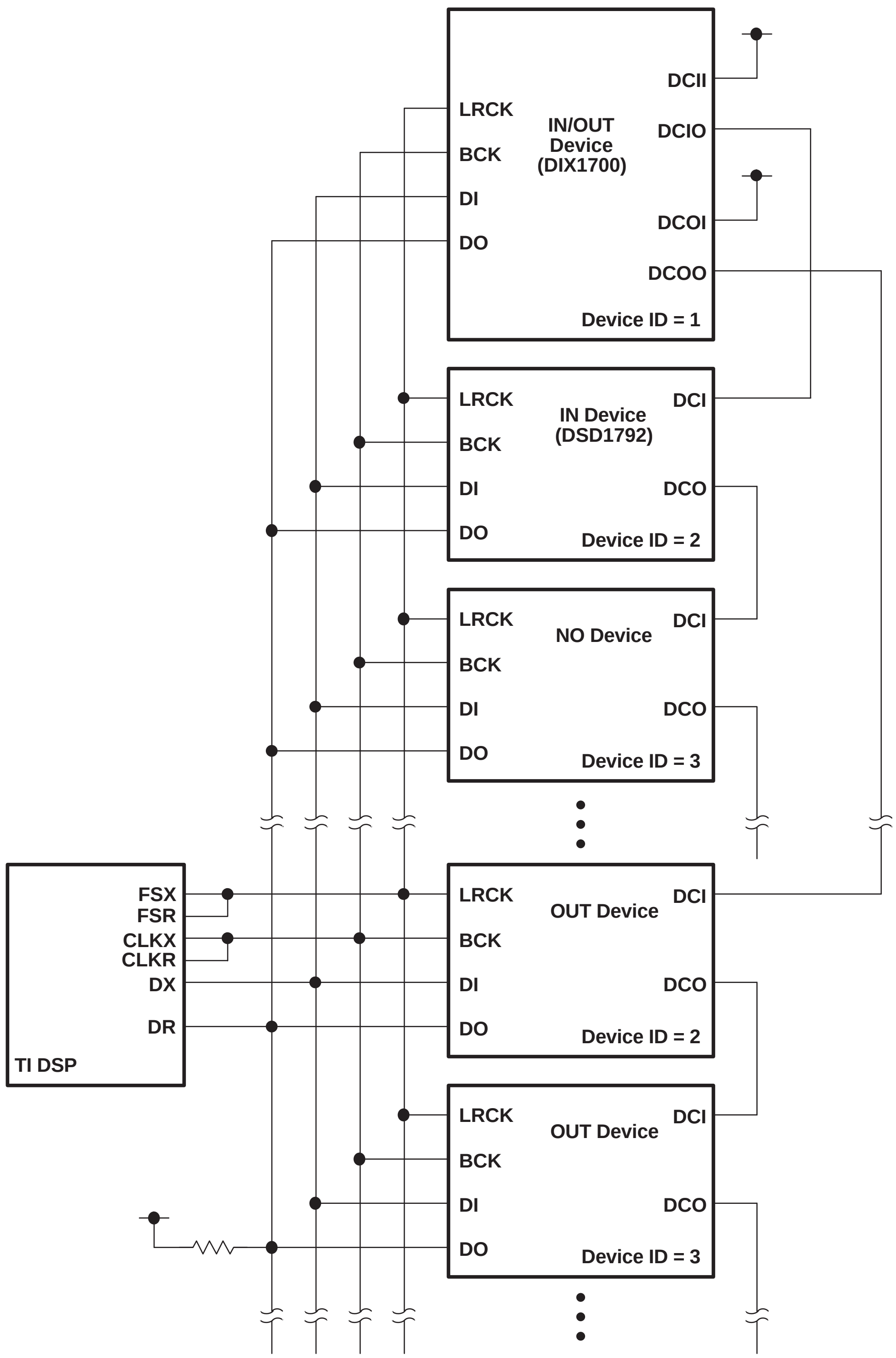


Figure 53. IN Daisy Chain and OUT Daisy Chain Connection for a Multichip System

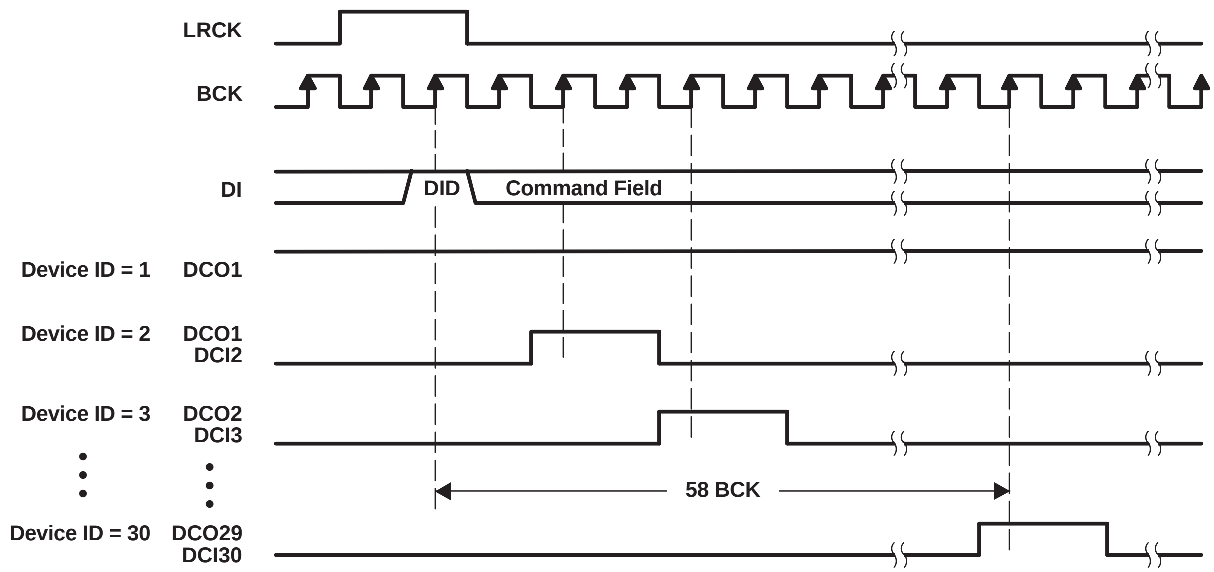


Figure 54. Device ID Determination Sequence

TDMCA Frame

In general, the TDMCA frame consists of the command field, extended command (EMD) field, and audio data fields. All of them are 32 bits in length, but the lowest byte has no meaning. The MSB is transferred first for each field. The command field is always transferred as the first packet of the frame. The EMD field is transferred if the EMD flag of the command field is HIGH. If any EMD packets are transferred, no audio data follows the EMD packets. This frame is for quick system initialization. All devices of a daisy chain should respond to the command field and extended command field. The DSD1792 has two audio channels that can be selected by OPE (register 19). If the OPE bit is not set HIGH, those audio channels are transferred. Figure 55 shows the general TDMCA frame. If some DACs are enabled, but corresponding audio data packets are not transferred, the analog outputs are unpredictable.

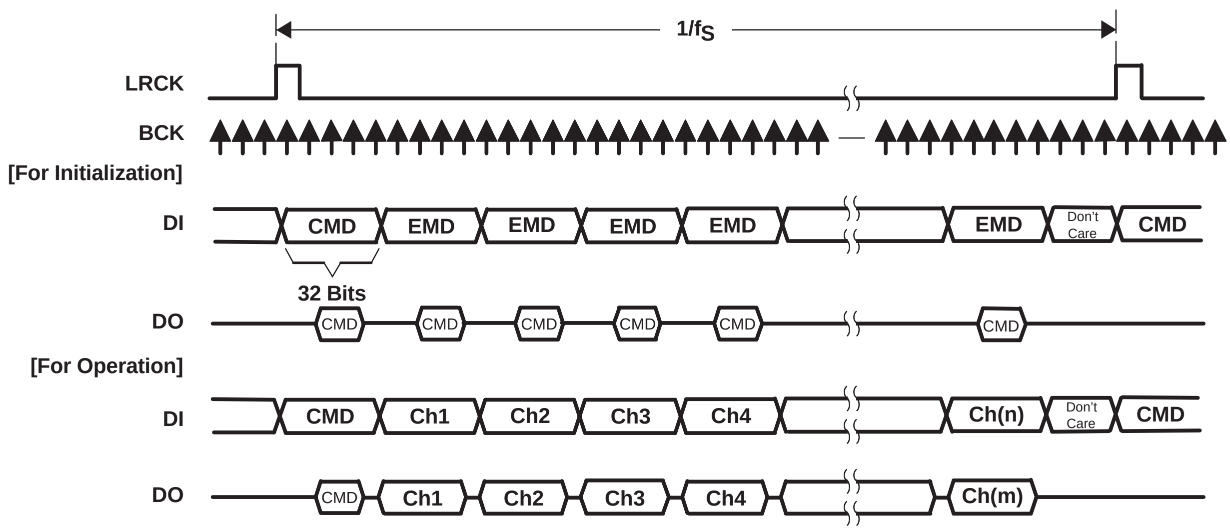


Figure 55. General TDMCA Frame

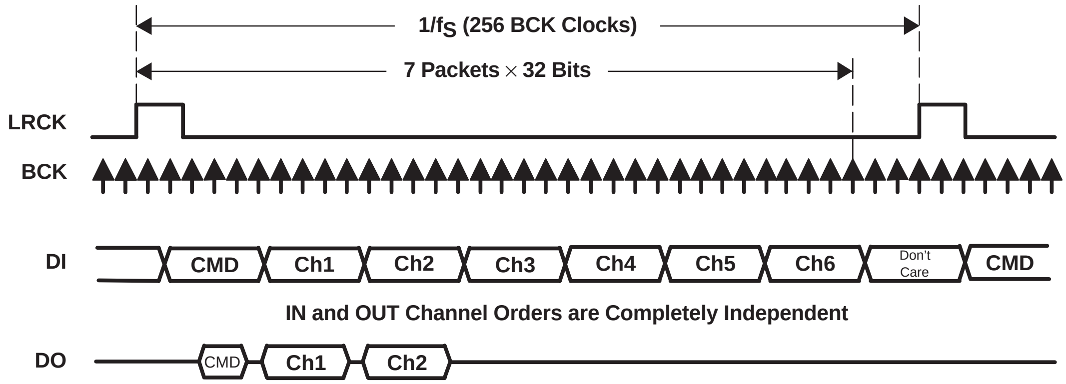


Figure 56. TDMCA Frame Example of 6-Ch DAC and 2-Ch ADC With Command Read

Command Field

The normal command field is defined as follows. When the DID bit (MSB) is 1, this frame is used only for device ID determination, and all remaining bits in the field are ignored.

	31	30	29	28–24	23	22–16	15–8	7–0
command	DID	EMD	DCS	device ID	R/$\overline{W}$	register ID	data	not used

Bit 31: Device ID enable flag

The DSD1792 operates to get its own device ID for TDMCA initialization if this bit is HIGH.

Bit 30: Extended command enable flag

EMD packet is transferred if this bit is HIGH, otherwise skipped. Once this bit is HIGH, this frame does not contain any audio data. This is for system initialization.

Bit 29: Daisy chain selection flag

HIGH designates OUT-chain devices, LOW designates IN-chain devices. The DSD1792 is an IN device, so the DCS bit must be set to LOW.

Bits[28:24]: Device ID. It is 5 bits length, and it can be defined.

These bits identify the order of a device in the IN or OUT daisy chain. The top of the daisy chain defines device ID 1 and successive devices are numbered 2, 3, 4, etc. All devices for which the DCI is fixed HIGH are also defined as ID 1. The maximum device ID is 30 each in the IN and OUT chains. If a device ID of 0x1F is used, all devices are selected as broadcast when in the write mode. If a device ID of 0x00 is used, no device is selected.

Bit 23: Command Read/Write flag

If this bit is HIGH, the command is a read operation.

Bits[22:16]: Register ID

It is 7 bits in length.

Bits[15:8]: Command data

It is 8 bits in length. Any valid data can be chosen for each register.

Bits[7:0]: Not used

These bits are never transported when a read operation is performed.

Extended command field

The extended command field is the same as the command field, except that it does not have a DID flag.

	31	30	29	28–24	23	22–16	15–8	7–0
extended command	rsvd	EMD	DCS	device ID	R/$\overline{W}$	register ID	data	not used

Audio Fields

The audio field is 32 bits in length and the audio data is transferred MSB first, so the other fields must be stuffed with 0s as shown in the following example.

	31	16	12	8	7	4 3	0
audio data	MSB	24 bits		LSB		All 0s	

TDMCA Register Requirements

TDMCA mode requires device ID and audio channel information, previously described. The OPE bit in register 19 indicates audio channel availability and register 23 indicates the device ID. Register 23 is used only in the TDMCA mode. See the mode control register map (Table 3).

Register Write/Read Operation

The command supports register write and read operations. If the command requests to read one register, the read data is transferred on DO during the data phase of the timing cycle. The DI signal can be retrieved at the positive edge of BCK, and the DO signal is driven at the negative edge of BCK. DO is activated one BCK cycle early to compensate for the output delay caused by high impedance. Figure 57 shows the TDMCA write and read timing.

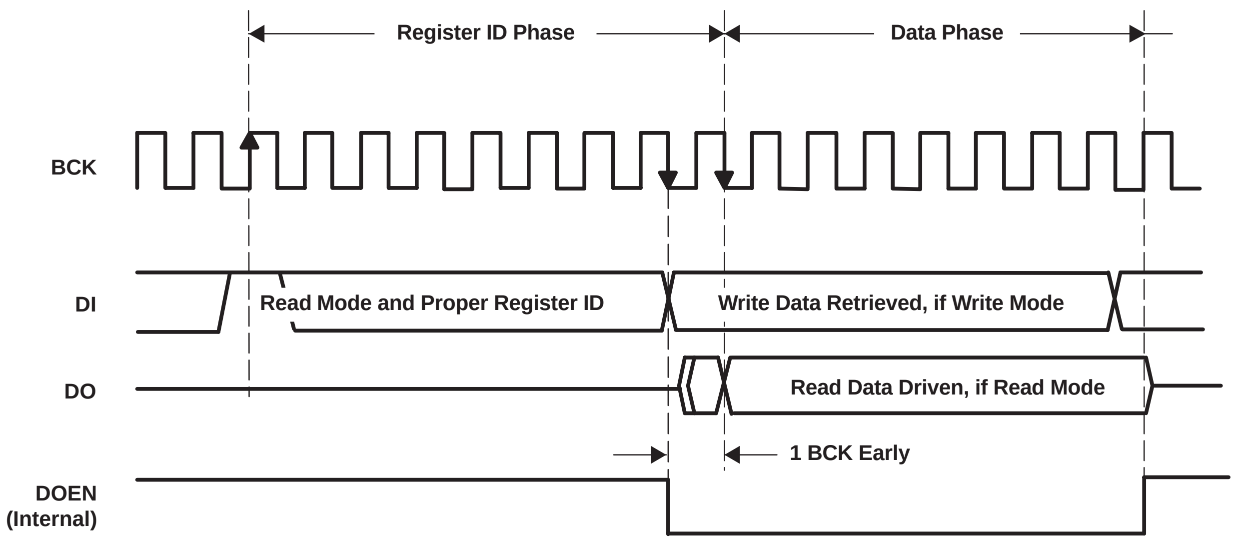


Figure 57. TDMCA Write and Read Operation Timing

TDMCA-Mode Operation

DCO specifies the owner of the next audio channel in TDMCA-mode operation. When a device retrieves its own audio channel data, DCO goes HIGH during the last audio channel period. Figure 58 shows the DCO output timing in TDMCA-mode operation. The host controller ignores the behavior of DCI and DCO. DCO indicates the last audio channel of each device. Therefore, DCI means the next audio channel is allocated.

If some devices are skipped due to no active audio channel, the skipped devices must notify the next device that the DCO will be passed through the next DCI. Figure 59 and Figure 60 show DCO timing with skip operation. Figure 61 shows the ac timing of the daisy chain signals.

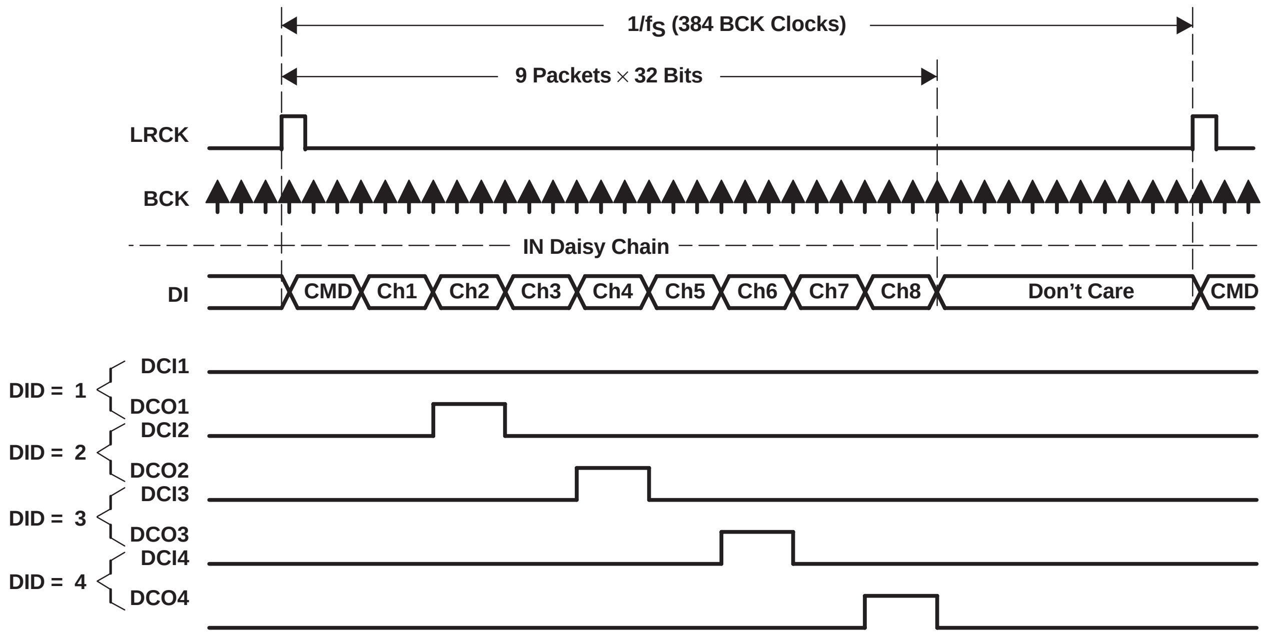


Figure 58. DCO Output Timing of TDMCA Mode Operation

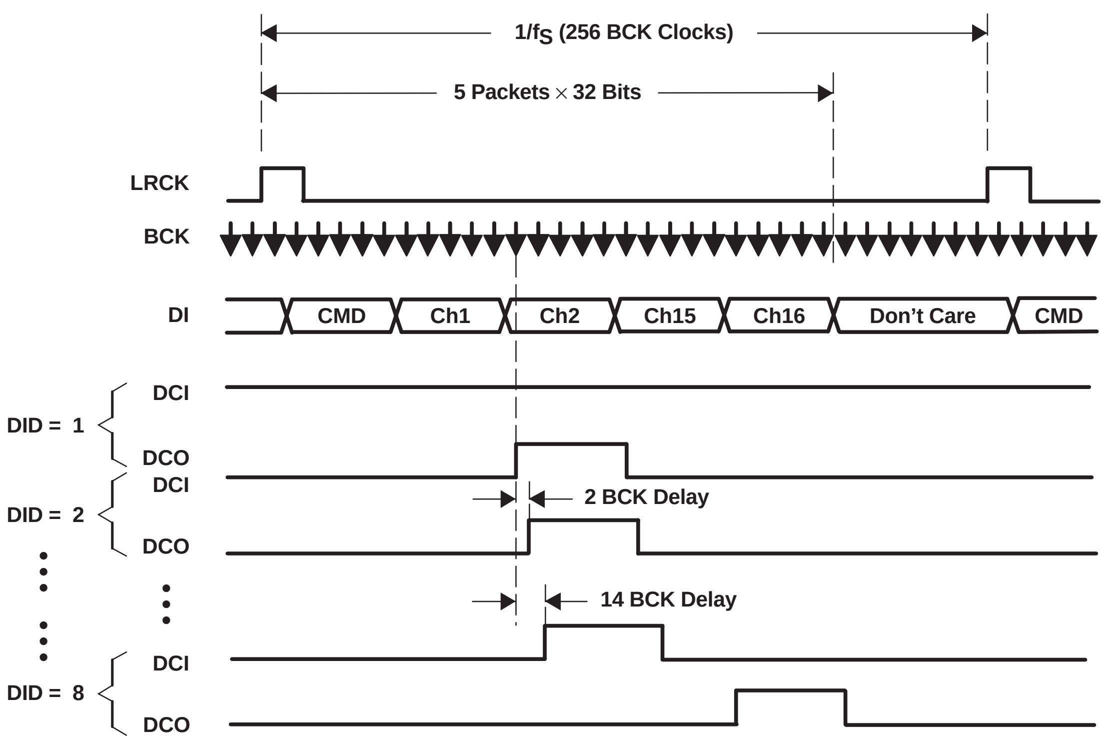


Figure 59. DCO Output Timing With Skip Operation

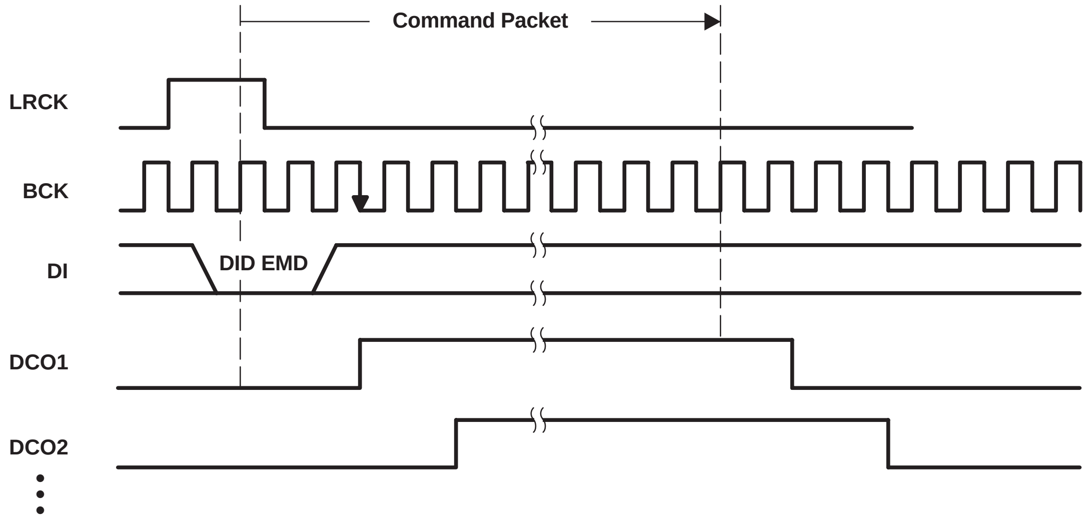
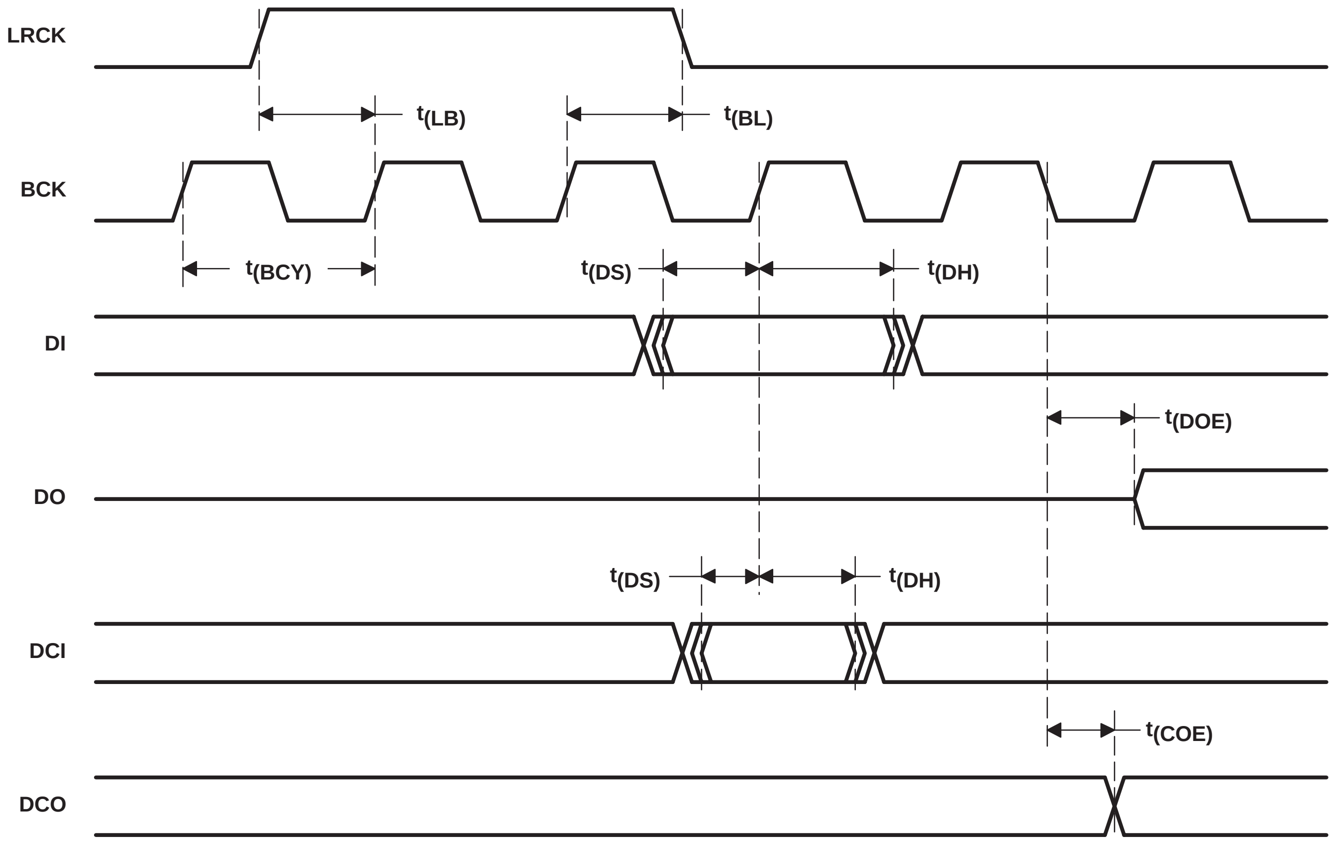


Figure 60. DCO Output Timing With Skip Operation (for Command Packet 1)



PARAMETER		MIN	MAX	UNITS
$t_{(BCY)}$	BCK pulse cycle time	20		ns
$t_{(LB)}$	LRCK setup time	0		ns
$t_{(BL)}$	LRCK hold time	3		ns
$t_{(DS)}$	DI setup time	0		ns
$t_{(DH)}$	DI hold time	3		ns
$t_{(DS)}$	DCI setup time	0		ns
$t_{(DH)}$	DCI hold time	3		ns
$t_{(DOE)}$	DO output delay(1)		8	ns
$t_{(COE)}$	DCO output delay(1)		6	ns

(1) Load capacitance is 10 pF.

Figure 61. AC Timing of Daisy Chain Signals

THEORY OF OPERATION

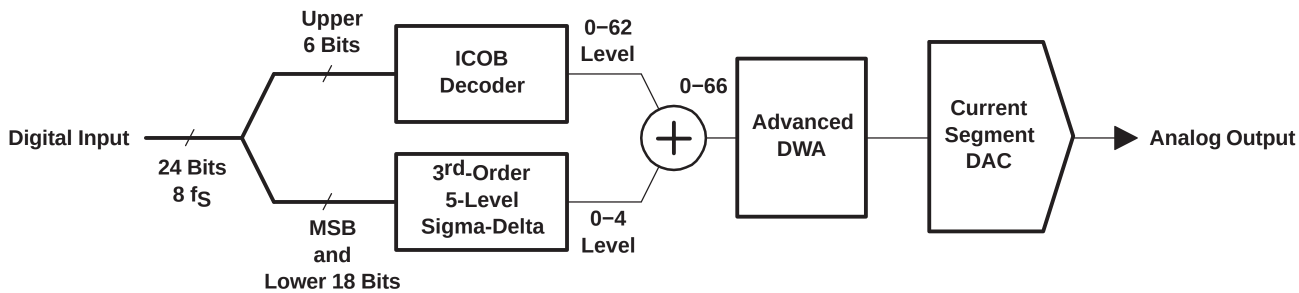


Figure 62. Advanced Segments DAC

The DSD1792 uses TI's advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The DSD1792 provides balanced voltage outputs.

Digital input data via the digital filter is separated into six upper bits and 18 lower bits. The six upper bits are converted to inverted complementary offset binary (ICOB) code. The lower 18 bits, associated with the MSB, are processed by a five-level third-order delta-sigma modulator operated at 64 f_S by default. The 1 level of the modulator is equivalent to the 1 LSB of the ICOB code converter. The data groups processed in the ICOB converter and third-order delta-sigma modulator are summed together to an up to 66-level digital code, and then processed by data-weighted averaging (DWA) to reduce the noise produced by element mismatch. The data of up to 66 levels from the DWA is converted to an analog output in the differential-current segment section.

This architecture has overcome the various drawbacks of conventional multibit processing and also achieves excellent dynamic performance.

Analog output

The following table and Figure 63 show the relationship between the digital input code and analog output.

	800000 (–FS)	000000 (BPZ)	7FFFFF (+FS)
I_{OUT}N [mA]	–2.3	–6.2	–10.1
I_{OUT}P [mA]	–10.1	–6.2	–2.3
V_{OUT}N [V]	–1.725	–4.650	–7.575
V_{OUT}P [V]	–7.575	–4.650	–1.725
V_{OUT} [V]	–2.821	0	2.821

NOTE: V_{OUT}N is the output of U1, V_{OUT}P is the output of U2, and V_{OUT} is the output of U3 in the application circuit of Figure 33.

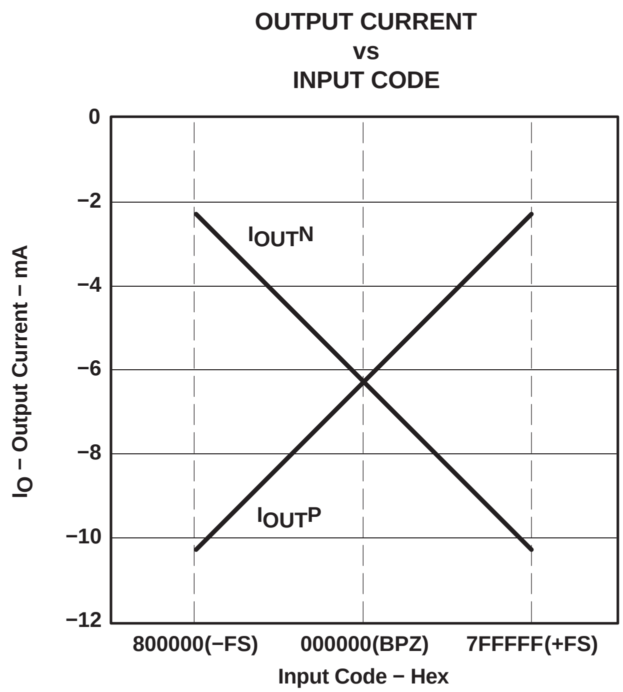
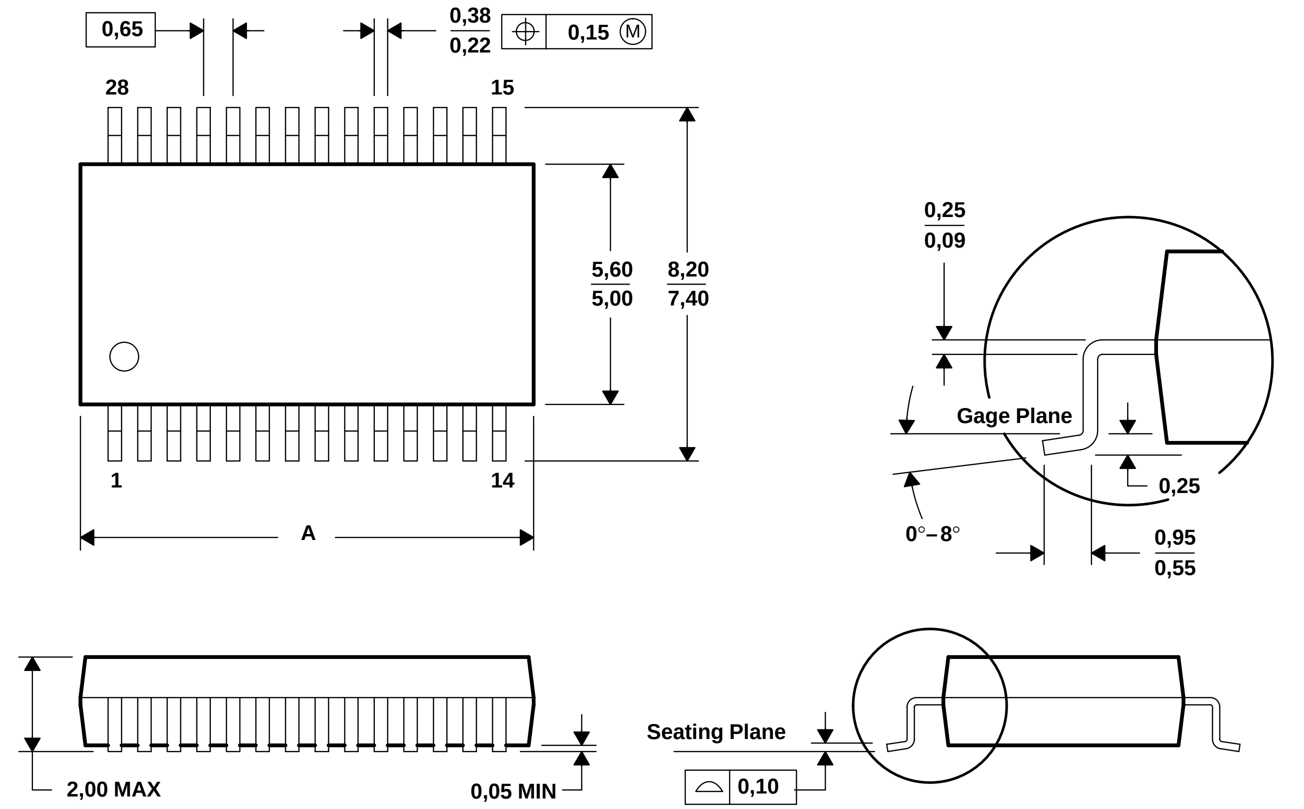


Figure 63. The Relationship Between Digital Input and Analog Output

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DSD1792DB	ACTIVE	SSOP	DB	28	47	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
DSD1792DBR	ACTIVE	SSOP	DB	28	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

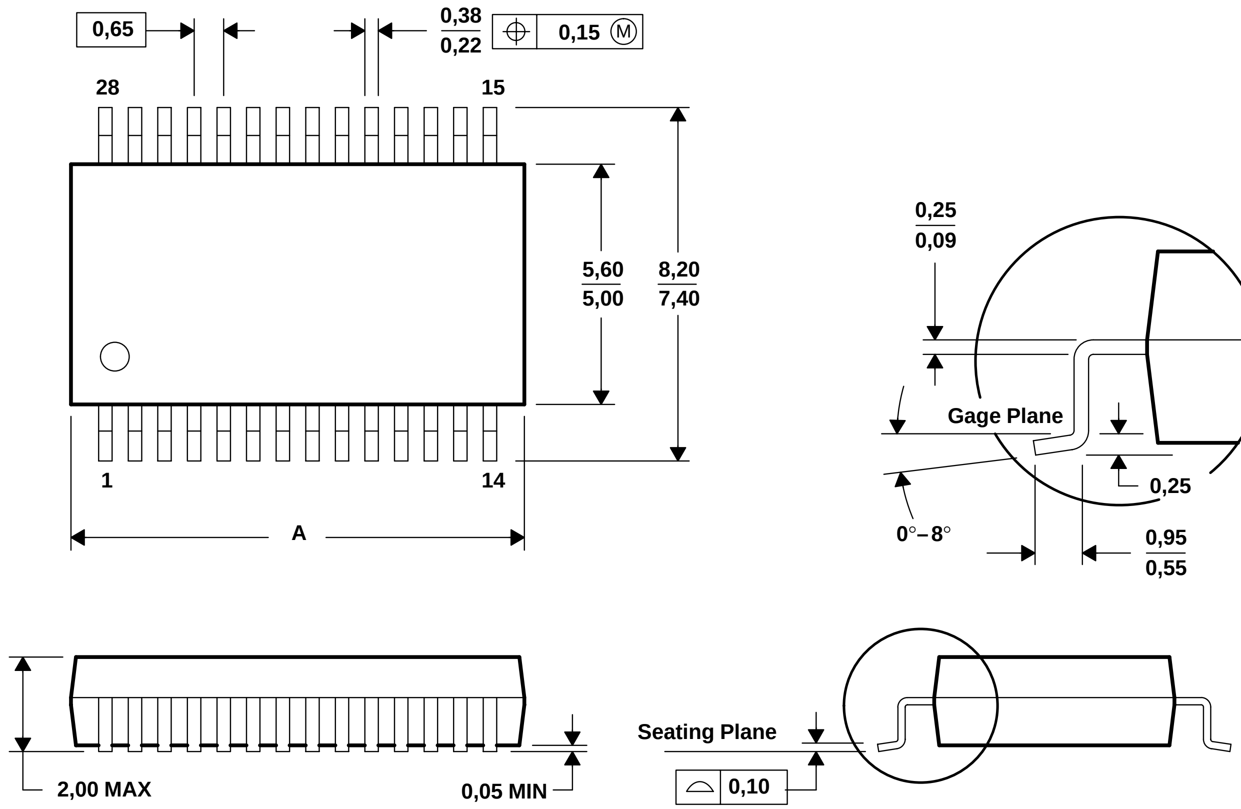
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150