CYPRESS

CY62167DV18
MoBL2™

PRELIMINARY

16M (1024K x 16) Static RAM

Features

- Very high speed: 55 ns and 70 ns
- Voltage range: 1.65V to 1.95V
- Ultra-low active power
  - Typical active current: 1.5 mA @ f = 1 MHz
  - Typical active current: 15 mA @ f = f_{MAX}
- Ultra-low standby power
- Easy memory expansion with CE</>1</>, CE2</> and OE</> features
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Packages offered in a 48-ball FBGA

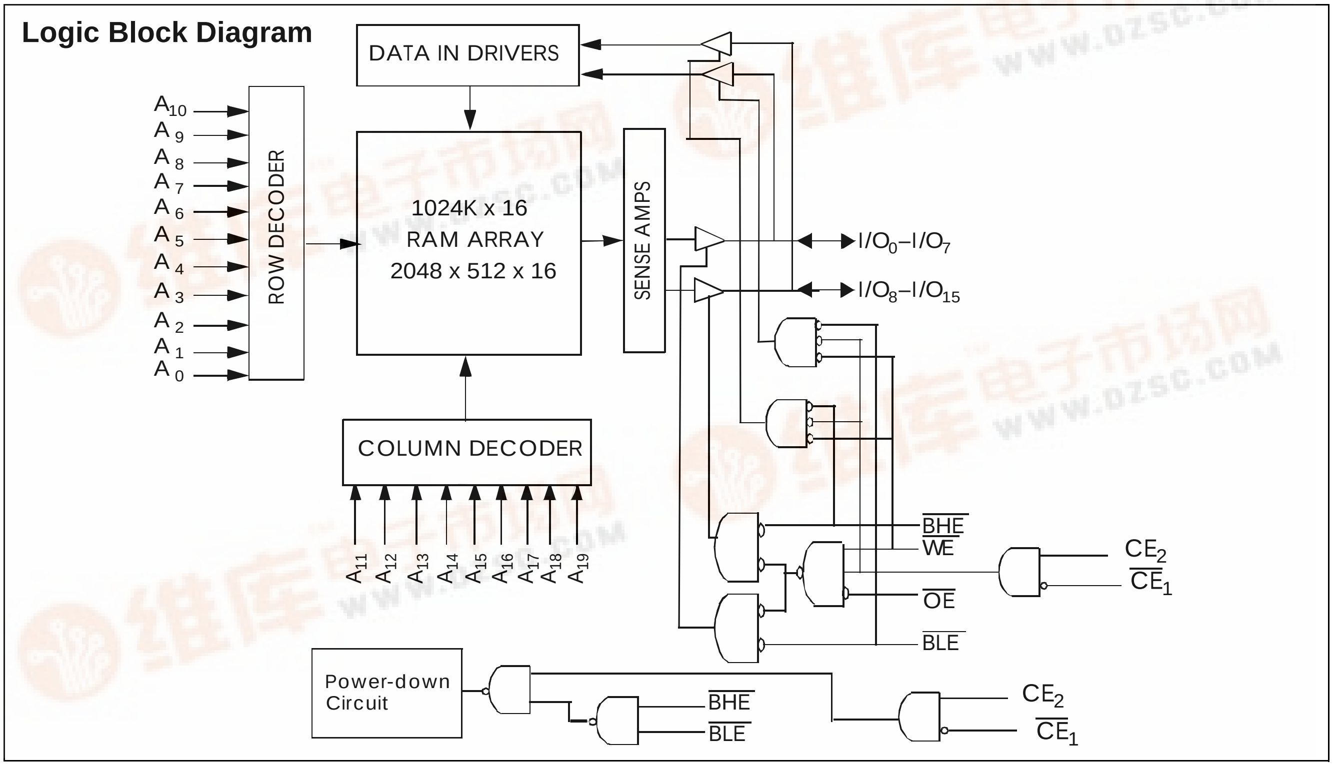
Functional Description[1]

The CY62167DV18 is a high-performance CMOS static RAM organized as 1024K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected Chip Enable 1 ($\overline{CE_1}$) HIGH or Chip Enable 2 (CE_2) LOW or both BHE and BLE are HIGH. The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected Chip Enable 1 (CE_1) HIGH or Chip Enable 2 (CE_2) LOW, outputs are disabled (OE HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH) or during a write operation (Chip Enable 1 (CE_1) LOW and Chip Enable 2 (CE_2) HIGH and WE LOW).

Writing to the device is accomplished by taking Chip Enable 1 (CE_1) LOW and Chip Enable 2 (CE_2) HIGH and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then das pins (A_0 through A_{19}). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the ad

Reading from the device is accomplished by taking Chip Enable 1 (CE_1) LOW and Chip Enable 2 (CE_2) HIGH and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (<>O_7. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of read and write modes.

Logic Block Diagram



Note:

1. For best practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Pin Configuration[2]

FBGA
Top View

1	2	3	4	5	6	
$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	CE_2	A
I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CE}_1$	I/O_0	B
I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2	C
V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	Vcc	D
V_{CC}	I/O_{12}	DNU	A_{16}	I/O_4	V_{SS}	E
I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6	F
I/O_{15}	A_{19}	A_{12}	A_{13}	$\overline{WE}$	I/O_7	G
A_{18}	A_8	A_9	A_{10}	A_{11}	DNU	H

Note:

2. DNU pins are to be connected to V_{SS} or left open.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with Power Applied..–55°C to +125°C

Supply Voltage to Ground Potential .... –0.2V to V_{CCMAX} + 0.2V

DC Voltage Applied to Outputs in High-Z State[3] ....–0.2V to V_{CC} + 0.2V

DC Input Voltage[3] .... –0.2V to V_{CC} + 0.2V

Output Current into Outputs (LOW)............................ 20 mA

Static Discharge Voltage... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current.. > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}[4]
Industrial	–40°C to +85°C	1.65V to 1.95V

Product Portfolio

Product	V_{CC} Range(V)			Speed (ns)	Power Dissipation					
					Operating, Icc (mA)				Standby, I_{SB2} (µA)	
					f = 1 MHz		f = f_{MAX}			
	Min.	Typ.	Max.		Typ.	Max.	Typ.	Max.	Typ.	Max.
CY62167DV18L	1.65	1.8	1.95	55	1.5	5	15	30	2.5	30
				70			12	25	2.5	30
CY62167DV18LL	1.65	1.8	1.95	55	1.5	5	15	30	2.5	20
				70			12	25	2.5	20

DC Electrical Characteristics (over the operating range)

Parameter	Description	Test Conditions		CY62167DV18-55			CY62167DV18-70			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 1.65V	1.4			1.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 1.65V			0.2			0.2	V
V_{IH}	Input HIGH Voltage			1.4		V_{CC} + 0.2	1.4		V_{CC} + 0.2	V
V_{IL}	Input LOW Voltage			–0.2		0.4	–0.2		0.4	V
I_{IX}	Input Leakage Current	GND $\leq V_I \leq V_{CC}$		–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled		–1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	Vcc = 1.95V, I_{OUT} = 0mA, CMOS level		15	30		12	25	mA
		f = 1 MHz			1.5	5		1.5	5	
I_{SB1}	Automatic CE Power-down Current – CMOS Inputs	$\overline{CE}_1 \geq V_{CC}$ – 0.2V, $CE_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, $V_{IN} \leq$ 0.2V, f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$)	L		2.5	30		2.5	30	µA
			LL		2.5	20		2.5	20	
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs	$\overline{CE}_1 \geq V_{CC}$ – 0.2V, $CE_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V, f = 0, V_{CC}=1.95V	L		2.5	30		2.5	30	µA
			LL		2.5	20		2.5	20	

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	TA = 25°C, f = 1 MHz $V_{CC} = V_{CC(typ)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit

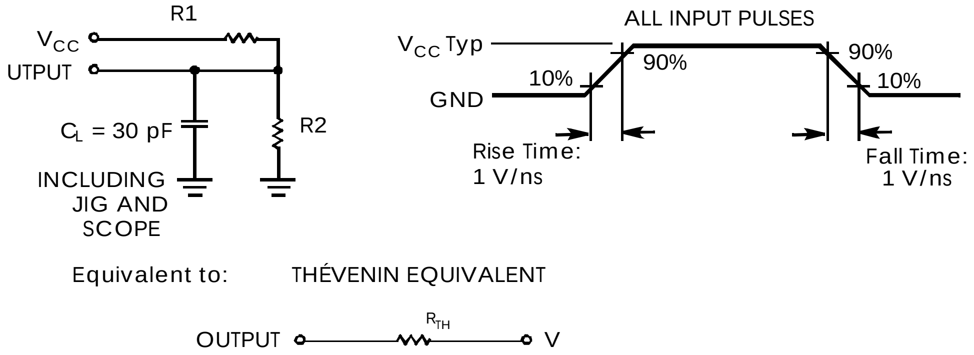
Notes:

3. $V_{IL(min.)} = -2.0V$ for pulse durations less than 20 ns.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25°C$.
5. Tested initially and after any design or proces changes that may affect these parameters.

Thermal Resistance

Parameter	Description	Test Conditions	BGA	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient)[5]	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	C/W
θ_{JC}	Thermal Resistance (Junction to Case)[5]		16	C/W

AC Test Loads and Waveforms

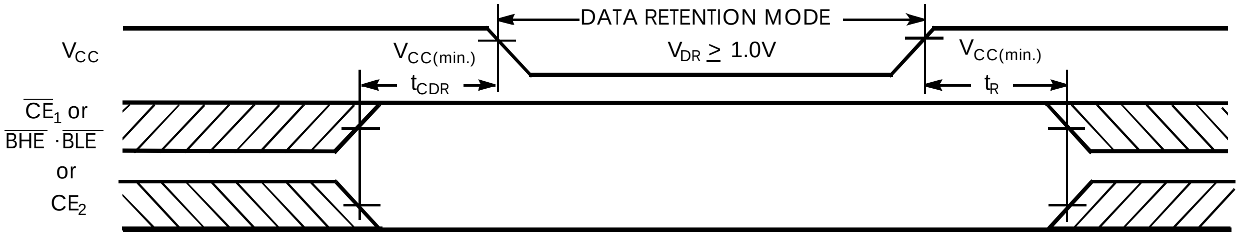


Parameters	1.8V	UNIT
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Data Retention Characteristics

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.0		1.95	V
I_{CCDR}	Data Retention Current	V_{CC}=1.0V, $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L			15	µA
			LL			10	
t_{CDR}[5]	Chip Deselect to Data Retention Time			0			ns
t_R[6]	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform[7]



Notes:

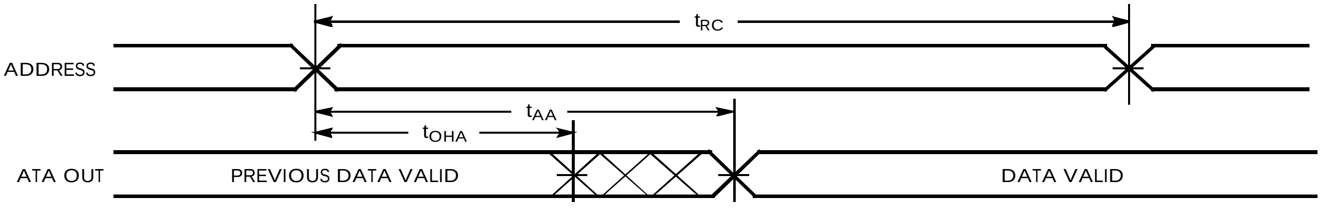
6. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)}$ > 100 µs or stable at $V_{CC(min.)}$ > 100 µs.
7. 7. $\overline{BHE} \cdot \overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics (over the operating range)[8]

Parameter	Description	CY62167DV18-55		CY62167DV18-70		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}_1$ LOW or CE_2 HIGH to Data Valid		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9, 11]		20		25	ns
t_{LZCE}	$\overline{CE}_1$ LOW or CE_2 HIGH to Low Z[9]	10		10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to High Z[9, 11]		20		25	ns
t_{PU}	$\overline{CE}_1$ LOW or CE_2 HIGH to Power-up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to Power-down		55		70	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Data Valid		55		70	ns
t_{LZBE}[10]	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z[9]	5		5		ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to High-Z[9, 11]		20		25	ns
Write Cycle[12]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	$\overline{CE}_1$ LOW or CE_2 HIGH to Write End	40		60		ns
t_{AW}	Address Set-up to Write End	40		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		45		ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to Write End	45		60		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[9, 11]		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9]	10		10		ns

Switching Waveforms

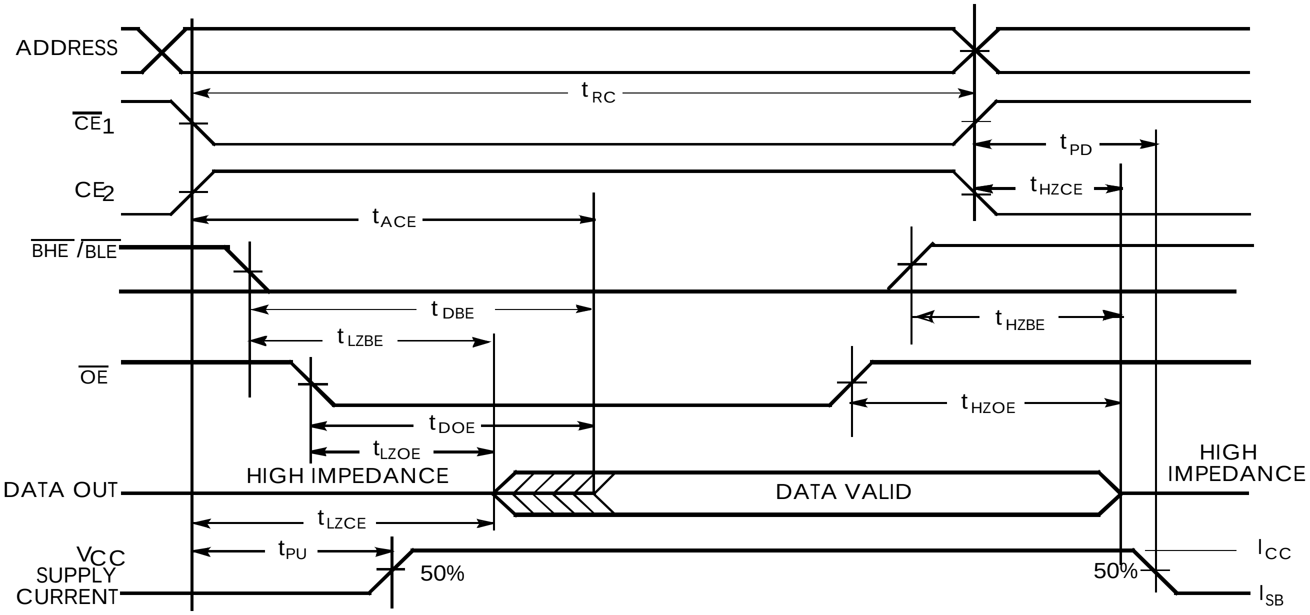
Read Cycle No. 1 (Address Transition Controlled)[13, 14]



Notes:

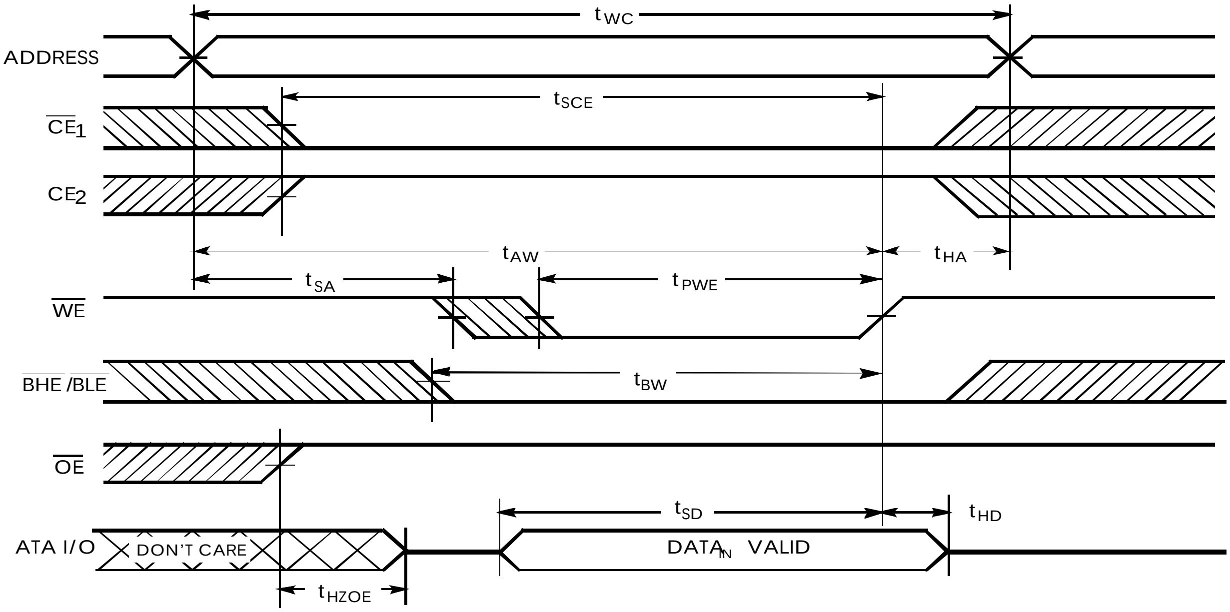
8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ.)/2}$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. If both byte enables are toggled together, this value is 10 ns.
11. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
12. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$.
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, $CE_{2<Def>}$
14. $\overline{WE}$ is HIGH for Read cycle.

Read Cycle No. 2 ($\overline{OE}$ Controlled)[14, 15]



Switching Waveforms (continued)

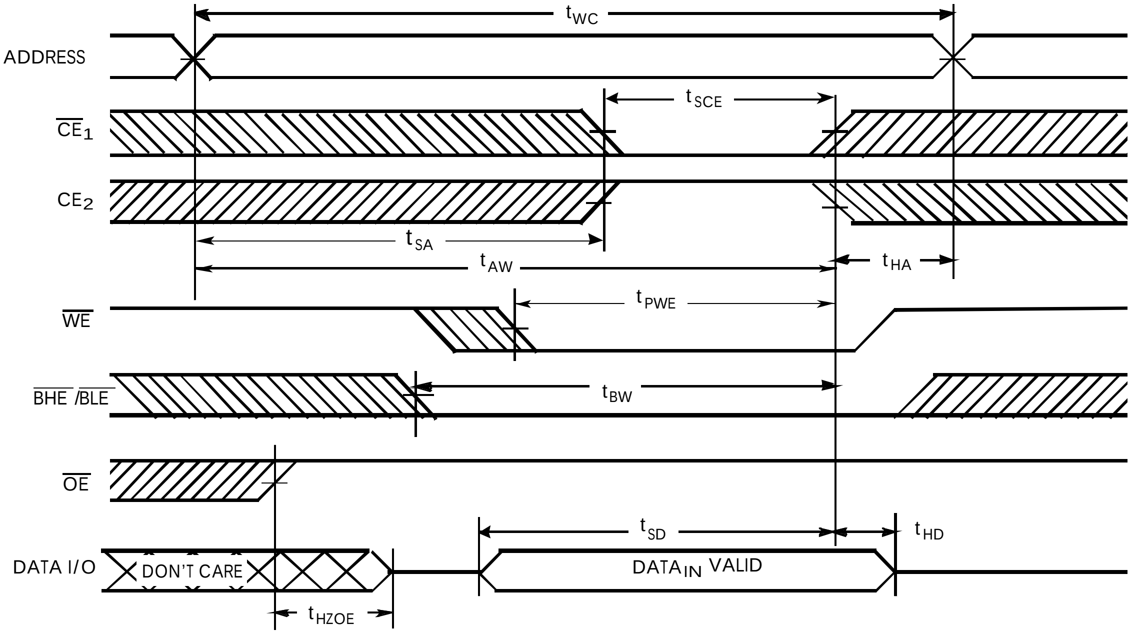
Write Cycle No. 1 ($\overline{WE}$ Controlled)[12, 16, 17, 18]



Note:

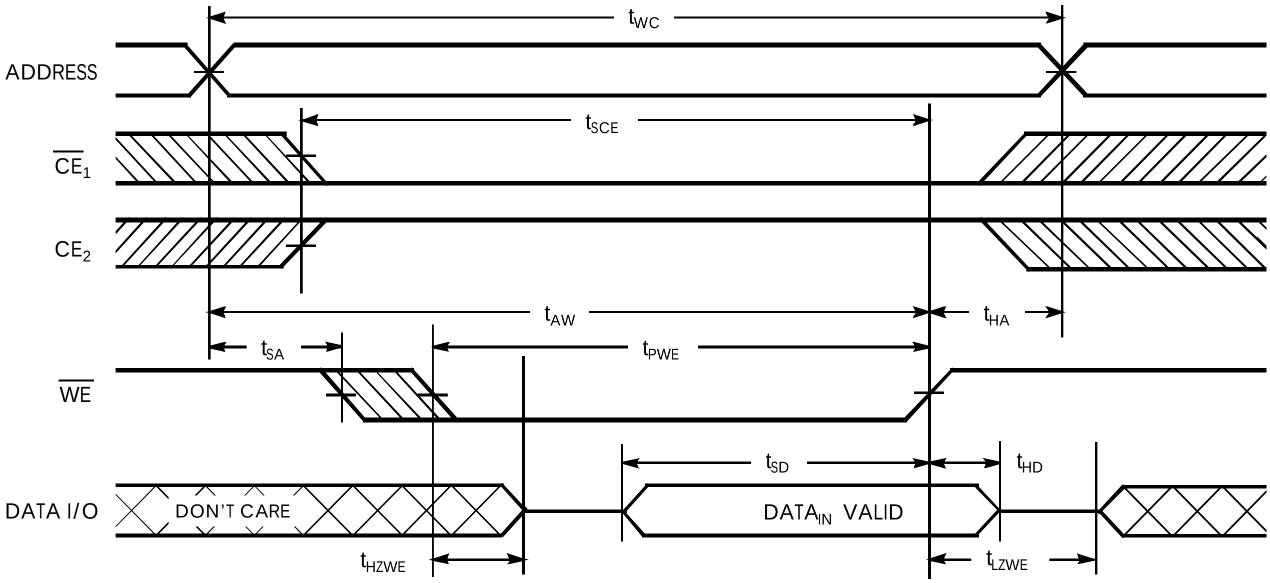
15. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Write Cycle No. 2 (CE</>1</> or CE</>2</> Controlled)[12, 16, 17, 18]

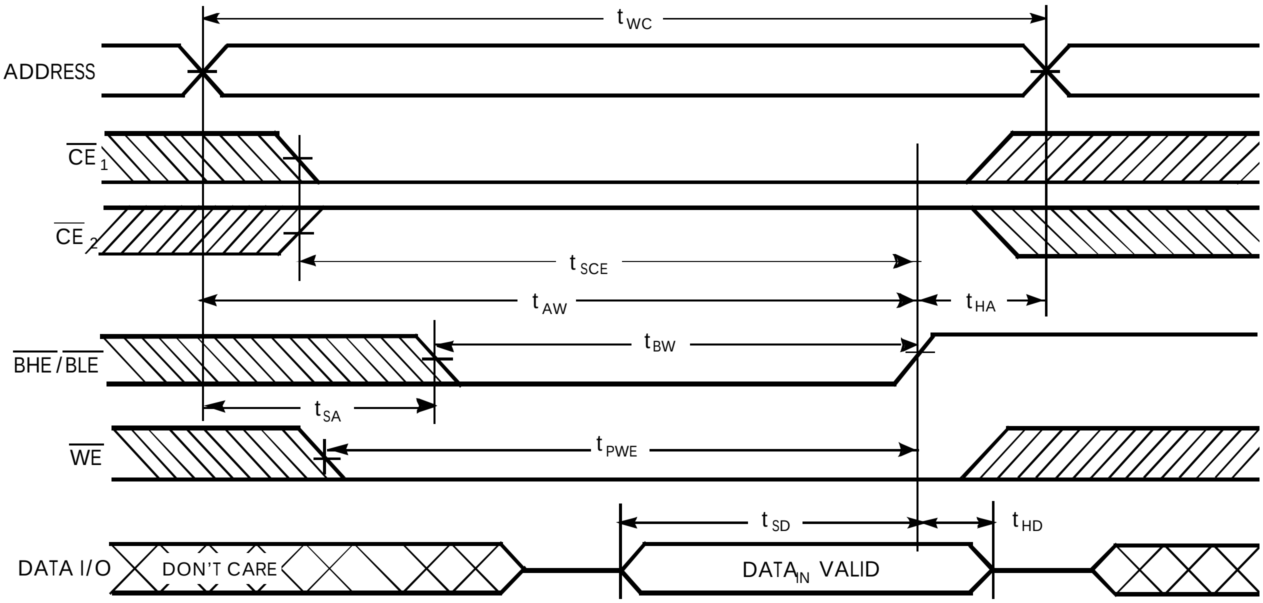


Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[17, 18]



Write Cycle No. 4 (BHE</>/BLE</> Controlled, OE</> LOW)</>[17]



Notes:

16. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
17. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
18. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Truth Table

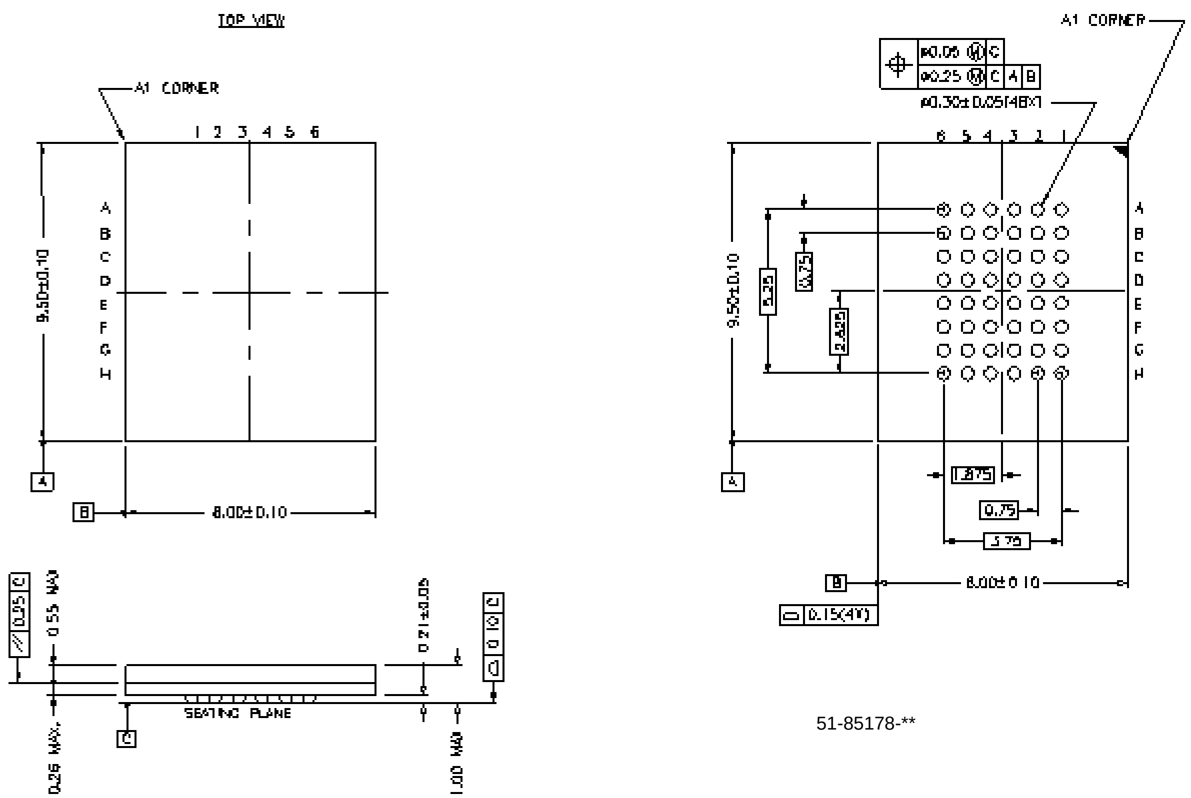
$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Input / Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O0–I/O15)	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O0–I/O7); High Z (I/O8–I/O15)	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O0–I/O7); Data Out (I/O8–I/O15)	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O0–I/O15)	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O0–I/O7); High Z (I/O8–I/O15)	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O0–I/O7); Data In (I/O8–I/O15)	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62167DV18L-55**I	TBD	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	Industrial
	CY62167DV18LL-55**I	TBD	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	
70	CY62167DV18L-70**I	TBD	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	Industrial
	CY62167DV18LL-70**I	TBD	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	

Package Diagram

48-lead VFBGA (8 x 9.5 x 1 mm) BV48B



51-85178-**

MoBL is a registered trademark, and MoBL2 and More Battery Life are trademarks of Cypress Semiconductor. All product and company names mentioned in this document are the trademarks of their respective holders.

Document History Page

Document Title: CY62167DV18MoBL2™ 16M (1024K x 16) Static RAM **Document Number: 38-05326**				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	118406	09/30/02	GUG	New Data Sheet
*A	123690	02/11/03	DPM	Changed Advance to Preliminary Added package diagram