

**SWITCHING  
N-CHANNEL POWER MOS FET**

**DESCRIPTION**

The  $\mu$ PA2707GR is N-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of notebook computer.

**FEATURES**

- Low on-state resistance  
 $R_{DS(on)1} = 4.3 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 9.0 \text{ A)}$   
 $R_{DS(on)2} = 5.6 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 9.0 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 6600 \text{ pF TYP. (} V_{DS} = 10 \text{ V, } V_{GS} = 0 \text{ V)}$
- Small and surface mount package (Power SOP8)

**ORDERING INFORMATION**

PART NUMBER	PACKAGE
$\mu$ PA2707GR-E1	Power SOP8
$\mu$ PA2707GR-E1-A <sup>Note</sup>	Power SOP8
$\mu$ PA2707GR-E2	Power SOP8
$\mu$ PA2707GR-E2-A <sup>Note</sup>	Power SOP8

**Note** Pb-free (This product does not contain Pb in external electrode and other parts.)

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C, All terminals are connected.)**

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	30	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC)	I <sub>D(DC)</sub>	±19	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±76	A
Total Power Dissipation <sup>Note2</sup>	P <sub>T1</sub>	1.1	W
Total Power Dissipation (PW = 10 sec) <sup>Note2</sup>	P <sub>T2</sub>	2.5	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Single Avalanche Current <sup>Note3</sup>	I <sub>AS</sub>	19	A
Single Avalanche Energy <sup>Note3</sup>	E <sub>AS</sub>	36	mJ

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

**2.** Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm

**3.** Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 15 V, R<sub>G</sub> = 25 Ω, L = 100 μH, V<sub>GS</sub> = 20 → 0 V

**THERMAL RESISTANCE**

Channel to Ambient <sup>Note</sup>	R <sub>th(ch-A)</sub>	114	°C/W
Channel to Drain Lead <sup>Note</sup>	R <sub>th(ch-L)</sub>	22	°C/W

**Note** Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm

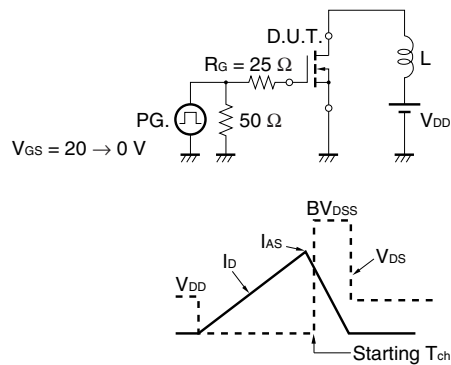
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**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)**

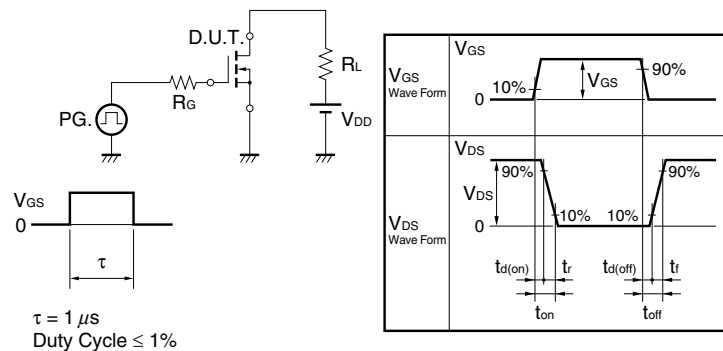
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.0		2.5	V
Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 A	12			S
Drain to Source On-state Resistance <sup>Note</sup>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		3.3	4.3	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		4.1	5.6	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		6600		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		970		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		530		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 10 A		24		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V		29		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		130		ns
Fall Time	t <sub>f</sub>			39		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 15 V		52		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 5 V		16		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 19 A		18		nC
Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-D)</sub>	I <sub>F</sub> = 19 A, V <sub>GS</sub> = 0 V		0.8		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 19 A, V <sub>GS</sub> = 0 V		42		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		41		nC
Gate Resistance	R <sub>G</sub>	f = 1 MHz		1.2		Ω

**Note** Pulsed

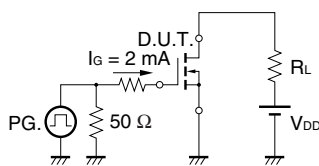
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



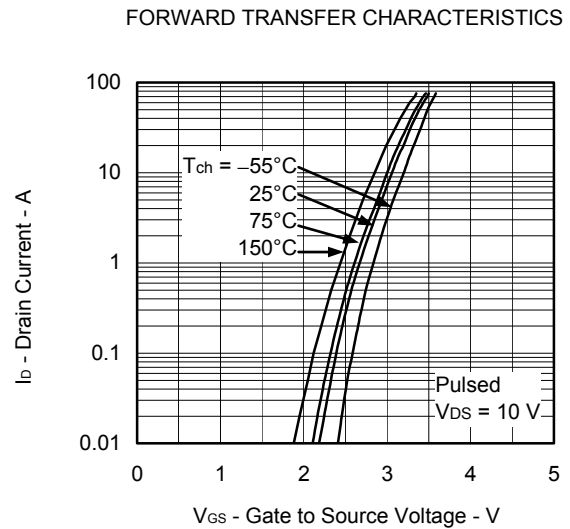
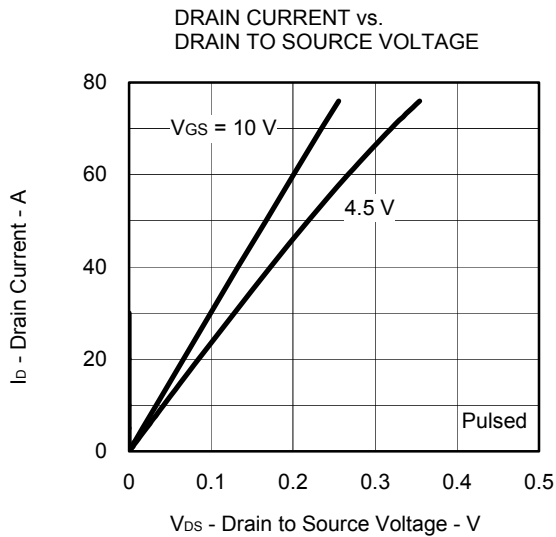
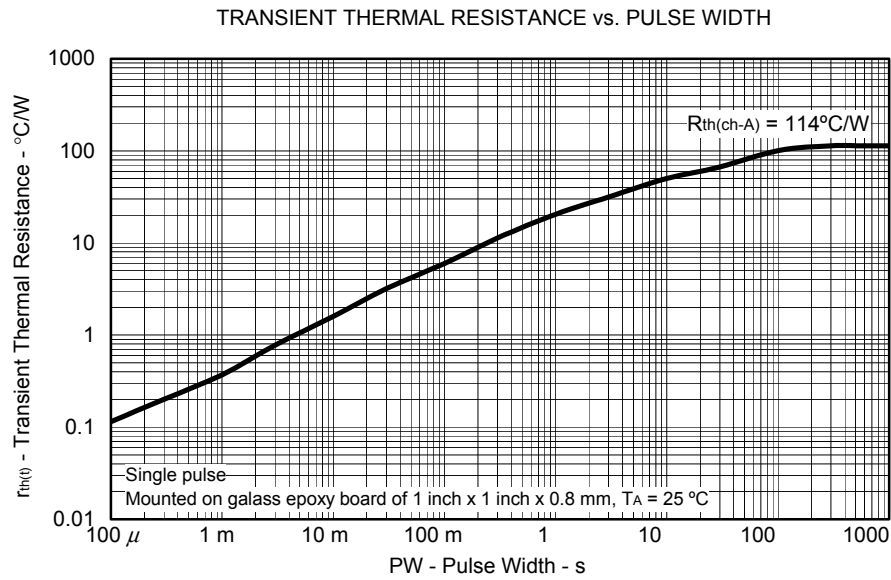
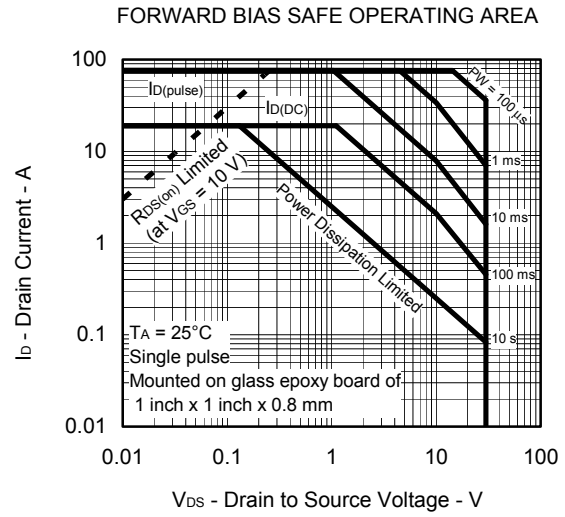
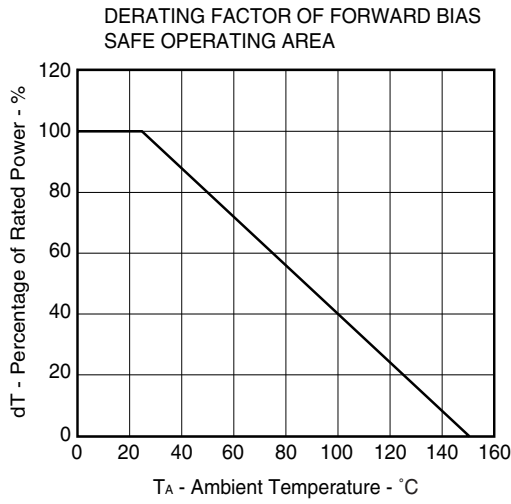
**TEST CIRCUIT 2 SWITCHING TIME**



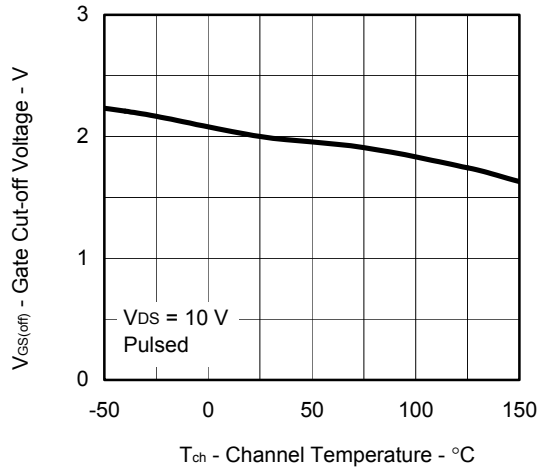
**TEST CIRCUIT 3 GATE CHARGE**



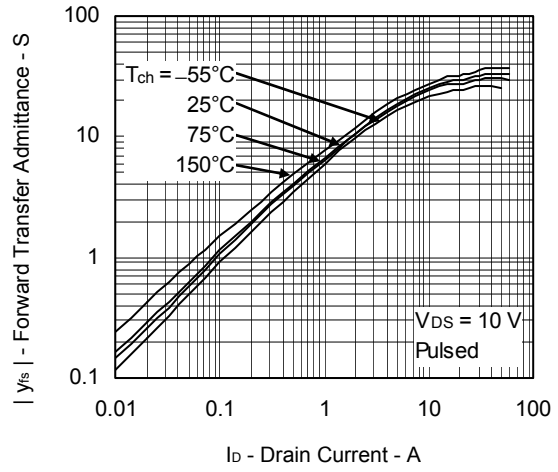
TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )



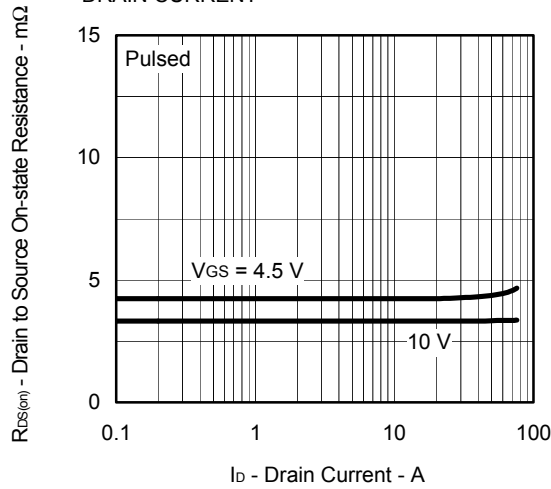
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



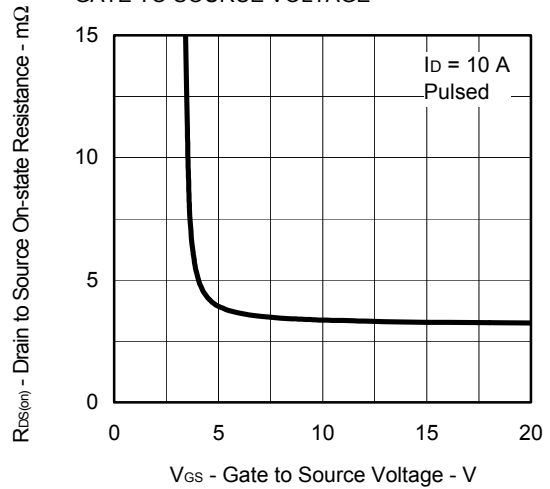
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



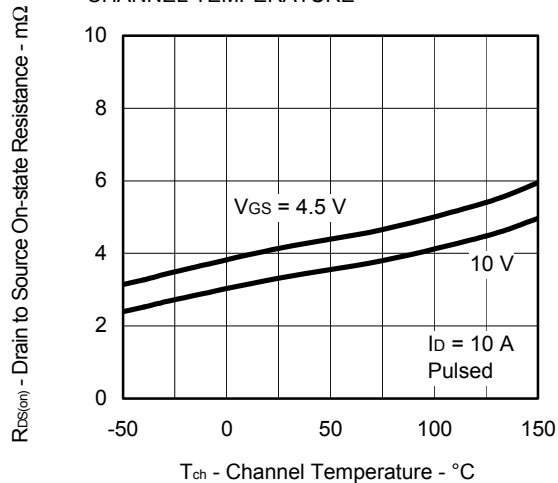
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



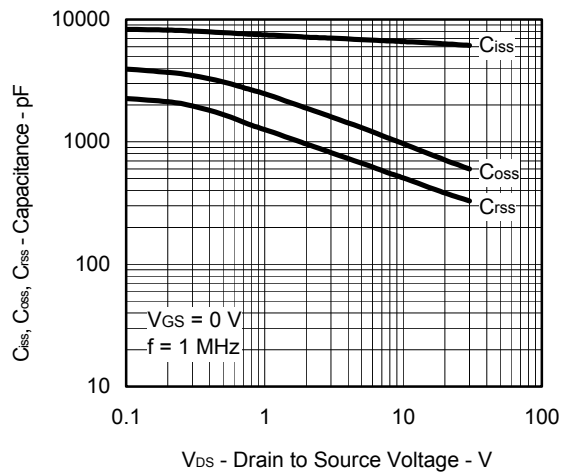
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



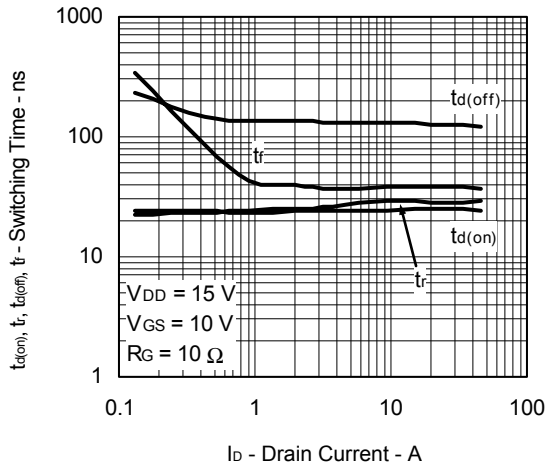
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



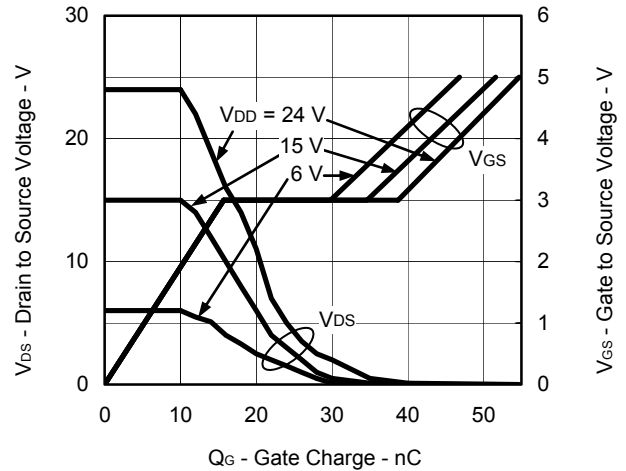
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



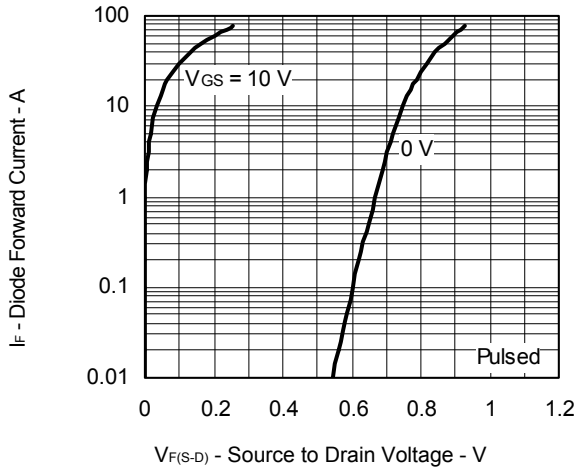
SWITCHING CHARACTERISTICS



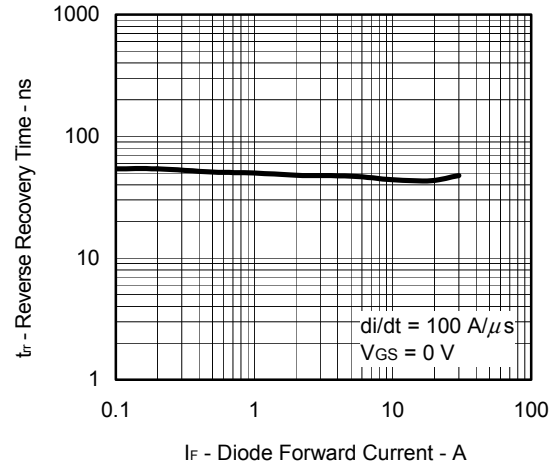
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



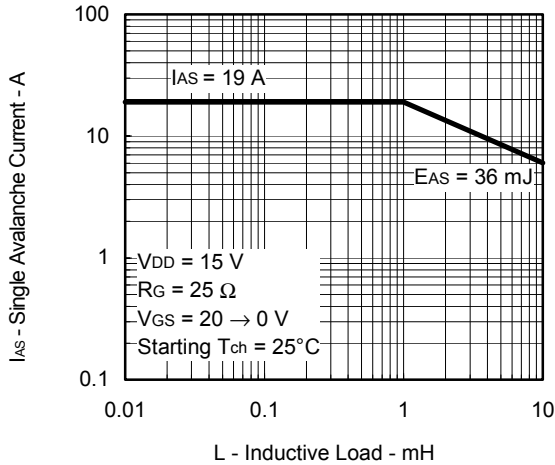
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



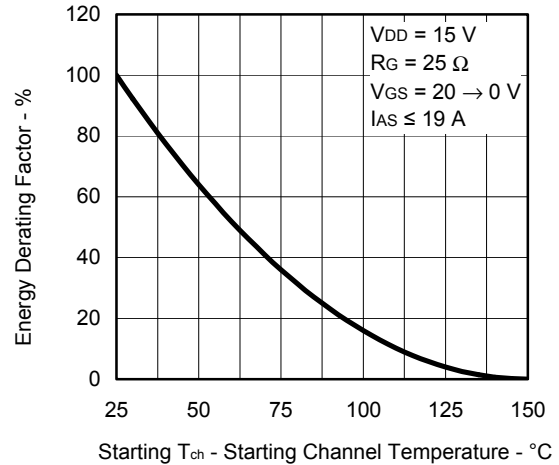
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

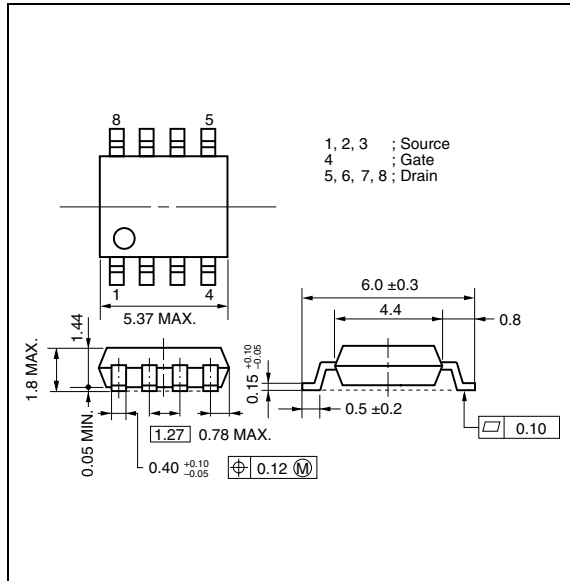


SINGLE AVALANCHE ENERGY DERATING FACTOR

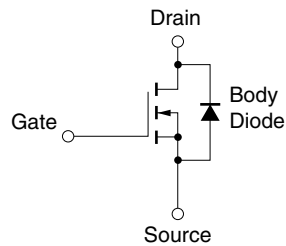


PACKAGE DRAWING (Unit: mm)

Power SOP8



EQUIVALENT CIRCUIT



**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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