



Edge118 Low Skew Clock Spreader

EDGE HIGH-PERFORMANCE PRODUCTS

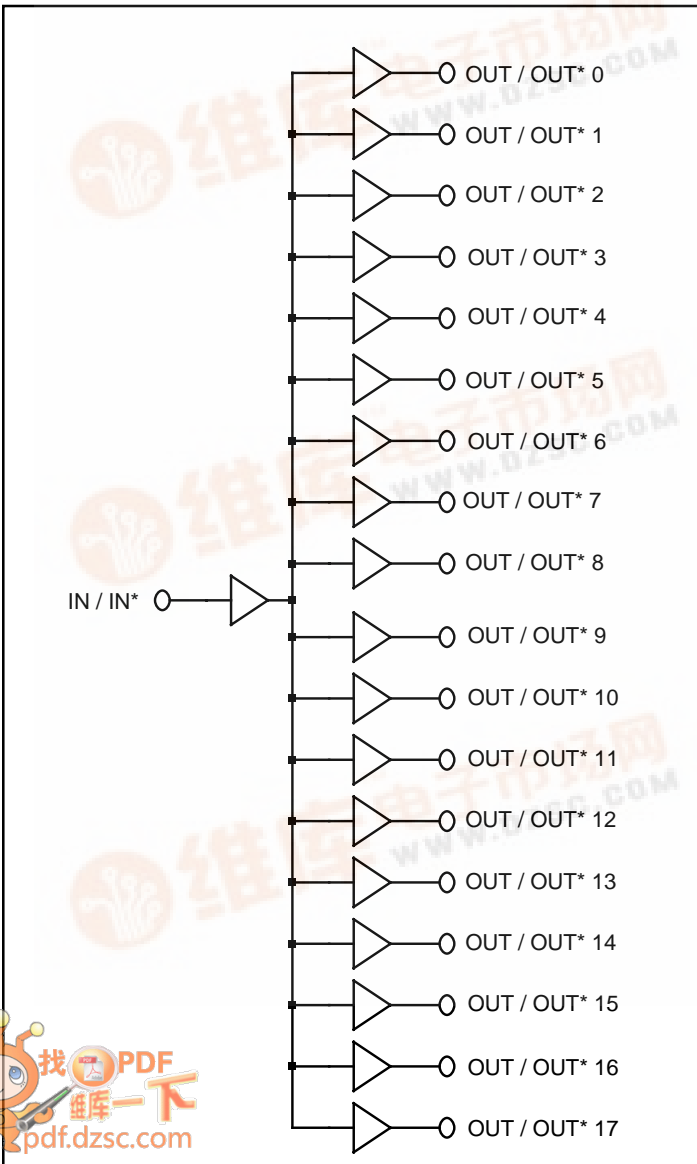
Description

The Edge118 is a fully differential 1:18 clock spreader. Manufactured in a high performance bipolar process, the Edge118 is designed to accurately fan out a multitude of clock signals with low channel to channel skew.

Features

- Low Timing Error vs. Duty Cycle & Frequency
- Low Channel to Channel Skew
- Small Footprint (64 MQFP Package, 14 mm X 14 mm Body)

Functional Block Diagram



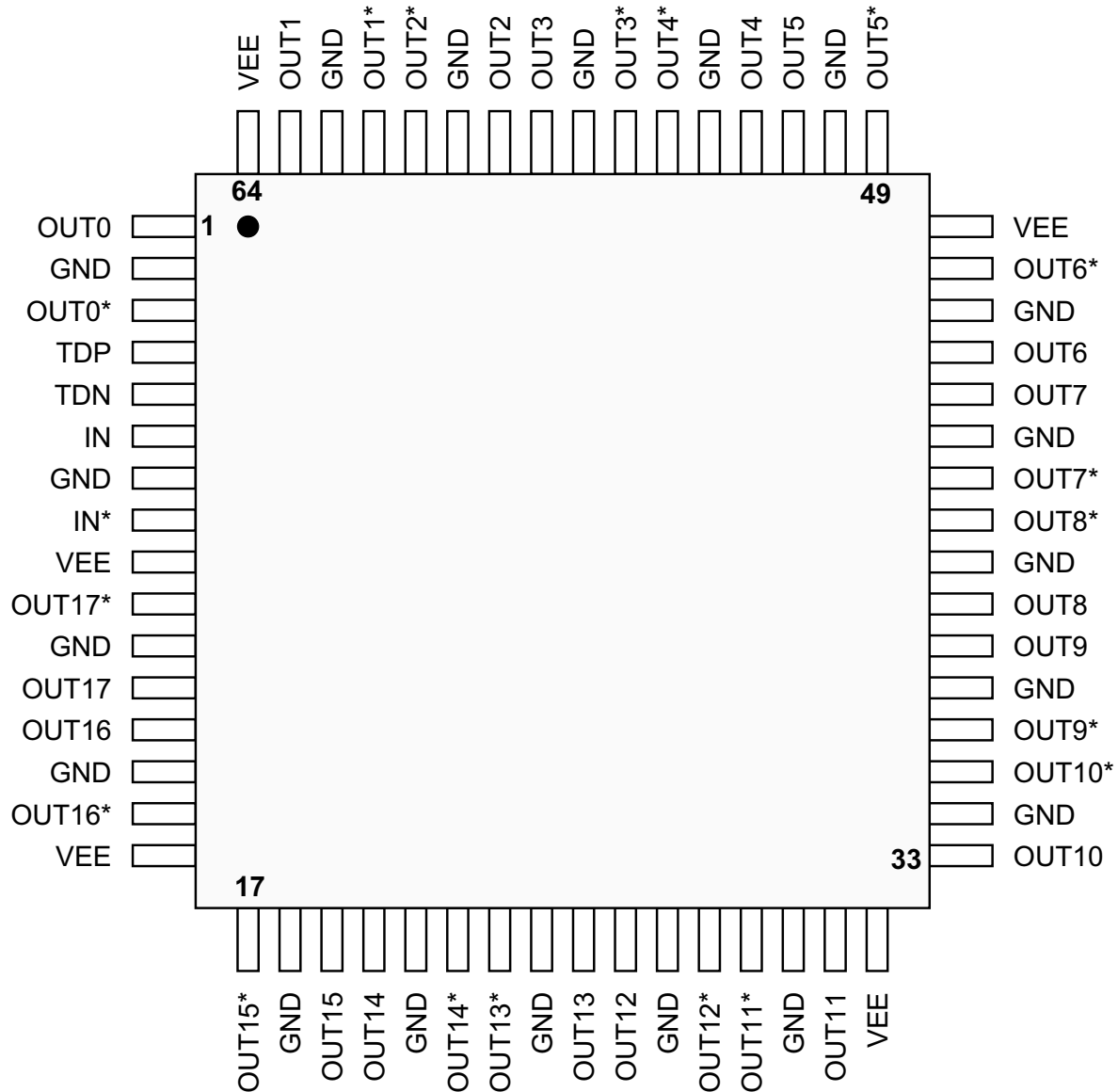
Applications

- Test Equipment



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PIN Description

Pin Name	Pin #	Description
IN, IN*	6, 8	Differential input signal.
OUT0, OUT0*	1, 3	Differential ECL output signals.
OUT1, OUT1*	63, 61	
OUT2, OUT2*	58, 60	
OUT3, OUT3*	57, 55	
OUT4, OUT4*	52, 54	
OUT5, OUT5*	51, 49	
OUT6, OUT6*	45, 47	
OUT7, OUT7*	44, 42	
OUT8, OUT8*	39, 41	
OUT9, OUT9*	38, 36	
OUT10, OUT10*	33, 35	
OUT11, OUT11*	31, 29	
OUT12, OUT12*	26, 28	
OUT13, OUT13*	25, 23	
OUT14, OUT14*	20, 22	
OUT15, OUT15*	19, 17	
OUT16, OUT16*	13, 15	
OUT17, OUT17*	12, 10	
<i>Power Supplies</i>		
GND	2, 7, 11, 14, 18, 21, 24, 27, 30, 34, 37, 40, 43, 46, 50, 53, 56, 59, 62	Positive Power Supply
VEE	9, 16, 32, 48, 64	Negative Power Supply
TDP, TDN	4, 5	Thermal Diode Connections



Chip Overview

The Edge118 is a clock distribution chip designed to take one input signal (IN / IN*) and fan it out 18 times to identical outputs (OUT / OUT*). The chip is designed to minimize channel to channel skew and any timing jitter.

The part's wide fanout is extremely useful in applications where many distinct copies of a signal are required on one PC Board, and these signals must all be aligned. This signal can be distributed without creating a distribution tree using multiple devices.

Inputs

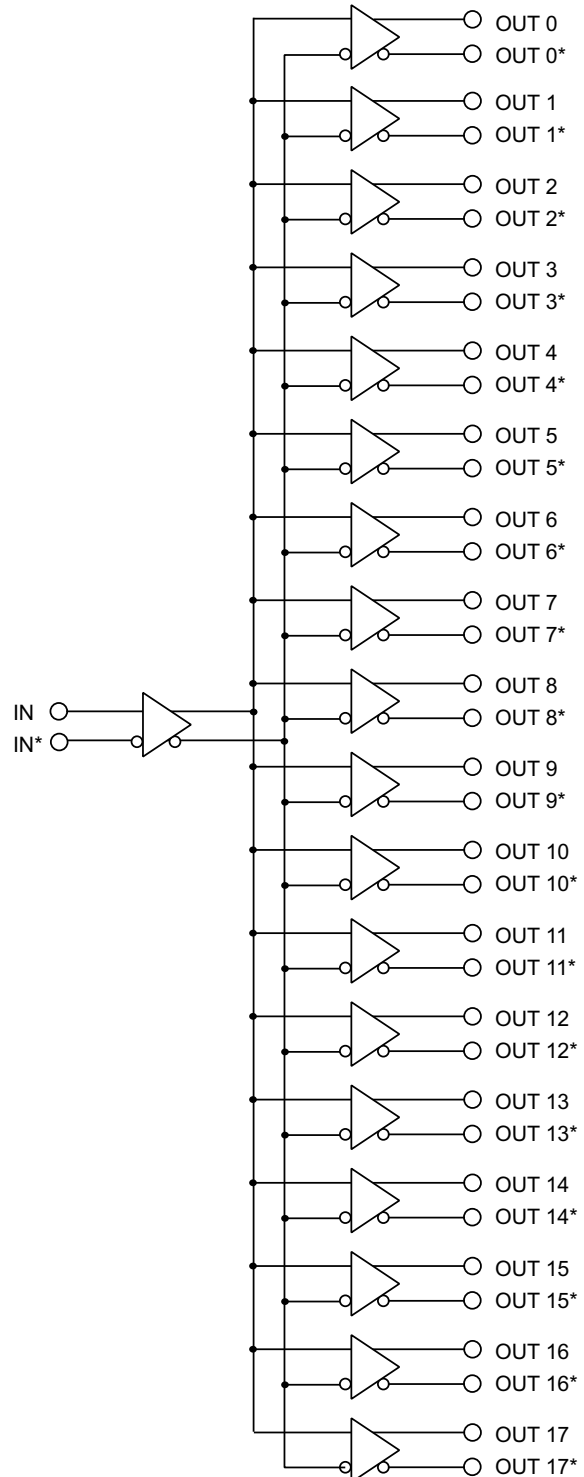
The input signal is differential, requiring 250 mV swings for full performance operation. The inputs are ECL compatible, but may also be operated over a common mode voltage range between $V_{EE} + 1.3V$ and $V_{CC} - .5V$.

Outputs

The outputs are ECL compatible differential signals with 800 mV voltage swings centered around 1.3V below GND.

Operating Frequency

The Edge118 is designed to maintain full performance up to at least 1000 MHz and pass 500 ps pulses.



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A .1 μ F or .01 μ F capacitor (with excellent high frequency characteristics, is recommended between GND and VEE. In addition, solid GND and VEE planes are recommended to provide a low inductance path for the power supply currents.

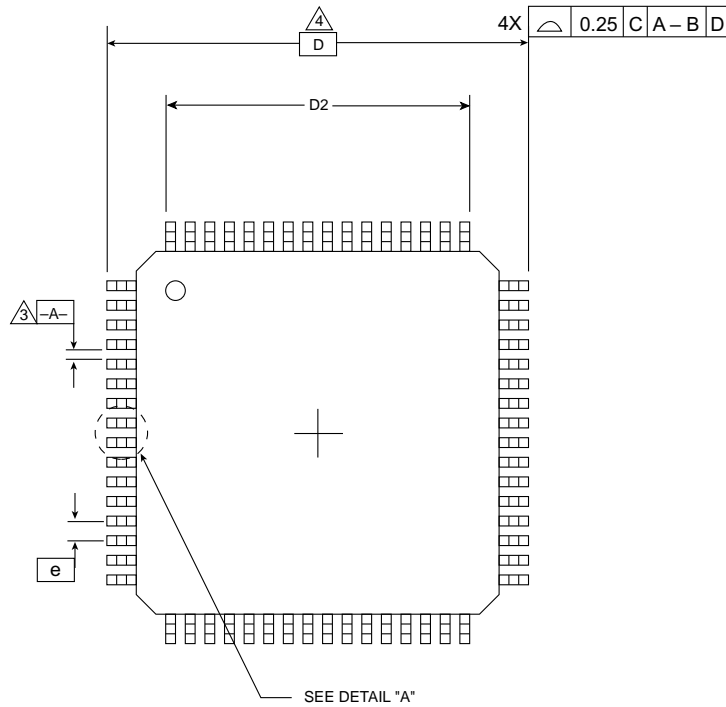
Output Terminations

For optimal results, all output pairs (used or unused) should be terminated, and terminated in the same manner.

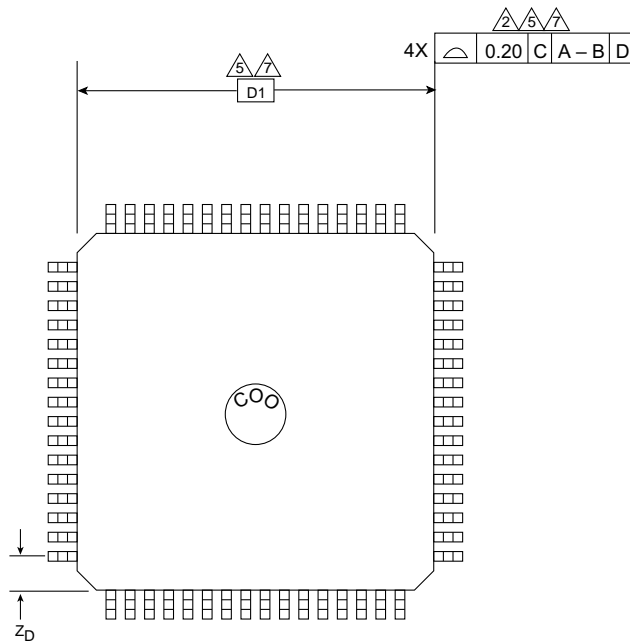
Thermal Information

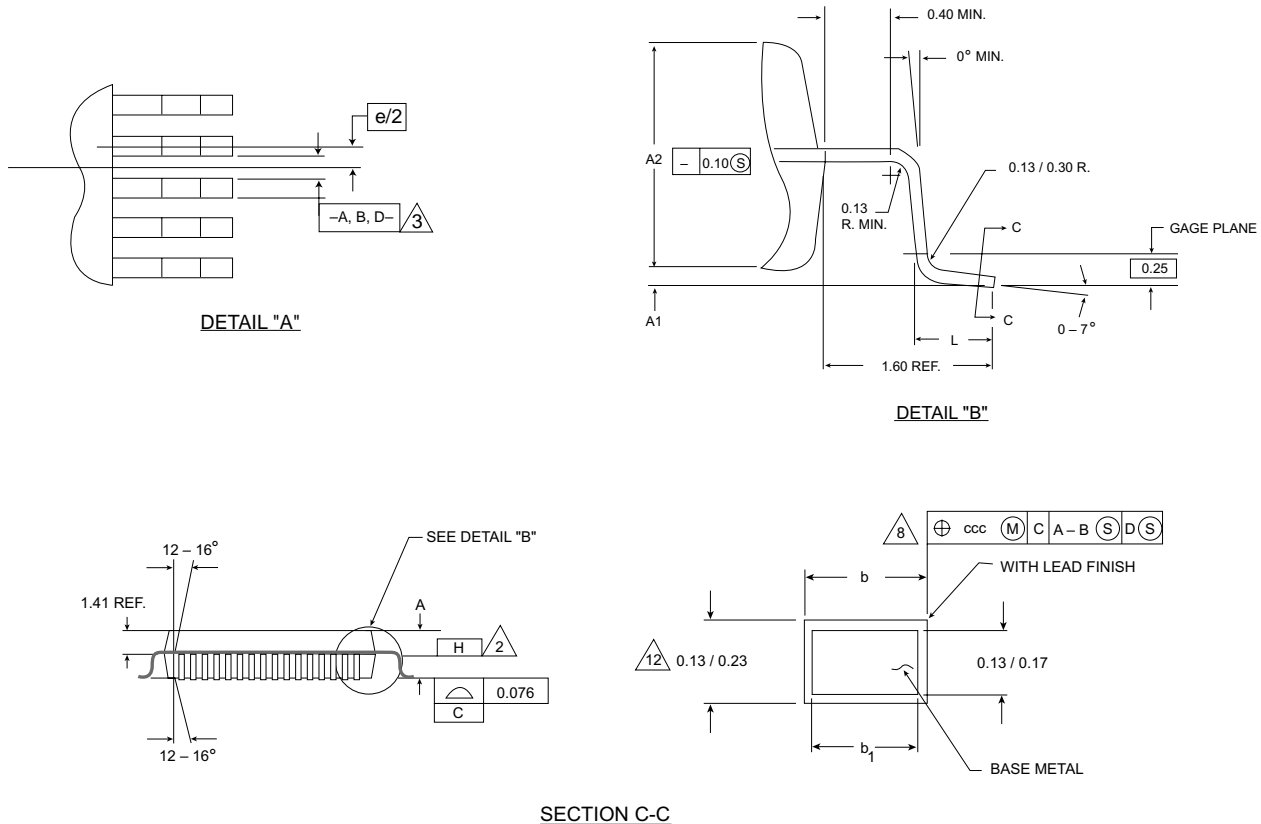
Parameter	Symbol	Value	Units
Thermal Resistance (300 LFM, part soldered to a PC Board)			
Junction to Air	θ JA	~25	$^{\circ}$ C / W

Top View



Bottom View



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Package Information (continued)

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined at centerline between leads where leads exit plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane -H-.
6. "N" is the total # of terminals.
7. Package top dimensions are smaller than bottom dimensions by 0.20 mm, and top of package will not overhang bottom of package.
8. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
9. All dimensions are in millimeters.
10. Maximum allowable die thickness to be assembled in this package family is 0.635 millimeters.
11. This drawing conforms to JEDEC registered outlines MO-108 and MS-022.
12. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

**JEDEC Variation
All Dimensions in Millimeters**

	AC			Note
	Min.	Nom.	Max.	
A		2.82	3.00	
A1	0.10	0.15	0.25	
A2	2.55	2.67	2.75	
D	17.20 BSC.			4
D1	14.00 BSC.			5
D2	12.00 BSC.			
Z0	1.00 REF.			
E	17.20 BSC.			4
E1	14.00 BSC.			5
E2	12.00 BSC.			
ZE	1.00 REF.			
L	0.73	.088	1.03	
N	64			6
e	0.80 BSC.			
b	0.30		0.45	
b1	0.30	0.35	0.40	
ccc	0.16			

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Power Supply	GND	0	0	0	V
Negative Analog Power Supply	VEE	-5.5		-4.2	V
Junction Temperature	TJ			+125	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Total Analog Power Supply	GND – VEE	-7.0		0	V
Digital Inputs	IN / IN*	VEE – .5		GND + .5	V
Ambient Operating Temperature	TA			+125	°C
Storage Temperature		-55		+150	°C
Junction Temperature	TJ	-65		+150	°C
Soldering Temperature				260	°C

Stresses above listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
IN / IN*					
Input High Voltage	IN – IN*	200			mV
Input Low Voltage	IN* – IN	200			mV
Input Bias Current	I _{in}	-250		250	μA
Input Common Mode Range	IN, IN*	VEE + 1.3		GND – .5	V
OUT / OUT*					
Output Current	I _{out DC}				
Output High Voltage	OUT – OUT*	600	800		mV
Output Low Voltage	OUT* – OUT	600	800		mV
Output Common Mode Range	$\frac{OUT - OUT^*}{2}$	-1.5	-1.3	-1.1	V
Supply Current		225	275	325	mA

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AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delay IN / IN* to OUT / OUT* (Notes 1, 5) Channel-to-Channel Skew (Note 6)	Tpd	450	550 <25	650 100	ps ps
Maximum Operating Frequency (Notes 1, 2, 3, 4)	Fmax	1000	>1200		MHz
Minimum Pulse Width (Notes 1, 2, 3, 4)	PW min		400	500	ps
Output Rise and Fall Times (Notes 1, 4) 20% - 80%, 50Ω Load 10% - 90%, 50Ω Load	Tr / Tf Tr / Tf		260 400	400 500	ps ps
Jitter (Notes 1, 4) Peak-to-Peak			<.1	1	ps
ΔTpd vs. Duty Cycle, T = 100 ns (Notes 1, 4) 3.0% ≤ Duty Cycle ≤ 97% 0.5% ≤ Duty Cycle ≤ 99.5%	ΔTpd ΔTpd		<10 <25		ps ps
ΔTpd vs. Frequency (Notes 1, 4) 10 MHz ≤ Frequency ≤ 1.0 GHz	ΔTpd		<30		ps
Temperature Coefficient (Notes 1, 4)	ΔTpd		1		ps / °C

Note 1: Measured in a terminated 50Ω transmission line environment.

Note 2: And still maintain 80% amplitude.

Note 3: And still maintain a propagation delay variation (measured at the differential crossing points) of TPD ± 30 ps.

Note 4: This parameter is guaranteed by characterization. It is not production tested against the specification limit.

Note 5: This parameter is guaranteed by design and characterization. It is production tested against tester limits of Tpd = 550 ps ± 200 ps.

Note 6: This parameter is guaranteed by design and characterization. It is production tested against a tester limit of 160 ps.



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Ordering Information

Model Number	Package
E118AHF	64-pin MQFP 14 mm x 14 mm Body w/Internal Spreader
D118	Die Form
EVM118AHF	Edge118 Evaluation Module

Contact Information

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