SEMTECH

Edge142
Per Pin timing Deskew w 4x2 Cross Point Switch

EDGE HIGH-PERFORMANCE PRODUCTS

Description

The Edge142 is a 4 X 2 cross point switch with output edge deskew capability. Manufactured in a high performance bipolar process, it is designed primarily for channel deskew applications in VLSI and Mixed-Signal test equipment.

Any of the four input signals may be selected as the source for either output. The 142 performs test head multiplexing, adjacent channel multiplexing, and signal buffering for both the drive and receive signals, in addition to timing deskew.

The delay value (and resolution) is controlled via an external voltage DAC. The delay element is designed specifically to be monotonic and very stable while delaying a very narrow pulse over a limited delay range.

The part offers separate delays for rising vs. falling edges. The rising edge delay range is 1.5 ns and the falling edge adjustment range is 300 ps.

The Edge142 is also well suited for 1:2 or 1:4 signal fanout applications that require:

- multiple signal sources
- output enable / disable
- timing deskew on the output signals.

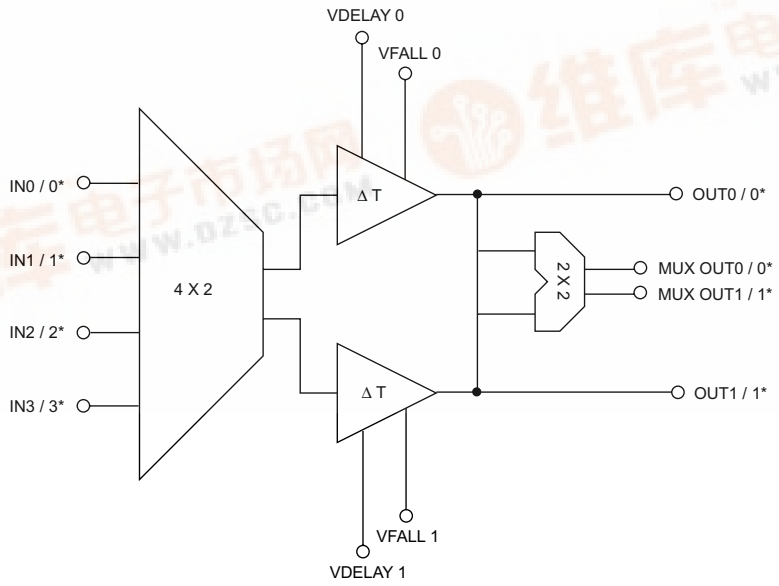
Features

- Very Narrow (<1 ns) Pulse Width Capability
- Fmax > 850 MHz
- Independent Delay Adjustments for Positive and Negative Transitions
- Delay Range of 1.5 ns
- Trailing Edge Adjust Range of 300 ps
- Small Footprint: 52-pin MQFP Package (10 X 10 mm) with Internal Heat Spreader or Die Form

Applications

- Automatic Test Equipment
  - Per pin deskew in VLSI, Mixed-Signal, and Memory Testers
  - Clock Distribution with timing adjustment

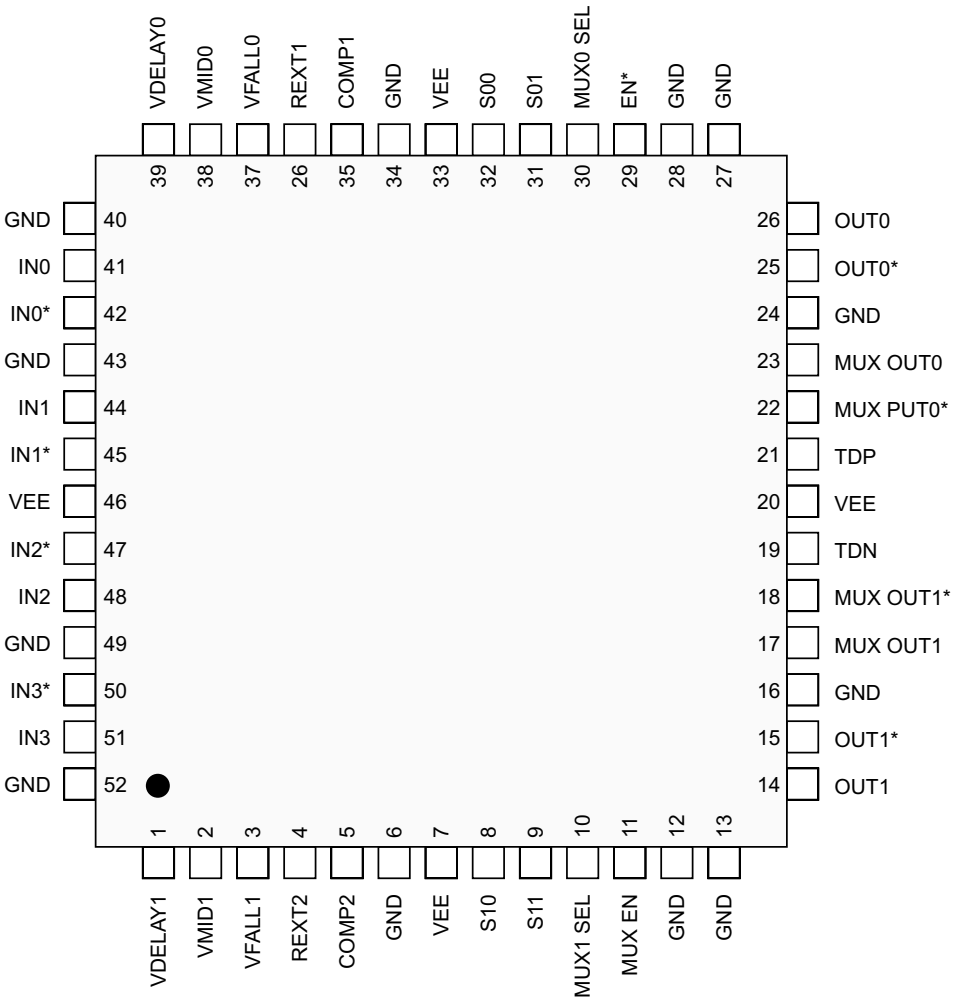
Functional Block Diagram



PIN Description

Pin Name	Pin #	Description
Digital		
IN0, IN0* IN1, IN1* IN2, IN2* IN3, IN3*	41, 42 44, 45 48, 47 51, 50	The multiplexer input signals. (Differential digital inputs.)
OUT0, OUT* OUT1, OUT1*	26, 25 14, 15	The selected and delayed output signals. (Differential ECL compatible outputs.)
MUX OUT0, 0* MUX OUT1, 1*	23, 22 17, 18	Selected monitor outputs. (Differential ECL compatible levels.)
S00, S01 S10, S11	32, 31 8, 9	Single-ended 10KH ECL compatible inputs which select the channel 0 and channel 1 source.
MUX0 SEL MUX1 SEL	30 10	Single-ended 10KH ECL compatible inputs which select the two output monitor sources.
EN*	29	Single-ended 10KH ECL compatible input which enables the delayed outputs.
MUX EN	11	Single-ended 10KH ECL compatible input which enables the monitor outputs.
Analog		
VDELAY0 VDELAY1	39 1	Analog voltage inputs which control the amount of propagation delay for each channel.
VFALL0 VFALL1	37 3	Analog voltage inputs which control the amount of falling edge delay for each channel.
VMID0 VMID1	38 2	Analog voltage inputs which control the amount of pulse width compensation for each channel.
REXT1	36	Analog input current used to establish the bias current for the VDELAY, VFALL, and VMIDinputs.
REXT2	4	Analog input current used to establish the bias level for the delay cells.
COMP1, COMP2	35 5	Op Amp compensation capacitors.
TDP, TDN	21, 19	Positive and negative terminals to the thermal diode string.
Power		
GND	6, 12, 13, 16, 24, 27, 28, 34, 40, 43, 49, 52	Device ground (positive device supply).
VEE	7, 20, 33, 46	

PIN Description *(continued)*



52-Pin MQFP 10mm x 10mm
with Internal Heat Spreader

Circuit Description

Chip Overview

The Edge142 is a 4 X 2 cross point switch and deskew element, offering an 1.5 ns delay (Tspan), where the VDELAY inputs adjust the overall propagation delay of the part. In addition, the part supports a separate falling edge delay of 300 ps (Tfall), where the VFALL inputs control the falling edge delay.

Two additional outputs, which are selectable from either OUT0 or OUT1, are provided. These outputs are useful when attempting to fanout a selected input to multiple destination without using and external buffer. All output signals may be enabled or disabled.

The Edge142 is designed to be monotonic and very stable. Figure 1 shows a simplified block diagram.

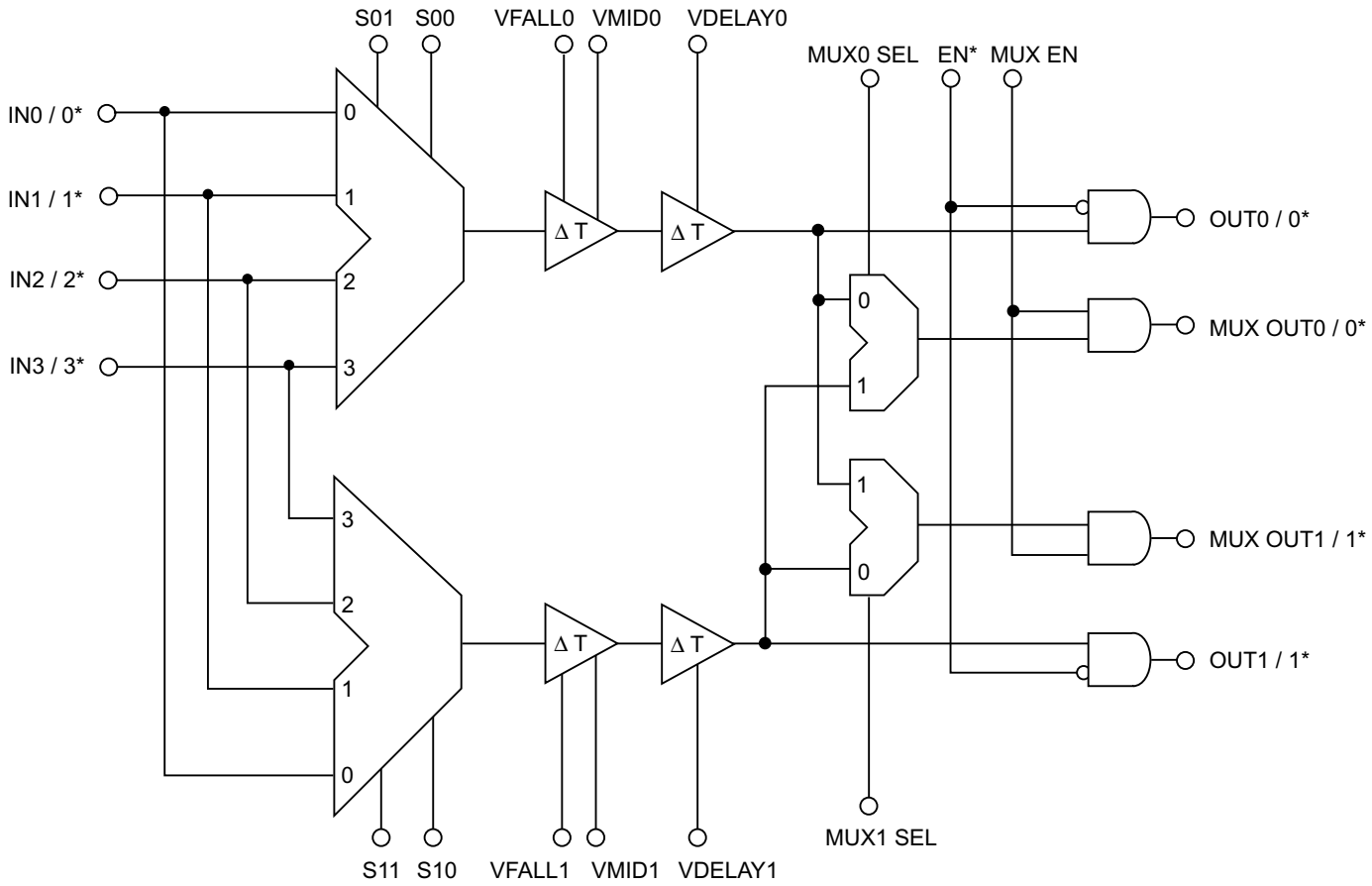


Figure 1. Edge142 Block Diagram

Circuit Description *(continued)*

Input Multiplexer

The Edge142 offers a 4 X 2 cross point switch in which one of four input signals are selected to two independent outputs. Each output signal's propagation delay and pulse width may then be adjusted via external control.

The truth table below documents the multiplexer functionality. Notice that there are no restrictions between the selection of channel 0 and channel 1.

SEL01	SEL00	OUT0	SEL11	SEL10	OUT1
0	0	IN0	0	0	IN0
0	1	IN1	0	1	IN1
1	0	IN2	1	0	IN2
1	1	IN3	1	1	IN3

Output Multiplexer

The Edge142 provides MUX OUT0 / MUX OUT0* and MUX OUT1 / MUX OUT1*, additional buffered differential output signals. These signals are selected from OUT0 or OUT1, depending on the state of MUX SEL, as indicated in the table below.

MUX(0,1) SEL	MUXOUT0	MUXOUT1
0	OUT0 / OUT0*	OUT1 / OUT1*
1	OUT1 / OUT1*	OUT0 / OUT0*

The MUX OUT signals allow either of the delayed outputs to be sent to an alternative destination without having to daisy chain the outputs to multiple destinations. This feature permits point to point routing of all critical timing signals in an effort to maintain the cleanest transmission lines for these signals.

The MUX OUT signals also provide a method for sending one common selected input signal to two independent destinations. This feature is useful when fanning out driver data and driver enable signals to multiple test heads.

Output Enable

Both the output and multiplexer output signals may be enabled or disabled, as documented below.

EN*	OUT / OUT*	MUX EN	MUX(0,1)OUT
0	Active	0	0
1	0	1	Active

Propagation Delay Adjust

The Edge142 supports two independent delay functions, which are described in the table below.

	Tpd+	Tpd-
VDELAY	1.5 ns	1.5 ns
VFALL	0 ps	300 ps

VDELAY controls the propagation delay of both the rising and falling edge (see Figure 2). An input signal is selected and then delayed by some programmable amount (Tspan) determined by the analog input VDELAY. The rising and falling edges are delayed equally. The propagation delay for a rising and a falling edge is defined as

$$Tpd+, Tpd- = Tpd(nom) + Tspan$$

where Tpd(nom) is the propagation delay of the part with zero programmed delay, and Tspan is the additional delay programmed via the VDELAY input. Notice that Tspan can be either positive or negative, depending on the nominal biasing of VDELAY, thus allowing bidirectional propagation delay adjustment. The transfer function for Tspan vs. VDELAY is shown in Figure 4.

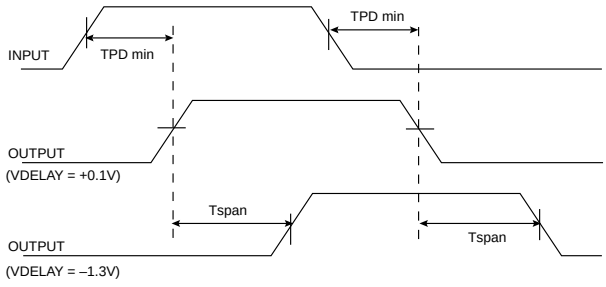


Figure 2. VDELAY Control

Falling Edge Adjust

VFALL allows independent adjustment of the falling edge (see Figure 3). The propagation delay for a falling edge is defined as

$$Tpd- = Tpd(nom) + Tspan + Tfall$$

where Tfall is defined as the additional delay incurred by adjusting the VFALL input. Notice that Tfall can be either positive or negative over a ± 150 ps range, depending on where VMID is set. This flexibility allows the part to either expand or contract an input signal .

Notice also that Tpd+ is a function of VDELAY only, while Tpd- is a function of VDELAY and VFALL. The transfer function for Tspan vs. VDELAY is shown in Figure 4. The transfer function for Tfall vs. VFALL is shown in Figure 5.

VMID

VMID is used in conjuction with VFALL to remove any systematic pulse width expansion or contraction. VMID and VFALL are differential analog voltage inputs which affect the falling edge delay.

When VFALL equals VMID, there will be no programmed pulse width variation between the input and the output signal. It is the difference between VMID and VFALL that expands or contracts a pulse.

VMID should be statically established at the midpoint of the voltage swing of VFALL.

Programming Sequence

VDELAY, in addition to affecting the placement of the rising edge, also affects the falling edge. Therefore, when calibrating a system, VDELAY should be adjusted first. As VFALL affects only the falling edge, it should be adjusted after VDELAY is established.

Default Conditions

All digital inputs have either an internal pull up (to ground) or pull down (to VEE) resistor (~50 KΩ) to protect against floating inputs migrating to an indeterminant state. All differential timing inputs are pulled to a logical zero state. All operating mode control inputs are pulled down to a logical zero. The mux select and mux enable inputs have pull down resistors to VEE. And the output enable is pulled up to ground.

The following chart summarizes the internal state of the digital inputs.

Input	Internal Resistor
IN0, IN1, IN2, IN3	Pull Down to VEE
IN0*, IN1*, IN2*, IN3*	Pull up to GND
S00, S10, S01, S11	Pull Down to VEE
MUX0 SEL, MUX1 SEL	Pull Down to VEE
MUX EN	Pull Down to VEE
EN*	Pull up to GND

However, despite the internal resistors providing a known default condition, it is recommended that no unused inputs be left floating.

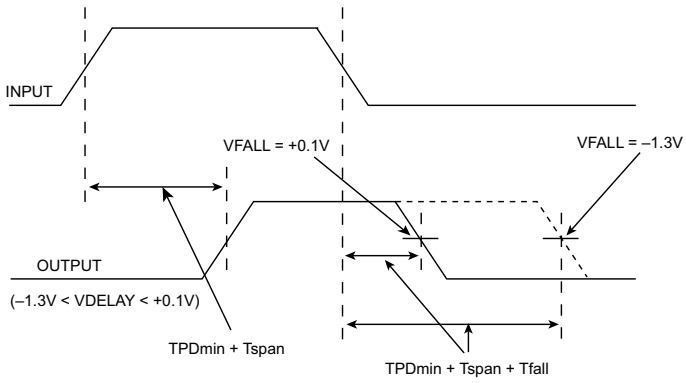


Figure 3. Falling Edge Control

Circuit Description *(continued)*

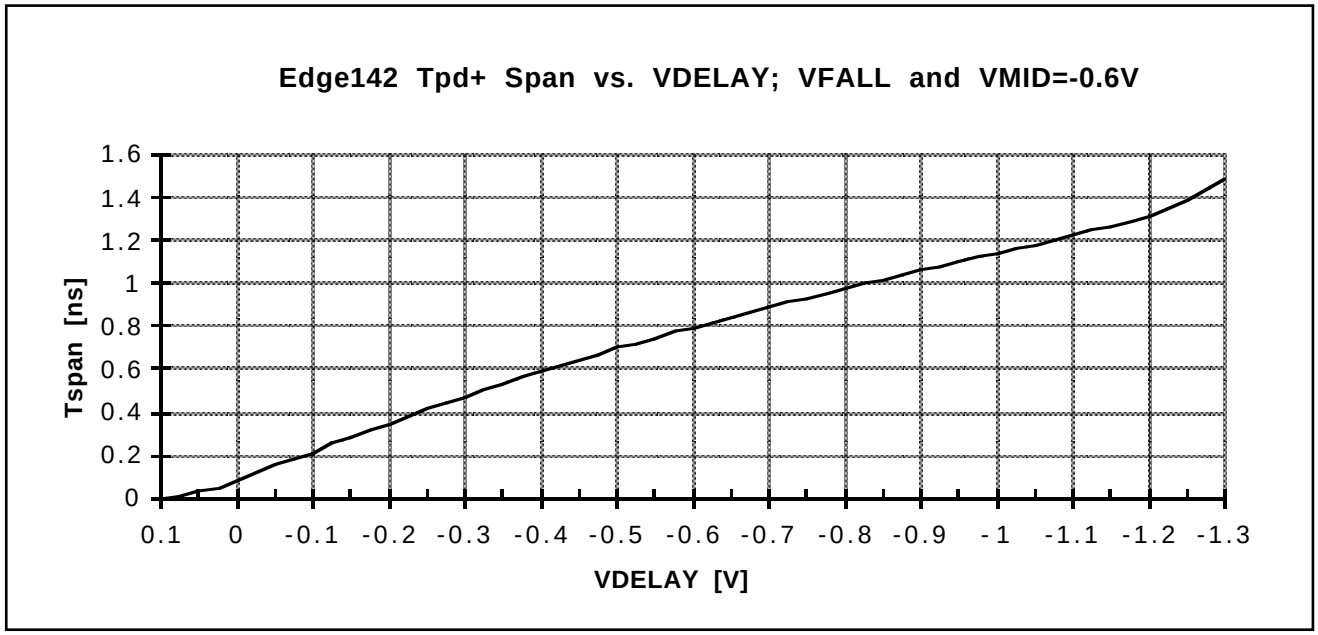


Figure 4. VDELAY Tranfer Function

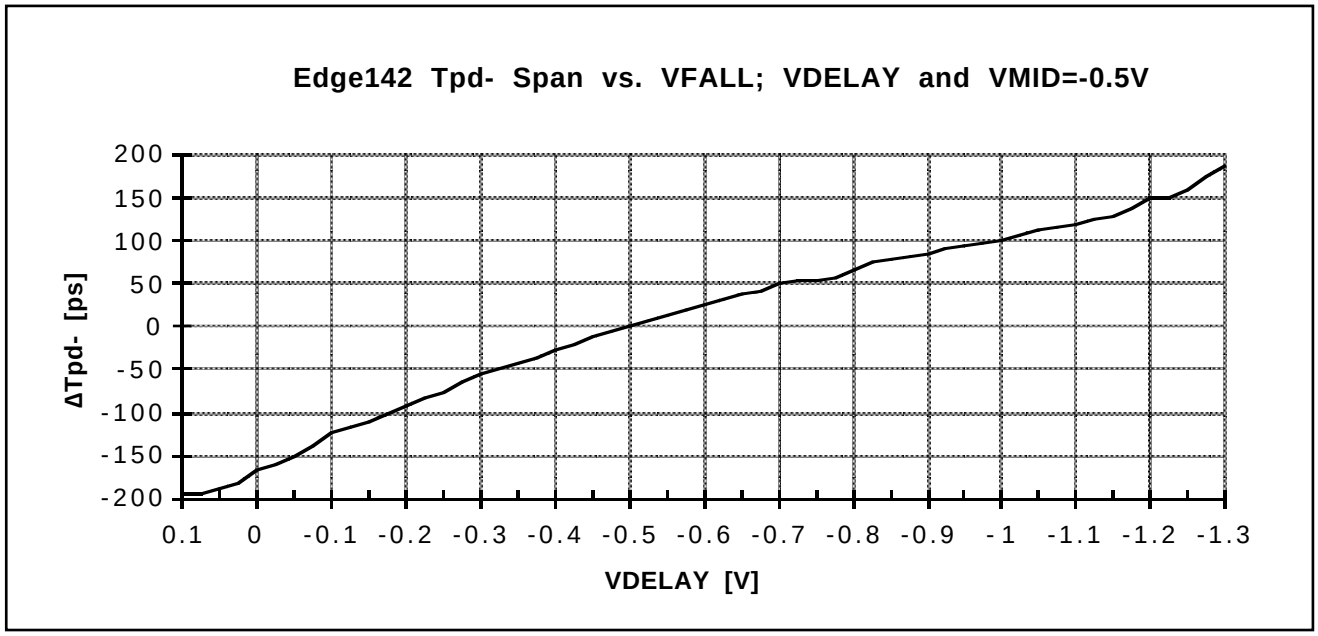


Figure 5. VFALL Transfer Function

Circuit Description *(continued)*

Analog Delay Inputs

VDELAY, VFALL, and VMID are analog voltage inputs which control the delay of the rising and falling edge. All three inputs may vary from +0.1V (minimum delay) to -1.3V (maximum delay).

VMID should be permanently set to the middle of the overall voltage range spanned by VFALL (~ -0.6V). A fixed resistor to ground will usually suffice. *The exact setting of VFALL will vary depending on the required delay range of the falling edge.*

These inputs are designed to sink a constant input current, typically 1.0 mA (with REXT1 = 2.94 KΩ), over their operating range from +0.1V to -1.3V. Any voltage DAC used to drive these inputs directly needs to source at least 1.0 mA. Any current DAC used needs to factor in the constant 1.0 mA input current.

The equation used to establish the VDELAY, VMID, and VFALL input currents is:

$$I(VFALL, VDELAY, VMID) = 3.0V / REXT1.$$

The fact that the VDELAY, VFALL, and VMID inputs have internal current sources allows a voltage DAC capable of generating only positive voltages and an external resistor network to be pulled down to the Edge142's negative input voltage compliance. These current sources are designed to be constant over temperature, so changes in system temperature will not translate into a delay voltage shift.

Using a different REXT1 will program a different input current. However, the value of this current does not affect deskew range or performance. The ability to vary this current allows a more flexible interface to a variety of DAC programming techniques.

VDELAY, VFALL, and VMID all require current flow. Do NOT leave any of these input pins floating. If an application does not require any falling edge delay, connect all VDELAY and VMID pins to ground.

Compensation Pins

COMP1 and COMP2 are Op Amp compensation pins. For proper Edge142 functionality, these pins require a .1 µF capacitor to ground.

Thermal Monitor

The Edge142 includes an on-chip thermal monitor accessible through the pins TDP and TDN. These nodes connect to five diodes in series (see Figure 6) and may be used to accurately measure the junction temperature at any time.

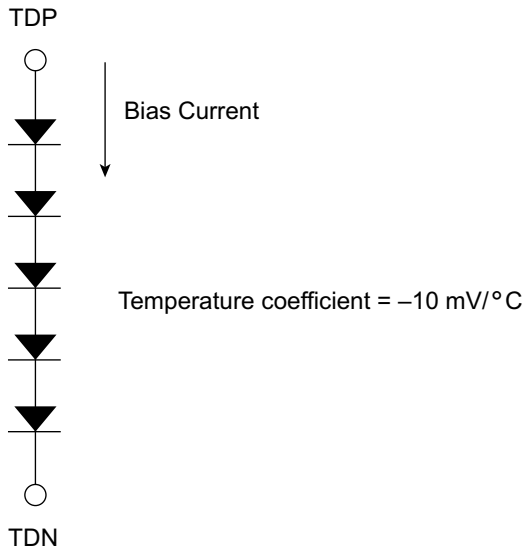


Figure 6. Thermal Diode String

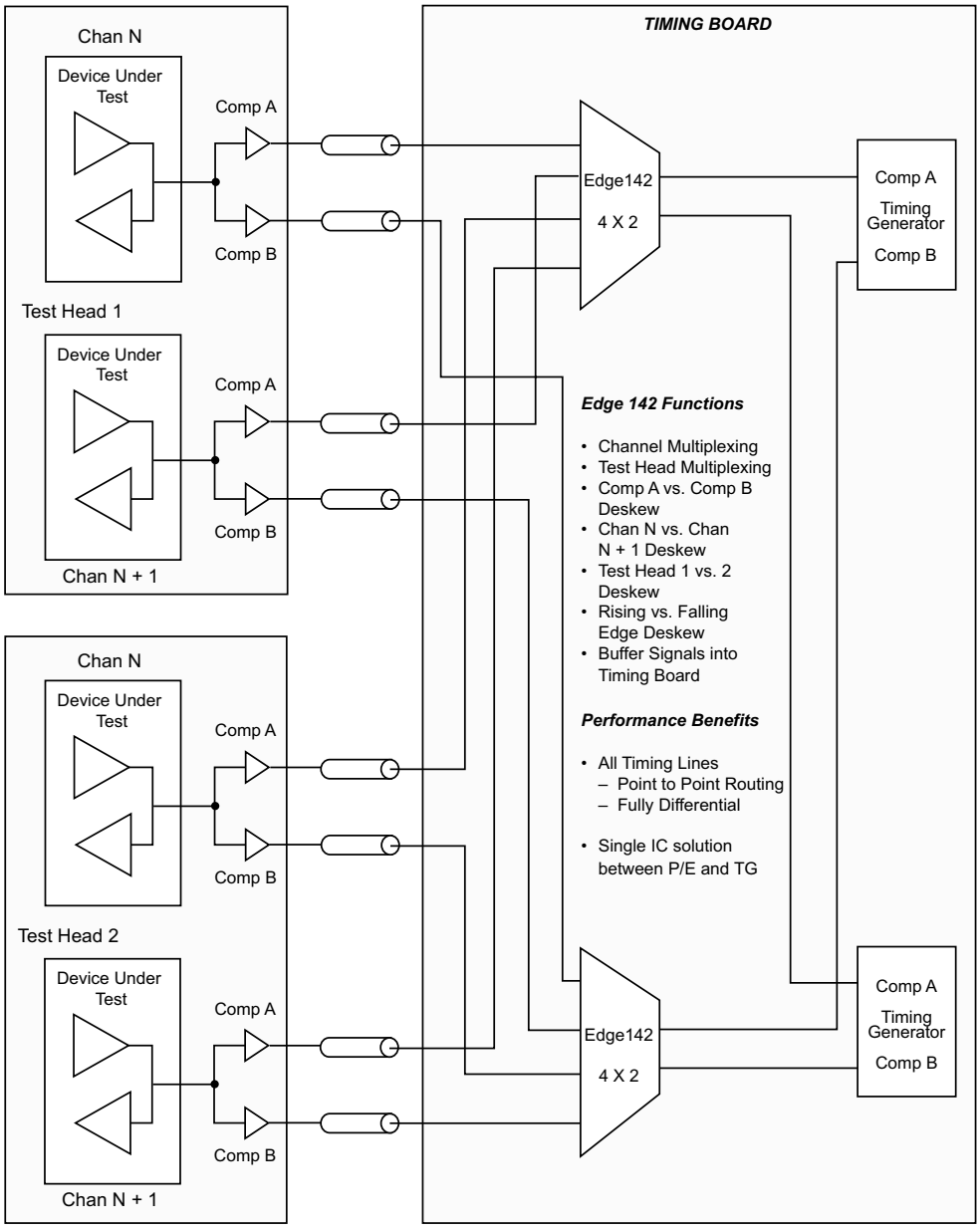
An external bias current of 100 µA is injected through the string, and the measured voltage corresponds to a specific junction temperature with the following equation:

$$T_J(^\circ C) = \{(V(TDP) - V(TDN)) / 5 - .7\} / (-.00208).$$

Application Information

Comparator Return Path

The Edge142 is designed specifically to buffer, multiplex, and deskew multiple comparator paths from multiple test heads to the timing generators located back in the tester mainframe. The Edge142 provides a one IC solution between the pin electronics and the error strobing circuitry. Most importantly, the Edge142 performs all of the timing deskew functions, thus removing the burden of timing compensation from the error section. By performing the calibration with the Edge142, there may be some improvement in the edge to edge retrigger time inside the timing generator.

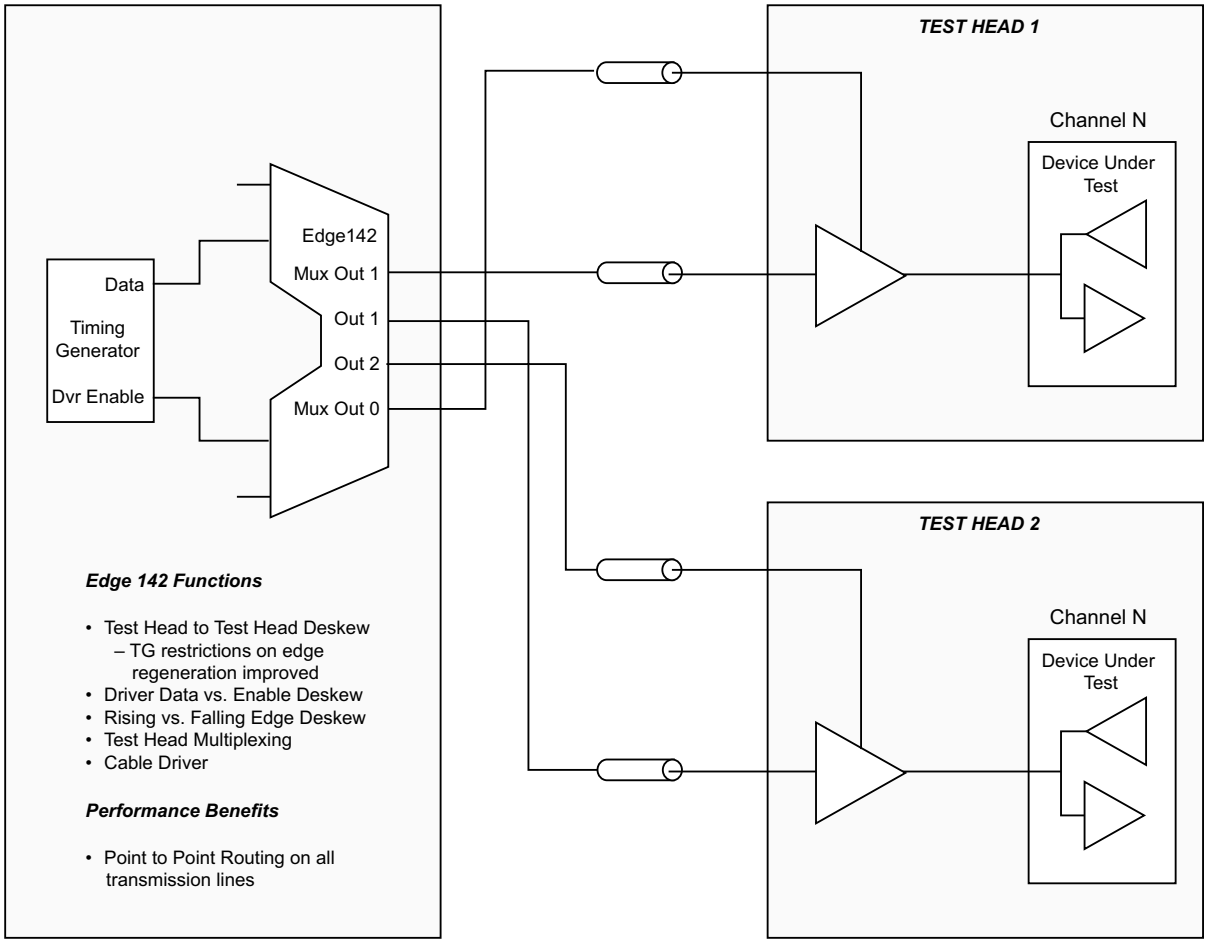


Application Information *(continued)*

Driver Fan Out

The Edge142 is also designed to support the fanning out and deskewing of driver data, driver enable, and load enable signals to multiple test heads. By controlling the multiplexer and output enable signals, the signals may be routed to either test head.

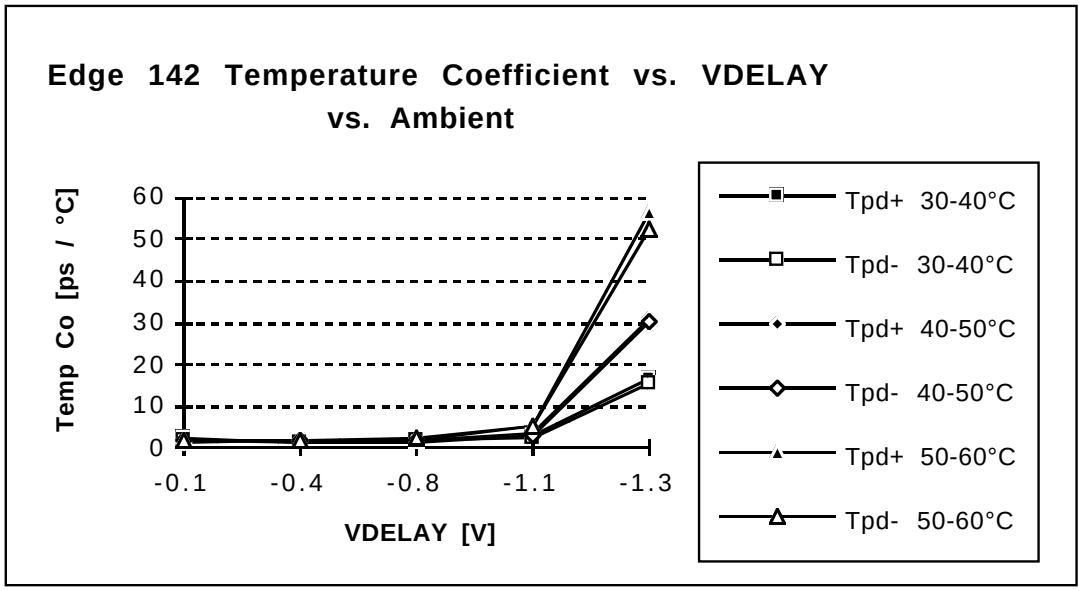
By using the Edge142 for timing calibration, the timing generator can generate “pure” timing signals, regardless of the timing errors associated with driving one test head vs. another. Removing the need for the timing generator to perform the deskew function, the restriction on consecutive edges may be improved.

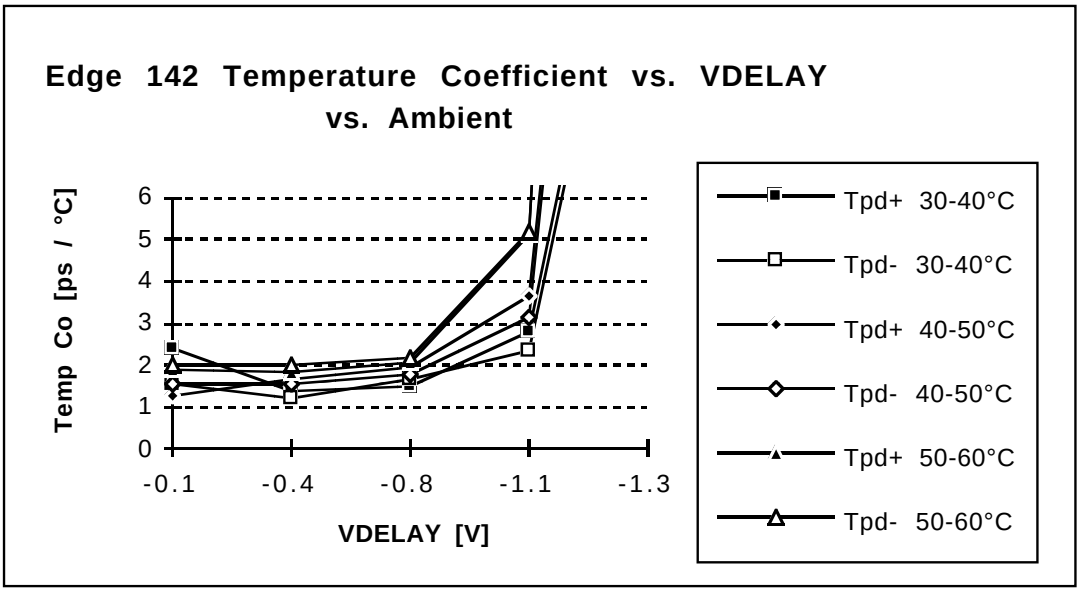


Application Information *(continued)*

Temperature Coefficient

The propagation delay temperature coefficient is shown in the above two charts. The same information is displayed on two different scales to enhance readability. The 142 functions over the entire VDELAY voltage range, but the timing error due to changes in the ambient temperature becomes large for VDELAY < -1.1V. If extreme accuracy is required, the recommended voltage range is: +0.1V >= VDELAY >= -1.1V. If greater range is needed and thermal drift can be tolerated, or the ambient temperature is very tightly controlled, the entire voltage range may be used.



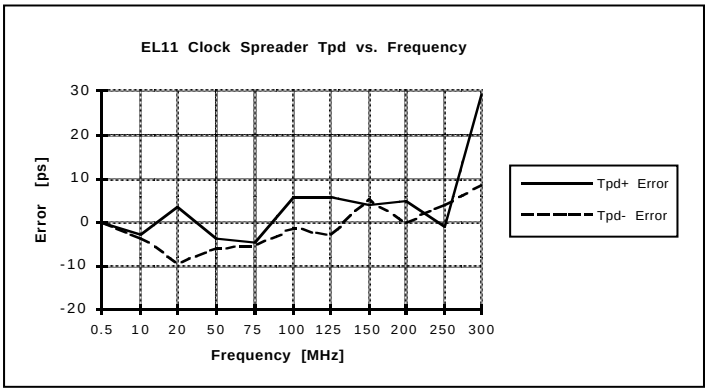


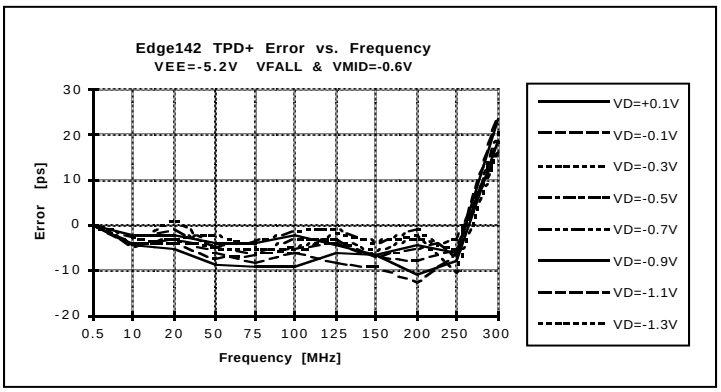
Prop Delay vs. Frequency

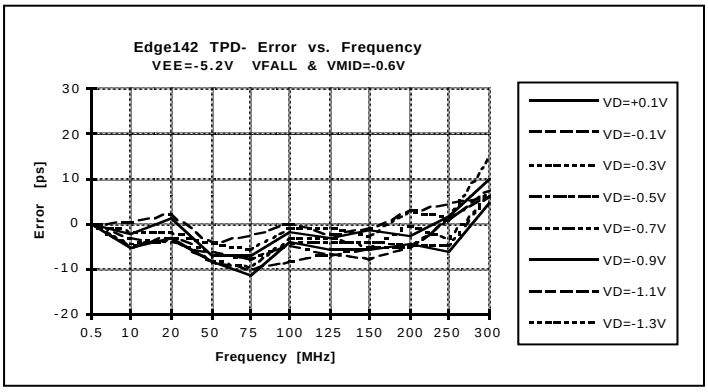
The 142 shows very little change in propagation delay vs. frequency. The following three charts show the variation in the prop delay of a rising edge and a falling edge as the frequency is varied over a wide range.

The first chart shows the Motorola 10EL11 clock spreader timing error for both the rising and falling edge with the input frequency varied from .5 MHz to 300 MHz. This information is used as a reference to compare the 142 against.

The second and third charts show the 142 under identical conditions. The data is broken out into one chart for the rising edge and a separate chart for the falling edge. In addition, the timing error is listed over the entire delay range of the 142.







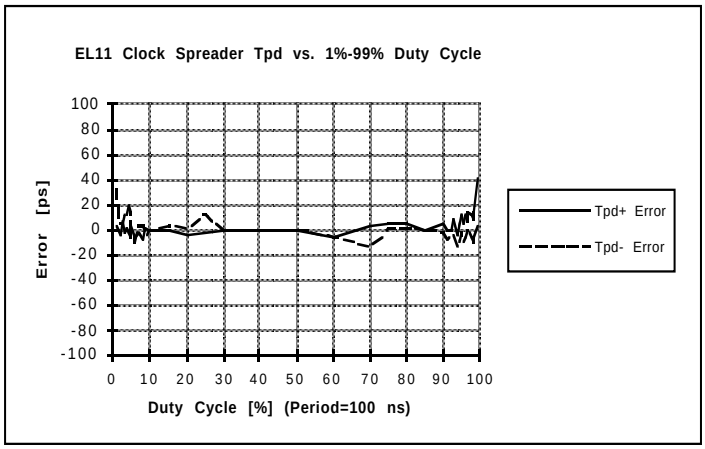
Application Information *(continued)*

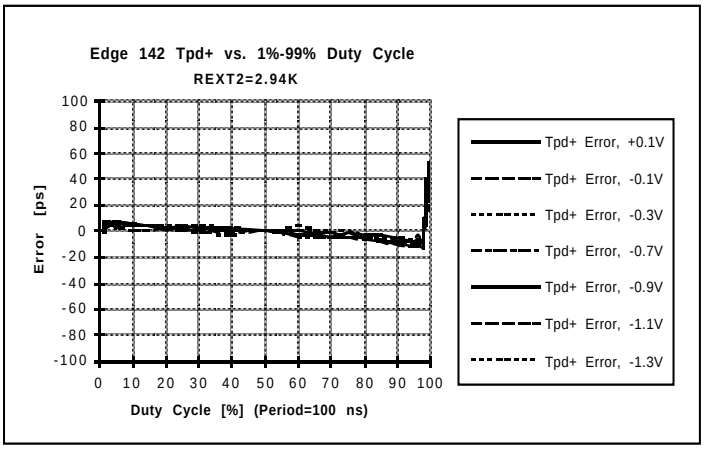
Prop Delay vs. Duty Cycle

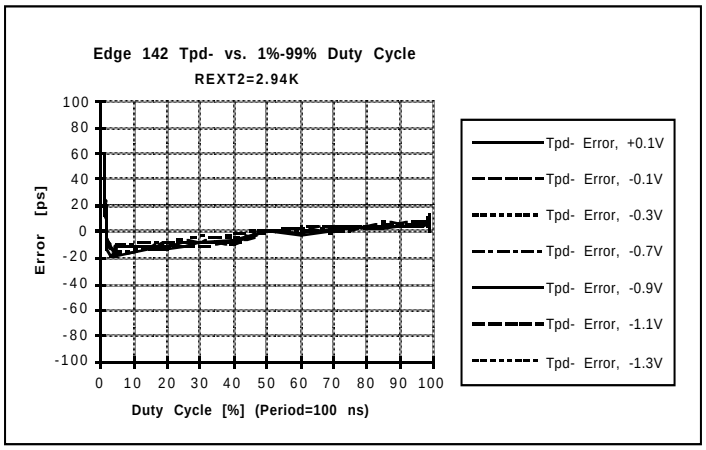
The 142 shows very little change in propagation delay vs. input duty cycle. The following three charts show the variation in the prop delay of a rising edge and a falling edge as the duty cycle is varied from 1% to 99%. Since the input signal period is 100 ns, a 1% duty cycle corresponds to a 1 ns positive input pulse. A 99% duty cycle corresponds to a 1 ns negative input pulse.

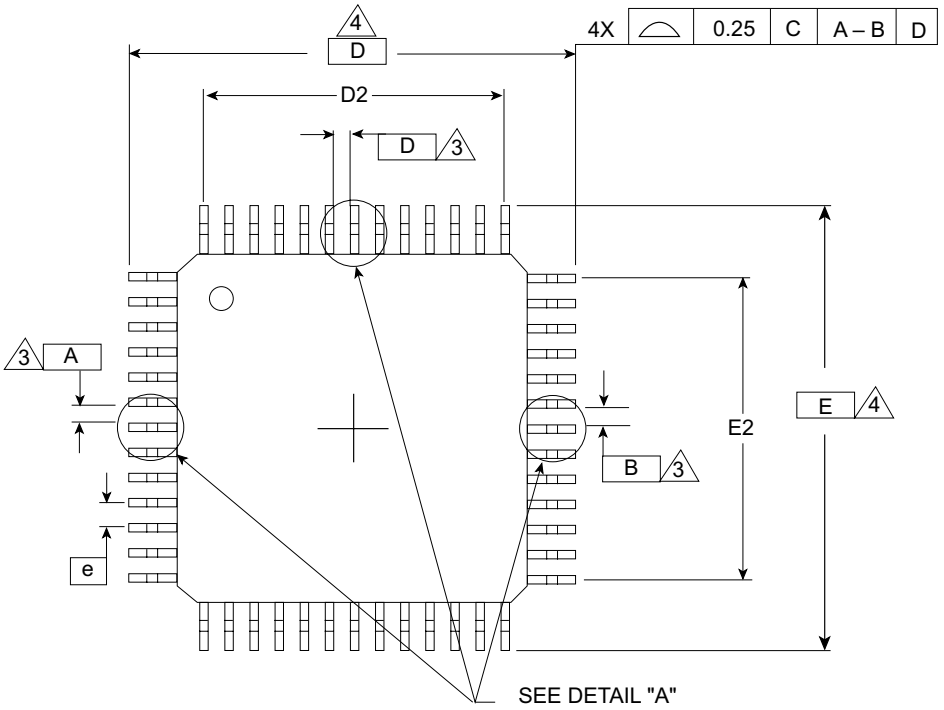
The first chart shows the Motorola 10EL11 clock spreader timing error for both the rising and falling edge. This information is used as a reference to compare the 142 against.

The second and third charts show the 142 under identical conditions. The data is broken out into one chart for the rising edge and a separate chart for the falling edge. In addition, the timing error is listed over the entire delay range of the 142.

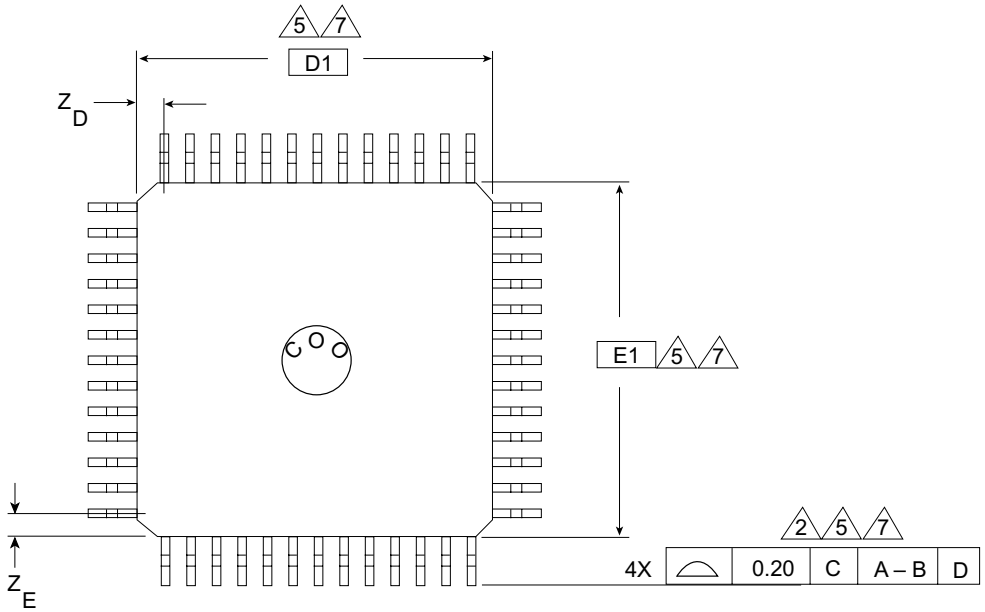






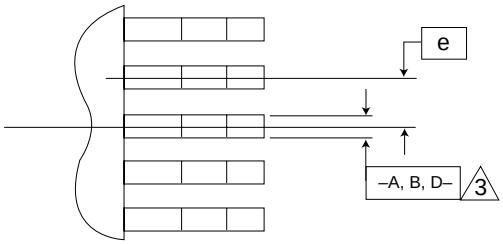


TOP VIEW

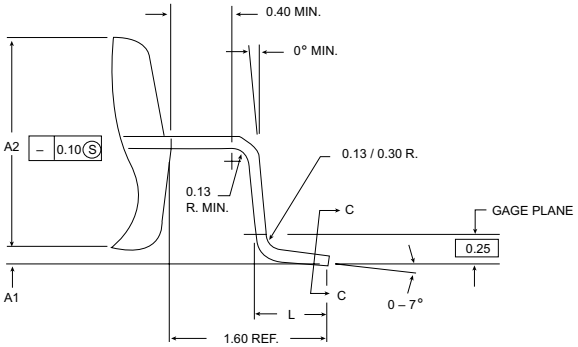


BOTTOM VIEW

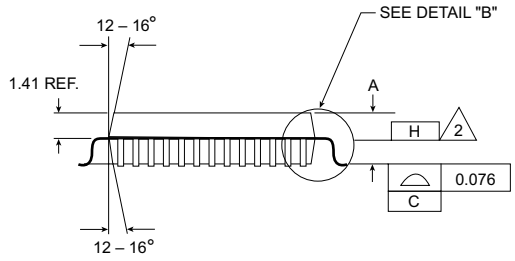
Package Information *(continued)*

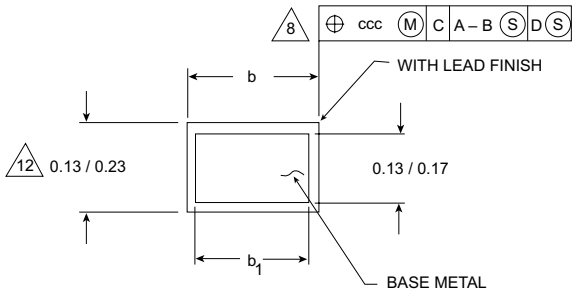


DETAIL "A"



DETAIL "B"





SECTION C-C

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined where centerline between leads exits plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plan -H-.
6. "N" is the total # of terminals.
7. Package top dimensions are smaller than bottom dimensions by 0.20 mm, and top of package will not overhang bottom of package.
8. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
9. All dimensions are in millimeters.
10. Maximum allowable die thickness to be assembled in this package family is 0.635 millimeters.
11. This drawing conforms to JEDEC registered outline MS-108.
12. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

	JEDEC VARIATION All Dimensions in Millimeters				
	AC				
	Min.	Nom.	Max.	Note	Comments
A		2.15	2.35		Soldered PkgHeight above PCB
A1	0.10	0.15	0.25		PCB Clearance
A2	1.95	2.00	2.10		Package Body Thickness
D	13.20 BSC.			4	
D1	10.00 BSC.			5	Package Body Length
D2	7.80 REF.				
ZD	1.10 REF.				
E	13.20 BSC.			4	
E1	10.00 BSC.			5	Package Body Width
E3	7.80 REF.				
ZE	1.10 REF.				
L	0.73	0.88	1.03		
N	52			6	# Pins
e	0.65				Lead Pitch
b	0.22		0.38		
b1	0.22	0.30	0.33		
aaa		0.12			

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	GND	0	0	0	V
Negative Power Supply	VEE	-4.2	-5.2	-5.5	V
Ambient Operating Temperature	TA	0		+70	^{o}C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (relative to GND)		-7.0		0	V
Voltage on any Digital Pin		VEE		GND	V
Output Current		-50			mA
Ambient Operating Temperature	TA	-55		+70	^{o}C
Storage Temperature	TS	-65		+150	^{o}C
Junction Temperature	TJ			+150	^{o}C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	^{o}C

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Differential Digital Input High Voltage IN, IN*	IN - IN*	300			mV
Differential Digital Input Low Voltage IN, IN*	IN* - IN	300			mV
Digital Input High Voltage S00, S01, S10, S11, MODE, EN*, MUX SEL, MUX EN	VIH	-1070		0	mV
Digital Input Low Voltage S00, S01, S10, S11, MODE, EN*, MUX SEL, MUX EN	VIL	VEE		-1450	mV
Input Common Mode Range	IN, IN*	-2.0		-0.5	V
Input High Current (Vin = VIHmax)	IIH	-100	120	250	µA
Input Low Current (Vin = VILmin)	IIL	-100	90	150	µA
VDELAY, VFALL, & VMID Input Currents	Iin	.84	.990	1.08	mA
Outputs OUT0 / OUT0*, OUT1 / OUT1* MUX OUT0 / MUX OUT0*, MUX OUT1 / MUX OUT1*					
Digital Output High Voltage	OUT - OUT*	700	800		mV
Digital Output Low Voltage	OUT* - OUT	700	800		mV
Output Common Mode Range	$\frac{OUT + OUT*}{2}$	-1.1	-1.35	-1.5	V
VEE Supply Current					
VEE = -4.5V	IEE	-255	-200	-155	mA
VEE = -5.0V	IEE	-260	-205	-160	mA
VEE = -5.5V	IEE	-265	-210	-165	mA

Test conditions (unless otherwise specified): “Recommended Operating Conditions” with REXT1 = 2.94 KΩ, and REXT2 = 2.94 KΩ. All parameters specified at 0°C are guaranteed by characterization and are not production tested. The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delays Minimum Delay (Pulse Width >= 1.0 ns) VDELAY = +0.1V, VFALL = +0.1V	TPDmin	1.75	2.05	2.45	ns
Delay Range vs. Pulse Width Input Pulse Width >= 1.0 ns (+0.1V < VDELAY < -1.2V)	Tspan	1.1	1.4		ns
VFALL Range of Adjustment Input Pulse Width >= 1.0 ns (+0.1V < VFALL < -1.2V)	Tfall	170	300		ps
Propagation Delay Tempco (Note 1) -1.1V <= VDELAY, VFALL <= +0.1V			<2		ps / ^{O}C
Output Rise/Fall Times (20% to 80%) (Note 1)	Tr, Tf	300	420	500	ps

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with TA = 25 °C with 400 LFPM of airflow, and all outputs terminated with 50 Ω to –2.0 V. Timing reference points at the differential crossing points for input and output signals, REXT1 = 2.94 KΩ, and REXT2 = 2.94 KΩ. All input signals are fully differential. Values are based on nominal temperature and a supply voltage of –5.2 V.

Note 1: Based upon characterization data. Not production tested. For more complete data, refer to the application information section of the data sheet.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Ordering Information

Model Number	Package
E142AHF	52 Pin 10mm x 10mm MQFP with Internal Heat Spreader
D142	Die Form
EVM142AHF	Edge142 Evaluation Module

Contact Information

Semtech Corporation
Edge High-Performance Division
10021 Willow Creek Rd., San Diego, CA 92131
Phone: (858)695-1801 FAX (858)695-2633