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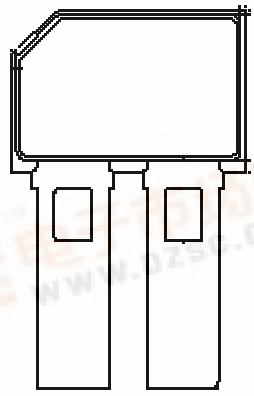
Differential Two-Wire Hall Effect Sensor IC

TLE4941
TLE4941C

Features

- **Two-wire current interface**
- **Dynamic self-calibration principle**
- **Single chip solution**
- **No external components needed**
- **High sensitivity**
- **South and north pole pre-induction possible**
- **High resistance to piezo effects**
- **Large operating air-gaps**
- **Wide operating temperature range**
- **TLE 4941C: 1.8nF overmolded capacitor**



PSSO2-1

Type	Marking	Ordering Code	Package
TLE 4941	4100E	Q62705-K427	PSSO2-1
TLE 4941C	41C0E	Q62705-K439	PSSO2-2

The Hall Effect sensor IC TLE4941 is designed to provide information about rotational speed to modern vehicle dynamics control systems and ABS. The output has been designed as a two wire current interface. The sensor operates without external components and combines a fast power-up time with a low cut-off frequency. Excellent accuracy and sensitivity is specified for harsh automotive requirements as a wide temperature range, high ESD and EMC robustness. State-of-the art BiCMOS technology is used for monolithic integration of the active sensor areas and the signal conditioning circuitry.

Finally, the optimised piezo compensation and the integrated dynamic offset compensation enable easy manufacturing and elimination of magnet offsets.

The TLE4941C is additionally provided with an overmolded 1.8nF capacitor for improved EMI performance.

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Functional Description

The differential hall sensor IC detects the motion of ferromagnetic and permanent magnet structures by measuring the differential flux density of the magnetic field. To detect the motion of ferromagnetic objects the magnetic field must be provided by a back biasing permanent magnet. Either south or north pole of the magnet can be attached to the rear unmarked side of the IC package.
Magnetic offsets of up to +/- 20mT and device offsets are cancelled by a self-calibration algorithm. Only a few transitions are necessary for self-calibration. After the initial calibration sequence switching occurs when the input signal is crossing the arithmetic mean of its max and min value. (E.g. zero-crossing for sinusoidal signals)
The ON and OFF state of the IC are indicated by ***High*** and ***Low*** current consumption.

Circuit Description

The circuit is supplied internally by a 3V voltage regulator. An on-chip oscillator serves as clock generator for the digital part of the circuit.
TLE4941 signal path is comprised of a pair of hall probes, spaced at 2.5mm, a differential amplifier including a noise-limiting low-pass filter and a comparator feeding a switched current output stage. In addition an offset cancellation feedback loop is provided by a signal-tracking A/D converter, a digital signal processor (DSP) and an offset cancellation D/A converter.

During the startup phase (un-calibrated mode) the output is disabled ($I=I_{Low}$).
The differential input signal is digitized in the speed A/D converter and fed into the DSP. The minimum and maximum values of the input signal are extracted and their corresponding arithmetic mean value is calculated. The offset of this mean value is determined and fed into the offset cancellation DAC.
After successful correction of the offset, the output switching is enabled.

In running mode (calibrated mode) the offset correction algorithm of the DSP is switched into a low-jitter mode, avoiding oscillation of the offset DAC LSB. Switching occurs at zero-crossing. It is only affected by the (small) remaining offset of the comparator and by the remaining propagation delay time of the signal path, mainly determined by the noise-limiting filter. Signals below a defined threshold ΔB_{Limit} are not detected to avoid unwanted parasitic switching.

Pin Configuration
(view on branded side of component)

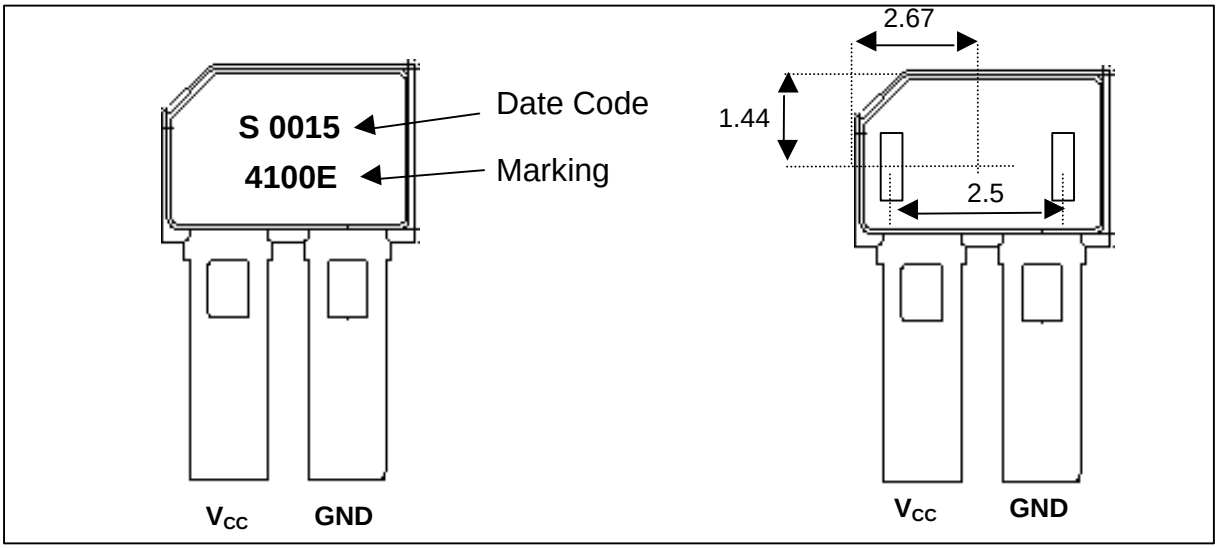


Figure 1

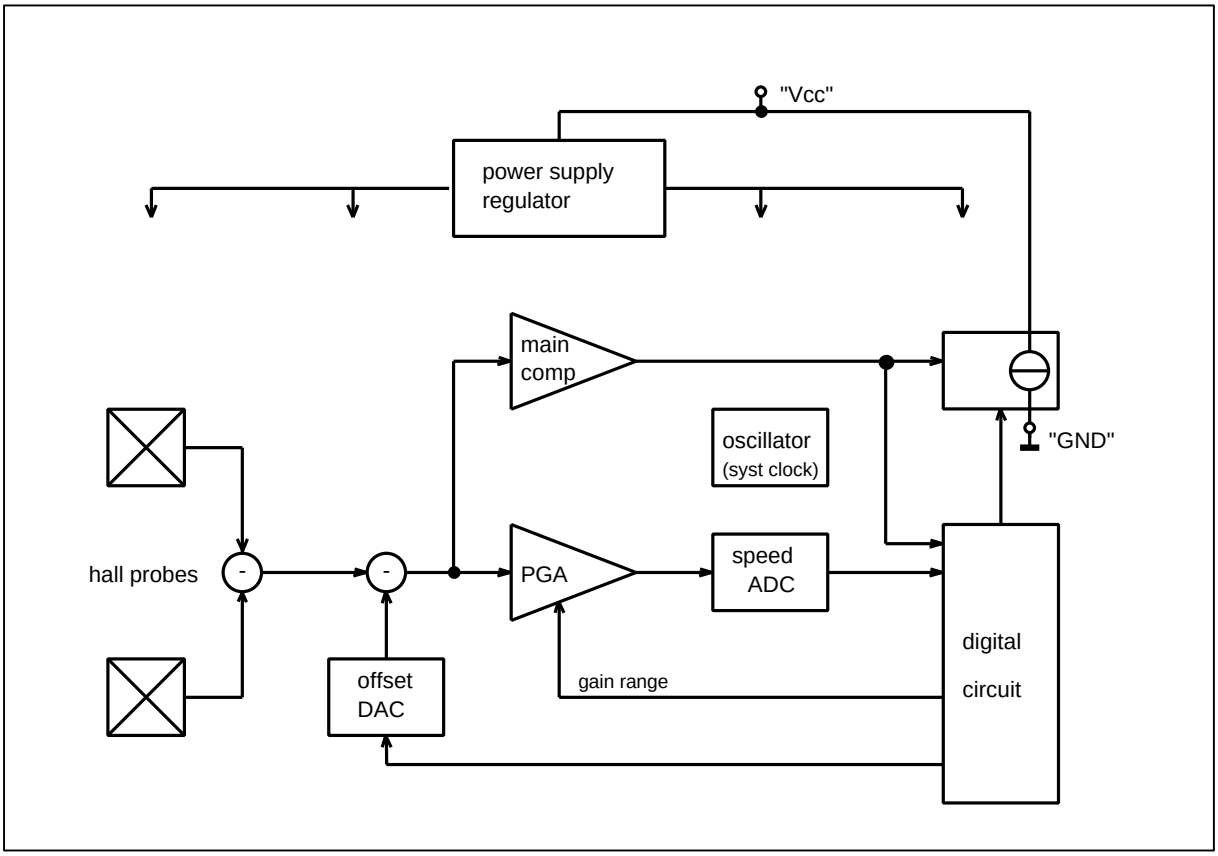


Figure 2 Block diagram

Absolute Maximum Ratings

T_j = -40 to 150°C, 4.5V ≤ V_{cc} ≤ 16.5V

Parameter	Symbol	Limit values		Unit	Remarks
		Min	Max		
Supply voltage	V_{cc}	-0.3			T_j < 80°C
Supply voltage	V_{cc}		16.5	V	T_j = 170°C
Supply voltage	V_{cc}		20	V	T_j = 150°C
Supply voltage	V_{cc}		22	V	t = 10 * 5 min
Supply voltage	V_{cc}		24	V	t = 10 * 5 min, R_M≤ 75Ω
Supply voltage	V_{cc}		27	V	t = 400 ms, R_M≤ 75Ω
Reverse polarity current	I_{rev}		200	mA	External current limitation required, t < 4h
Junction temperature Junction temperature Junction temperature Junction temperature	T_j T_j T_j T_j		150 160 170 190	°C °C °C °C	5000 h, V_{cc} < 16.5V 2500 h, V_{cc} < 16.5V 500 h, V_{cc} < 16.5V 4 h, V_{cc} < 16.5V
Active lifetime	$t_{B,active}$	10000		h	
Storage Temperature	T_s	-40	150	°C	
Thermal Resistance PSSO2-1	R_{thJA}		190	K/W	1)
ESD	U_{ESD}		±2	kV	According to standard EIA/JESD22-A114-B HBM 2) R=1500 Ω, C=100pF

1) can be improved significantly by further processing like overmolding
2) covers MIL STD 883D

Note: *Stresses in excess of those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Operating Range

Parameter	Symbol	Limit values		Unit	Remarks
		Min	Max		
Supply voltage	V_{CC}	4.5	20	V	
Supply voltage ripple	V_{AC}		6	V_{pp}	V_{CC}=13V 0 < f < 50kHz
Junction temperature	T_j	-40	150	°C	
Junction temperature	T_j		170	°C	$V_{CC} \leq$ 16.5V, increased jitter permissible
Pre-induction	B_0	-500	+500	mT	
Pre-induction offset between outer probes	$\Delta B_{stat., l/r}$	-20	+20	mT	
Differential Induction	ΔB	-120	+120	mT	

Note: *Within the operating range the functions given in the circuit description are fulfilled.*

AC/DC Characteristics

All values specified at constant amplitude and offset of input signal

Parameter	Symbol	Limit values			Unit	Remarks
		Min	Typ	Max		
Supply current	I_{Low}	5.9	7	8.4	mA	
Supply current	I_{High}	11.8	14	16.8	mA	
Supply current ratio	I_{High}/I_{Low}	1.9				
Output rise/fall slew rate TLE 4941	t_r, t_f	12 7.5		26 24	mA/µs	$R_M \leq 150\ \Omega$ $R_M \leq 750\ \Omega$ See Figure 4.
Output rise/fall slew rate TLE4941C	t_r, t_f	8 8		22 26	mA/µs	$R_M = 75\ \Omega$ T < 125°C T < 170°C See Figure 4.
Current ripple dI_X/dV_{CC}	I_X			90	µA/V	
Limit threshold	ΔB_{Limit}	0.35	0.8	1.5	mT	
Initial calibration delay time	$t_{d,input}$			300	µs	Additional to n_{start}
Magnetic edges required for initial calibration[1)]	n_{start}		3	6 *	magn. edges	
Frequency	f	1		2500	Hz	
Frequency changes	df/dt			±100	Hz/ms	
Duty cycle	duty	40	50	60	%	[2)] Measured @ΔB = 2mT sine wave Def. Figure 4
Jitter, T_j < 150°C T_j < 170°C	$S_{Jit-close}$			±2 ±3	% %	1 s value V_{CC} = 12 V ?B ≥ 2mT
Jitter, T_j < 150°C T_j < 170°C	$S_{Jit-far}$			±4 ±6	% %	1 s value V_{CC} = 12 V (2mT ≥) ΔB > ΔB_{Limit}
Jitter at board net ripple	S_{Jit-AC}			±2	%	V_{CC}=13V±6V_{pp} 0 < f < 50kHz ΔB = 15 mT

* See appendix B

[1)] The sensor requires up to n_{start} magnetic switching edges for valid speed information after power-up or after a stand still condition. During that phase the output is disabled.

[2)] During fast offset alterations, due to the calibration algorithm, exceeding the specified duty cycle is permitted for short time periods.

Output Description

Under ideal conditions, the output shows a duty cycle of 50 %. Under real conditions, the duty cycle is determined by the mechanical dimensions of the target wheel and its tolerances. (40% to 60% might be exceeded for pitch >> 5mm due to the zero-crossing principle.)

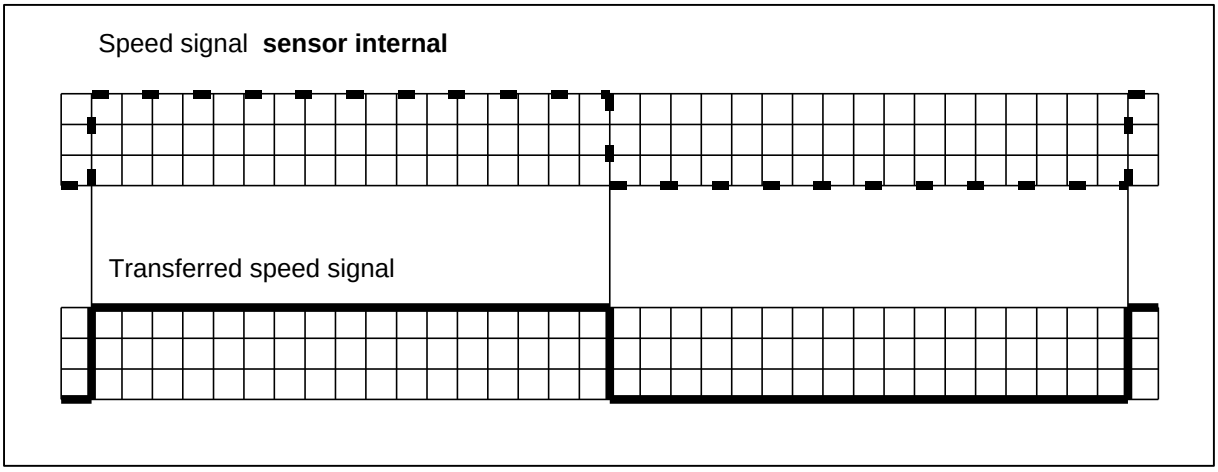


Figure 3 Speed Signal (half a period = 0.5 * 1/f_{speed})

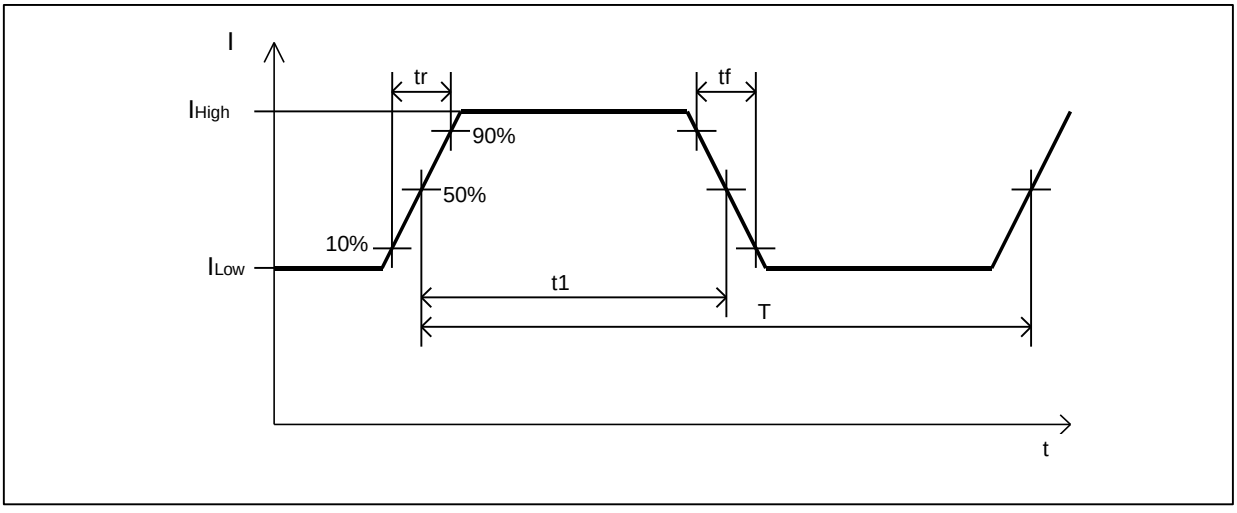


Figure 4 Definition of rise and fall time, duty = t1/T * 100%

Electro Magnetic Compatibility - *(values depend on R_M!)*

Ref. ISO 7637-1; test circuit 1;

ΔB = 2mT (amplitude of sinus signal); V_{CC}=13.5 V, f_B= 100 Hz; T= 25°C; $R_M \geq 75\ \Omega$

No.	Parameter	Symbol	Level/typ.	Status
1.1.1	Testpulse 1	V_{LD}	IV / -100 V	C(1)
	Testpulse 2		IV / 100 V	C(1)
	Testpulse 3a		IV / -150 V	A
	Testpulse 3b		IV / +100 V	A
	Testpulse 4		IV / -7 V	B(3)
	Testpulse 5		IV / +86,5 V(2)	C

(1) According to 7637-1 the supply switched „OFF“ for t=200ms. For battery „ON“ is valid status „A“.
(2) Applying in the board net a suppressor diode with sufficient energy absorption capability.
(3) According to 7637-1 for test pulse 4 the test voltage shall be 12V ± 0,2V

Values are valid for all TLE4941/42 types!

Ref. ISO 7637-3; test circuit 1;

ΔB = 2mT (amplitude of sinus signal); V_{CC}=13.5 V, f_B= 100 Hz; T= 25°C; $R_M \geq 75\ \Omega$

No.	Parameter	Symbol	Level/typ.	Status
1.2.1	Testpulse 1	V_{LD}	IV / -30 V	A
	Testpulse 2		IV / 30 V	A
	Testpulse 3a		IV / -60 V	A
	Testpulse 3b		IV / 40 V	A

Values are valid for all TLE4941/42 types!

Ref. ISO 11452-3; test circuit 1; measured in TEM-cell
ΔB = 2mT; V_{CC}=13.5V, f_B= 100 Hz; T= 25°C

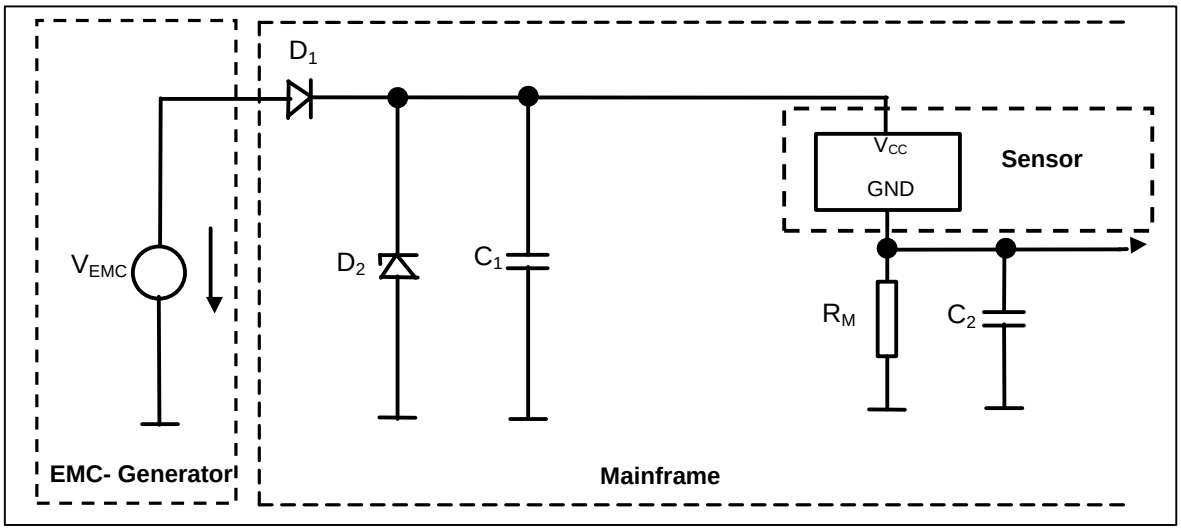
No.	Parameter	Symbol	Level/Max.	Remarks
1.2.2	EMC field strength	$E_{TEM\text{-}Cell}$	IV / 200 V/m	AM=80%, f=1kHz;

Only valid for non C- types!

Ref. ISO 11452-3; test circuit 1; measured in TEM-cell
ΔB = 2mT; V_{CC}=13.5V, f_B= 100 Hz; T= 25°C

No.	Parameter	Symbol	Level/Max.	Remarks
1.2.2	EMC field strength	$E_{TEM\text{-}Cell}$	IV / 250 V/m	AM=80%, f=1kHz;

Only valid for C-types!



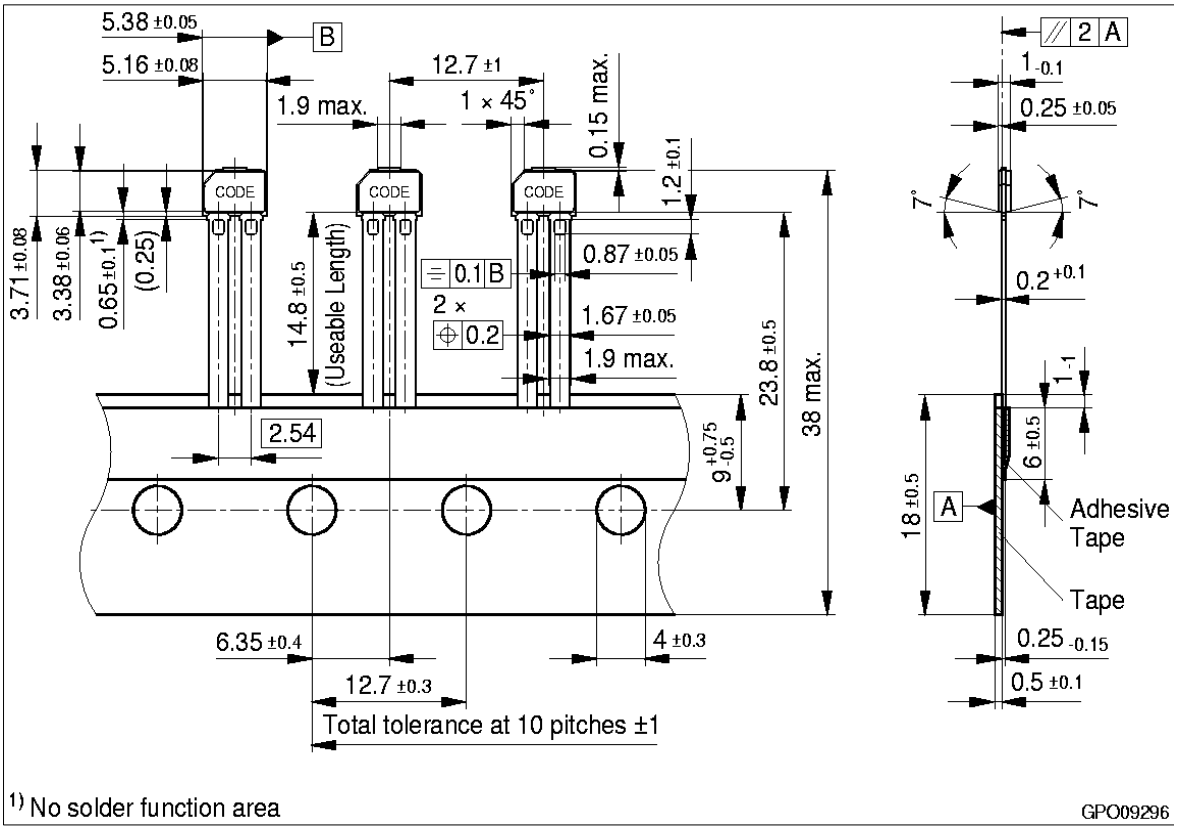
Components:

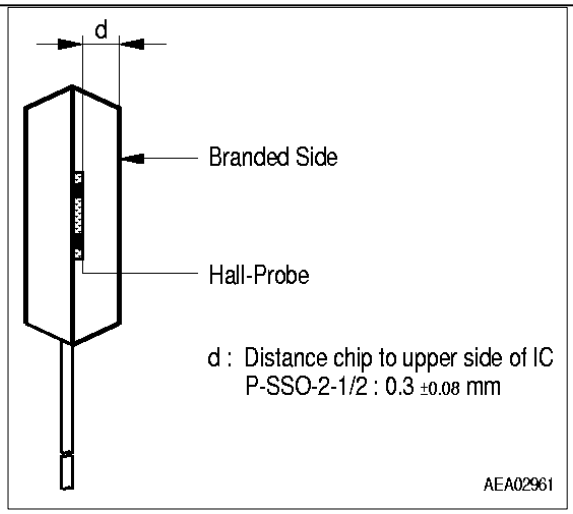
D1:	1N4007
D2:	T 5Z27 1J
C1:	10µF/35V
C2:	1nF/1000V
RM:	75Ω/5W

Figure 5 Test Circuit 1

Package Outlines

PSSO2-1
(Plastic Single Small Outline Package)





PSSO2-2
(Plastic Single Small Outline Package)