

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

**DESCRIPTION**

The 7531 Group is the 8-bit microcomputer based on the 740 family core technology.  
The 7531 Group has a serial I/O, 8-bit timers, and an A-D converter, and is useful for control of home electric appliances and office automation equipment.

**FEATURES**

- Basic machine-language instructions ..... 69
- The minimum instruction execution time ..... 0.50  $\mu$ s  
(at 8 MHz oscillation frequency for the shortest instruction, in high-speed mode)
- Memory size ROM ..... 8K to 16K bytes  
RAM ..... 256 to 384 bytes
- Programmable I/O ports ..... 29  
(25 in 32-pin version)
- Interrupts ..... 12 sources, 8 vectors  
(11 sources, 8 vectors for 32-pin version)
- Timers ..... 8-bit  $\times$  3
- Serial I/O1 ..... 8-bit  $\times$  1  
(UART)
- Serial I/O2 ..... 8-bit  $\times$  1  
(Clock-synchronized)
- A-D converter ..... 10-bit  $\times$  8 channels  
(6 channels for 32-pin version)
- Clock generating circuit ..... Built-in type  
(connect to external ceramic resonator or quartz-crystal oscillator

- ..... permitting CR oscillation)
- Watchdog timer ..... 16-bit  $\times$  1
- Power source voltage  
At 8 MHz XIN oscillation frequency at ceramic oscillation ..... 4.0 to 5.5 V  
At 4 MHz XIN oscillation frequency at ceramic oscillation ..... 2.4 to 5.5 V  
At 2 MHz XIN oscillation frequency at ceramic oscillation ..... 2.2 to 5.5 V  
At 4 MHz XIN oscillation frequency at CR oscillation ..... 4.0 to 5.5 V  
At 2 MHz XIN oscillation frequency at CR oscillation ..... 2.4 to 5.5 V  
At 1 MHz XIN oscillation frequency at CR oscillation ..... 2.2 to 5.5 V
- Power dissipation ..... 40 mW (standard)
- Operating temperature range ..... -20 to 85 °C  
(-40 to 85 °C or -40 to 125 °C for extended operating temperature version (Note))  
Note: The total time is limited as follows:  
6000 hours at 55 to 85 °C, 1000 hours at 85 to 125 °C

**APPLICATION**

Office automation equipment, factory automation equipment, home electric appliances, consumer electronics, car, etc.

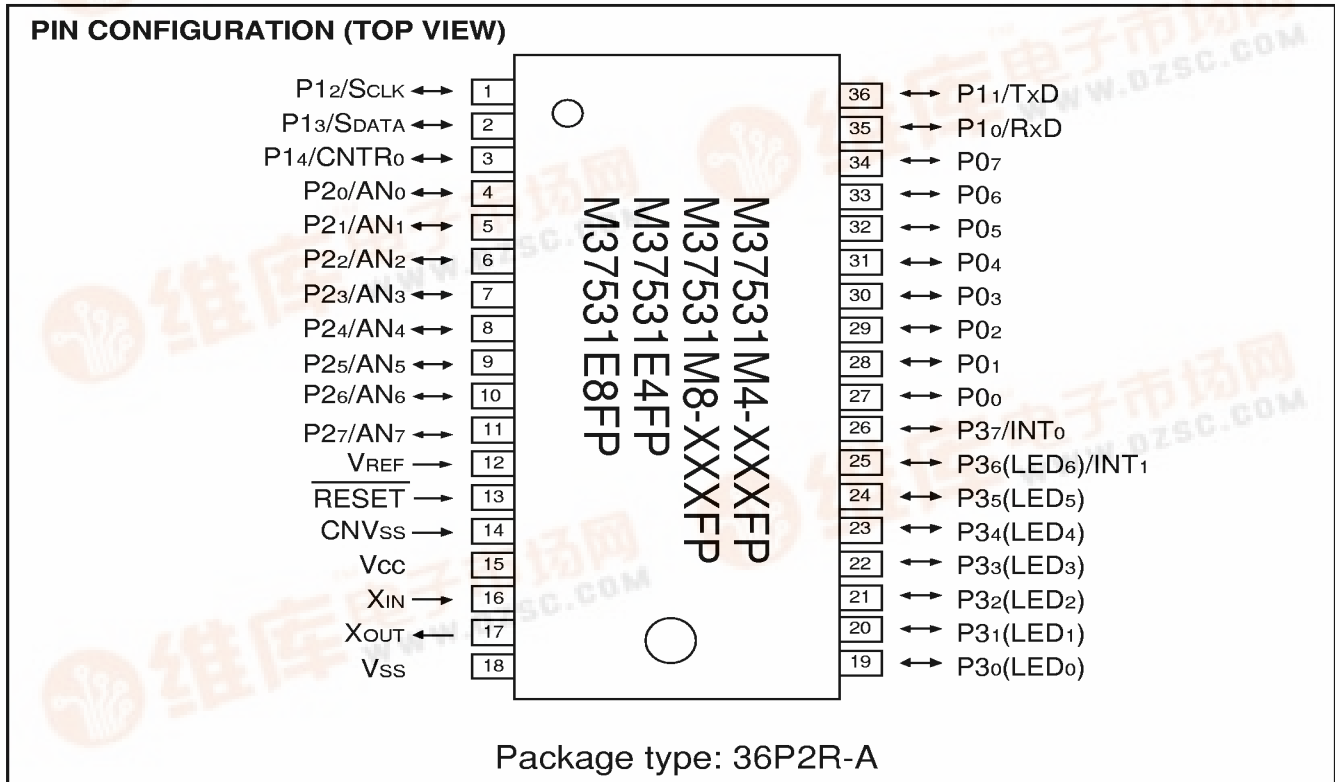


Fig. 1 Pin configuration (36P2R package type)



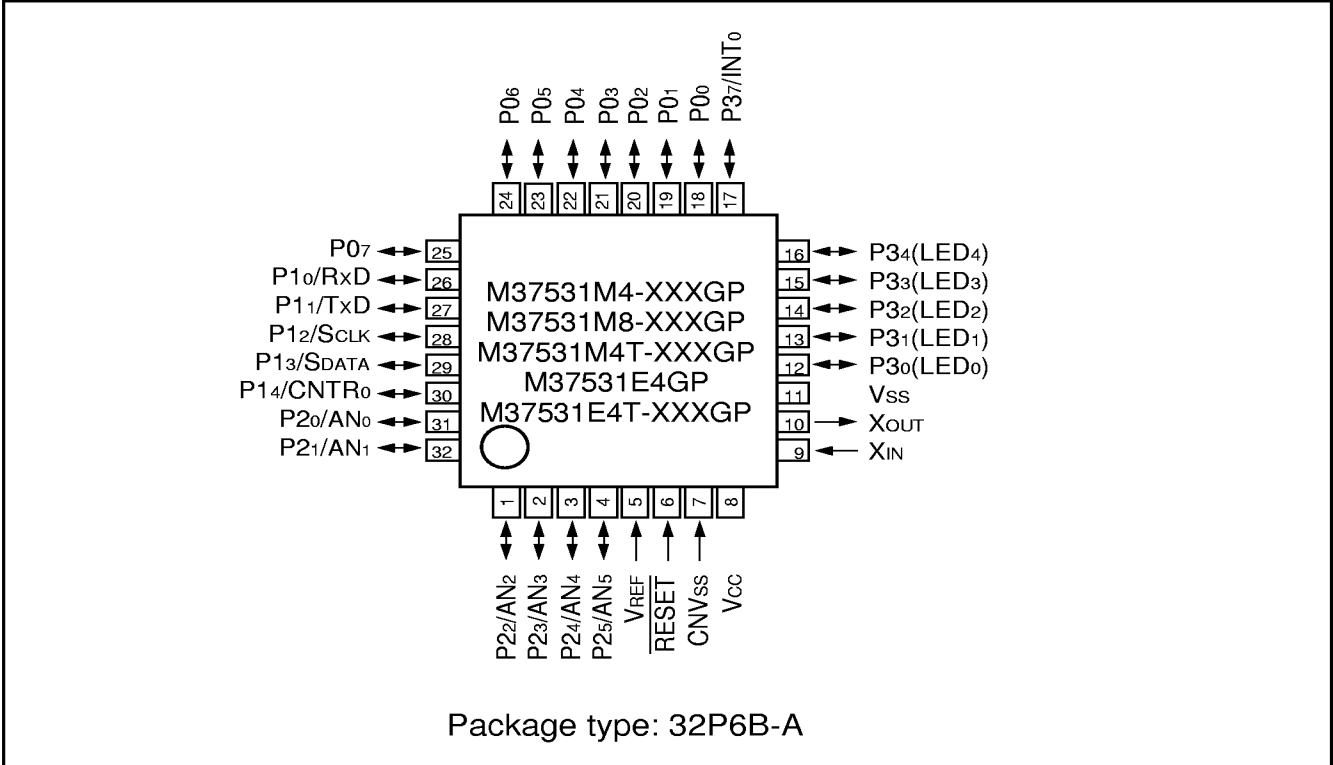


Fig. 2 Pin configuration (32P6B package type)

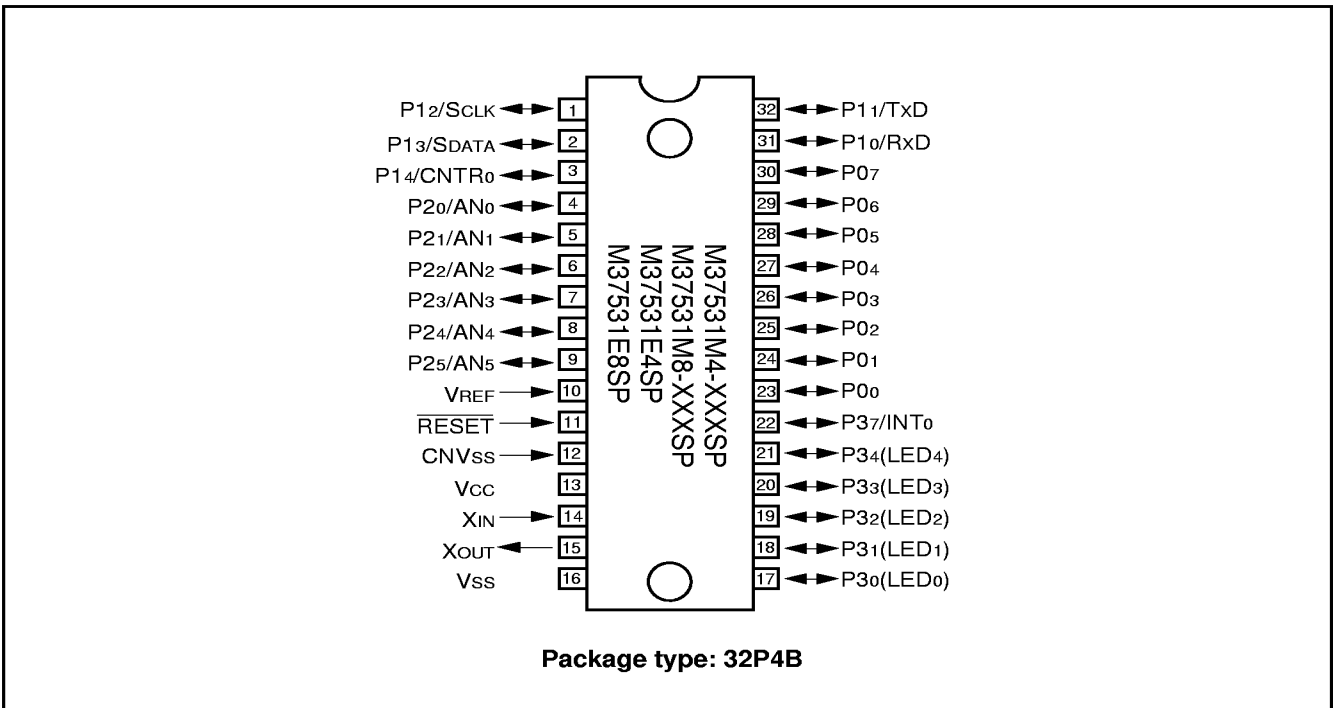


Fig. 3 Pin configuration (32P4B package type)

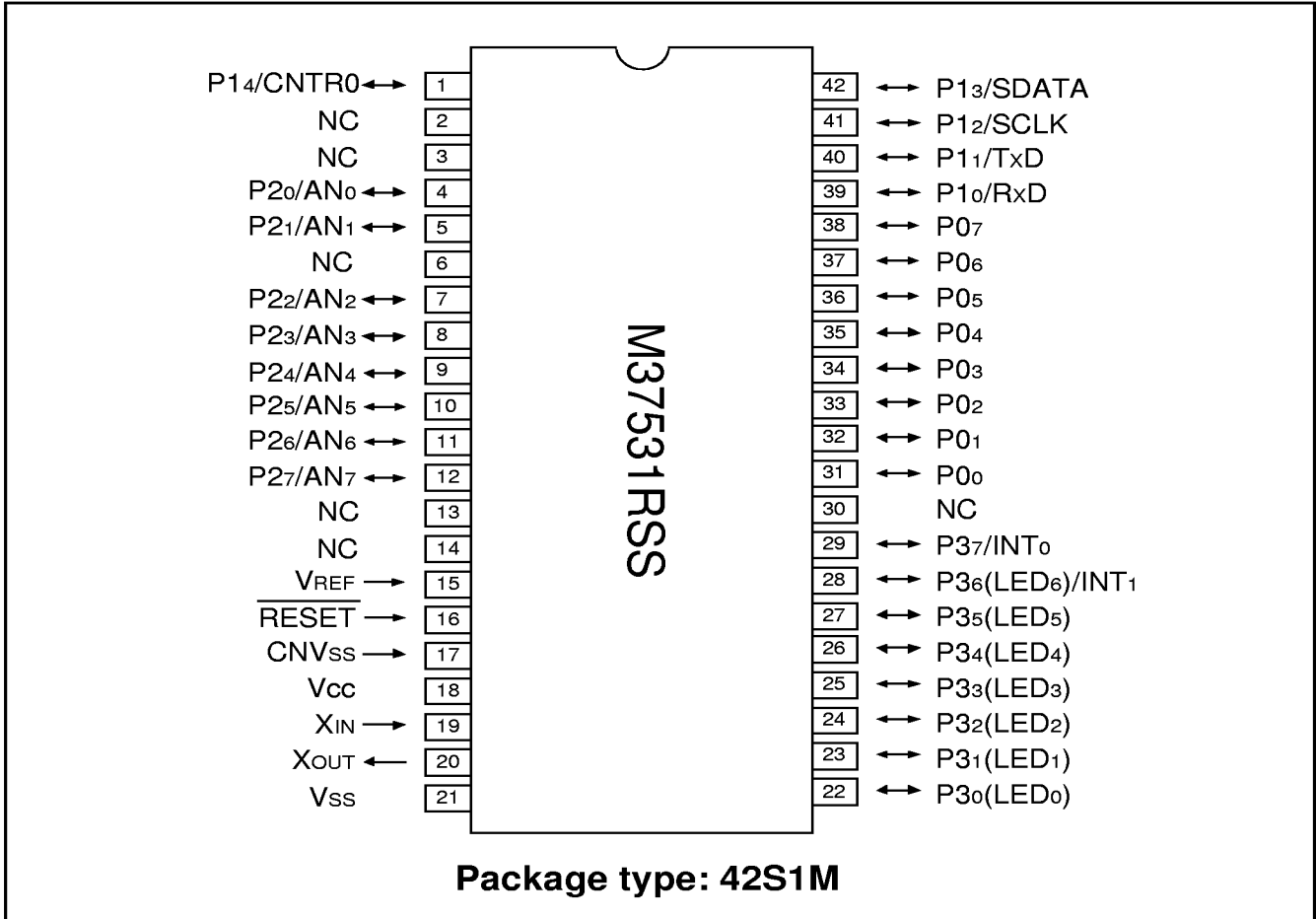


Fig. 4 Pin configuration (42S1M package type)

FUNCTIONAL BLOCK

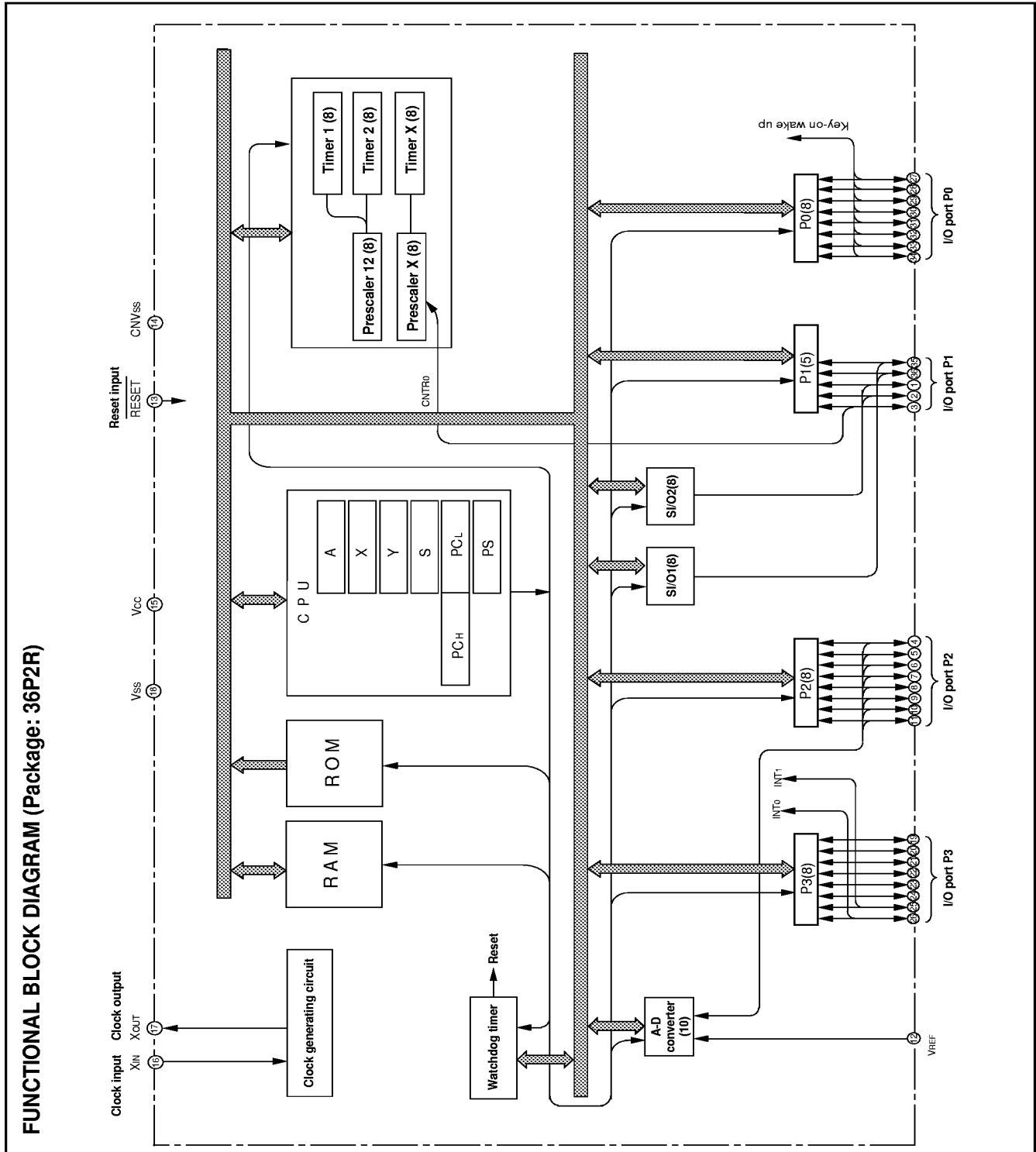


Fig. 5 Functional block diagram (36P2R package)

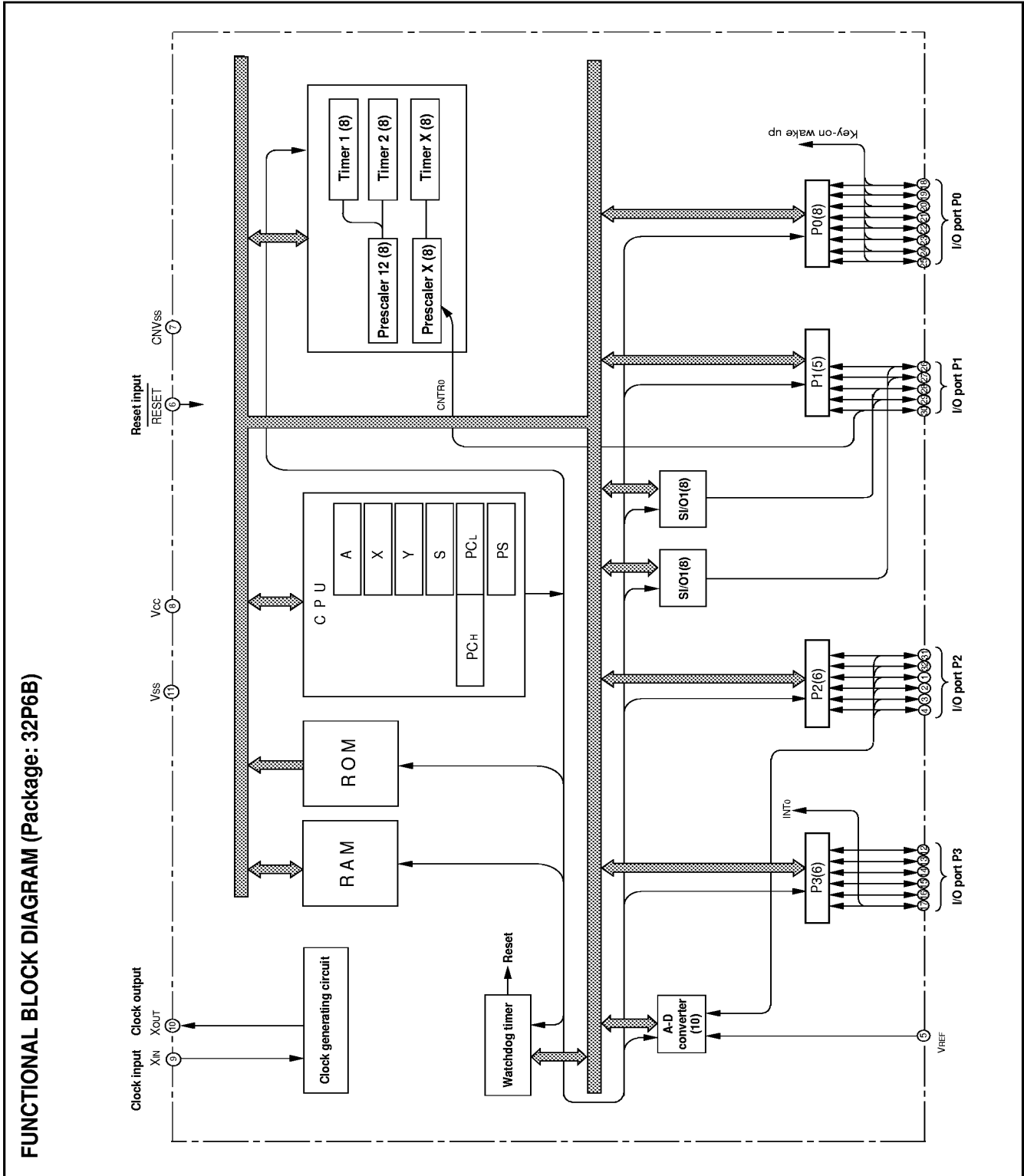


Fig. 6 Functional block diagram (32P6B package)

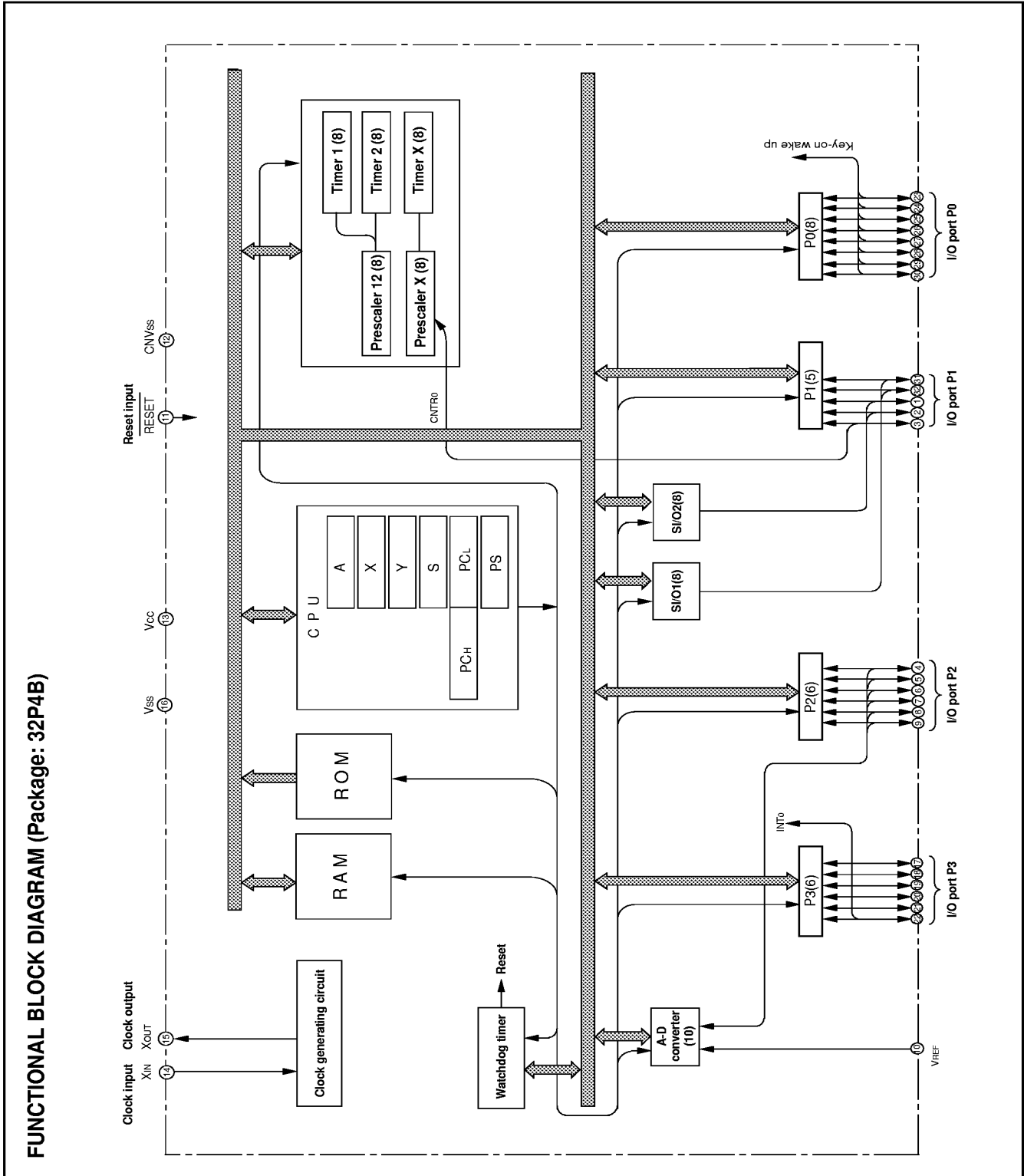


Fig. 7 Functional block diagram (32P4B package)

## PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	Function expect a port function
Vcc, Vss	Power source	•Apply voltage of 2.2–5.5 V to Vcc, and 0 V to Vss.	
VREF	Analog reference voltage	•Reference voltage input pin for A-D converter	
CNVss	CNVss	•Chip operating mode control pin, which is always connected to Vss.	
RESET	Reset input	•Reset input pin for active "L"	
XIN	Clock input	•Input and output pins for main clock generating circuit •Connect a ceramic resonator or quartz crystal oscillator between the XIN and XOUT pins.	
XOUT	Clock output	•For using CR oscillator, short between the XIN and XOUT pins, and connect the capacitor and resistor. •If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
P0 <sub>0</sub> –P0 <sub>7</sub>	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •Whether a built-in pull-up resistor is to be used or not can be determined by program.	•Key-input (key-on wake up interrupt input) pins
P1 <sub>0</sub> /RxD P1 <sub>1</sub> /TxD P1 <sub>2</sub> /SCLK P1 <sub>3</sub> /SDATA P1 <sub>4</sub> /CNTR <sub>0</sub>	I/O port P1	•5-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •CMOS/TTL level can be switched for P1 <sub>0</sub> , P1 <sub>2</sub> and P1 <sub>3</sub>	•Serial I/O1 function pin •Serial I/O2 function pin •Timer X function pin
P2 <sub>0</sub> /AN <sub>0</sub> – P2 <sub>7</sub> /AN <sub>7</sub>	I/O port P2	•8-bit I/O port having almost the same function as P0 •CMOS compatible input level •CMOS 3-state output structure	•Input pins for A-D converter
P3 <sub>0</sub> –P3 <sub>5</sub>  P3 <sub>6</sub> /INT <sub>1</sub> P3 <sub>7</sub> /INT <sub>0</sub>	I/O port P3	•8-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level (CMOS/TTL level can be switched for P3 <sub>6</sub> and P3 <sub>7</sub> ). •CMOS 3-state output structure •P3 <sub>0</sub> to P3 <sub>6</sub> can output a large current for driving LED. •Whether a built-in pull-up resistor is to be used or not can be determined by program.	•Interrupt input pins

# MITSUBISHI MICROCOMPUTERS

## 7531 Group

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### GROUP EXPANSION

Mitsubishi plans to expand the 7531 group as follow:

#### Memory type

Support for Mask ROM version, One Time PROM version, and Emulator MCU .

#### Memory size

ROM/PROM size ..... 8 K to 16 K bytes  
RAM size ..... 256 to 384 bytes

#### Package

32P4B ..... 32 pin shrink plastic molded DIP  
32P6B-A ..... 0.8 mm-pitch plastic molded QFP  
36P2R-A ..... 0.8 mm-pitch plastic molded SOP  
42S1M ..... 42 pin shrink ceramic PIGGY BACK

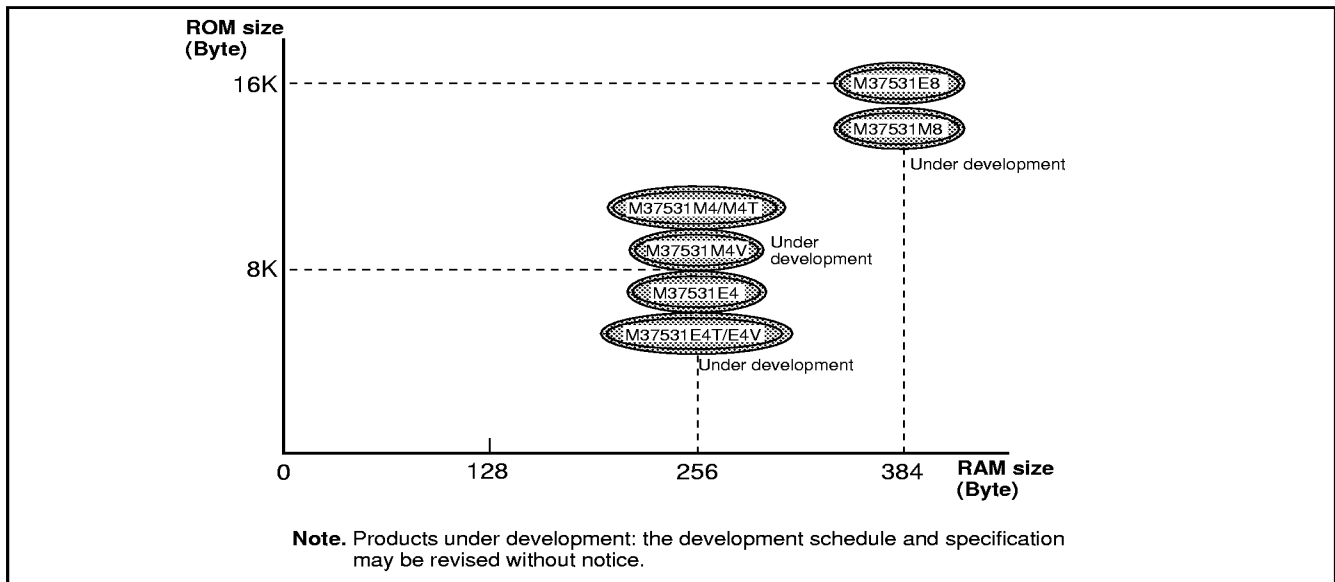


Fig. 8 Memory expansion plan

Currently supported products are listed below.

Table 2 List of supported products

Product	(P) ROM size (bytes) ROM size for User ( )	RAM size (bytes)	Package	Remarks
M37531M4-XXXSP	8192 (8062)	256	32P4B	Mask ROM version
M37531E4SP				One Time PROM version (blank)
M37531M4-XXXFP			36P2R-A	Mask ROM version
M37531E4FP				One Time PROM version (blank)
M37531M4-XXXGP			32P6B-A	Mask ROM version
M37531M4T-XXXGP				Mask ROM version (extended operating temperature version)
M37531M4V-XXXGP				Mask ROM version (extended operating temperature 125 °C version)
M37531E4GP				One Time PROM version (blank)
M37531E4T-XXXGP				One Time PROM version (shipped after writing, extended operating temperature version)
M37531E4V-XXXGP				One Time PROM version (shipped after writing, extended operating temperature 125 °C version)
M37531M8-XXXSP	16384 (16254)	384	32P4B	Mask ROM version
M37531E8SP				One Time PROM version (blank)
M37531M8-XXXFP			36P2R-A	Mask ROM version
M37531E8FP				One Time PROM version (blank)
M37531M8-XXXGP			32P6B-A	Mask ROM version
M37531RSS			42S1M	Emulator MCU



**FUNCTIONAL DESCRIPTION**

**Central Processing Unit (CPU)**

The 7531 Group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine-language instructions or the 740 Family Software MANUAL for details on each instruction set.

Machine-resident 740 family instructions are as follows:

1. The FST and SLW instructions cannot be used.
2. The MUL and DIV instructions cannot be used.
3. The WIT instruction can be used.
4. The STP instruction can be used.

**[CPU Mode Register] CPUM**

The CPU mode register contains the stack page selection bit. This register is allocated at address 003B<sub>16</sub>.

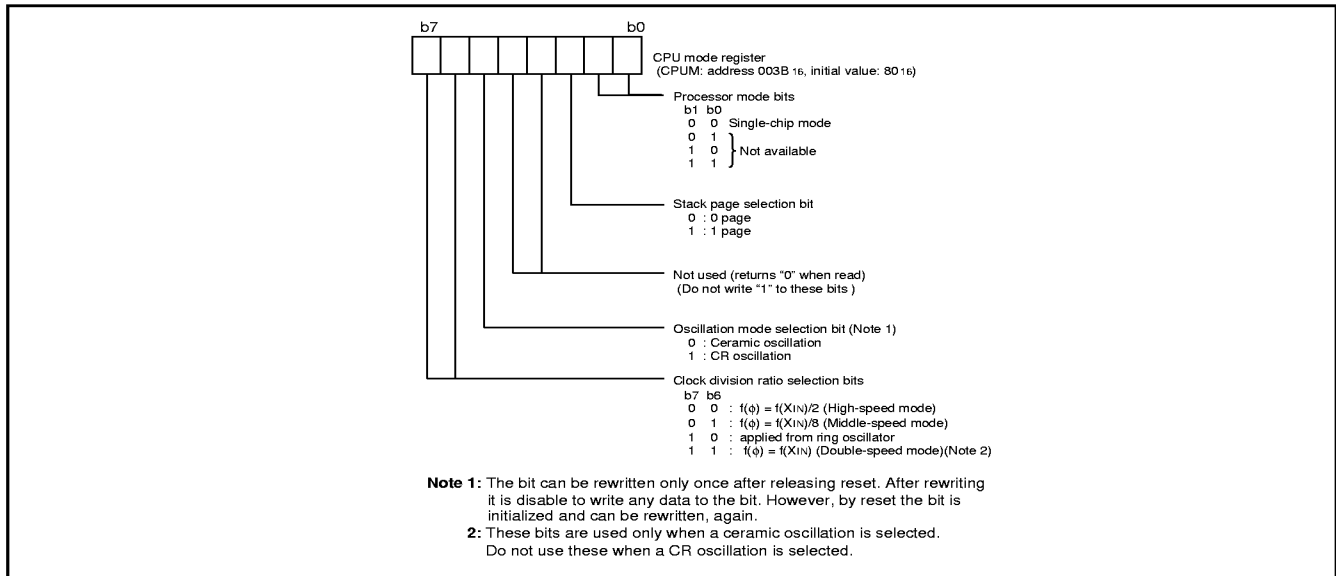


Fig. 9 Structure of CPU mode register

**Switching method of CPU mode register**

Switch the CPU mode register (CPUM) at the head of program after releasing Reset in the following method.

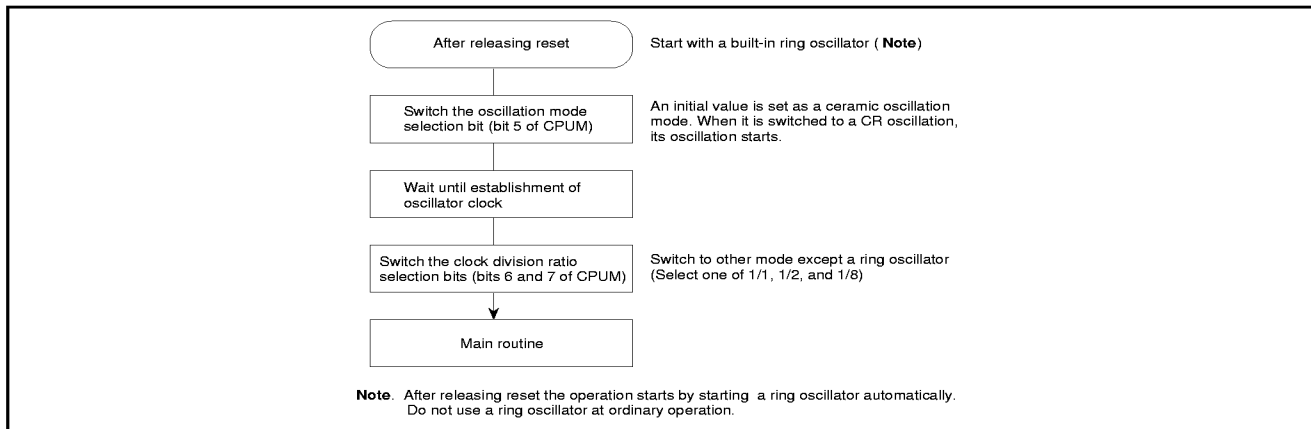


Fig. 10 Switching method of CPU mode register

## Memory

### Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

### RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

### ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

### Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

### Zero page

The 256 bytes from addresses  $0000_{16}$  to  $00FF_{16}$  are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

### Special page

The 256 bytes from addresses  $FF00_{16}$  to  $FFFF_{16}$  are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

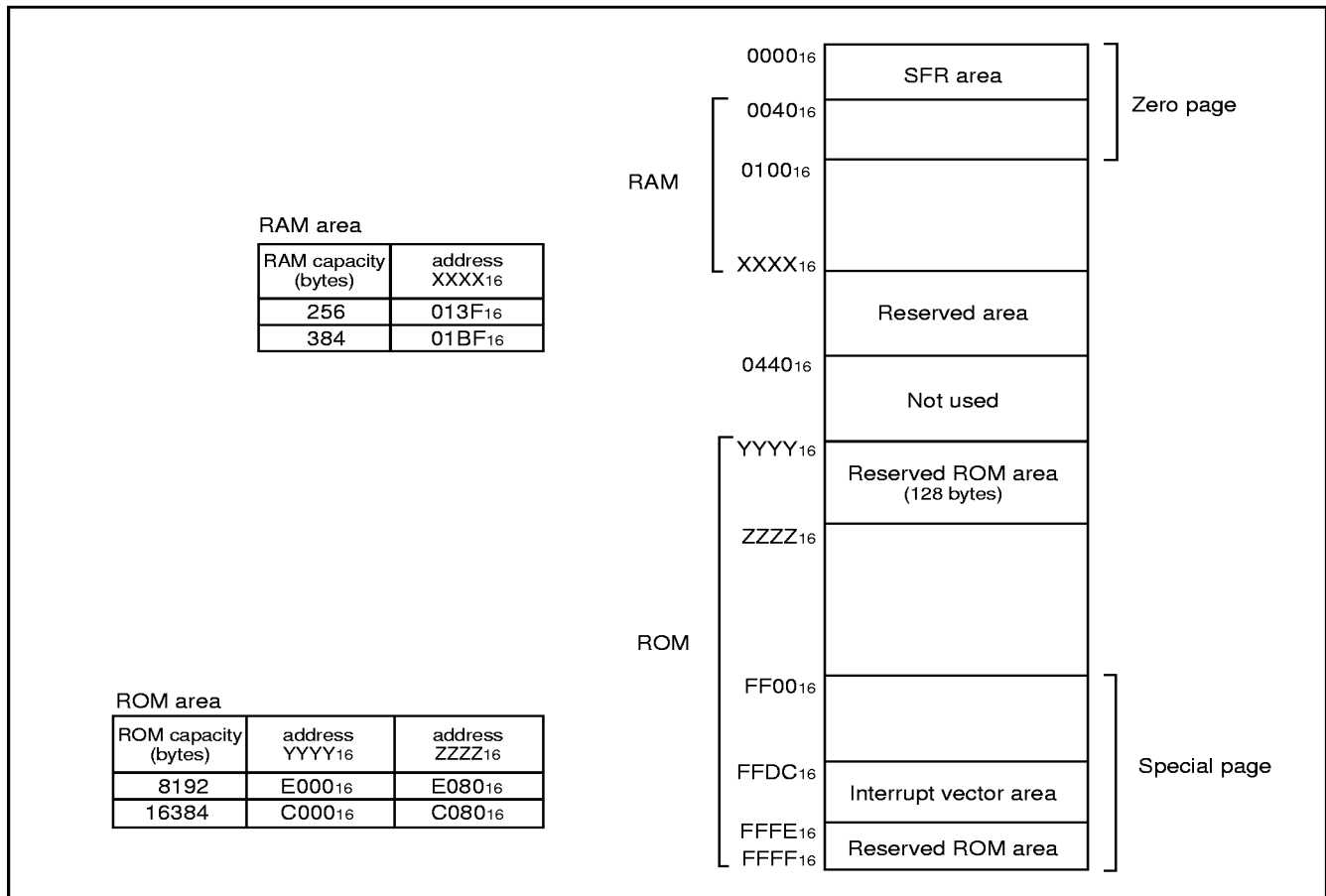


Fig. 11 Memory map diagram

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0000 <sub>16</sub>	Port P0 (P0)	0020 <sub>16</sub>	
0001 <sub>16</sub>	Port P0 direction register (P0D)	0021 <sub>16</sub>	
0002 <sub>16</sub>	Port P1 (P1)	0022 <sub>16</sub>	
0003 <sub>16</sub>	Port P1 direction register (P1D)	0023 <sub>16</sub>	
0004 <sub>16</sub>	Port P2 (P2)	0024 <sub>16</sub>	
0005 <sub>16</sub>	Port P2 direction register (P2D)	0025 <sub>16</sub>	
0006 <sub>16</sub>	Port P3 (P3)	0026 <sub>16</sub>	
0007 <sub>16</sub>	Port P3 direction register (P3D)	0027 <sub>16</sub>	
0008 <sub>16</sub>		0028 <sub>16</sub>	Prescaler 12 (PRE12)
0009 <sub>16</sub>		0029 <sub>16</sub>	Timer 1 (T1)
000A <sub>16</sub>		002A <sub>16</sub>	Timer 2 (T2)
000B <sub>16</sub>		002B <sub>16</sub>	Timer X mode register (TM)
000C <sub>16</sub>		002C <sub>16</sub>	Prescaler X (PREX)
000D <sub>16</sub>		002D <sub>16</sub>	Timer X (TX)
000E <sub>16</sub>		002E <sub>16</sub>	Timer count source set register (TCSS)
000F <sub>16</sub>		002F <sub>16</sub>	
0010 <sub>16</sub>		0030 <sub>16</sub>	Serial I/O2 control register (SIO2CON)
0011 <sub>16</sub>		0031 <sub>16</sub>	Serial I/O2 register (SIO2)
0012 <sub>16</sub>		0032 <sub>16</sub>	
0013 <sub>16</sub>		0033 <sub>16</sub>	
0014 <sub>16</sub>		0034 <sub>16</sub>	A-D control register (ADCON)
0015 <sub>16</sub>		0035 <sub>16</sub>	A-D conversion register (low-order) (ADL)
0016 <sub>16</sub>	Pull-up control register (PULL)	0036 <sub>16</sub>	A-D conversion register (high-order) (ADH)
0017 <sub>16</sub>	Port P1P3 control register (P1P3C)	0037 <sub>16</sub>	
0018 <sub>16</sub>	Transmit/Receive buffer register (TB/RB)	0038 <sub>16</sub>	MISRG
0019 <sub>16</sub>	Serial I/O1 status register (SIO1STS)	0039 <sub>16</sub>	Watchdog timer control register (WDTCN)
001A <sub>16</sub>	Serial I/O1 control register (SIO1CON)	003A <sub>16</sub>	Interrupt edge selection register (INTEEDGE)
001B <sub>16</sub>	UART control register (UARTCON)	003B <sub>16</sub>	CPU mode register (CPUM)
001C <sub>16</sub>	Baud rate generator (BRG)	003C <sub>16</sub>	Interrupt request register 1 (IREQ1)
001D <sub>16</sub>		003D <sub>16</sub>	
001E <sub>16</sub>		003E <sub>16</sub>	Interrupt control register 1 (ICON1)
001F <sub>16</sub>		003F <sub>16</sub>	

**Note :** Do not access to the SFR area including nothing.

Fig. 12 Memory map of special function register (SFR)

## I/O Ports

### [Direction registers] PiD

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output.

When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port. When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.

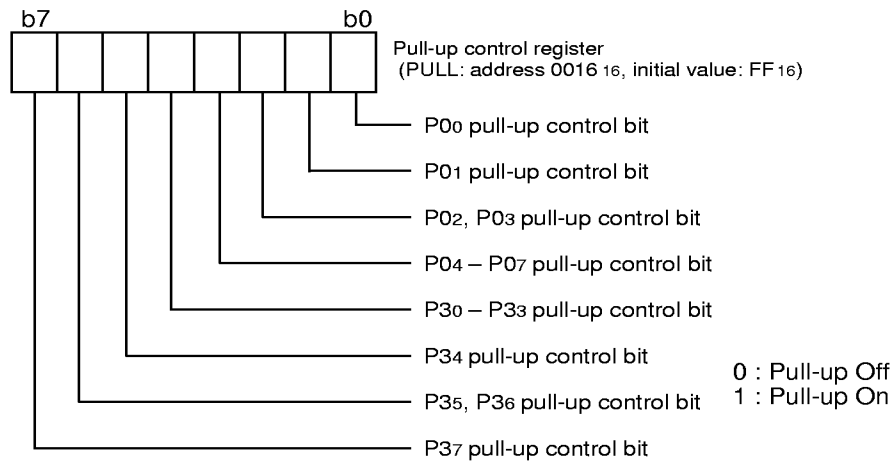
If a pin set to input is written to, only the port latch is written to and the pin remains floating.

### [Pull-up control] PULL

By setting the pull-up control register (address 0016<sub>16</sub>), ports P0 and P3 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

### [Port P1P3 control] P1P3C

By setting the port P1P3 control register (address 0017<sub>16</sub>), a CMOS input level or a TTL input level can be selected for ports P1<sub>0</sub>, P1<sub>2</sub>, P1<sub>3</sub>, P3<sub>6</sub>, and P3<sub>7</sub> by program.



**Note 1:** Pins set to output ports are disconnected from pull-up control.  
**Note 2:** Keep setting the P35, P36 pull-up control bit to "1" (initial value) for 32-pin version.

Fig. 13 Structure of pull-up control register

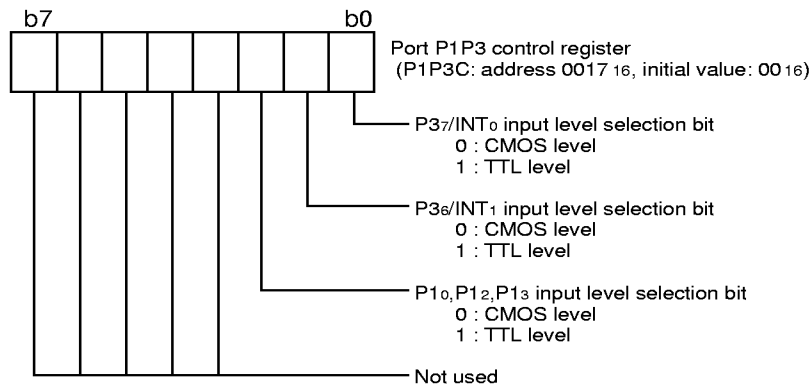


Fig. 14 Structure of port P1P3 control register

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**Table 3 I/O port function table**

Pin	Name	Input/output	I/O format	Non-port function	Related SFRs	Diagram No.
P0 <sub>0</sub> –P0 <sub>7</sub>	I/O port P0	I/O individual bits	•CMOS compatible input level •CMOS 3-state output (Note)	Key input interrupt	Pull-up control register	(1)
P1 <sub>0</sub> /RxD P1 <sub>1</sub> /TxD	I/O port P1			Serial I/O1 function input/output	Serial I/O1 control register	(2) (3)
P1 <sub>2</sub> /SCLK P1 <sub>3</sub> /SDATA				Serial I/O2 function input/output	Serial I/O2 control register	(4) (5)
P1 <sub>4</sub> /CNTR <sub>0</sub>				Timer X function input/output	Timer X mode register	(6)
P2 <sub>0</sub> /AN <sub>0</sub> – P2 <sub>7</sub> /AN <sub>7</sub>				I/O port P2	A-D conversion input	A-D control register
P3 <sub>0</sub> –P3 <sub>5</sub> P3 <sub>6</sub> /INT <sub>1</sub> P3 <sub>7</sub> /INT <sub>0</sub>	I/O port P3					(8)
				External interrupt input	Interrupt edge selection register	(9)

**Note:** Ports P1<sub>0</sub>, P1<sub>2</sub>, P1<sub>3</sub>, P3<sub>6</sub>, and P3<sub>7</sub> are CMOS/TTL level.

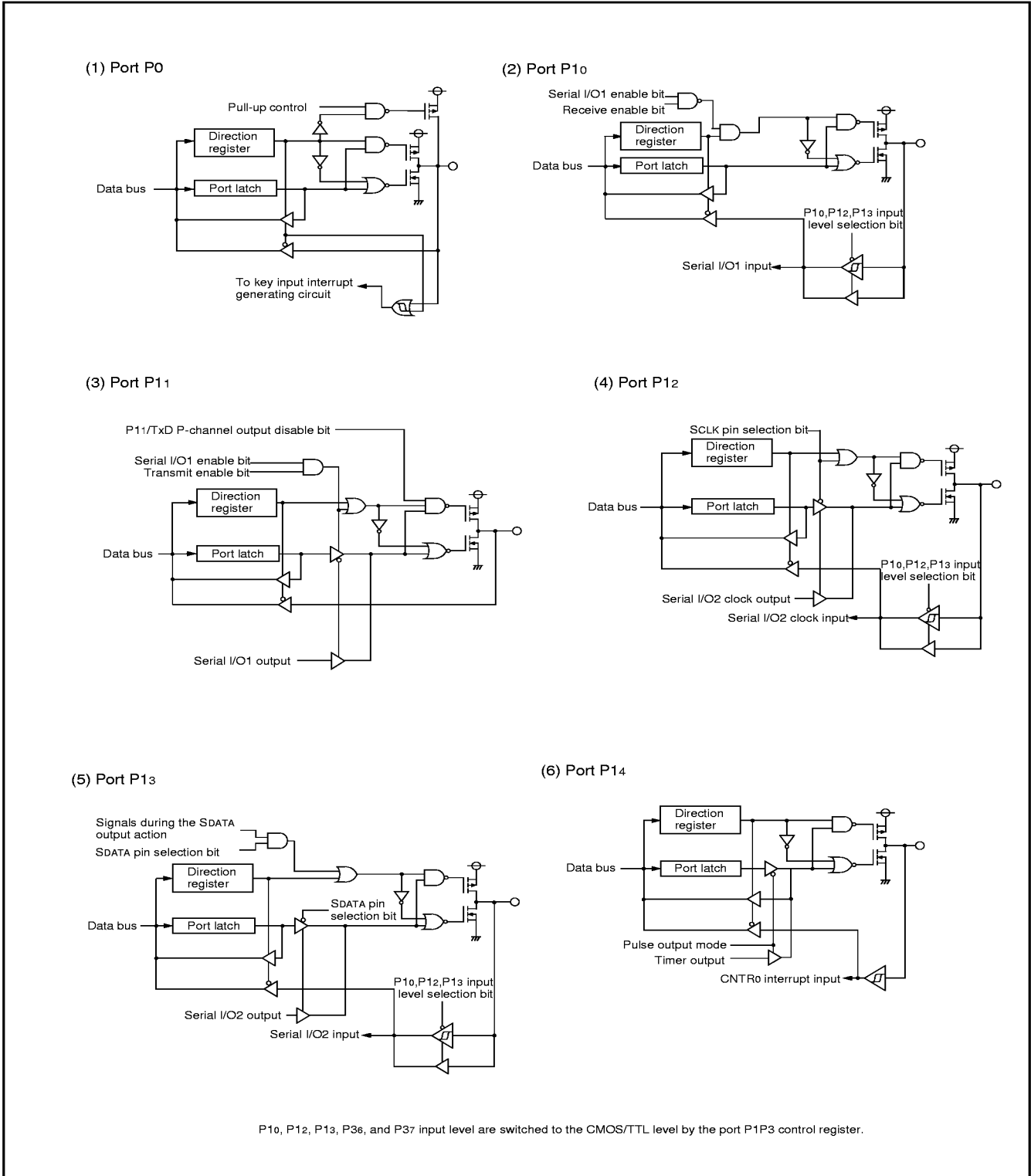


Fig. 15 Block diagram of ports (1)

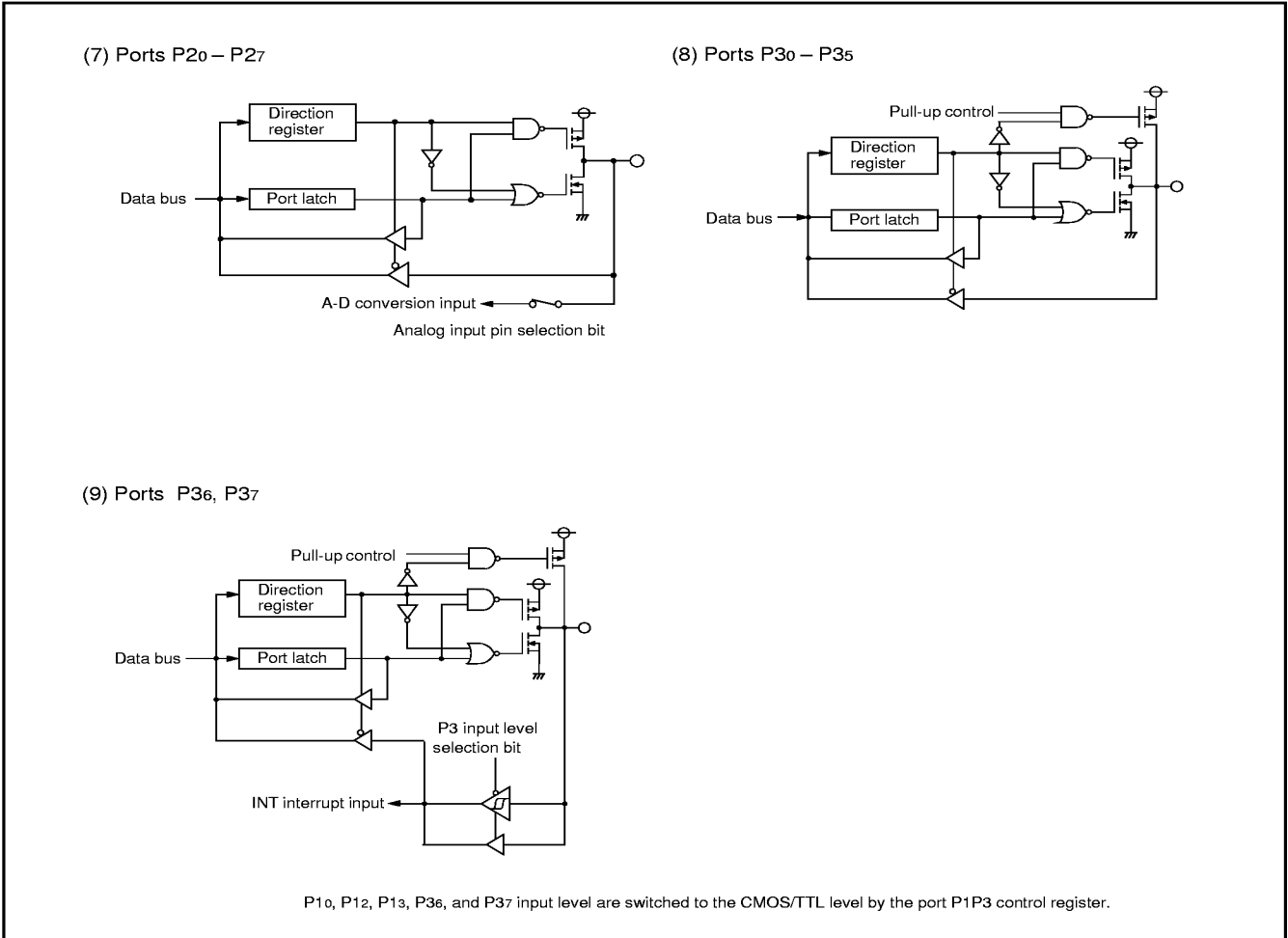


Fig. 16 Block diagram of ports (2)

## Interrupts

Interrupts occur by 12 different sources : 4 external sources, 7 internal sources and 1 software source.

### Interrupt control

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit, and they are controlled by the interrupt disable flag. When the interrupt enable bit and the interrupt request bit are set to "1" and the interrupt disable flag is set to "0", an interrupt is accepted.

The interrupt request bit can be cleared by program but not be set. The interrupt enable bit can be set and cleared by program.

It becomes usable by switching CNTR<sub>0</sub> and AD conversion interrupt sources with bit 7 of the interrupt edge selection register, timer 2 and serial I/O<sub>2</sub> interrupt sources with bit 6, timer X and key-on wake-up interrupt sources with bit 5, and serial I/O<sub>1</sub> transmit and INT<sub>1</sub> interrupt sources with bit 4.

The reset and BRK instruction interrupt can never be disabled with any flag or bit. All interrupts except these are disabled when the interrupt disable flag is set.

When several interrupts occur at the same time, the interrupts are received according to priority.

### Interrupt operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. Concurrently with the push operation, the interrupt destination address is read from the vector table into the program counter.

### Notes on use

When the active edge of an external interrupt (INT<sub>0</sub>, INT<sub>1</sub>, CNTR<sub>0</sub>) is set, the interrupt request bit may be set.

Therefore, please take following sequence:

1. Disable the external interrupt which is selected.
2. Change the active edge in interrupt edge selection register. (in case of CNTR<sub>0</sub>: Timer X mode register)
3. Clear the set interrupt request bit to "0".
4. Enable the external interrupt which is selected.

**Table 4 Interrupt vector address and priority**

Interrupt source	Priority	Vector addresses (Note 1)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (Note 2)	1	FFFD <sub>16</sub>	FFFC <sub>16</sub>	At reset input	Non-maskable
Serial I/O <sub>1</sub> receive	2	FFFB <sub>16</sub>	FFFA <sub>16</sub>	At completion of serial I/O <sub>1</sub> data receive	Valid when serial I/O <sub>1</sub> is selected
Serial I/O <sub>1</sub> transmit	3	FFF9 <sub>16</sub>	FFF8 <sub>16</sub>	At completion of serial I/O <sub>1</sub> transmit shift or when transmit buffer is empty	Valid when serial I/O <sub>1</sub> is selected
INT <sub>1</sub> (Note 3)				At detection of either rising or falling edge of INT <sub>1</sub> input	External interrupt (active edge selectable)
INT <sub>0</sub>	4	FFF7 <sub>16</sub>	FFF6 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>0</sub> input	External interrupt (active edge selectable)
Timer X	5	FFF5 <sub>16</sub>	FFF4 <sub>16</sub>	At timer X underflow	
Key-on wake-up				At falling of conjunction of input logical level for port P <sub>0</sub> (at input)	External interrupt (valid at falling)
Timer 1	6	FFF3 <sub>16</sub>	FFF2 <sub>16</sub>	At timer 1 underflow	STP release timer underflow
Timer 2	7	FFF1 <sub>16</sub>	FFF0 <sub>16</sub>	At timer 2 underflow	
Serial I/O <sub>2</sub>				At completion of transmit/receive shift	
CNTR <sub>0</sub>	8	FEEF <sub>16</sub>	FEE0 <sub>16</sub>	At detection of either rising or falling edge of CNTR <sub>0</sub> input	External interrupt (active edge selectable)
A-D conversion				At completion of A-D conversion	
BRK instruction	9	FFED <sub>16</sub>	FFEC <sub>16</sub>	At BRK instruction execution	Non-maskable software interrupt

**Note 1:** Vector addressed contain internal jump destination addresses.

**2:** Reset function in the same way as an interrupt with the highest priority.

**3:** It is an interrupt which can use only for 32 pin version.



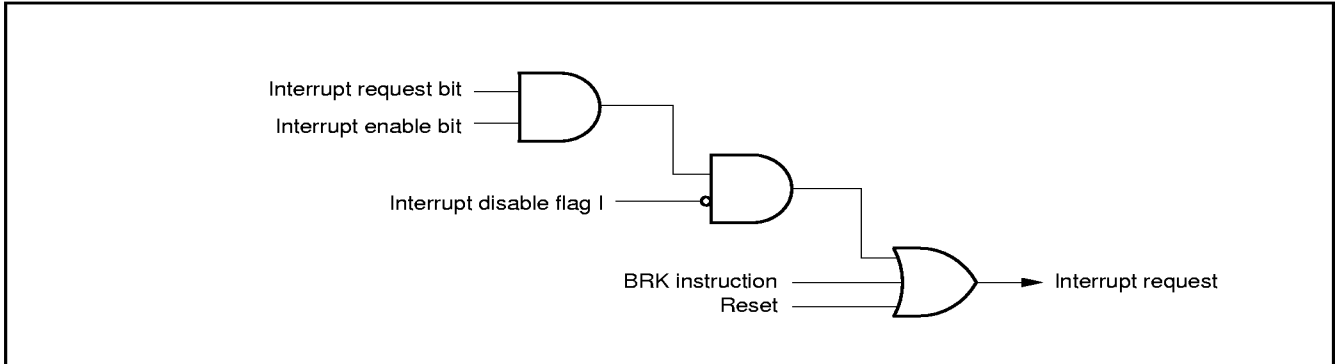


Fig. 17 Interrupt control

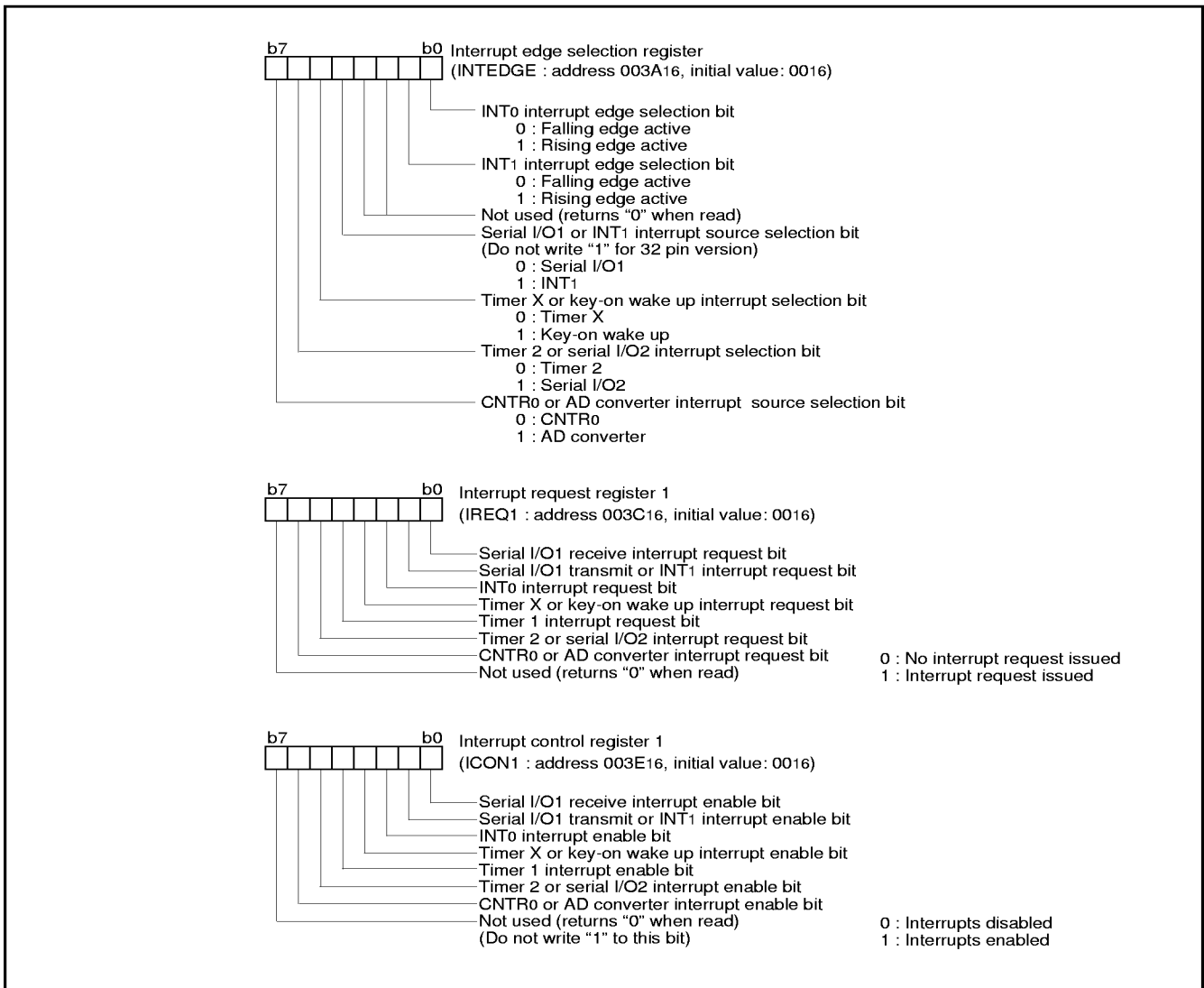


Fig. 18 Structure of Interrupt-related registers

### Key Input Interrupt (Key-On Wake-Up)

A key-on wake-up interrupt request is generated by applying "L" level to any pin of port P0 that has been set to input mode.

In other words, it is generated when the AND of input level goes from "1" to "0". An example of using a key input interrupt is shown in Figure 19, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports P00 to P04 as input ports.

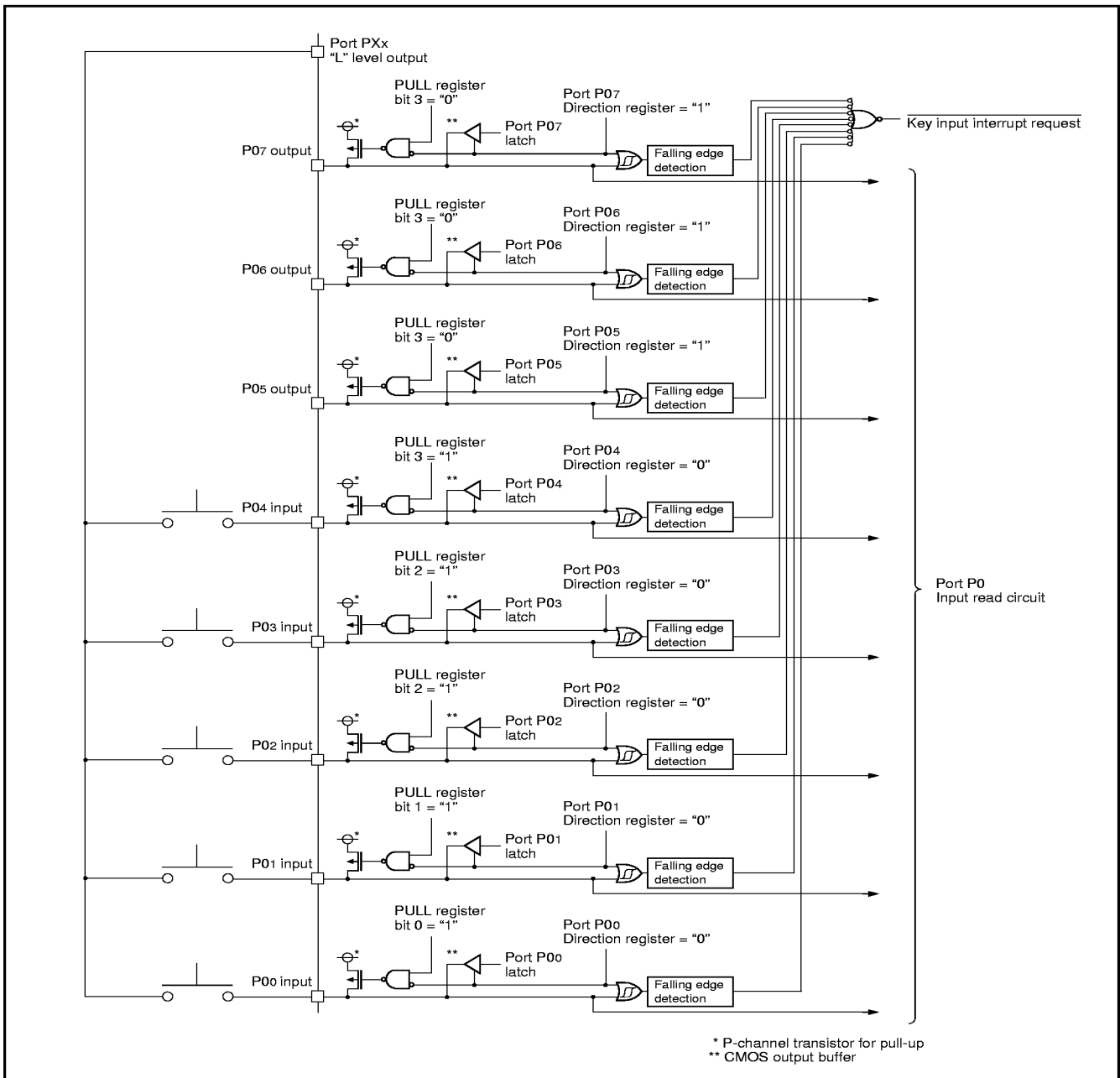


Fig. 19 Connection example when using key input interrupt and port P0 block diagram

## Timers

The 7531 Group has 3 timers: timer X, timer 1 and timer 2. The division ratio of every timer and prescaler is  $1/(n+1)$  provided that the value of the timer latch or prescaler is  $n$ . All the timers are down count timers. When a timer reaches "0", an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to "1".

### ●Timer 1, Timer 2

Prescaler 12 always counts  $f(X_{IN})/16$ . Timer 1 and timer 2 always count the prescaler output and periodically sets the interrupt request bit.

### ●Timer X

Timer X can be selected in one of 4 operating modes by setting the timer X mode register.

#### • Timer Mode

The timer counts the signal selected by the timer X count source selection bit.

#### • Pulse Output Mode

The timer counts the signal selected by the timer X count source selection bit, and outputs a signal whose polarity is inverted each time the timer value reaches "0", from the CNTR<sub>0</sub> pin. When the CNTR<sub>0</sub> active edge switch bit is "0", the output of the CNTR<sub>0</sub> pin is started with an "H" output. At "1", this output is started with an "L" output. When using a timer in this mode, set the port P14 direction register to output mode.

#### • Event Counter Mode

The operation in the event counter mode is the same as that in the timer mode except that the timer counts the input signal from the CNTR<sub>0</sub> pin. When the CNTR<sub>0</sub> active edge switch bit is "0", the timer counts the rising edge of the CNTR<sub>0</sub> pin. When this bit is "1", the timer counts the falling edge of the CNTR<sub>0</sub> pin.

#### • Pulse Width Measurement Mode

When the CNTR<sub>0</sub> active edge switch bit is "0", the timer counts the signal selected by the timer X count source selection bit while the CNTR<sub>0</sub> pin is "H". When this bit is "1", the timer counts the signal while the CNTR<sub>0</sub> pin is "L". In any mode, the timer count can be stopped by setting the timer X count stop bit to "1". Each time the timer overflows, the interrupt request bit is set.

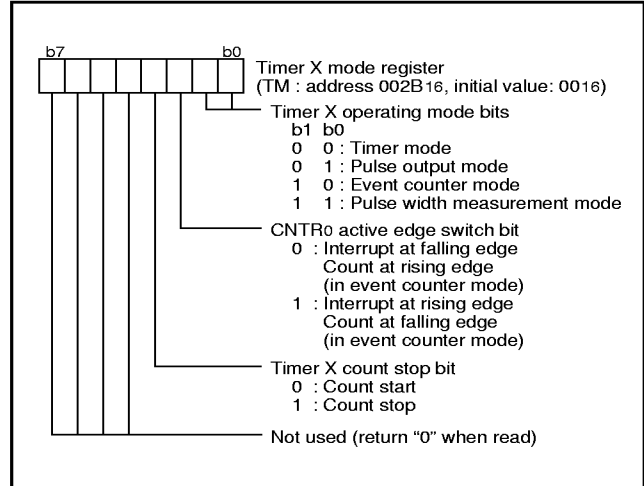


Fig. 20 Structure of timer X mode register

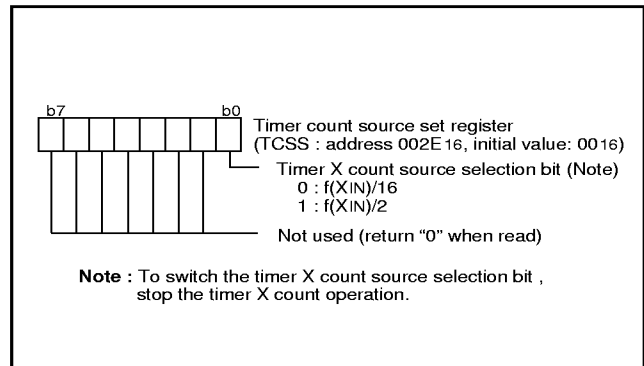


Fig. 21 Timer count source setting register

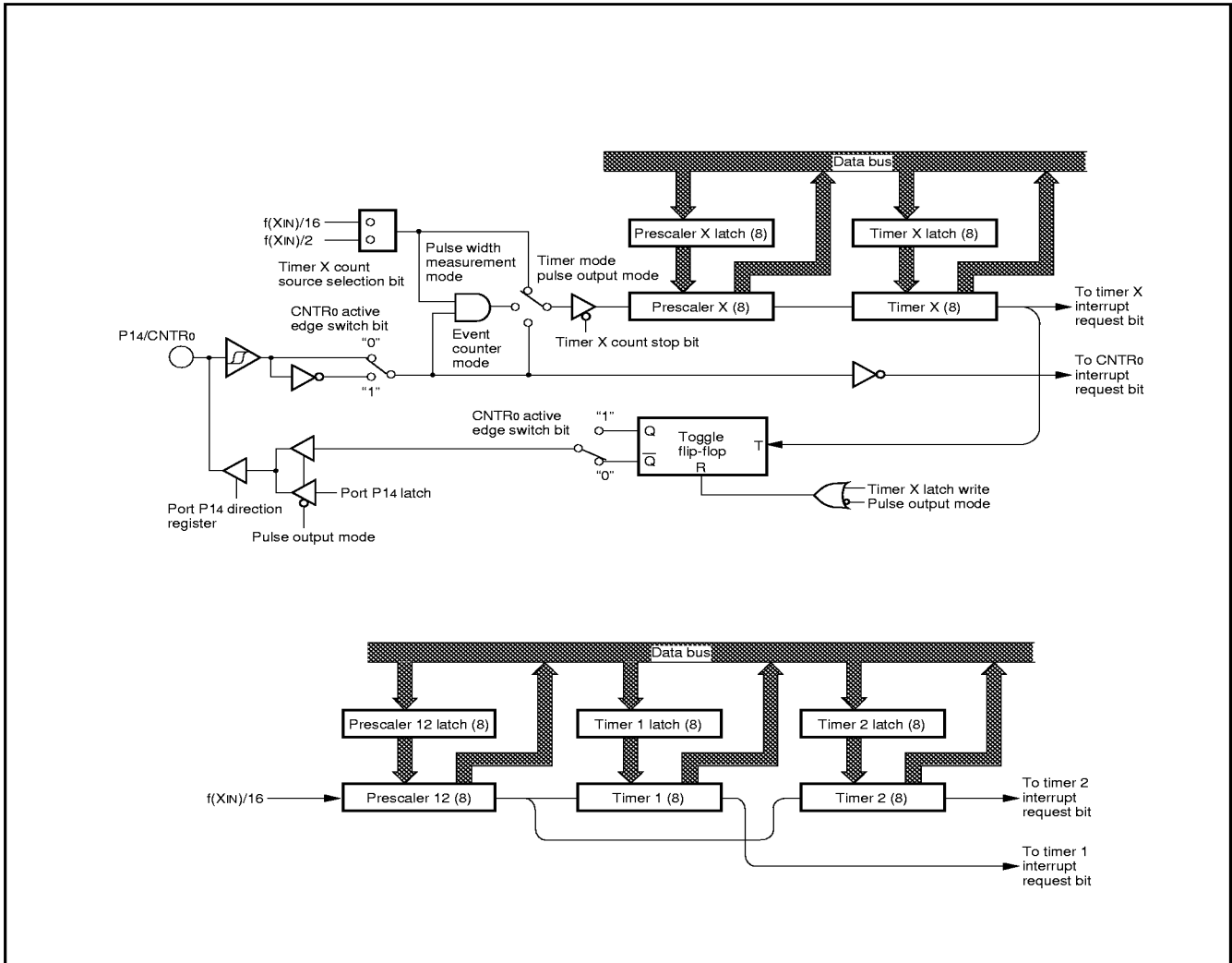


Fig. 22 Block diagram of timer X, timer 1 and timer 2

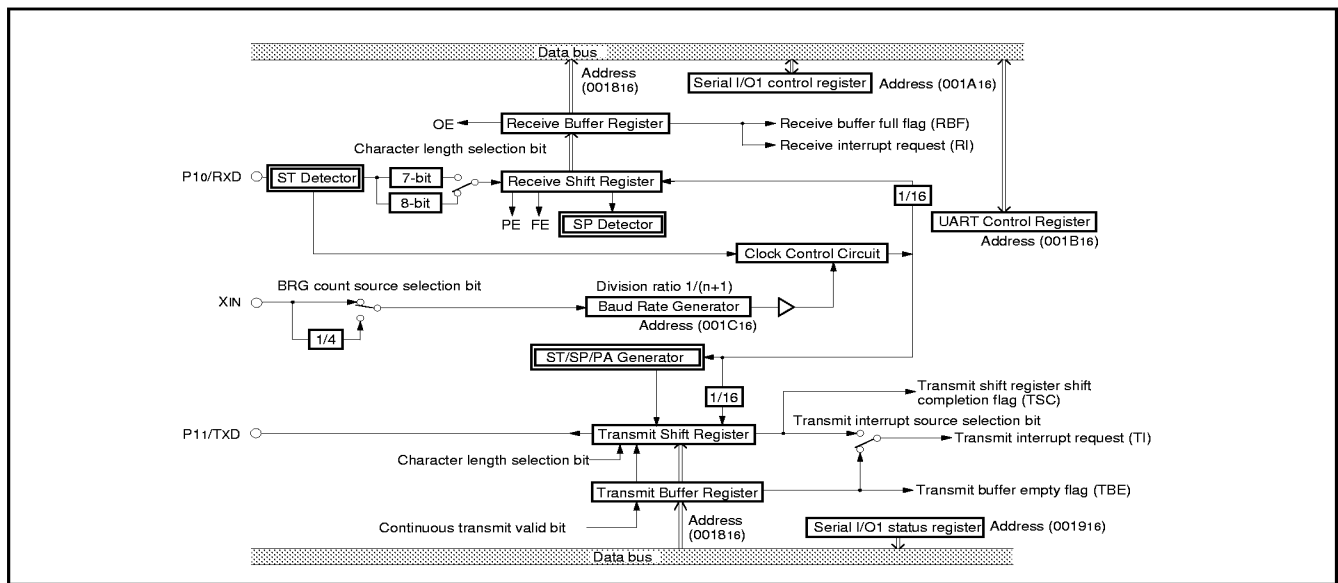
**Serial I/O**

**Serial I/O1**

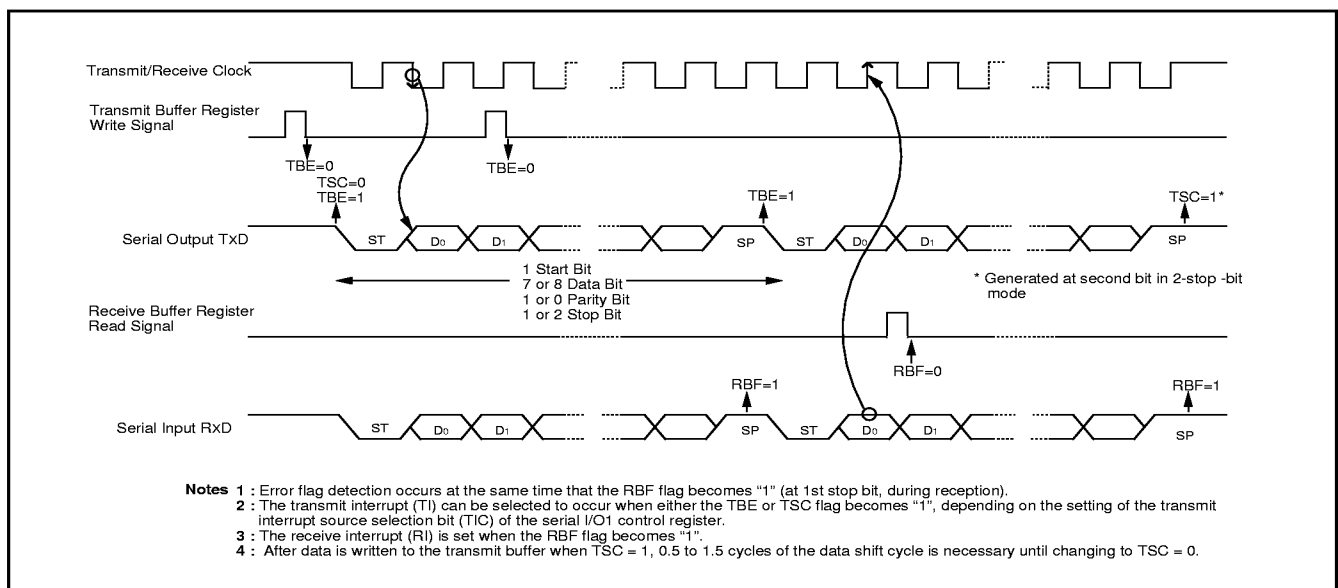
Serial I/O1 can be used as an asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation when serial I/O1 is in operation.

Eight serial data transfer formats can be selected, and the transfer formats to be used by a transmitter and a receiver must be identical. Each of the transmit and receive shift registers has a buffer register (the same address on memory). Since the shift register cannot be written to or read from directly, transmit data is written to the transmit

buffer, and receive data is read from the respective buffer registers. These buffer registers can also hold the next data to be transmitted and receive 2-byte receive data in succession. By selecting "1" for continuous transmit valid bit (bit 2 of SIO1CON), continuous transmission of the same data is made possible. This can be used as a simplified PWM.



**Fig. 23 Block diagram of UART serial I/O**



**Fig. 24 Operation of UART serial I/O function**

**[Serial I/O1 control register] SIO1CON**

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

**[UART control register] UARTCON**

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P11/TxD pin.

**[Serial I/O1 status register] SIO1STS**

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "11" to bits 7 and 6 of the serial I/O1 control register initializes this register.

All bits of the serial I/O1 status register are initialized to "8116" at reset.

**[Transmit/Receive buffer register] TB/RB**

The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7-bit, the MSB of data stored in the receive buffer is "0".

**[Baud Rate Generator] BRG**

The baud rate generator determines the baud rate for serial transfer. The baud rate generator divides the frequency of the count source by  $1/(n + 1)$ , where n is the value written to the baud rate generator.

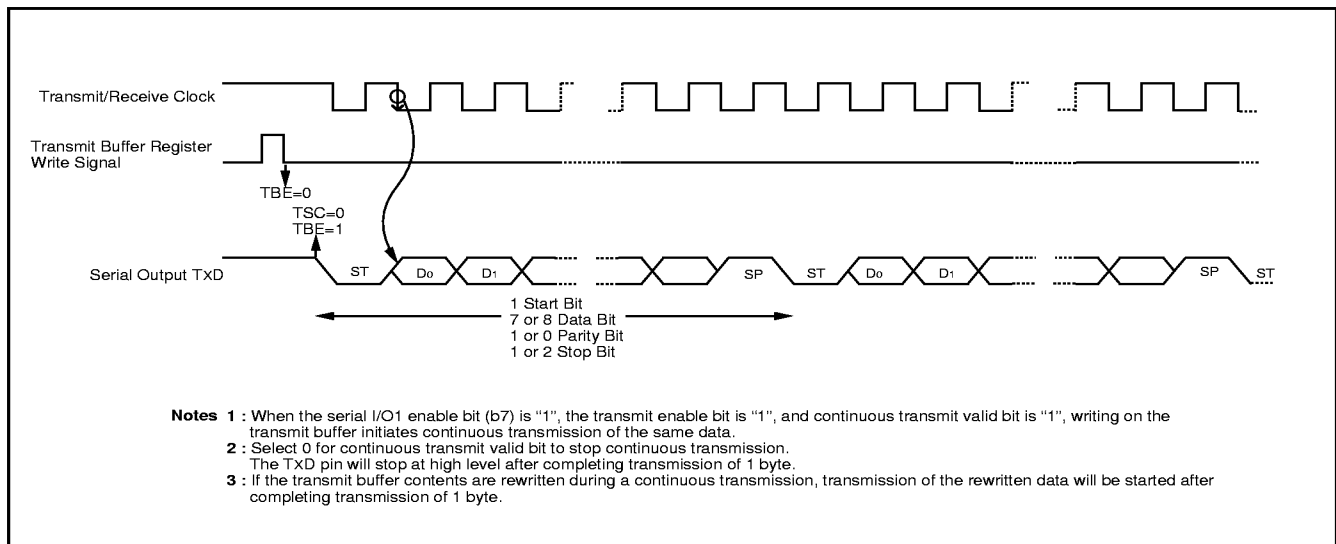


Fig. 25 Continuous transmission operation of UART serial I/O

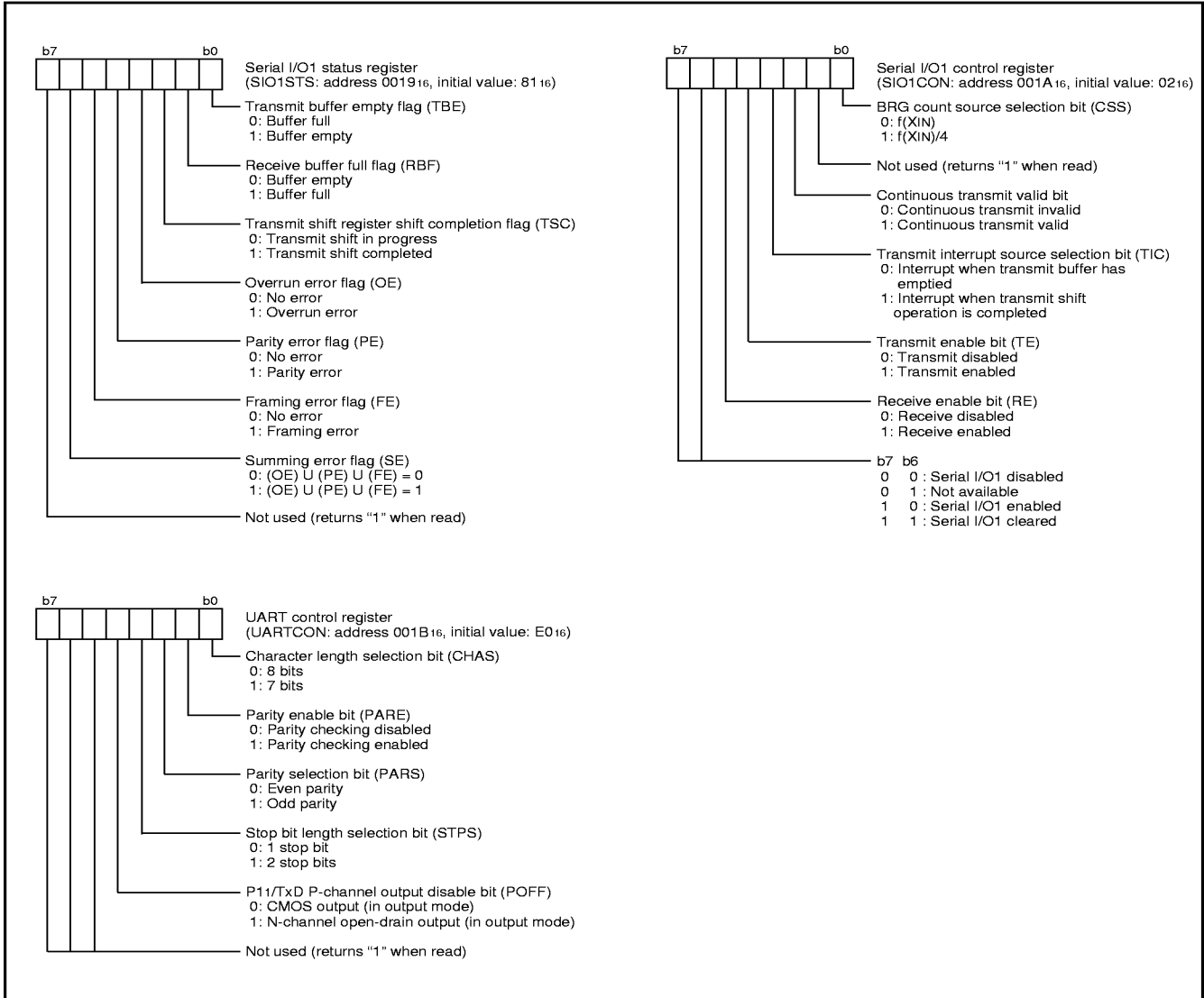


Fig. 26 Structure of serial I/O1-related registers (1)

●Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O2 the transmitter and the receiver must use the same clock. When the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

[Serial I/O2 control register] SIO2CON

The serial I/O2 control register contains 8 bits which control various serial I/O functions.

- Set "0" to bit 3 to receive.
- At reception, clear bit 7 to "0" by writing a dummy data to the serial I/O2 register after completion of shift.
- Bit 7 is set to "1" a half cycle (of the shift clock) earlier than completion of shift operation. Accordingly, when using this bit to confirm shift completion, a half cycle or more of the shift clock must pass after confirming that this bit is set to "1", before performing read/write to the serial I/O2 register.

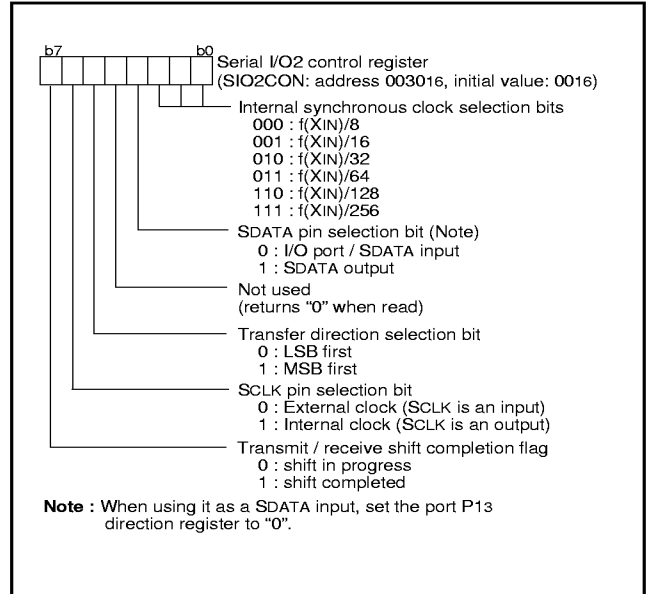


Fig. 27 Structure of serial I/O2 control registers

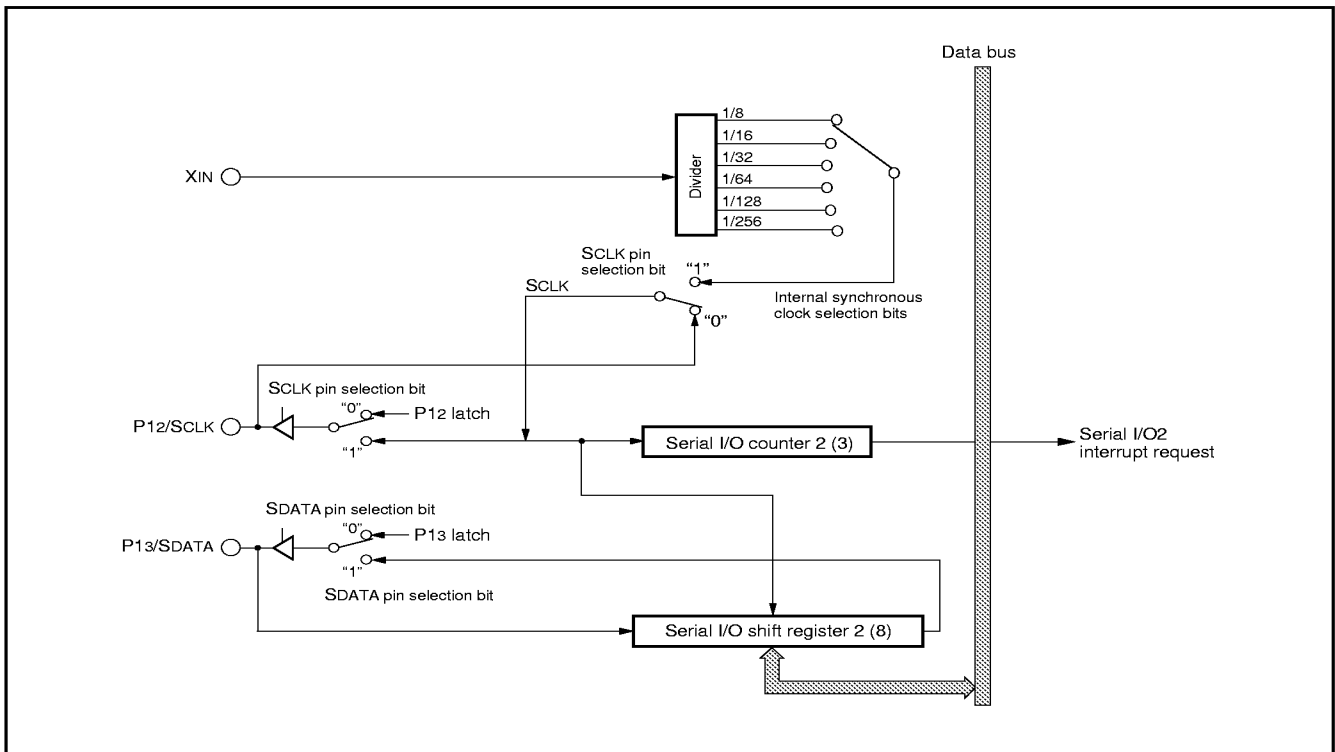


Fig. 28 Block diagram of serial I/O2



**Serial I/O2 operation**

By writing to the serial I/O2 register (address 0031<sub>16</sub>) the serial I/O2 counter is set to "7".

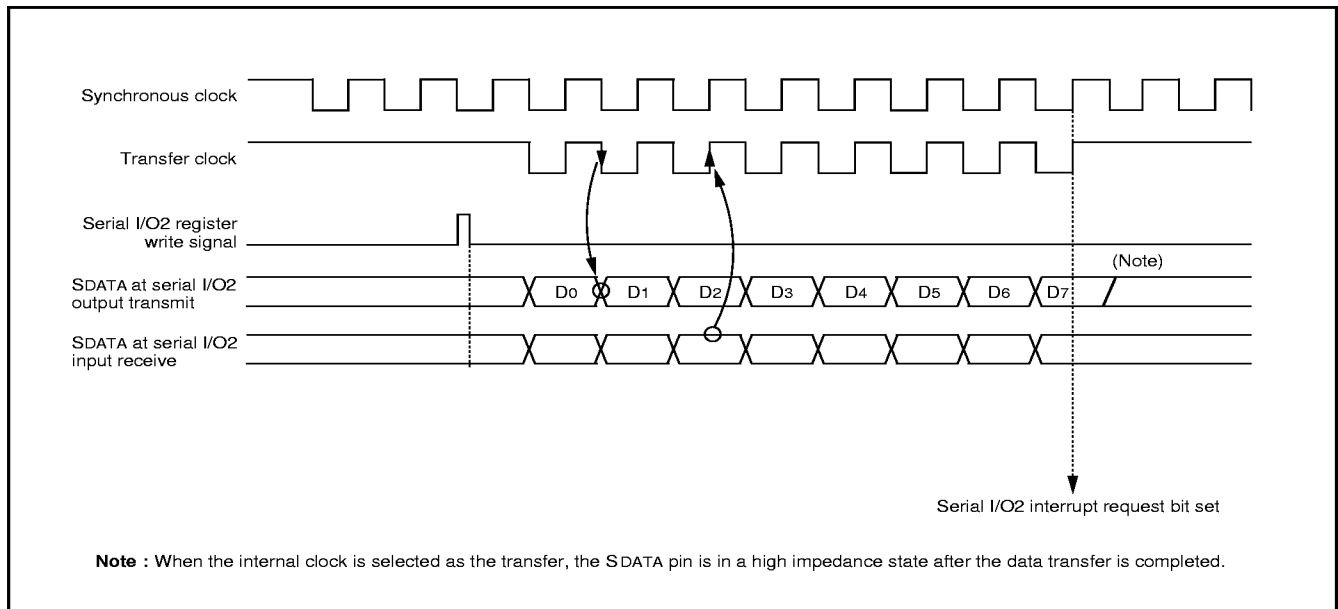
After writing, the SDATA pin outputs data every time the transfer clock shifts from a high to a low level. And, as the transfer clock shifts from a low to a high, the SDATA pin reads data, and at the same time the contents of the serial I/O2 register are shifted by 1 bit.

When the internal clock is selected as the transfer clock source, the following operations execute as the transfer clock counts up to 8.

- Serial I/O2 counter is cleared to "0".
- Transfer clock stops at an "H" level.
- Interrupt request bit is set.
- Shift completion flag is set.

Also, the SDATA pin is in a high impedance state after the data transfer is complete.

When the external clock is selected as the transfer clock source, the interrupt request bit is set as the transfer clock counts up to 8, but external control of the clock is required since it does not stop. Notice that the SDATA pin is not in a high impedance state on the completion of data transfer.



**Fig. 29 Serial I/O2 timing (LSB first)**

## A-D Converter

The functional blocks of the A-D converter are described below.

### [A-D conversion register] AD

The A-D conversion register is a read-only register that stores the result of A-D conversion. Do not read out this register during an A-D conversion.

### [A-D control register] ADCON

The A-D control register controls the A-D converter. Bit 2 to 0 are analog input pin selection bits. Bit 4 is the AD conversion completion bit. The value of this bit remains at "0" during A-D conversion, and changes to "1" at completion of A-D conversion. A-D conversion is started by setting this bit to "0".

### [Comparison voltage generator]

The comparison voltage generator divides the voltage between AVSS and VREF by 1024, and outputs the divided voltages.

### [Channel Selector]

The channel selector selects one of ports P27/AN7 to P20/AN0, and inputs the voltage to the comparator.

### [Comparator and control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the A-D conversion register. When A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1". Because the comparator is constructed linked to a capacitor, set f(XIN) to 500 kHz or more during A-D conversion.

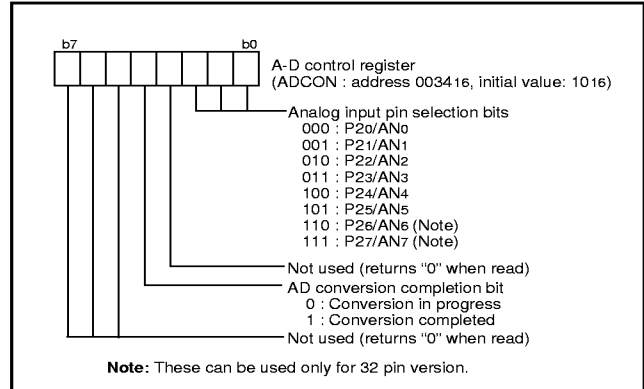


Fig. 30 Structure of A-D control register

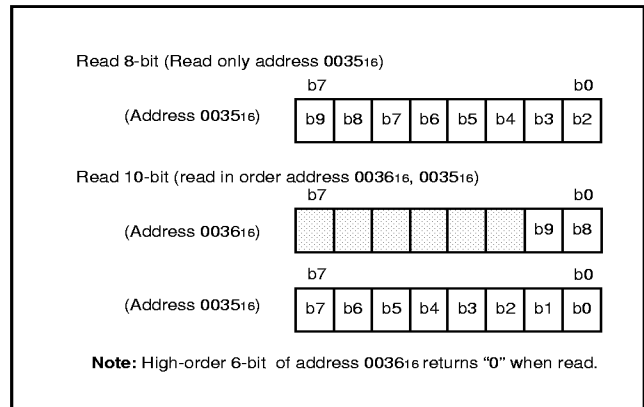


Fig. 31 Structure of A-D conversion register

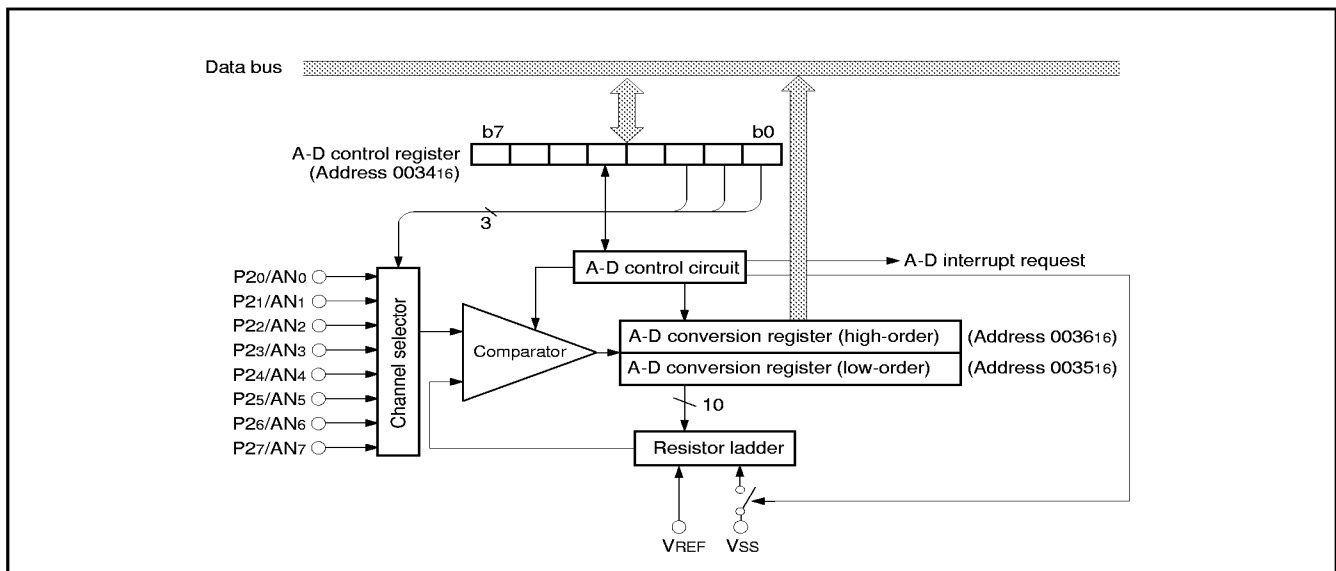


Fig. 32 Block diagram of A-D converter

## Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter.

### Standard operation of watchdog timer

The watchdog timer stops when the watchdog timer control register (address 0039<sub>16</sub>) is not set after reset. Writing an optional value to the watchdog timer control register (address 0039<sub>16</sub>) causes the watchdog timer to start to count down. When the watchdog timer H underflows, an internal reset occurs. Accordingly, it is programmed that the watchdog timer control register (address 0039<sub>16</sub>) can be set before an underflow occurs.

When the watchdog timer control register (address 0039<sub>16</sub>) is read, the values of the high-order 6-bit of the watchdog timer H, STP instruction disable bit and watchdog timer H count source selection bit are read.

### Initial value of watchdog timer

By a reset or writing to the watchdog timer control register (address 0039<sub>16</sub>), the watchdog timer H is set to "FF<sub>16</sub>" and the watchdog timer L is set to "FF<sub>16</sub>".

### Operation of watchdog timer H count source selection bit

A watchdog timer H count source can be selected by bit 7 of the watchdog timer control register (address 0039<sub>16</sub>). When this bit is "0", the count source becomes a watchdog timer L underflow signal. The detection time is 131.072 ms at f(X<sub>IN</sub>)=8 MHz.

When this bit is "1", the count source becomes f(X<sub>IN</sub>)/16. In this case, the detection time is 512 μs at f(X<sub>IN</sub>)=8 MHz.

This bit is cleared to "0" after reset.

### Operation of STP instruction disable bit

When the watchdog timer is in operation, the STP instruction can be disabled by bit 6 of the watchdog timer control register (address 0039<sub>16</sub>).

When this bit is "0", the STP instruction is enabled.

When this bit is "1", the STP instruction is disabled, and an internal reset occurs if the STP instruction is executed.

Once this bit is set to "1", it cannot be changed to "0" by program.

This bit is cleared to "0" after reset.

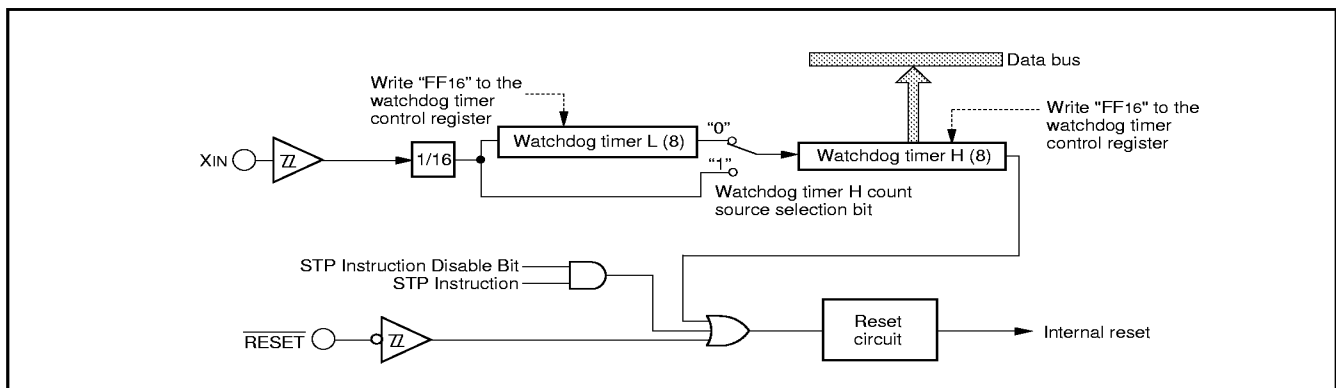


Fig. 33 Block diagram of watchdog timer

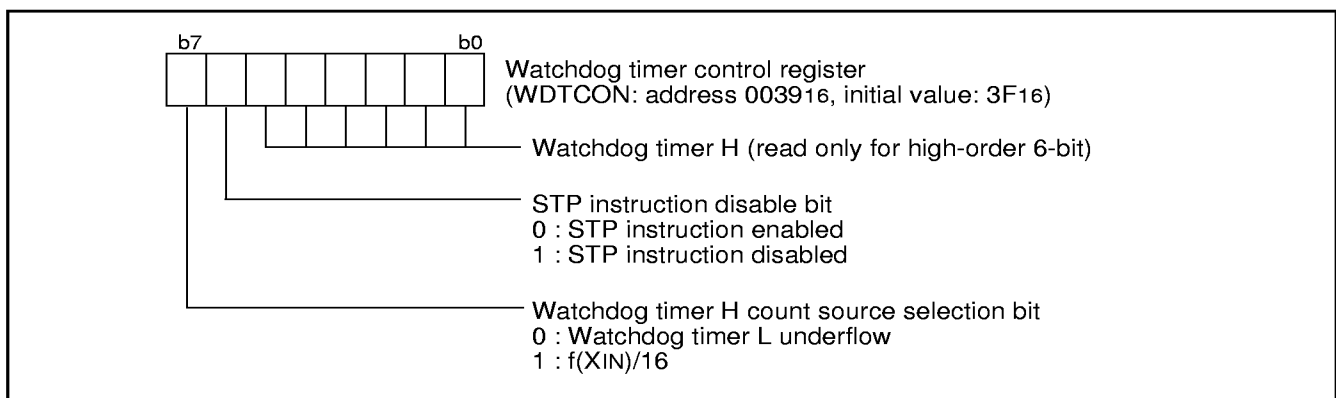


Fig. 34 Structure of watchdog timer control register

### Reset Circuit

The microcomputer is put into a reset status by holding the  $\overline{\text{RESET}}$  pin at the "L" level for 2  $\mu\text{s}$  or more when the power source voltage is 2.2 to 5.5 V and  $X_{\text{IN}}$  is in stable oscillation.

After that, this reset status is released by returning the  $\overline{\text{RESET}}$  pin to the "H" level. The program starts from the address having the contents of address  $\text{FFFD}_{16}$  as high-order address and the contents of address  $\text{FFFC}_{16}$  as low-order address.

In the case of  $f(\phi) \leq 4 \text{ MHz}$ , the reset input voltage must be 0.8 V or less when the power source voltage passes 4.0 V.

In the case of  $f(\phi) \leq 2 \text{ MHz}$ , the reset input voltage must be 0.48 V or less when the power source voltage passes 2.4 V.

In the case of  $f(\phi) \leq 1 \text{ MHz}$ , the reset input voltage must be 0.44 V or less when the power source voltage passes 2.2 V.

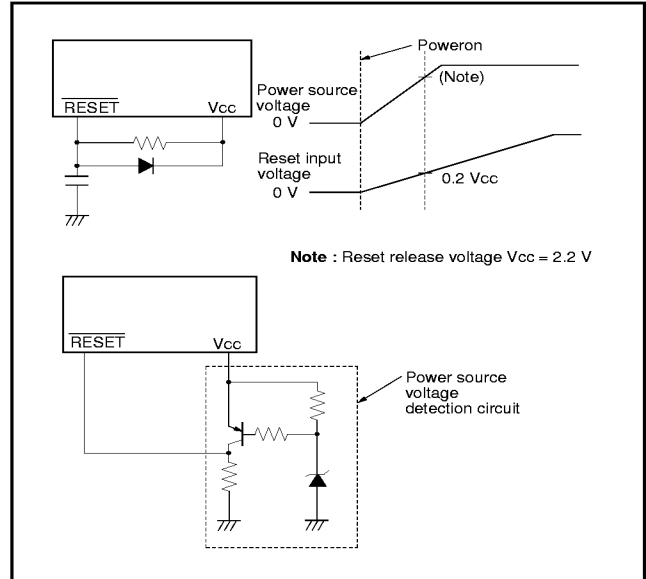


Fig. 35 Example of reset circuit

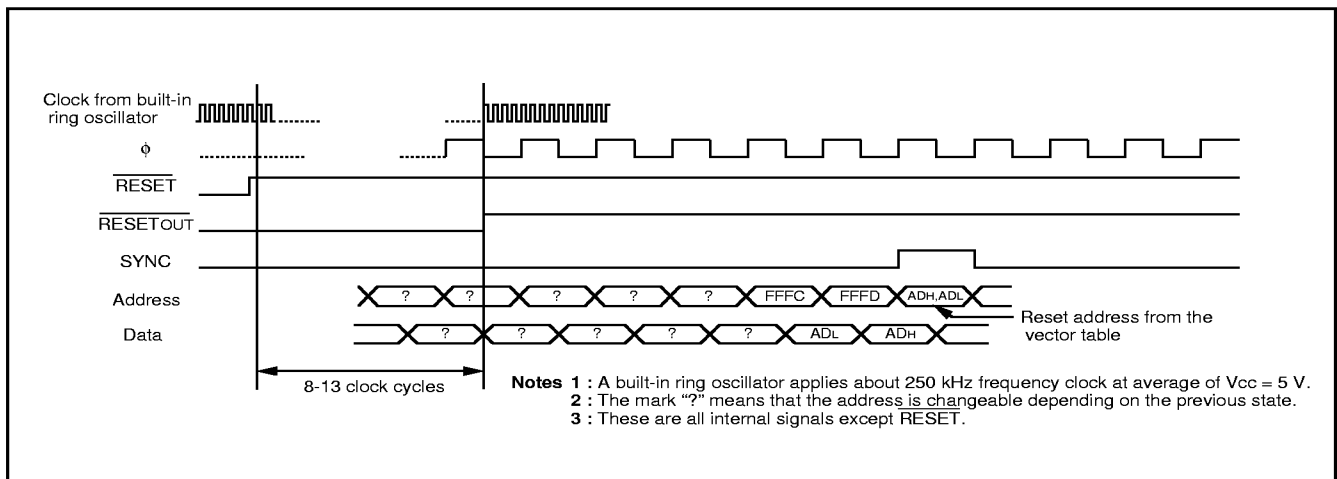


Fig. 36 Timing diagram at reset

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	Address	Register contents
(1) Port P0 direction register	0001 <sub>16</sub>	00 <sub>16</sub>
(2) Port P1 direction register	0003 <sub>16</sub>	X X X 0 0 0 0 0
(3) Port P2 direction register	0005 <sub>16</sub>	00 <sub>16</sub>
(4) Port P3 direction register	0007 <sub>16</sub>	00 <sub>16</sub>
(5) Pull-up control register	0016 <sub>16</sub>	FF <sub>16</sub>
(6) Port P1P3 control register	0017 <sub>16</sub>	00 <sub>16</sub>
(7) Serial I/O1 status register	0019 <sub>16</sub>	1 0 0 0 0 0 0 1
(8) Serial I/O1 control register	001A <sub>16</sub>	02 <sub>16</sub>
(9) UART control register	001B <sub>16</sub>	1 1 1 0 0 0 0 0
(10) Prescaler 12	0028 <sub>16</sub>	FF <sub>16</sub>
(11) Timer 1	0029 <sub>16</sub>	01 <sub>16</sub>
(12) Timer 2	002A <sub>16</sub>	00 <sub>16</sub>
(13) Timer X mode register	002B <sub>16</sub>	00 <sub>16</sub>
(14) Prescaler X	002C <sub>16</sub>	FF <sub>16</sub>
(15) Timer X	002D <sub>16</sub>	FF <sub>16</sub>
(16) Timer count source set register	002E <sub>16</sub>	00 <sub>16</sub>
(17) Serial I/O2 control register	0030 <sub>16</sub>	00 <sub>16</sub>
(18) A-D control register	0034 <sub>16</sub>	10 <sub>16</sub>
(19) MISRG	0038 <sub>16</sub>	00 <sub>16</sub>
(20) Watchdog timer control register	0039 <sub>16</sub>	0 0 1 1 1 1 1 1
(21) Interrupt edge selection register	003A <sub>16</sub>	00 <sub>16</sub>
(22) CPU mode register	003B <sub>16</sub>	1 0 0 0 0 0 0 0
(23) Interrupt request register 1	003C <sub>16</sub>	00 <sub>16</sub>
(24) Interrupt control register 1	003E <sub>16</sub>	00 <sub>16</sub>
(25) Processor status register	(PS)	X X X X X 1 X X
(26) Program counter	(PCH)	Contents of address FFFD <sub>16</sub>
	(PCL)	Contents of address FFFC <sub>16</sub>

**Note X** : Undefined

Fig. 37 Internal status of microcomputer at reset

### Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between  $X_{IN}$  and  $X_{OUT}$ , and a CR oscillation circuit can be formed by connecting a resistor and a capacitor.

Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between  $X_{IN}$  and  $X_{OUT}$  since a feed-back resistor exists on-chip.

Set the constants of the resistor and capacitor when a CR oscillator is used, so that a frequency variation due to LSI variation and resistor and capacitor variations may not exceed the standard input frequency.

### ●Oscillation control

#### • Stop mode

When the STP instruction is executed, the internal clock  $f$  stops at an "H" level and the  $X_{IN}$  oscillator stops. At this time, timer 1 is set to "0116" and prescaler 12 is set to "FF16" when the oscillation stabilization time set bit after release of the STP instruction is "0". On the other hand, timer 1 and prescaler 12 are not set when the above bit is "1". Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used.  $f(X_{IN})/16$  is forcibly connected to the input of prescaler 12. When an external interrupt is accepted, oscillation is restarted but the internal clock  $f$  remains at "H" until timer 1 underflows. As soon as timer 1 underflows, the internal clock  $f$  is supplied. This is because when a ceramic oscillator is used, some time is required until a start of oscillation. In case oscillation is restarted by reset, no wait time is generated. So apply an "L" level to the RESET pin while oscillation becomes stable.

#### • Wait mode

If the WIT instruction is executed, the internal clock  $f$  stops at an "H" level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

When the STP status is released, prescaler 12 and timer 1 will start counting clock which is  $X_{IN}$  divided by 16, so set the timer 1 interrupt enable bit to "0" before the STP instruction is executed.

#### Note

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 12 after fully appreciating the oscillation stabilization time of the oscillator to be used.

### ●Switch of ceramic and CR oscillations

After releasing reset the operation starts by starting a built-in ring oscillator. Then, a ceramic oscillation or a CR oscillation is selected by setting bit 5 of the CPU mode register.

The bit 5 can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit.

### ●Double-speed mode

When a ceramic oscillation is selected, a double-speed mode can be used. Do not use it when a CR oscillation is selected.

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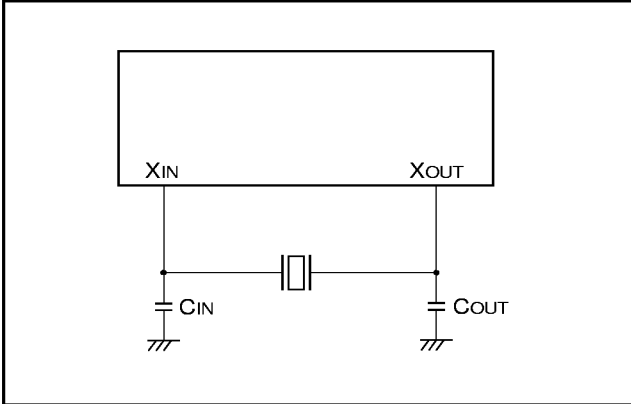


Fig. 38 External circuit of ceramic resonator

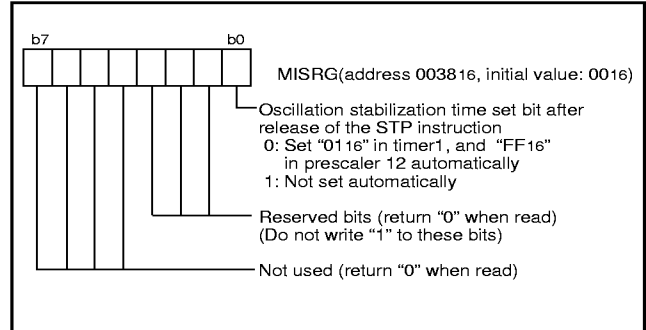


Fig. 41 Structure of MISRG

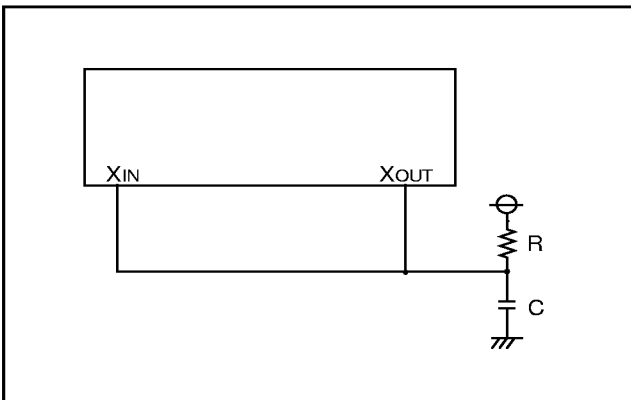


Fig. 39 External circuit of CR oscillation

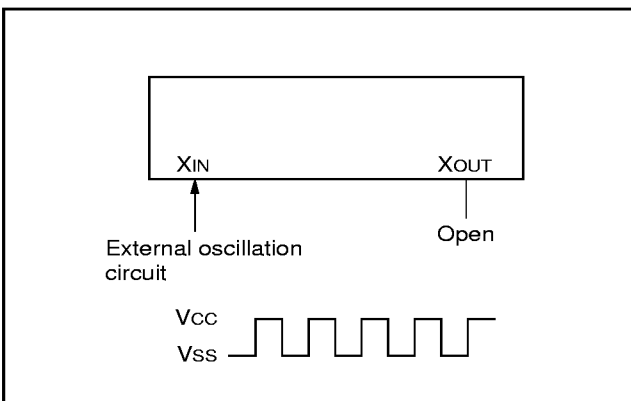


Fig. 40 External clock input circuit

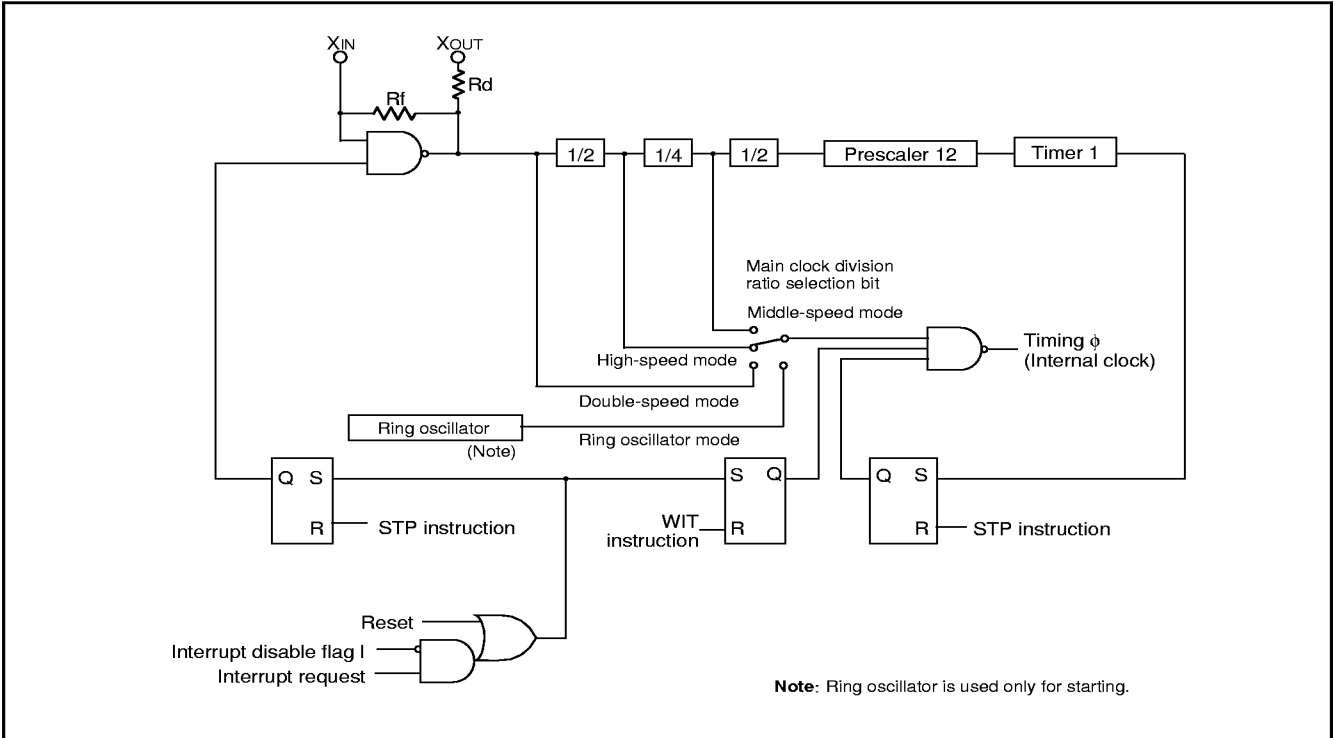


Fig. 42 Block diagram of internal clock generating circuit (for ceramic resonator)

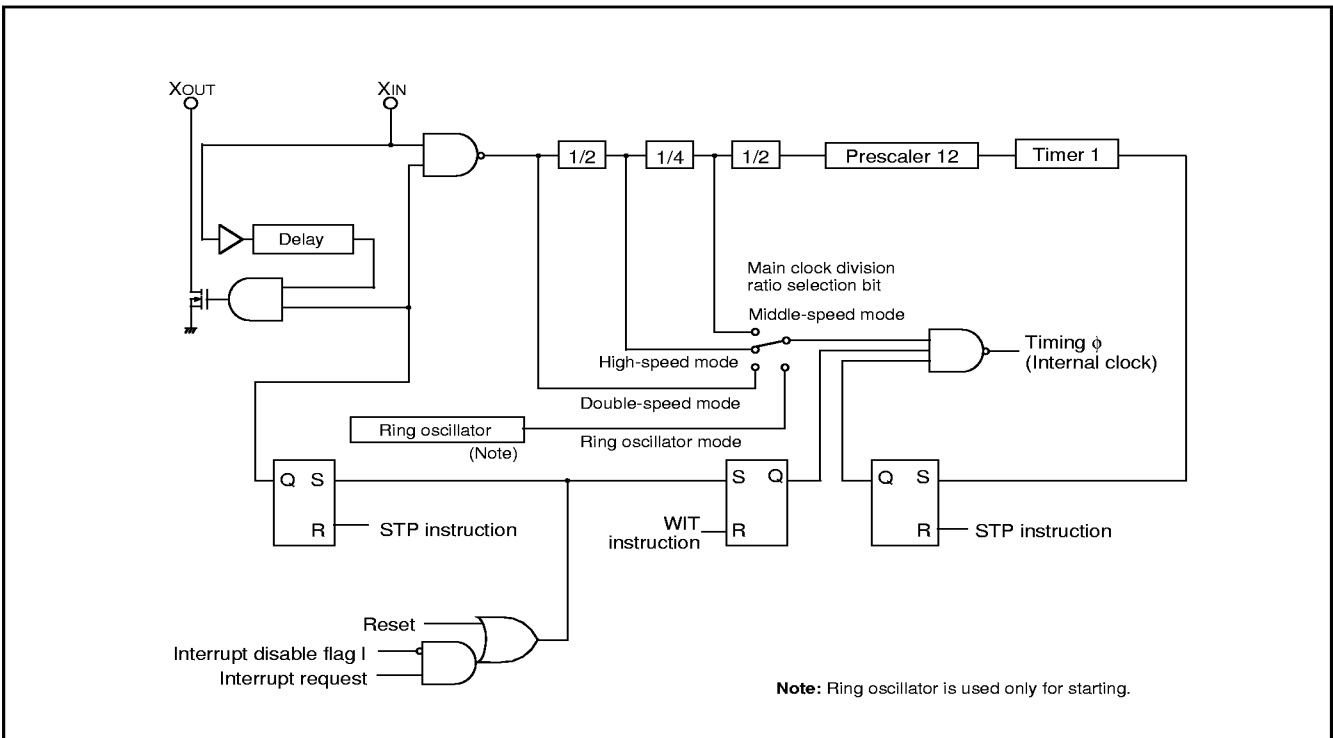


Fig. 43 Block diagram of internal clock generating circuit (for CR oscillation)



## NOTES ON PROGRAMMING

### Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is "1". After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations.

### Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

### Decimal Calculations

- For calculations in decimal notation, set the decimal mode flag D to "1", then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.
- In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

### Timers

- When n (0 to 255) is written to a timer latch, the frequency division ratio is  $1/(n+1)$ .
- When a count source of timer X is switched, stop a count of timer X.

### Ports

- The values of the port direction registers cannot be read. That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS. It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR. For setting direction registers, use the LDM instruction, STA instruction, etc.
- Set "1" to each bit 6 of the port P3 direction register and the port P3 register.

### A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low. Make sure that  $f(X_{IN})$  is 500kHz or more during A-D conversion. Do not execute the STP instruction during A-D conversion.

### Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock  $\phi$  by the number of cycles mentioned in the machine-language instruction table.

The frequency of the internal clock  $\phi$  is the same as that of the  $X_{IN}$  in double-speed mode, twice the  $X_{IN}$  cycle in high-speed mode and 8 times the  $X_{IN}$  cycle in middle-speed mode.

### CPU Mode Register

The oscillation mode selection bit can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit.

When a ceramic oscillation is selected, a double-speed mode of the clock division ratio selection bits can be used. Do not use it when a CR oscillation is selected.

## NOTES ON USE

### Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin ( $V_{CC}$  pin) and GND pin ( $V_{SS}$  pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01  $\mu$ F to 0.1  $\mu$ F is recommended.

### One Time PROM Version

The  $CNV_{SS}$  pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin ( $V_{PP}$  pin) as well.

To improve the noise reduction, connect a track between  $CNV_{SS}$  pin and  $V_{SS}$  pin with 1 to 10 k $\Omega$  resistance.

The mask ROM version track of  $CNV_{SS}$  pin has no operational interference even if it is connected via a resistor.

**DATA REQUIRED FOR MASK ORDERS**

The following are necessary when ordering a mask ROM production:

- (1) Mask ROM Order Confirmation Form
- (2) Mark Specification Form
- (3) Data to be written to ROM, in EPROM form  
(three identical copies)

**DATA REQUIRED FOR ROM PROGRAMMING ORDERS**

The following are necessary when ordering a ROM writing:

- (1) ROM Programming Confirmation Form
- (2) Mark Specification Form (for Special Mark)
- (3) Data to be written to ROM, in EPROM form  
(three identical copies)

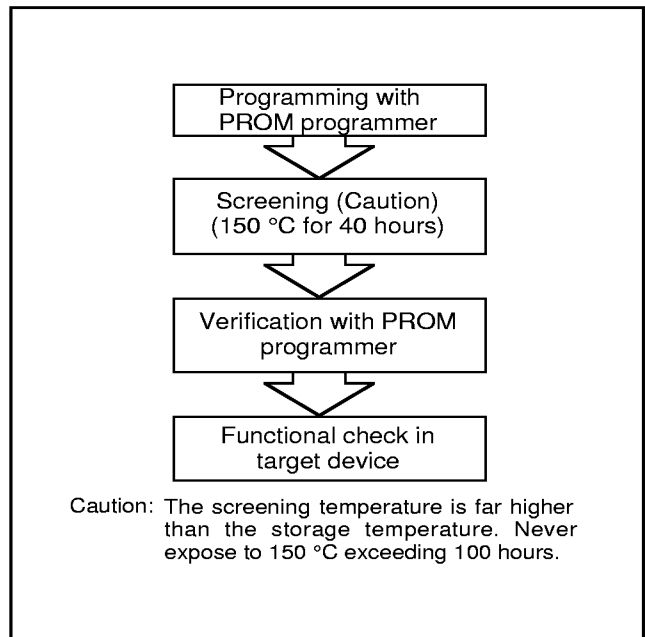
**ROM PROGRAMMING METHOD**

The built-in PROM of the blank One Time PROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

**Table 5 Special programming adapter**

Package	Name of Programming Adapter
32P4B	PCA7435SP
32P6B-A	PCA7435GP
36P2R-A	PCA7435FP

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 44 is recommended to verify programming.



**Fig. 44 Programming and testing of One Time PROM version**

## ELECTRICAL CHARACTERISTICS

### 1.7531Group (General purpose)

Applied to: M37531M4-XXXFP/SP/GP, M37531M8-XXXFP/SP/GP, M37531E4FP/SP/GP, M37531E8FP/SP

### Absolute Maximum Ratings (General purpose)

Table 6 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Power source voltage	All voltages are based on V <sub>SS</sub> . Output transistors are cut off.	-0.3 to 7.0	V
V <sub>I</sub>	Input voltage P00-P07, P10-P14, P20-P27, P30-P37, VREF		-0.3 to V <sub>CC</sub> + 0.3	V
V <sub>I</sub>	Input voltage RESET, XIN		-0.3 to V <sub>CC</sub> + 0.3	V
V <sub>I</sub>	Input voltage CNVSS (Note 1)		-0.3 to 13	V
V <sub>O</sub>	Output voltage P00-P07, P10-P14, P20-P27, P30-P37, XOUT		-0.3 to V <sub>CC</sub> + 0.3	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25°C	300 (Note 2)	mW
T <sub>opr</sub>	Operating temperature		-20 to 85	°C
T <sub>stg</sub>	Storage temperature		-40 to 125	°C

**Note 1:** It is a rating only for the One Time PROM version. Connect to V<sub>SS</sub> for the mask ROM version.

**2:** 200 mW for the 32P6B package product.

Recommended Operating Conditions (General purpose)

Table 7 Recommended operating conditions (1) ( $V_{CC} = 2.2$  to  $5.5$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V <sub>CC</sub>	Power source voltage (ceramic)	f(X <sub>IN</sub> ) = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X <sub>IN</sub> ) = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X <sub>IN</sub> ) = 2 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
		f(X <sub>IN</sub> ) = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		f(X <sub>IN</sub> ) = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
		f(X <sub>IN</sub> ) = 1 MHz (Double-speed mode)	2.2	5.0	5.5	V
	Power source voltage (CR)	f(X <sub>IN</sub> ) = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X <sub>IN</sub> ) = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
V <sub>SS</sub>	Power source voltage			0		V
V <sub>REF</sub>	Analog reference voltage		2.0		V <sub>CC</sub>	V
V <sub>IH</sub>	"H" input voltage	P00–P07, P10–P14, P20–P27, P30–P37	0.8V <sub>CC</sub>		V <sub>CC</sub>	V
V <sub>IH</sub>	"H" input voltage (TTL input level selected)	P10, P12, P13, P36, P37 (Note 1)	2.0		V <sub>CC</sub>	V
V <sub>IH</sub>	"H" input voltage	RESET, X <sub>IN</sub>	0.8V <sub>CC</sub>		V <sub>CC</sub>	V
V <sub>IL</sub>	"L" input voltage	P00–P07, P10–P14, P20–P27, P30–P37	0		0.3V <sub>CC</sub>	V
V <sub>IL</sub>	"L" input voltage (TTL input level selected)	P10, P12, P13, P36, P37 (Note 1)	0		0.8	V
V <sub>IL</sub>	"L" input voltage	RESET, CNV <sub>SS</sub>	0		0.2V <sub>CC</sub>	V
V <sub>IL</sub>	"L" input voltage	X <sub>IN</sub>	0		0.16V <sub>CC</sub>	V
ΣI <sub>OH(peak)</sub>	"H" total peak output current (Note 2)	P00–P07, P10–P14, P20–P27, P30–P37			–80	mA
ΣI <sub>OL(peak)</sub>	"L" total peak output current (Note 2)	P00–P07, P10–P14, P20–P27, P37			80	mA
ΣI <sub>OL(peak)</sub>	"L" total peak output current (Note 2)	P30–P36			60	mA
ΣI <sub>OH(avg)</sub>	"H" total average output current (Note 2)	P00–P07, P10–P14, P20–P27, P30–P37			–40	mA
ΣI <sub>OL(avg)</sub>	"L" total average output current (Note 2)	P00–P07, P10–P14, P20–P27, P37			40	mA
ΣI <sub>OL(avg)</sub>	"L" total average output current (Note 2)	P30–P36			30	mA

Note 1: V<sub>CC</sub> = 4.0 to 5.5V

2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Recommended Operating Conditions (General purpose)(continued)

Table 8 Recommended operating conditions (2) (V<sub>CC</sub> = 2.2 to 5.5 V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
I <sub>OH</sub> (peak)	"H" peak output current (Note 1)	P00-P07, P10-P14, P20-P27, P30-P37			-10	mA
I <sub>OL</sub> (peak)	"L" peak output current (Note 1)	P00-P07, P10-P14, P20-P27, P37			10	mA
I <sub>OL</sub> (peak)	"L" peak output current (Note 1)	P30-P36			30	mA
I <sub>OH</sub> (avg)	"H" average output current (Note 2)	P00-P07, P10-P14, P20-P27, P30-P37			-5	mA
I <sub>OL</sub> (avg)	"L" average output current (Note 2)	P00-P07, P10-P14, P20-P27, P37			5	mA
I <sub>OL</sub> (avg)	"L" average output current (Note 2)	P30-P36			15	mA
f(X <sub>IN</sub> )	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 4.0 to 5.5 V Double-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 2.4 to 5.5 V Double-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 2.2 to 5.5 V Double-speed mode			1	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 2.2 to 5.5 V High-, Middle-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at CR oscillation	V <sub>CC</sub> = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at CR oscillation	V <sub>CC</sub> = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at CR oscillation	V <sub>CC</sub> = 2.2 to 5.5 V High-, Middle-speed mode			1	MHz

- Notes 1:** The peak output current is the peak current flowing in each port.  
**2:** The average output current I<sub>OL</sub> (avg), I<sub>OH</sub> (avg) in an average value measured over 100 ms.  
**3:** When the oscillation frequency has a duty cycle of 50 %.

Electrical Characteristics (General purpose)

Table 9 Electrical characteristics (VCC = 2.2 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
VOH	"H" output voltage P00-P07, P10-P14, P20-P27, P30-P37 (Note 1)		IOH = -5 mA VCC = 4.0 to 5.5 V	VCC-1.5			V
			IOH = -1.0 mA VCC = 2.2 to 5.5 V	VCC-1.0			V
VOL	"L" output voltage P00-P07, P10-P14, P20-P27, P37		IOL = 5 mA VCC = 4.0 to 5.5 V			1.5	V
			IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
			IOL = 1.0 mA VCC = 2.2 to 5.5 V			1.0	V
VOL	"L" output voltage P30-P36		IOL = 15 mA VCC = 4.0 to 5.5 V			2.0	V
			IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
			IOL = 10 mA VCC = 2.2 to 5.5 V			1.0	V
VT+~VT-	Hysteresis	CNTR0, INT0, INT1 (Note 2) P00-P07 (Note 3)		0.4			V
VT+~VT-	Hysteresis	RxD, SCLK, SData (Note 2)		0.5			V
VT+~VT-	Hysteresis	RESET		0.5			V
IiH	"H" input current	P00-P07, P10-P14, P20-P27, P30-P37	Vi = VCC (Pin floating. Pull up transistors "off")			5.0	μA
IiH	"H" input current	RESET	Vi = VCC			5.0	μA
IiH	"H" input current	XIN	Vi = VCC	4.0			μA
IiL	"L" input current	P00-P07, P10-P14, P20-P27, P30-P37	Vi = VSS (Pin floating. Pull up transistors "off")			-5.0	μA
IiL	"L" input current	RESET, CNVSS	Vi = VSS			-5.0	μA
IiL	"L" input current	XIN	Vi = VSS	-4.0			μA
IiL	"L" input current	P00-P07, P30-P37	Vi = VSS (Pull up transistors "on")	-0.2	-0.5		mA
VRAM	RAM hold voltage		When clock stopped	2.0		5.5	V
ICC	Power source current		High-speed mode, f(XIN) = 8 MHz Output transistors "off"		5.0	8.0	mA
			High-speed mode, f(XIN) = 2 MHz, VCC = 2.2 V Output transistors "off"		0.5	1.5	mA
			Double-speed mode, f(XIN) = 4 MHz Output transistors "off"		5.0	8.0	mA
			Middle-speed mode, f(XIN) = 8 MHz Output transistors "off"		2.0	5.0	mA
			f(XIN) = 8 MHz (in WIT state) Output transistors "off"		1.6	3.2	mA
			f(XIN) = 2 MHz, VCC = 2.2 V (in WIT state) Output transistors "off"		0.2		mA
			Increment when A-D conversion is executed f(XIN) = 8 MHz, VCC = 5 V		0.5		mA
			All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C	0.1	1.0	μA
	Ta = 85 °C		10	μA			

Notes 1: P11 is measured when the P11/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".  
2: RxD, SCLK, SData, INT0, and INT1 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).  
3: It is available only when operating key-on wake up.

**A-D Converter Characteristics (General purpose)**

**Table 10 A-D Converter characteristics (1) ( $V_{CC} = 2.7$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)**

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy (excluding quantization error)	$V_{CC} = 2.7$ to $5.5$ V $T_a = 25$ °C			$\pm 3$	LSB
—	Differential nonlinear error	$V_{CC} = 2.7$ to $5.5$ V $T_a = 25$ °C			$\pm 0.9$	LSB
VOT	Zero transition voltage	$V_{CC} = V_{REF} = 5.12$ V	0	5	20	mV
		$V_{CC} = V_{REF} = 3.072$ V	0	3	15	mV
VFST	Full scale transition voltage	$V_{CC} = V_{REF} = 5.12$ V	5105	5115	5125	mV
		$V_{CC} = V_{REF} = 3.072$ V	3060	3069	3075	mV
tCONV	Conversion time				122	tc(XIN)
RLADDER	Ladder resistor			55		k $\Omega$
IVREF	Reference power source input current	$V_{REF} = 5.0$ V	50	150	200	$\mu$ A
		$V_{REF} = 3.0$ V	30	70	120	
I <sub>I(AD)</sub>	A-D port input current				5.0	$\mu$ A

Timing Requirements (General purpose)

Table 11 Timing requirements (1) ( $V_{CC} = 4.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\text{RESET})$	Reset input "L" pulse width	2			$\mu\text{s}$
$t_c(\text{XIN})$	External clock input cycle time	125			ns
$t_{WH}(\text{XIN})$	External clock input "H" pulse width	50			ns
$t_{WL}(\text{XIN})$	External clock input "L" pulse width	50			ns
$t_c(\text{CNTR})$	CNTR0 input cycle time	200			ns
$t_{WH}(\text{CNTR})$	CNTR0, INT0, INT1, input "H" pulse width	80			ns
$t_{WL}(\text{CNTR})$	CNTR0, INT0, INT1, input "L" pulse width	80			ns
$t_c(\text{SCLK})$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH}(\text{SCLK})$	Serial I/O2 clock input "H" pulse width	400			ns
$t_{WL}(\text{SCLK})$	Serial I/O2 clock input "L" pulse width	400			ns
$t_{su}(\text{SCLK-SDATA})$	Serial I/O2 input set up time	200			ns
$t_h(\text{SCLK-SDATA})$	Serial I/O2 input hold time	200			ns

Table 12 Timing requirements (2) ( $V_{CC} = 2.2$  to  $5.5$  V or  $2.4$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\text{RESET})$	Reset input "L" pulse width	2			$\mu\text{s}$
$t_c(\text{XIN})$	External clock input cycle time	$V_{CC} = 2.2$ to $5.5$ V	500		ns
		$V_{CC} = 2.4$ to $5.5$ V	250		ns
$t_{WH}(\text{XIN})$	External clock input "H" pulse width	$V_{CC} = 2.2$ to $5.5$ V	200		ns
		$V_{CC} = 2.4$ to $5.5$ V	100		ns
$t_{WL}(\text{XIN})$	External clock input "L" pulse width	$V_{CC} = 2.2$ to $5.5$ V	200		ns
		$V_{CC} = 2.4$ to $5.5$ V	100		ns
$t_c(\text{CNTR})$	CNTR0 input cycle time	$V_{CC} = 2.2$ to $5.5$ V	1000		ns
		$V_{CC} = 2.4$ to $5.5$ V	500		ns
$t_{WH}(\text{CNTR})$	CNTR0, INT0, INT1, input "H" pulse width	$V_{CC} = 2.2$ to $5.5$ V	460		ns
		$V_{CC} = 2.4$ to $5.5$ V	230		ns
$t_{WL}(\text{CNTR})$	CNTR0, INT0, INT1, input "L" pulse width	$V_{CC} = 2.2$ to $5.5$ V	460		ns
		$V_{CC} = 2.4$ to $5.5$ V	230		ns
$t_c(\text{SCLK})$	Serial I/O2 clock input cycle time	$V_{CC} = 2.2$ to $5.5$ V	4000		ns
		$V_{CC} = 2.4$ to $5.5$ V	2000		ns
$t_{WH}(\text{SCLK})$	Serial I/O2 clock input "H" pulse width	$V_{CC} = 2.2$ to $5.5$ V	1900		ns
		$V_{CC} = 2.4$ to $5.5$ V	950		ns
$t_{WL}(\text{SCLK})$	Serial I/O2 clock input "L" pulse width	$V_{CC} = 2.2$ to $5.5$ V	1900		ns
		$V_{CC} = 2.4$ to $5.5$ V	950		ns
$t_{su}(\text{SCLK-SDATA})$	Serial I/O2 input set up time	400			ns
$t_h(\text{SCLK-SDATA})$	Serial I/O2 input hold time	400			ns



### Switching Characteristics (General purpose)

**Table 13 Switching characteristics (1) ( $V_{CC} = 4.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)**

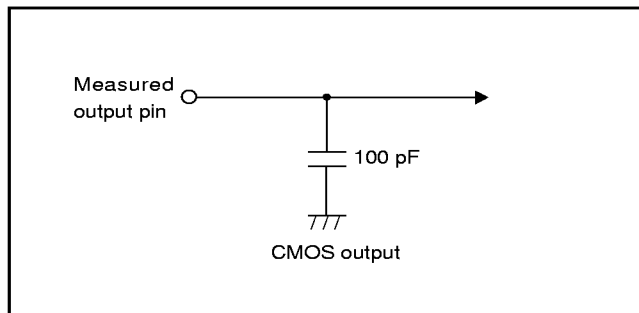
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>WH</sub> (SCLK)	Serial I/O2 clock output "H" pulse width	t <sub>c</sub> (SCLK)/2-30			ns
t <sub>WL</sub> (SCLK)	Serial I/O2 clock output "L" pulse width	t <sub>c</sub> (SCLK)/2-30			ns
t <sub>d</sub> (SCLK-SDATA)	Serial I/O2 output delay time			140	ns
t <sub>v</sub> (SCLK-SDATA)	Serial I/O2 output valid time	0			ns
t <sub>r</sub> (SCLK)	Serial I/O2 clock output rising time			30	ns
t <sub>f</sub> (SCLK)	Serial I/O2 clock output falling time			30	ns
t <sub>r</sub> (CMOS)	CMOS output rising time (Note 1)		10	30	ns
t <sub>f</sub> (CMOS)	CMOS output falling time (Note 1)		10	30	ns

**Note 1:** Pin XOUT is excluded.

**Table 14 Switching characteristics (2) ( $V_{CC} = 2.2$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)**

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>WH</sub> (SCLK)	Serial I/O2 clock output "H" pulse width	t <sub>c</sub> (SCLK)/2-50			ns
t <sub>WL</sub> (SCLK)	Serial I/O2 clock output "L" pulse width	t <sub>c</sub> (SCLK)/2-50			ns
t <sub>d</sub> (SCLK-SDATA)	Serial I/O2 output delay time			350	ns
t <sub>v</sub> (SCLK-SDATA)	Serial I/O2 output valid time	0			ns
t <sub>r</sub> (SCLK)	Serial I/O2 clock output rising time			50	ns
t <sub>f</sub> (SCLK)	Serial I/O2 clock output falling time			50	ns
t <sub>r</sub> (CMOS)	CMOS output rising time (Note 1)		20	50	ns
t <sub>f</sub> (CMOS)	CMOS output falling time (Note 1)		20	50	ns

**Note 1:** Pin XOUT is excluded.



**Fig. 45 Switching characteristics measurement circuit diagram (General purpose)**

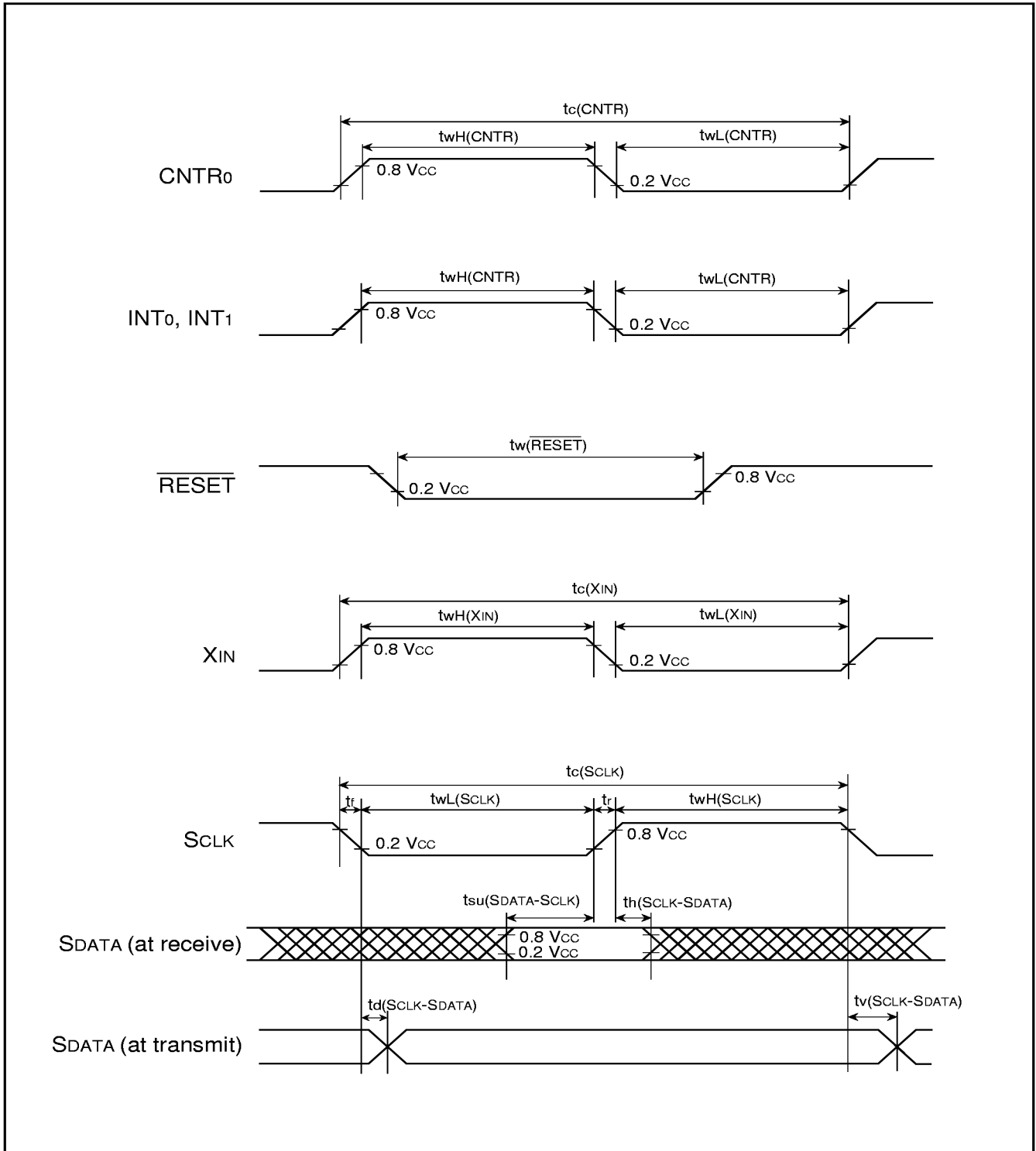


Fig. 46 Timing chart (General purpose)

**2.7531 Group (Extended operating temperature version)**

Applied to: M37531M4T-XXXGP, M37531E4T-XXXGP

**Absolute Maximum Ratings (Extended operating temperature version)**

**Table 15 Absolute maximum ratings**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Power source voltage	All voltages are based on V <sub>SS</sub> . Output transistors are cut off.	-0.3 to 7.0	V
V <sub>I</sub>	Input voltage P00-P07, P10-P14, P20-P25, P30-P34, P37, VREF		-0.3 to V <sub>CC</sub> + 0.3	V
V <sub>I</sub>	Input voltage RESET, X <sub>IN</sub>		-0.3 to V <sub>CC</sub> + 0.3	V
V <sub>I</sub>	Input voltage CNV <sub>SS</sub> (Note 1)		-0.3 to 13	V
V <sub>O</sub>	Output voltage P00-P07, P10-P14, P20-P25, P30-P34, P37, X <sub>OUT</sub>		-0.3 to V <sub>CC</sub> + 0.3	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25 °C	200	mW
T <sub>opr</sub>	Operating temperature		-40 to 85	°C
T <sub>stg</sub>	Storage temperature		-65 to 150	°C

**Note 1:** It is a rating only for the One Time PROM version. Connect to V<sub>SS</sub> for the mask ROM version.

**Recommended Operating Conditions (Extended operating temperature version)**

**Table 16 Recommended operating conditions (1) ( $V_{CC} = 2.4$  to  $5.5$  V,  $T_a = -40$  to  $85$  °C, unless otherwise noted)**

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V <sub>CC</sub>	Power source voltage (ceramic)	f(X <sub>IN</sub> ) = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X <sub>IN</sub> ) = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X <sub>IN</sub> ) = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		f(X <sub>IN</sub> ) = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
	Power source voltage (CR)	f(X <sub>IN</sub> ) = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X <sub>IN</sub> ) = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
V <sub>SS</sub>	Power source voltage			0		V
V <sub>REF</sub>	Analog reference voltage		2.0		V <sub>CC</sub>	V
V <sub>IH</sub>	"H" input voltage	P00–P07, P10–P14, P20–P25, P30–P34, P37	0.8V <sub>CC</sub>		V <sub>CC</sub>	V
V <sub>IH</sub>	"H" input voltage (TTL input level selected)	P10, P12, P13, P37 (Note 1)	2.0		V <sub>CC</sub>	V
V <sub>IH</sub>	"H" input voltage	RESET, X <sub>IN</sub>	0.8V <sub>CC</sub>		V <sub>CC</sub>	V
V <sub>IL</sub>	"L" input voltage	P00–P07, P10–P14, P20–P25, P30–P34, P37	0		0.3V <sub>CC</sub>	V
V <sub>IL</sub>	"L" input voltage (TTL input level selected)	P10, P12, P13, P37 (Note 1)	0		0.8	V
V <sub>IL</sub>	"L" input voltage	RESET, CNV <sub>SS</sub>	0		0.2V <sub>CC</sub>	V
V <sub>IL</sub>	"L" input voltage	X <sub>IN</sub>	0		0.16V <sub>CC</sub>	V
ΣI <sub>OH(peak)</sub>	"H" total peak output current (Note 2)	P00–P07, P10–P14, P20–P25, P30–P34, P37			–80	mA
ΣI <sub>OL(peak)</sub>	"L" total peak output current (Note 2)	P00–P07, P10–P14, P20–P25, P37			80	mA
ΣI <sub>OL(peak)</sub>	"L" total peak output current (Note 2)	P30–P34			60	mA
ΣI <sub>OH(avg)</sub>	"H" total average output current (Note 2)	P00–P07, P10–P14, P20–P25, P30–P34, P37			–40	mA
ΣI <sub>OL(avg)</sub>	"L" total average output current (Note 2)	P00–P07, P10–P14, P20–P25, P37			40	mA
ΣI <sub>OL(avg)</sub>	"L" total average output current (Note 2)	P30–P34			30	mA

**Note 1:** V<sub>CC</sub> = 4.0 to 5.5V

**2:** The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

**MITSUBISHI MICROCOMPUTERS**  
**7531 Group**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

**Recommended Operating Conditions (Extended operating temperature version) (continued)**

**Table 17 Recommended operating conditions (2) (V<sub>CC</sub> = 2.4 to 5.5 V, T<sub>a</sub> = -40 to 85 °C, unless otherwise noted)**

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
I <sub>OH</sub> (peak)	"H" peak output current (Note 1)	P00-P07, P10-P14, P20-P25, P30-P34, P37			-10	mA
I <sub>OL</sub> (peak)	"L" peak output current (Note 1)	P00-P07, P10-P14, P20-P25, P37			10	mA
I <sub>OL</sub> (peak)	"L" peak output current (Note 1)	P30-P34			30	mA
I <sub>OH</sub> (avg)	"H" average output current (Note 2)	P00-P07, P10-P14, P20-P25, P30-P34, P37			-5	mA
I <sub>OL</sub> (avg)	"L" average output current (Note 2)	P00-P07, P10-P14, P20-P25, P37			5	mA
I <sub>OL</sub> (avg)	"L" average output current (Note 2)	P30-P34			15	mA
f(XIN)	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 4.0 to 5.5 V Double-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 2.4 to 5.5 V Double-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at CR oscillation	V <sub>CC</sub> = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at CR oscillation	V <sub>CC</sub> = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz

**Notes 1:** The peak output current is the peak current flowing in each port.

**2:** The average output current I<sub>OL</sub> (avg), I<sub>OH</sub> (avg) in an average value measured over 100 ms.

**3:** When the oscillation frequency has a duty cycle of 50 %.

Electrical Characteristics (Extended operating temperature version)

Table 18 Electrical characteristics (VCC = 2.4 to 5.5 V, VSS = 0 V, Ta = -40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	"H" output voltage P00-P07, P10-P14, P20-P25, P30-P34 (Note 1)	IOH = -5 mA VCC = 4.0 to 5.5 V	VCC-1.5			V
		IOH = -1.0 mA VCC = 2.4 to 5.5 V	VCC-1.0			V
VOL	"L" output voltage P00-P07, P10-P14, P20-P25, P37	IOL = 5 mA VCC = 4.0 to 5.5 V			1.5	V
		IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
		IOL = 1.0 mA VCC = 2.4 to 5.5 V			1.0	V
VOL	"L" output voltage P30-P34	IOL = 15 mA VCC = 4.0 to 5.5 V			2.0	V
		IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
		IOL = 10 mA VCC = 2.4 to 5.5 V			1.0	V
VT+~VT-	Hysteresis CNTR0, INT0 (Note 2) P00-P07 (Note 3)			0.4		V
VT+~VT-	Hysteresis RXD, SCLK, SDATA (Note 2)			0.5		V
VT+~VT-	Hysteresis RESET			0.5		V
IiH	"H" input current P00-P07, P10-P14, P20-P25, P30-P34, P37	Vi = VCC (Pin floating. Pull up transistors "off")			5.0	µA
IiH	"H" input current RESET	Vi = VCC			5.0	µA
IiH	"H" input current XIN	Vi = VCC		4.0		µA
IiL	"L" input current P00-P07, P10-P14, P20-P25, P30-P34, P37	Vi = VSS (Pin floating. Pull up transistors "off")			-5.0	µA
IiL	"L" input current RESET, CNVSS	Vi = VSS			-5.0	µA
IiL	"L" input current XIN	Vi = VSS		-4.0		µA
IiL	"L" input current P00-P07, P30-P34, P37	Vi = VSS (Pull up transistors "on")		-0.2	-0.5	mA
VRAM	RAM hold voltage	When clock stopped	2.0		5.5	V
ICC	Power source current	High-speed mode, f(XIN) = 8 MHz Output transistors "off"		5.0	8.0	mA
		High-speed mode, f(XIN) = 2 MHz, VCC = 2.4 V Output transistors "off"		0.5	1.5	mA
		Double-speed mode, f(XIN) = 4 MHz Output transistors "off"		5.0	8.0	mA
		Middle-speed mode, f(XIN) = 8 MHz, Output transistors "off"		2.0	5.0	mA
		f(XIN) = 8 MHz (in WIT state) Functions except Timer 1 and Timer 2 stop Output transistors "off"		1.6	3.2	mA
		f(XIN) = 2 MHz, VCC = 2.4 V (in WIT state) Output transistors "off"		0.2		mA
		Increment when A-D conversion is executed f(XIN) = 8 MHz, VCC = 5 V		0.5		mA
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C		0.1	1.0
	Ta = 85 °C			10	µA	

Notes 1: P11 is measured when the P11/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".  
2: RXD, SCLK, SDATA, and INT0 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).  
3: It is available only when operating key-on wake up.

**A-D Converter Characteristics (Extended operating temperature version)**

**Table 19 A-D Converter characteristics (1) ( $V_{CC} = 2.7$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -40$  to  $85$  °C, unless otherwise noted)**

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy (excluding quantization error)	$V_{CC} = 2.7$ to $5.5$ V $T_a = 25$ °C			±3	LSB
—	Differential nonlinear error	$V_{CC} = 2.7$ to $5.5$ V $T_a = 25$ °C			±0.9	LSB
VOT	Zero transition voltage	$V_{CC} = V_{REF} = 5.12$ V	0	5	20	mV
		$V_{CC} = V_{REF} = 3.072$ V	0	3	15	mV
VFST	Full scale transition voltage	$V_{CC} = V_{REF} = 5.12$ V	5105	5115	5125	mV
		$V_{CC} = V_{REF} = 3.072$ V	3060	3069	3075	mV
tCONV	Conversion time				122	tc(XIN)
RLADDER	Ladder resistor			55		kΩ
IVREF	Reference power source input current	$V_{REF} = 5.0$ V	50	150	200	μA
		$V_{REF} = 3.0$ V	30	70	120	
I <sub>I(AD)</sub>	A-D port input current				5.0	μA

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**Timing Requirements (Extended operating temperature version)**

**Table 20 Timing requirements (1) ( $V_{CC} = 4.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -40$  to  $85$  °C, unless otherwise noted)**

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width	2			μs
tc(XIN)	External clock input cycle time	125			ns
tWH(XIN)	External clock input "H" pulse width	50			ns
tWL(XIN)	External clock input "L" pulse width	50			ns
tc(CNTR)	CNTR0 input cycle time	200			ns
tWH(CNTR)	CNTR0, INT0 input "H" pulse width	80			ns
tWL(CNTR)	CNTR0, INT0 input "L" pulse width	80			ns
tc(SCLK)	Serial I/O2 clock input cycle time	1000			ns
tWH(SCLK)	Serial I/O2 clock input "H" pulse width	400			ns
tWL(SCLK)	Serial I/O2 clock input "L" pulse width	400			ns
tsu(SCLK-SDATA)	Serial I/O2 input set up time	200			ns
th(SCLK-SDATA)	Serial I/O2 input hold time	200			ns

**Table 21 Timing requirements (2) ( $V_{CC} = 2.4$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -40$  to  $85$  °C, unless otherwise noted)**

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width	2			μs
tc(XIN)	External clock input cycle time	250			ns
tWH(XIN)	External clock input "H" pulse width	100			ns
tWL(XIN)	External clock input "L" pulse width	100			ns
tc(CNTR)	CNTR0 input cycle time	500			ns
tWH(CNTR)	CNTR0, INT0 input "H" pulse width	230			ns
tWL(CNTR)	CNTR0, INT0 input "L" pulse width	230			ns
tc(SCLK)	Serial I/O2 clock input cycle time	2000			ns
tWH(SCLK)	Serial I/O2 clock input "H" pulse width	950			ns
tWL(SCLK)	Serial I/O2 clock input "L" pulse width	950			ns
tsu(SCLK-SDATA)	Serial I/O2 input set up time	400			ns
th(SCLK-SDATA)	Serial I/O2 input hold time	400			ns



Switching Characteristics (Extended operating temperature version)

Table 22 Switching characteristics (1) ( $V_{CC} = 4.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -40$  to  $85$  °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>WH</sub> (SCLK)	Serial I/O2 clock output "H" pulse width	t <sub>c</sub> (SCLK)/2-30			ns
t <sub>WL</sub> (SCLK)	Serial I/O2 clock output "L" pulse width	t <sub>c</sub> (SCLK)/2-30			ns
t <sub>d</sub> (SCLK-SDATA)	Serial I/O2 output delay time			140	ns
t <sub>v</sub> (SCLK-SDATA)	Serial I/O2 output valid time	0			ns
t <sub>r</sub> (SCLK)	Serial I/O2 clock output rising time			30	ns
t <sub>f</sub> (SCLK)	Serial I/O2 clock output falling time			30	ns
t <sub>r</sub> (CMOS)	CMOS output rising time (Note 1)		10	30	ns
t <sub>f</sub> (CMOS)	CMOS output falling time (Note 1)		10	30	ns

Note 1: Pin XOUT is excluded.

Table 23 Switching characteristics (2) ( $V_{CC} = 2.4$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -40$  to  $85$  °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>WH</sub> (SCLK)	Serial I/O2 clock output "H" pulse width	t <sub>c</sub> (SCLK)/2-50			ns
t <sub>WL</sub> (SCLK)	Serial I/O2 clock output "L" pulse width	t <sub>c</sub> (SCLK)/2-50			ns
t <sub>d</sub> (SCLK-SDATA)	Serial I/O2 output delay time			350	ns
t <sub>v</sub> (SCLK-SDATA)	Serial I/O2 output valid time	0			ns
t <sub>r</sub> (SCLK)	Serial I/O2 clock output rising time			50	ns
t <sub>f</sub> (SCLK)	Serial I/O2 clock output falling time			50	ns
t <sub>r</sub> (CMOS)	CMOS output rising time (Note 1)		20	50	ns
t <sub>f</sub> (CMOS)	CMOS output falling time (Note 1)		20	50	ns

Note 1: Pin XOUT is excluded.

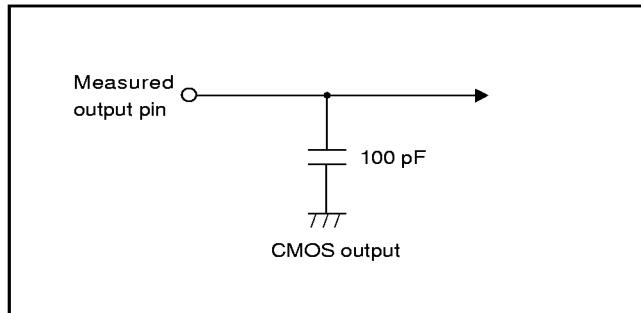


Fig. 47 Switching characteristics measurement circuit diagram (Extended operating temperature version)

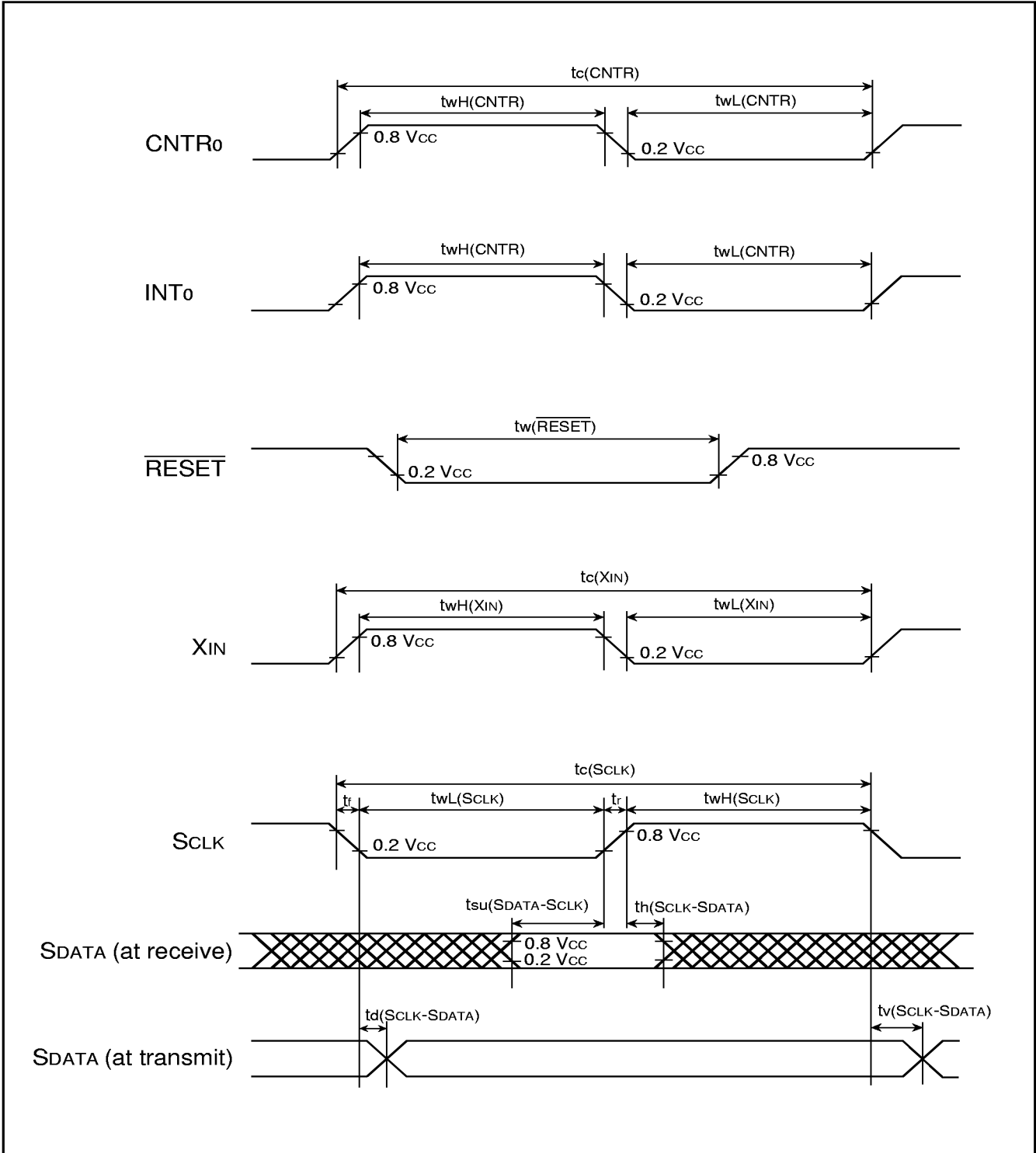


Fig. 48 Timing chart (Extended operating temperature version)

**3.7531 Group (Extended operating temperature 125 °C version)**

Applied to: M37531M4V-XXXGP, M37531E4V-XXXGP

**Absolute Maximum Ratings (Extended operating temperature 125 °C version)**

**Table 24 Absolute maximum ratings**

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Power source voltage	All voltages are based on VSS. Output transistors are cut off.	-0.3 to 7.0	V
Vi	Input voltage P00-P07, P10-P14, P20-P25, P30-P34, P37, VREF		-0.3 to VCC + 0.3	V
Vi	Input voltage RESET, XIN		-0.3 to VCC + 0.3	V
Vi	Input voltage CNVSS (Note 1)		-0.3 to 13	V
Vo	Output voltage P00-P07, P10-P14, P20-P25, P30-P34, P37, XOUT		-0.3 to VCC + 0.3	V
Pd	Power dissipation	Ta = 25 °C	200	mW
Topr	Operating temperature (Note 2)		-40 to 125	°C
Tstg	Storage temperature		-65 to 150	°C

**Notes 1:** It is a rating only for the One Time PROM version. Connect to VSS for the mask ROM version.

**2:** The total time is limited as follows:  
6000 hours at 55 to 85 °C, 1000 hours at 85 to 125 °C

**Recommended Operating Conditions (Extended operating temperature 125 °C version)**

**Table 25 Recommended operating conditions (1) (V<sub>CC</sub> = 2.4 to 5.5 V, T<sub>a</sub> = -40 to 125 °C, unless otherwise noted)**

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V <sub>CC</sub>	Power source voltage (ceramic)	f(X <sub>IN</sub> ) = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X <sub>IN</sub> ) = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X <sub>IN</sub> ) = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		f(X <sub>IN</sub> ) = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
	Power source voltage (CR)	f(X <sub>IN</sub> ) = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X <sub>IN</sub> ) = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
V <sub>SS</sub>	Power source voltage			0		V
V <sub>REF</sub>	Analog reference voltage		2.0		V <sub>CC</sub>	V
V <sub>IH</sub>	"H" input voltage	P00-P07, P10-P14, P20-P25, P30-P34, P37	0.8V <sub>CC</sub>		V <sub>CC</sub>	V
V <sub>IH</sub>	"H" input voltage (TTL input level selected)	P10, P12, P13, P37 (Note 1)	2.0		V <sub>CC</sub>	V
V <sub>IH</sub>	"H" input voltage	RESET, X <sub>IN</sub>	0.8V <sub>CC</sub>		V <sub>CC</sub>	V
V <sub>IL</sub>	"L" input voltage	P00-P07, P10-P14, P20-P25, P30-P34, P37	0		0.3V <sub>CC</sub>	V
V <sub>IL</sub>	"L" input voltage (TTL input level selected)	P10, P12, P13, P37 (Note 1)	0		0.8	V
V <sub>IL</sub>	"L" input voltage	RESET, CNV <sub>SS</sub>	0		0.2V <sub>CC</sub>	V
V <sub>IL</sub>	"L" input voltage	X <sub>IN</sub>	0		0.16V <sub>CC</sub>	V
ΣI <sub>OH(peak)</sub>	"H" total peak output current (Note 2)	P00-P07, P10-P14, P20-P25, P30-P34, P37			-80	mA
ΣI <sub>OL(peak)</sub>	"L" total peak output current (Note 2)	P00-P07, P10-P14, P20-P25, P37			80	mA
ΣI <sub>OL(peak)</sub>	"L" total peak output current (Note 2)	P30-P34			60	mA
ΣI <sub>OH(avg)</sub>	"H" total average output current (Note 2)	P00-P07, P10-P14, P20-P25, P30-P34, P37			-40	mA
ΣI <sub>OL(avg)</sub>	"L" total average output current (Note 2)	P00-P07, P10-P14, P20-P25, P37			40	mA
ΣI <sub>OL(avg)</sub>	"L" total average output current (Note 2)	P30-P34			30	mA

**Note 1:** V<sub>CC</sub> = 4.0 to 5.5V

**2:** The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

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**Recommended Operating Conditions (Extended operating temperature 125 °C version) (continued)**

**Table 26 Recommended operating conditions (2) (V<sub>CC</sub> = 2.4 to 5.5 V, T<sub>a</sub> = -40 to 125 °C, unless otherwise noted)**

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
I <sub>OH</sub> (peak)	"H" peak output current (Note 1)	P00-P07, P10-P14, P20-P25, P30-P34, P37			-10	mA
I <sub>OL</sub> (peak)	"L" peak output current (Note 1)	P00-P07, P10-P14, P20-P25, P37			10	mA
I <sub>OL</sub> (peak)	"L" peak output current (Note 1)	P30-P34			30	mA
I <sub>OH</sub> (avg)	"H" average output current (Note 2)	P00-P07, P10-P14, P20-P25, P30-P34, P37			-5	mA
I <sub>OL</sub> (avg)	"L" average output current (Note 2)	P00-P07, P10-P14, P20-P25, P37			5	mA
I <sub>OL</sub> (avg)	"L" average output current (Note 2)	P30-P34			15	mA
f(XIN)	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 4.0 to 5.5 V Double-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 2.4 to 5.5 V Double-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V <sub>CC</sub> = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at CR oscillation	V <sub>CC</sub> = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at CR oscillation	V <sub>CC</sub> = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz

**Notes 1:** The peak output current is the peak current flowing in each port.

**2:** The average output current I<sub>OL</sub> (avg), I<sub>OH</sub> (avg) in an average value measured over 100 ms.

**3:** When the oscillation frequency has a duty cycle of 50 %.

Electrical Characteristics (Extended operating temperature 125 °C version)

Table 27 Electrical characteristics (VCC = 2.4 to 5.5 V, VSS = 0 V, Ta = -40 to 125 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	"H" output voltage P00-P07, P10-P14, P20-P25, P30-P34 (Note 1)	IOH = -5 mA VCC = 4.0 to 5.5 V	VCC-1.5			V
		IOH = -1.0 mA VCC = 2.4 to 5.5 V	VCC-1.0			V
VOL	"L" output voltage P00-P07, P10-P14, P20-P25, P37	IOL = 5 mA VCC = 4.0 to 5.5 V			1.5	V
		IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
		IOL = 1.0 mA VCC = 2.4 to 5.5 V			1.0	V
VOL	"L" output voltage P30-P34	IOL = 15 mA VCC = 4.0 to 5.5 V			2.0	V
		IOL = 1.5 mA VCC = 4.0 to 5.5 V			0.3	V
		IOL = 10 mA VCC = 2.4 to 5.5 V			1.0	V
VT+~VT-	Hysteresis CNTR0, INT0, (Note 2) P00-P07 (Note 3)			0.4		V
VT+~VT-	Hysteresis RXD, SCLK, SDATA (Note 2)			0.5		V
VT+~VT-	Hysteresis RESET			0.5		V
IiH	"H" input current P00-P07, P10-P14, P20-P25, P30-P34, P37	Vi = VCC (Pin floating. Pull up transistors "off")			5.0	µA
IiH	"H" input current RESET	Vi = VCC			5.0	µA
IiH	"H" input current XIN	Vi = VCC		4.0		µA
IiL	"L" input current P00-P07, P10-P14, P20-P25, P30-P34, P37	Vi = VSS (Pin floating. Pull up transistors "off")			-5.0	µA
IiL	"L" input current RESET, CNVSS	Vi = VSS			-5.0	µA
IiL	"L" input current XIN	Vi = VSS		-4.0		µA
IiL	"L" input current P00-P07, P30-P34, P37	Vi = VSS (Pull up transistors "on")		-0.2	-0.5	mA
VRAM	RAM hold voltage	When clock stopped	2.0		5.5	V
ICC	Power source current	High-speed mode, f(XIN) = 8 MHz Output transistors "off"		5.0	8.0	mA
		High-speed mode, f(XIN) = 2 MHz, VCC = 2.4 V Output transistors "off"		0.5	1.5	mA
		Double-speed mode, f(XIN) = 4 MHz Output transistors "off"		5.0	8.0	mA
		Middle-speed mode, f(XIN) = 8 MHz, Output transistors "off"		2.0	5.0	mA
		f(XIN) = 8 MHz (in WIT state) Functions except Timer 1 and Timer 2 stop Output transistors "off"		1.6	3.2	mA
		f(XIN) = 2 MHz, VCC = 2.4 V (in WIT state) Output transistors "off"		0.2		mA
		Increment when A-D conversion is executed f(XIN) = 8 MHz, VCC = 5 V		0.5		mA
		All oscillation stopped (in STP state) Output transistors "off"	Ta = 25 °C		0.1	1.0
	Ta = 125 °C			50	µA	

Notes 1: P11 is measured when the P11/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".  
2: RXD, SCLK, SDATA, and INT0 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).  
3: It is available only when operating key-on wake up.

**A-D Converter Characteristics (Extended operating temperature 125 °C version)**

**Table 28 A-D Converter characteristics (1) (VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = -40 to 125 °C, unless otherwise noted)**

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy (excluding quantization error)	VCC = 2.7 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	VCC = 2.7 to 5.5 V Ta = 25 °C			±0.9	LSB
VOT	Zero transition voltage	VCC = VREF = 5.12 V	0	5	20	mV
		VCC = VREF = 3.072 V	0	3	15	mV
VFST	Full scale transition voltage	VCC = VREF = 5.12 V	5105	5115	5125	mV
		VCC = VREF = 3.072 V	3060	3069	3075	mV
tCONV	Conversion time				122	tc(XIN)
RLADDER	Ladder resistor			55		kΩ
IVREF	Reference power source input current	VREF = 5.0 V	50	150	200	μA
		VREF = 3.0 V	30	70	120	
Ii(AD)	A-D port input current				5.0	μA

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**Timing Requirements (Extended operating temperature 125 °C version)**

**Table 29 Timing requirements (1) (V<sub>CC</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -40 to 125 °C, unless otherwise noted)**

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>w</sub> (RESET)	Reset input "L" pulse width	2			μs
t <sub>c</sub> (XIN)	External clock input cycle time	125			ns
t <sub>WH</sub> (XIN)	External clock input "H" pulse width	50			ns
t <sub>WL</sub> (XIN)	External clock input "L" pulse width	50			ns
t <sub>c</sub> (CNTR)	CNTR <sub>0</sub> input cycle time	200			ns
t <sub>WH</sub> (CNTR)	CNTR <sub>0</sub> , INT <sub>0</sub> input "H" pulse width	80			ns
t <sub>WL</sub> (CNTR)	CNTR <sub>0</sub> , INT <sub>0</sub> input "L" pulse width	80			ns
t <sub>c</sub> (SCLK)	Serial I/O2 clock input cycle time	1000			ns
t <sub>WH</sub> (SCLK)	Serial I/O2 clock input "H" pulse width	400			ns
t <sub>WL</sub> (SCLK)	Serial I/O2 clock input "L" pulse width	400			ns
t <sub>su</sub> (SCLK-SDATA)	Serial I/O2 input set up time	200			ns
t <sub>h</sub> (SCLK-SDATA)	Serial I/O2 input hold time	200			ns

**Table 30 Timing requirements (2) (V<sub>CC</sub> = 2.4 to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -40 to 125 °C, unless otherwise noted)**

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>w</sub> (RESET)	Reset input "L" pulse width	2			μs
t <sub>c</sub> (XIN)	External clock input cycle time	250			ns
t <sub>WH</sub> (XIN)	External clock input "H" pulse width	100			ns
t <sub>WL</sub> (XIN)	External clock input "L" pulse width	100			ns
t <sub>c</sub> (CNTR)	CNTR <sub>0</sub> input cycle time	500			ns
t <sub>WH</sub> (CNTR)	CNTR <sub>0</sub> , INT <sub>0</sub> , input "H" pulse width	230			ns
t <sub>WL</sub> (CNTR)	CNTR <sub>0</sub> , INT <sub>0</sub> , input "L" pulse width	230			ns
t <sub>c</sub> (SCLK)	Serial I/O2 clock input cycle time	2000			ns
t <sub>WH</sub> (SCLK)	Serial I/O2 clock input "H" pulse width	950			ns
t <sub>WL</sub> (SCLK)	Serial I/O2 clock input "L" pulse width	950			ns
t <sub>su</sub> (SCLK-SDATA)	Serial I/O2 input set up time	400			ns
t <sub>h</sub> (SCLK-SDATA)	Serial I/O2 input hold time	400			ns



Switching Characteristics (Extended operating temperature 125 °C version)

Table 31 Switching characteristics (1) ( $V_{CC} = 4.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -40$  to  $125$  °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>WH</sub> (SCLK)	Serial I/O2 clock output "H" pulse width	t <sub>c</sub> (SCLK)/2-50			ns
t <sub>WL</sub> (SCLK)	Serial I/O2 clock output "L" pulse width	t <sub>c</sub> (SCLK)/2-50			ns
t <sub>d</sub> (SCLK-SDATA)	Serial I/O2 output delay time			200	ns
t <sub>v</sub> (SCLK-SDATA)	Serial I/O2 output valid time	0			ns
t <sub>r</sub> (SCLK)	Serial I/O2 clock output rising time			50	ns
t <sub>f</sub> (SCLK)	Serial I/O2 clock output falling time			50	ns
t <sub>r</sub> (CMOS)	CMOS output rising time (Note 1)		10	50	ns
t <sub>f</sub> (CMOS)	CMOS output falling time (Note 1)		10	50	ns

Note 1: Pin XOUT is excluded.

Table 32 Switching characteristics (2) ( $V_{CC} = 2.4$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -40$  to  $125$  °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>WH</sub> (SCLK)	Serial I/O2 clock output "H" pulse width	t <sub>c</sub> (SCLK)/2-80			ns
t <sub>WL</sub> (SCLK)	Serial I/O2 clock output "L" pulse width	t <sub>c</sub> (SCLK)/2-80			ns
t <sub>d</sub> (SCLK-SDATA)	Serial I/O2 output delay time			400	ns
t <sub>v</sub> (SCLK-SDATA)	Serial I/O2 output valid time	0			ns
t <sub>r</sub> (SCLK)	Serial I/O2 clock output rising time			80	ns
t <sub>f</sub> (SCLK)	Serial I/O2 clock output falling time			80	ns
t <sub>r</sub> (CMOS)	CMOS output rising time (Note 1)		20	80	ns
t <sub>f</sub> (CMOS)	CMOS output falling time (Note 1)		20	80	ns

Note 1: Pin XOUT is excluded.

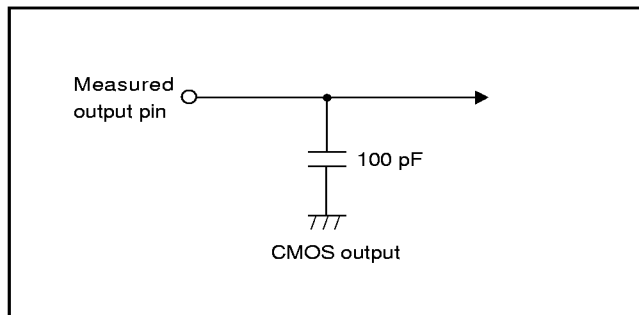


Fig. 49 Switching characteristics measurement circuit diagram (Extended operating temperature 125 °C version)

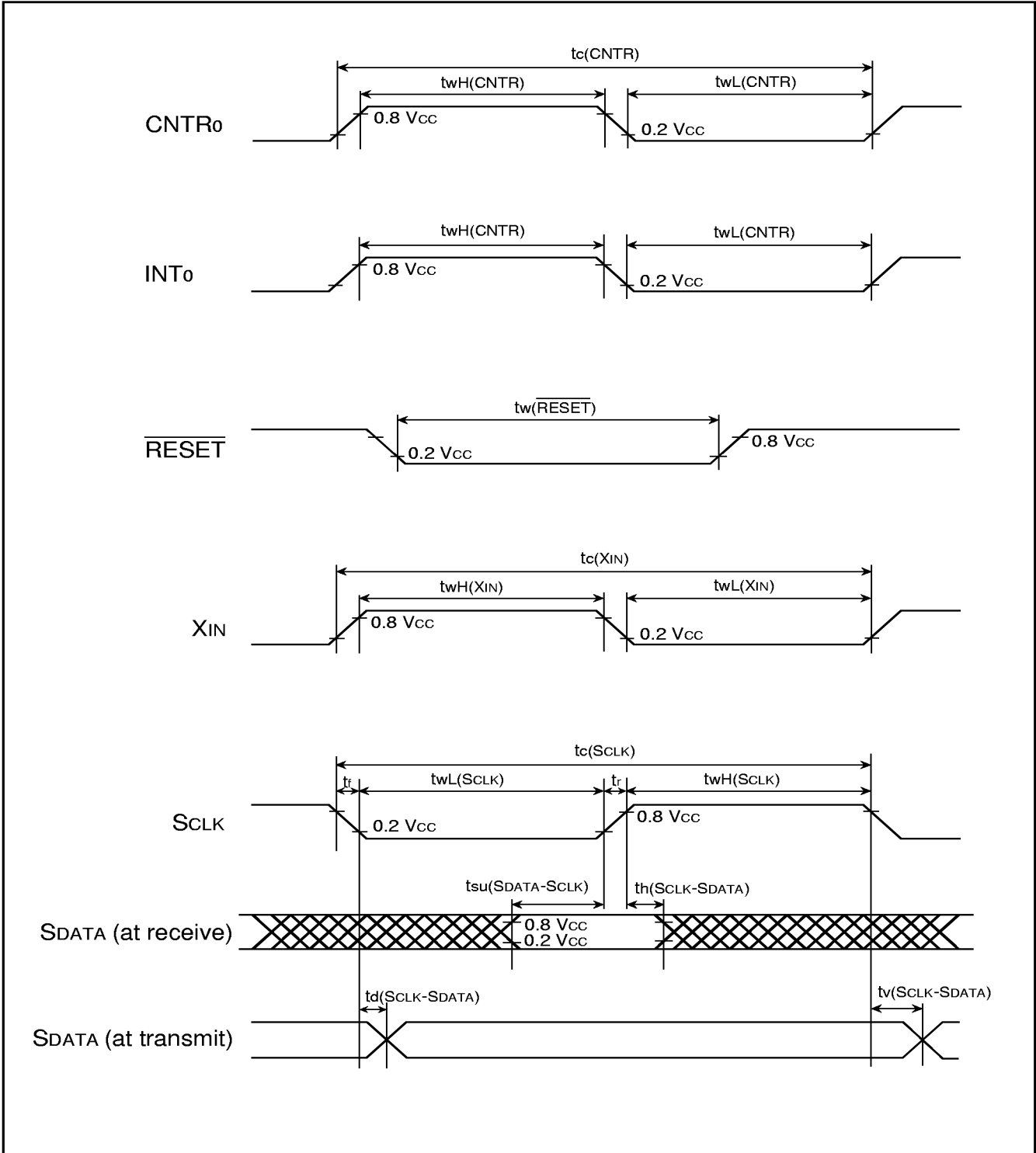


Fig. 50 Timing chart (Extended operating temperature 125 °C version)

**MASK ROM CONFIRMATION FORM**

GZZ-SH52-89B<85B0>

Mask ROM number	
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**740 FAMILY MASK ROM CONFIRMATION FORM**  
**SINGLE-CHIP MICROCOMPUTER**  
**M37531M4-XXXFP/GP/SP**  
**MITSUBISHI ELECTRIC**

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked \*.

*	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

\* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern (Check @ in the appropriate box).

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name :     M37531M4-XXXFP     M37531M4-XXXGP     M37531M4-XXXSP

Checksum code for entire EPROM    

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 (hexadecimal notation)

EPROM type (indicate the type used)

<input type="checkbox"/> <b>27C256</b>	<input type="checkbox"/> <b>27C512</b>																
<p>EPROM address</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">0000<sub>16</sub></td> <td rowspan="3">Area for ASCII codes of the name of the product 'M37531M4-'</td> </tr> <tr> <td>000F<sub>16</sub> 0010<sub>16</sub></td> </tr> <tr> <td style="background-color: #cccccc;">607F<sub>16</sub> 6080<sub>16</sub></td> </tr> <tr> <td></td> <td style="text-align: center;">Data ROM (8K-130) bytes</td> </tr> <tr> <td>7FFD<sub>16</sub> 7FFE<sub>16</sub> 7FFF<sub>16</sub></td> <td style="background-color: #cccccc;"></td> </tr> </table>	0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531M4-'	000F <sub>16</sub> 0010 <sub>16</sub>	607F <sub>16</sub> 6080 <sub>16</sub>		Data ROM (8K-130) bytes	7FFD <sub>16</sub> 7FFE <sub>16</sub> 7FFF <sub>16</sub>		<p>EPROM address</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">0000<sub>16</sub></td> <td rowspan="3">Area for ASCII codes of the name of the product 'M37531M4-'</td> </tr> <tr> <td>000F<sub>16</sub> 0010<sub>16</sub></td> </tr> <tr> <td style="background-color: #cccccc;">E07F<sub>16</sub> E080<sub>16</sub></td> </tr> <tr> <td></td> <td style="text-align: center;">Data ROM (8K-130) bytes</td> </tr> <tr> <td>FFFD<sub>16</sub> FFFE<sub>16</sub> FFFF<sub>16</sub></td> <td style="background-color: #cccccc;"></td> </tr> </table>	0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531M4-'	000F <sub>16</sub> 0010 <sub>16</sub>	E07F <sub>16</sub> E080 <sub>16</sub>		Data ROM (8K-130) bytes	FFFD <sub>16</sub> FFFE <sub>16</sub> FFFF <sub>16</sub>	
0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531M4-'																
000F <sub>16</sub> 0010 <sub>16</sub>																	
607F <sub>16</sub> 6080 <sub>16</sub>																	
	Data ROM (8K-130) bytes																
7FFD <sub>16</sub> 7FFE <sub>16</sub> 7FFF <sub>16</sub>																	
0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531M4-'																
000F <sub>16</sub> 0010 <sub>16</sub>																	
E07F <sub>16</sub> E080 <sub>16</sub>																	
	Data ROM (8K-130) bytes																
FFFD <sub>16</sub> FFFE <sub>16</sub> FFFF <sub>16</sub>																	

In the address space of the microcomputer, the internal ROM area is from addresses E080<sub>16</sub> to FFFD<sub>16</sub>. The reset vector is stored in addresses FFFC<sub>16</sub> and FFFD<sub>16</sub>.

- (1) Set "FF<sub>16</sub>" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37531M4-' to addresses 0000<sub>16</sub> to 000F<sub>16</sub>. ASCII codes 'M37531M4-' are listed on the right. The addresses and data are in hexadecimal notation.

Address	Address	Address
0000 <sub>16</sub>	'M' = 4D <sub>16</sub>	0008 <sub>16</sub>
0001 <sub>16</sub>	'3' = 33 <sub>16</sub>	0009 <sub>16</sub>
0002 <sub>16</sub>	'7' = 37 <sub>16</sub>	000A <sub>16</sub>
0003 <sub>16</sub>	'5' = 35 <sub>16</sub>	000B <sub>16</sub>
0004 <sub>16</sub>	'3' = 33 <sub>16</sub>	000C <sub>16</sub>
0005 <sub>16</sub>	'1' = 31 <sub>16</sub>	000D <sub>16</sub>
0006 <sub>16</sub>	'M' = 4D <sub>16</sub>	000E <sub>16</sub>
0007 <sub>16</sub>	'4' = 34 <sub>16</sub>	000F <sub>16</sub>
		'-' = 2D <sub>16</sub>
		FF <sub>16</sub>
		FF <sub>16</sub>
		FF <sub>16</sub>
		FF <sub>16</sub>
		FF <sub>16</sub>
		FF <sub>16</sub>
		FF <sub>16</sub>

GZZ-SH52-89B<85B0>

Mask ROM number	
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**740 FAMILY MASK ROM CONFIRMATION FORM**  
**SINGLE-CHIP MICROCOMPUTER M37531M4-XXXFP/GP/SP**  
**MITSUBISHI ELECTRIC**

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27C256	27C512
The pseudo-command	$\Delta^*=\Delta\$8000$ $\Delta.BYTE \Delta'M37531M4.'$	$\Delta^*=\Delta\$0000$ $\Delta.BYTE \Delta'M37531M4.'$

ASCII codes, that indicates the name of the product, are written in addresses 0000<sub>16</sub> to 0008<sub>16</sub> of the EPROM by programming the above pseudo-command, which depends on a type of EPROM to be written, at beginning of the source program.

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

\* 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (36P2R for M37531M4-XXXFP, 32P6B for M37531M4-XXXGP, 32P4B for M37531M4-XXXSP) and attach to the mask ROM confirmation form.

\* 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X<sub>IN</sub>-X<sub>OUT</sub> oscillator?

- Ceramic resonator  
 External clock input       Other (      )

At what frequency?

f(X<sub>IN</sub>) =  MHz

\* 4. Comments

MITSUBISHI MICROCOMPUTERS  
7531 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

GZZ-SH52-90B<85B0>

Mask ROM number	
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**740 FAMILY MASK ROM CONFIRMATION FORM**  
**SINGLE-CHIP MICROCOMPUTER**  
**M37531M4T-XXXGP**  
**MITSUBISHI ELECTRIC**

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked \*.

*	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

\* 1. Confirmation

Specify the type of EPROMs submitted.

Three EPROMs are required for each pattern (Check @ in the appropriate box).

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM

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(hexadecimal notation)

EPROM type (indicate the type used)

<input type="checkbox"/> <b>27C256</b>	<input type="checkbox"/> <b>27C512</b>																				
<table border="1"> <tr><td colspan="2">EPROM address</td></tr> <tr><td>0000<sub>16</sub></td><td rowspan="2">Area for ASCII codes of the name of the product 'M37531M4T-'</td></tr> <tr><td>000F<sub>16</sub> 0010<sub>16</sub></td></tr> <tr><td>607F<sub>16</sub> 6080<sub>16</sub></td><td rowspan="4">Data ROM (8K-130) bytes</td></tr> <tr><td>7FFD<sub>16</sub></td></tr> <tr><td>7FFE<sub>16</sub></td></tr> <tr><td>7FFF<sub>16</sub></td></tr> </table>	EPROM address		0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531M4T-'	000F <sub>16</sub> 0010 <sub>16</sub>	607F <sub>16</sub> 6080 <sub>16</sub>	Data ROM (8K-130) bytes	7FFD <sub>16</sub>	7FFE <sub>16</sub>	7FFF <sub>16</sub>	<table border="1"> <tr><td colspan="2">EPROM address</td></tr> <tr><td>0000<sub>16</sub></td><td rowspan="2">Area for ASCII codes of the name of the product 'M37531M4T-'</td></tr> <tr><td>000F<sub>16</sub> 0010<sub>16</sub></td></tr> <tr><td>E07F<sub>16</sub> E080<sub>16</sub></td><td rowspan="4">Data ROM (8K-130) bytes</td></tr> <tr><td>FFFD<sub>16</sub></td></tr> <tr><td>FFFE<sub>16</sub></td></tr> <tr><td>FFFF<sub>16</sub></td></tr> </table>	EPROM address		0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531M4T-'	000F <sub>16</sub> 0010 <sub>16</sub>	E07F <sub>16</sub> E080 <sub>16</sub>	Data ROM (8K-130) bytes	FFFD <sub>16</sub>	FFFE <sub>16</sub>	FFFF <sub>16</sub>
EPROM address																					
0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531M4T-'																				
000F <sub>16</sub> 0010 <sub>16</sub>																					
607F <sub>16</sub> 6080 <sub>16</sub>	Data ROM (8K-130) bytes																				
7FFD <sub>16</sub>																					
7FFE <sub>16</sub>																					
7FFF <sub>16</sub>																					
EPROM address																					
0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531M4T-'																				
000F <sub>16</sub> 0010 <sub>16</sub>																					
E07F <sub>16</sub> E080 <sub>16</sub>	Data ROM (8K-130) bytes																				
FFFD <sub>16</sub>																					
FFFE <sub>16</sub>																					
FFFF <sub>16</sub>																					

In the address space of the microcomputer, the internal ROM area is from addresses E080<sub>16</sub> to FFFD<sub>16</sub>. The reset vector is stored in addresses FFFC<sub>16</sub> and FFFD<sub>16</sub>.

- (1) Set "FF<sub>16</sub>" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37531M4T-' to addresses 0000<sub>16</sub> to 000F<sub>16</sub>. ASCII codes 'M37531M4T-' are listed on the right. The addresses and data are in hexadecimal notation.

Address	
0000 <sub>16</sub>	'M' = 4D <sub>16</sub>
0001 <sub>16</sub>	'3' = 33 <sub>16</sub>
0002 <sub>16</sub>	'7' = 37 <sub>16</sub>
0003 <sub>16</sub>	'5' = 35 <sub>16</sub>
0004 <sub>16</sub>	'3' = 33 <sub>16</sub>
0005 <sub>16</sub>	'1' = 31 <sub>16</sub>
0006 <sub>16</sub>	'M' = 4D <sub>16</sub>
0007 <sub>16</sub>	'4' = 34 <sub>16</sub>

Address	
0008 <sub>16</sub>	'T' = 54 <sub>16</sub>
0009 <sub>16</sub>	'-' = 2D <sub>16</sub>
000A <sub>16</sub>	FF <sub>16</sub>
000B <sub>16</sub>	FF <sub>16</sub>
000C <sub>16</sub>	FF <sub>16</sub>
000D <sub>16</sub>	FF <sub>16</sub>
000E <sub>16</sub>	FF <sub>16</sub>
000F <sub>16</sub>	FF <sub>16</sub>

GZZ-SH52-90B<85B0>

Mask ROM number	
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**740 FAMILY MASK ROM CONFIRMATION FORM  
SINGLE-CHIP MICROCOMPUTER M37531M4T-XXXGP  
MITSUBISHI ELECTRIC**

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27C256	27C512
The pseudo-command	$\Delta^*=\Delta\$8000$ $\Delta.BYTE \Delta'M37531M4T-'$	$\Delta^*=\Delta\$0000$ $\Delta.BYTE \Delta'M37531M4T-'$

ASCII codes, that indicates the name of the product, are written in addresses 0000<sub>16</sub> to 0008<sub>16</sub> of the EPROM by programming the above pseudo-command, which depends on the type of EPROM to be written, at beginning of the source program.

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

\* 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (32P6B for M37531M4T-XXXGP) and attach to the mask ROM confirmation form.

\* 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the XIN-XOUT oscillator?

- Ceramic resonator  
 External clock input                       Other (                      )

At what frequency?                      f(XIN) =  MHz

\* 4. Comments

GZZ-SH53-64B<87B0>

Mask ROM number	
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**740 FAMILY MASK ROM CONFIRMATION FORM**  
**SINGLE-CHIP MICROCOMPUTER**  
**M37531M8-XXXFP/GP/SP**  
**MITSUBISHI ELECTRIC**

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked \*.

*	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

\* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three EPROMs are required for each pattern (Check @ in the appropriate box).

If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Microcomputer name :     M37531M8-XXXFP     M37531M8-XXXGP     M37531M8-XXXSP

Checksum code for entire EPROM    

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 (hexadecimal notation)

EPROM type (indicate the type used)

<input type="checkbox"/> <b>27C256</b>	<input type="checkbox"/> <b>27C512</b>																						
<p>EPROM address</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">0000<sub>16</sub></td> <td rowspan="3">Area for ASCII codes of the name of the product 'M37531M8-'</td> </tr> <tr> <td>000F<sub>16</sub></td> </tr> <tr> <td>0010<sub>16</sub></td> </tr> <tr> <td>407F<sub>16</sub></td> <td rowspan="2">Data ROM (16K-130) bytes</td> </tr> <tr> <td>4080<sub>16</sub></td> </tr> <tr> <td>7FFD<sub>16</sub></td> <td rowspan="3">Shaded area</td> </tr> <tr> <td>7FFE<sub>16</sub></td> </tr> <tr> <td>7FFF<sub>16</sub></td> </tr> </table>	0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531M8-'	000F <sub>16</sub>	0010 <sub>16</sub>	407F <sub>16</sub>	Data ROM (16K-130) bytes	4080 <sub>16</sub>	7FFD <sub>16</sub>	Shaded area	7FFE <sub>16</sub>	7FFF <sub>16</sub>	<p>EPROM address</p> <table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">0000<sub>16</sub></td> <td rowspan="3">Area for ASCII codes of the name of the product 'M37531M8-'</td> </tr> <tr> <td>000F<sub>16</sub></td> </tr> <tr> <td>0010<sub>16</sub></td> </tr> <tr> <td>C07F<sub>16</sub></td> <td rowspan="2">Data ROM (16K-130) bytes</td> </tr> <tr> <td>C080<sub>16</sub></td> </tr> <tr> <td>FFFD<sub>16</sub></td> <td rowspan="3">Shaded area</td> </tr> <tr> <td>FFFE<sub>16</sub></td> </tr> <tr> <td>FFFF<sub>16</sub></td> </tr> </table>	0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531M8-'	000F <sub>16</sub>	0010 <sub>16</sub>	C07F <sub>16</sub>	Data ROM (16K-130) bytes	C080 <sub>16</sub>	FFFD <sub>16</sub>	Shaded area	FFFE <sub>16</sub>	FFFF <sub>16</sub>
0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531M8-'																						
000F <sub>16</sub>																							
0010 <sub>16</sub>																							
407F <sub>16</sub>	Data ROM (16K-130) bytes																						
4080 <sub>16</sub>																							
7FFD <sub>16</sub>	Shaded area																						
7FFE <sub>16</sub>																							
7FFF <sub>16</sub>																							
0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531M8-'																						
000F <sub>16</sub>																							
0010 <sub>16</sub>																							
C07F <sub>16</sub>	Data ROM (16K-130) bytes																						
C080 <sub>16</sub>																							
FFFD <sub>16</sub>	Shaded area																						
FFFE <sub>16</sub>																							
FFFF <sub>16</sub>																							

In the address space of the microcomputer, the internal ROM area is from addresses C080<sub>16</sub> to FFFD<sub>16</sub>. The reset vector is stored in addresses FFFC<sub>16</sub> and FFFD<sub>16</sub>.

- (1) Set "FF<sub>16</sub>" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37531M8-' to addresses 0000<sub>16</sub> to 000F<sub>16</sub>. ASCII codes 'M37531M8-' are listed on the right. The addresses and data are in hexadecimal notation.

Address	Address	Address
0000 <sub>16</sub>	'M' = 4D <sub>16</sub>	0008 <sub>16</sub>
0001 <sub>16</sub>	'3' = 33 <sub>16</sub>	0009 <sub>16</sub>
0002 <sub>16</sub>	'7' = 37 <sub>16</sub>	000A <sub>16</sub>
0003 <sub>16</sub>	'5' = 35 <sub>16</sub>	000B <sub>16</sub>
0004 <sub>16</sub>	'3' = 33 <sub>16</sub>	000C <sub>16</sub>
0005 <sub>16</sub>	'1' = 31 <sub>16</sub>	000D <sub>16</sub>
0006 <sub>16</sub>	'M' = 4D <sub>16</sub>	000E <sub>16</sub>
0007 <sub>16</sub>	'8' = 38 <sub>16</sub>	000F <sub>16</sub>
		'-' = 2D <sub>16</sub>
		FF <sub>16</sub>
		FF <sub>16</sub>
		FF <sub>16</sub>
		FF <sub>16</sub>
		FF <sub>16</sub>
		FF <sub>16</sub>
		FF <sub>16</sub>

GZZ-SH53-64B<87B0>

Mask ROM number	
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**740 FAMILY MASK ROM CONFIRMATION FORM**  
**SINGLE-CHIP MICROCOMPUTER M37531M8-XXXFP/GP/SP**  
**MITSUBISHI ELECTRIC**

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27C256	27C512
The pseudo-command	$\Delta * = \Delta \$ 8000$ $\Delta . \text{BYTE } \Delta ' \text{M37531M8} - '$	$\Delta * = \Delta \$ 0000$ $\Delta . \text{BYTE } \Delta ' \text{M37531M8} - '$

ASCII codes, that indicates the name of the product, are written in addresses 0000<sub>16</sub> to 000F<sub>16</sub> of the EPROM by programming the above pseudo-command, which depends on a type of EPROM to be written, at beginning of the source program.

Note : If the name of the product written to the EPROMs does not match the name of the mask confirmation, the ROM processing is disabled. Write the data correctly.

\* 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (36P2R for M37531M8-XXXFP, 32P6B for M37531M8-XXXGP, 32P4B for M37531M8-XXXSP) and attach to the mask ROM confirmation form.

\* 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X<sub>IN</sub>-X<sub>OUT</sub> oscillator?

- Ceramic resonator  
 External clock input       Other (      )

At what frequency?

f(X<sub>IN</sub>) =  MHz

\* 4. Comments



ROM PROGRAMMING CONFIRMATION FORM

GZZ-SH54-78B<91A0>

ROM number	
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740 FAMILY ROM PROGRAMMING CONFIRMATION FORM  
SINGLE-CHIP MICROCOMPUTER  
M37531E4T-XXXGP  
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked \*.

*	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

\* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.  
Three EPROMs are required for each pattern (Check @ in the appropriate box).  
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM data based on this data.  
We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data.  
Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM 

--	--	--	--

 (hexadecimal notation)

EPROM type (indicate the type used)

<input type="checkbox"/> 27C256	<input type="checkbox"/> 27C512
<p>EPROM address</p> <p>0000<sub>16</sub> Area for ASCII codes of the name of the product 'M37531E4T-'</p> <p>000F<sub>16</sub> 0010<sub>16</sub> </p> <p>607F<sub>16</sub> 6080<sub>16</sub> Data ROM (8K-130) bytes</p> <p>7FFD<sub>16</sub> 7FFE<sub>16</sub> 7FFF<sub>16</sub> </p>	<p>EPROM address</p> <p>0000<sub>16</sub> Area for ASCII codes of the name of the product 'M37531E4T-'</p> <p>000F<sub>16</sub> 0010<sub>16</sub> </p> <p>E07F<sub>16</sub> E080<sub>16</sub> Data ROM (8K-130) bytes</p> <p>FFFD<sub>16</sub> FFFE<sub>16</sub> FFFF<sub>16</sub> </p>

In the address space of the microcomputer, the internal ROM area is from addresses E080<sub>16</sub> to FFFD<sub>16</sub>. The reset vector is stored in addresses FFFC<sub>16</sub> and FFFD<sub>16</sub>.

- Set "FF<sub>16</sub>" in the shaded area.
- Write the ASCII codes that indicates the name of the product 'M37531E4T-' to addresses 0000<sub>16</sub> to 000F<sub>16</sub>. ASCII codes 'M37531E4T-' are listed on the right. The addresses and data are in hexadecimal notation.

Address	'M' = 4D <sub>16</sub>	Address	'T' = 54 <sub>16</sub>
0000 <sub>16</sub>		0008 <sub>16</sub>	'-' = 2D <sub>16</sub>
0001 <sub>16</sub>	'3' = 33 <sub>16</sub>	0009 <sub>16</sub>	FF <sub>16</sub>
0002 <sub>16</sub>	'7' = 37 <sub>16</sub>	000A <sub>16</sub>	FF <sub>16</sub>
0003 <sub>16</sub>	'5' = 35 <sub>16</sub>	000B <sub>16</sub>	FF <sub>16</sub>
0004 <sub>16</sub>	'3' = 33 <sub>16</sub>	000C <sub>16</sub>	FF <sub>16</sub>
0005 <sub>16</sub>	'1' = 31 <sub>16</sub>	000D <sub>16</sub>	FF <sub>16</sub>
0006 <sub>16</sub>	'E' = 45 <sub>16</sub>	000E <sub>16</sub>	FF <sub>16</sub>
0007 <sub>16</sub>	'4' = 34 <sub>16</sub>	000F <sub>16</sub>	FF <sub>16</sub>

GZZ-SH54-78B<91A0>

ROM number	
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**740 FAMILY ROM PROGRAMMING CONFIRMATION FORM**  
**SINGLE-CHIP MICROCOMPUTER M37531E4T-XXXGP**  
**MITSUBISHI ELECTRIC**

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27C256	27C512
The pseudo-command	$\Delta * = \Delta \$ 8000$ $\Delta . \text{BYTE } \Delta ' \text{M37531E4T}'$	$\Delta * = \Delta \$ 0000$ $\Delta . \text{BYTE } \Delta ' \text{M37531E4T}'$

ASCII codes, that indicates the name of the product, are written in addresses 0000<sub>16</sub> to 0008<sub>16</sub> of the EPROM by programming the above pseudo-command, which depends on a type of EPROM to be written, at beginning of the source program.

Note : If the name of the product written to the EPROMs does not match the name of the ROM programming confirmation form, the ROM processing is disabled. Write the data correctly.

\* 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (32P6B for M37531E4T-XXXGP) and attach to the ROM programming confirmation form.

\* 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X<sub>IN</sub>-X<sub>OUT</sub> oscillator?

- Ceramic resonator  
 External clock input       Other (         )

At what frequency?

f(X<sub>IN</sub>) =  MHz

\* 4. Comments

GZZ-SH54-79B<91A0>

ROM number	
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**740 FAMILY ROM PROGRAMMING CONFIRMATION FORM**  
**SINGLE-CHIP MICROCOMPUTER**  
**M37531E4V-XXXGP**  
**MITSUBISHI ELECTRIC**

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked \*.

*	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date:			

\* 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.  
Three EPROMs are required for each pattern (Check @ in the appropriate box).  
If at least two of the three sets of EPROMs submitted contain identical data, we will produce ROM data based on this data.  
We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data.  
Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM 

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 (hexadecimal notation)

EPROM type (indicate the type used)

<input type="checkbox"/> <b>27C256</b>	<input type="checkbox"/> <b>27C512</b>														
<p>EPROM address</p> <table border="1" style="width: 100%;"> <tr><td style="text-align: center;">0000<sub>16</sub></td><td rowspan="2">Area for ASCII codes of the name of the product 'M37531E4V-'</td></tr> <tr><td style="text-align: center;">000F<sub>16</sub> 0010<sub>16</sub></td></tr> <tr><td style="text-align: center;">607F<sub>16</sub> 6080<sub>16</sub></td><td style="text-align: center;">Data ROM (8K-130) bytes</td></tr> <tr><td style="text-align: center;">7FFD<sub>16</sub> 7FFE<sub>16</sub> 7FFF<sub>16</sub></td><td style="background-color: #cccccc;"></td></tr> </table>	0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531E4V-'	000F <sub>16</sub> 0010 <sub>16</sub>	607F <sub>16</sub> 6080 <sub>16</sub>	Data ROM (8K-130) bytes	7FFD <sub>16</sub> 7FFE <sub>16</sub> 7FFF <sub>16</sub>		<p>EPROM address</p> <table border="1" style="width: 100%;"> <tr><td style="text-align: center;">0000<sub>16</sub></td><td rowspan="2">Area for ASCII codes of the name of the product 'M37531E4V-'</td></tr> <tr><td style="text-align: center;">000F<sub>16</sub> 0010<sub>16</sub></td></tr> <tr><td style="text-align: center;">E07F<sub>16</sub> E080<sub>16</sub></td><td style="text-align: center;">Data ROM (8K-130) bytes</td></tr> <tr><td style="text-align: center;">FFFD<sub>16</sub> FFFE<sub>16</sub> FFFF<sub>16</sub></td><td style="background-color: #cccccc;"></td></tr> </table>	0000 <sub>16</sub>	Area for ASCII codes of the name of the product 'M37531E4V-'	000F <sub>16</sub> 0010 <sub>16</sub>	E07F <sub>16</sub> E080 <sub>16</sub>	Data ROM (8K-130) bytes	FFFD <sub>16</sub> FFFE <sub>16</sub> FFFF <sub>16</sub>	
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In the address space of the microcomputer, the internal ROM area is from addresses E080<sub>16</sub> to FFFD<sub>16</sub>. The reset vector is stored in addresses FFFC<sub>16</sub> and FFFD<sub>16</sub>.

- (1) Set "FF<sub>16</sub>" in the shaded area.
- (2) Write the ASCII codes that indicates the name of the product 'M37531E4V-' to addresses 0000<sub>16</sub> to 000F<sub>16</sub>. ASCII codes 'M37531E4V-' are listed on the right. The addresses and data are in hexadecimal notation.

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GZZ-SH54-79B<91A0>

ROM number	
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**740 FAMILY ROM PROGRAMMING CONFIRMATION FORM**  
**SINGLE-CHIP MICROCOMPUTER M37531E4V-XXXGP**  
**MITSUBISHI ELECTRIC**

Recommend to writing the following pseudo-command to the assembler source file :

EPROM type	27C256	27C512
The pseudo-command	$\Delta^*=\Delta\$8000$ $\Delta.BYTE \Delta'M37531E4V'$	$\Delta^*=\Delta\$0000$ $\Delta.BYTE \Delta'M37531E4V'$

ASCII codes, that indicates the name of the product, are written in addresses 0000<sub>16</sub> to 0008<sub>16</sub> of the EPROM by programming the above pseudo-command, which depends on a type of EPROM to be written, at beginning of the source program.

Note : If the name of the product written to the EPROMs does not match the name of the ROM programming confirmation form, the ROM processing is disabled. Write the data correctly.

\* 2. Mark specification

Mark specification must be submitted using the correct form for the package being ordered fill out the appropriate mark specification form (32P6B for M37531E4V-XXXGP) and attach to the ROM programming confirmation form.

\* 3. Usage conditions

Please answer the following questions about usage for use in our product inspection :

(1) How will you use the X<sub>IN</sub>-X<sub>OUT</sub> oscillator?

- Ceramic resonator  
 External clock input       Other (         )

At what frequency?

f(X<sub>IN</sub>) =  MHz

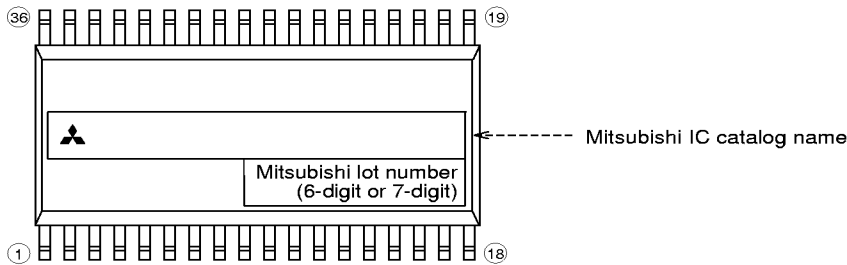
\* 4. Comments

**MARK SPECIFICATION FORM**  
**36P2R-A (36-PIN SHRINK SOP) MARK SPECIFICATION FORM**

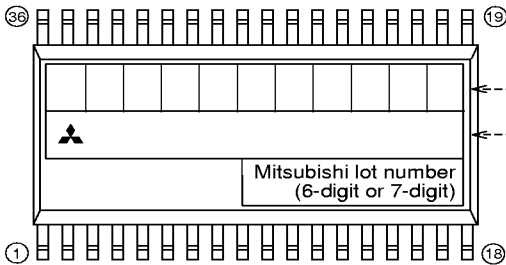
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi catalog name and the special mark (if needed).

**A. Standard Mitsubishi Mark**



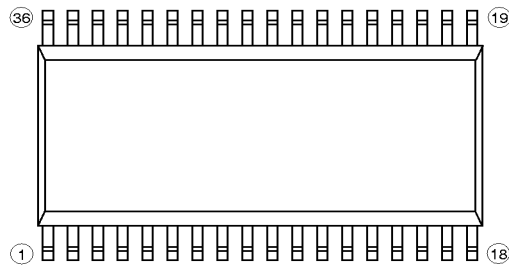
**B. Customer's Parts Number + Mitsubishi catalog name**



- Customer's Parts Number
- Note : The fonts and size of characters are standard Mitsubishi type.
- Mitsubishi IC catalog name
- Note1 : The mark field should be written right aligned.
- 2 : The fonts and size of characters are standard Mitsubishi type.
- 3 : Customer's Parts Number can be up to 11 characters : Only 0 ~ 9, A ~ Z, +, -, /, (, ), &, @, . (periods), , (commas) are usable.
- 4 : If the Mitsubishi logo is not required, check the box below.

Mitsubishi logo is not required

**C. Special Mark Required**



- Note1 : If the Special Mark is to be Printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible.
- Mitsubishi lot number (6-digit or 7-digit) and Mask ROM number (3-digit) are always marked.
- 2 : If the customer's trade mark logo must be used in the Special Mark, check the box below.
- Please submit a clean original of the logo.
- For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

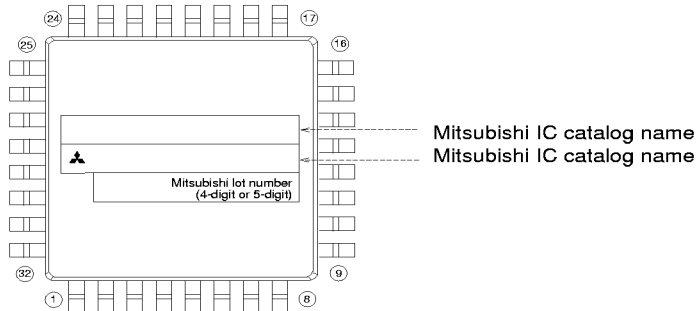
- 3 : The standard Mitsubishi font is used for all characters except for a logo.

**32P6B (32-PIN LQFP) MARK SPECIFICATION FORM**

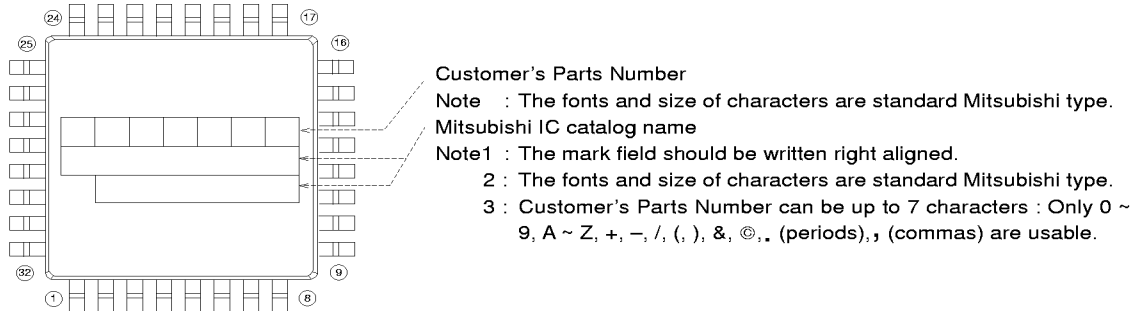
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B), and enter the Mitsubishi catalog name and the special mark (if needed).

**A. Standard Mitsubishi Mark**



**B. Customer's Parts Number + Mitsubishi catalog name**

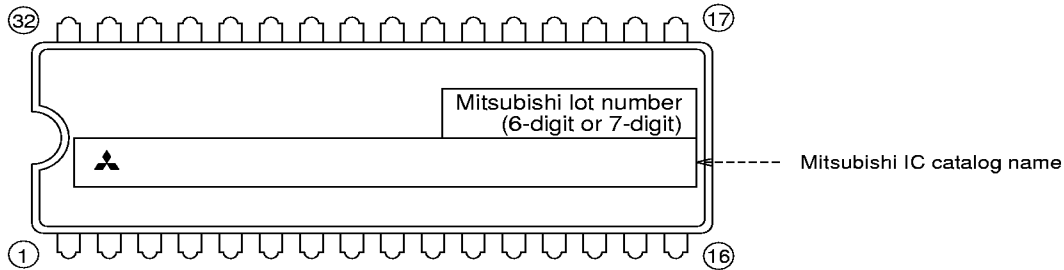


**32P4B (32-PIN SHRINK DIP) MARK SPECIFICATION FORM**

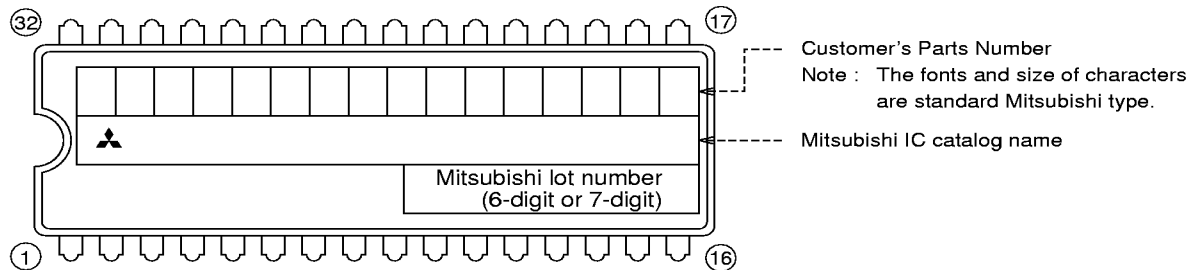
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

**A. Standard Mitsubishi Mark**



**B. Customer's Parts Number + Mitsubishi catalog name**



Note1 : The mark field should be written right aligned.

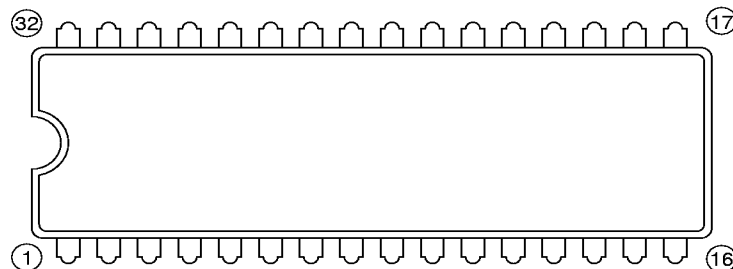
2 : The fonts and size of characters are standard Mitsubishi type.

3 : Customer's Parts Number can be up to 16 characters : Only 0 ~ 9, A ~ Z, +, -, /, (, ), &, ©, . (periods), and , (commas) are usable.

4 : If the Mitsubishi logo is not required, check the box on the right.

Mitsubishi logo is not required

**C. Special Mark Required**



Note1 : If the Special Mark is to be Printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and Mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the Special Mark, check the box on the right. Please submit a clean original of the logo. For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required

3 : The standard Mitsubishi font is used for all characters except for a logo.

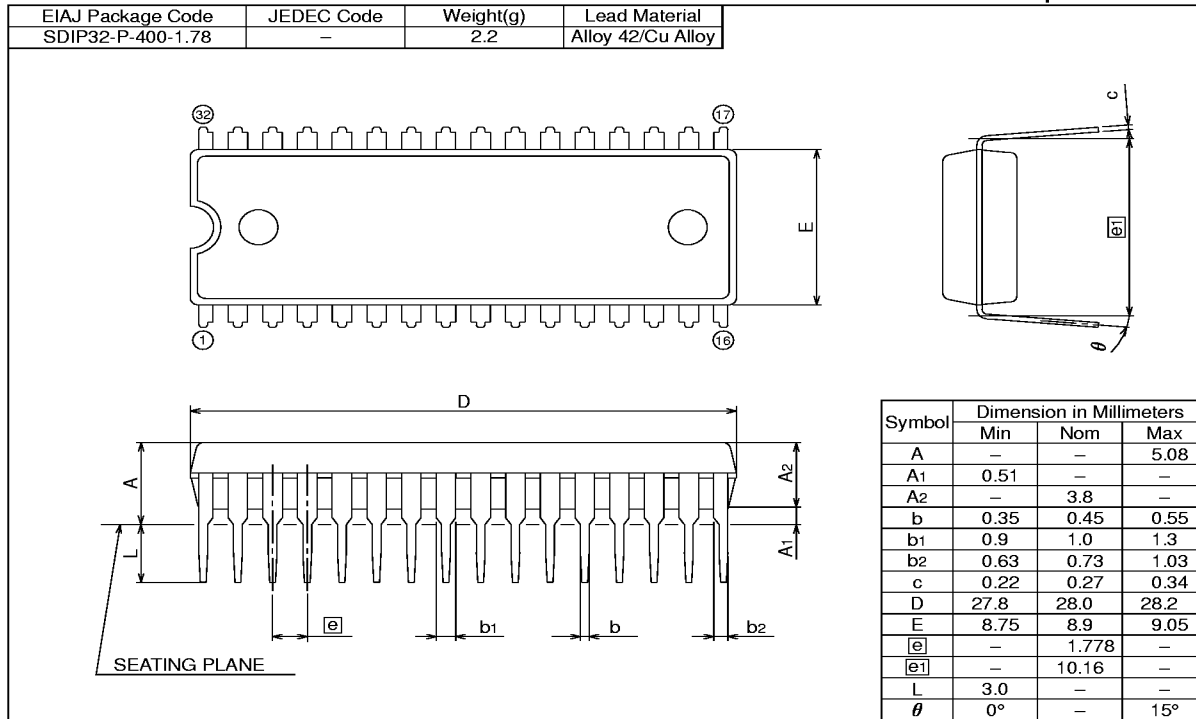
MITSUBISHI MICROCOMPUTERS  
7531 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PACKAGE OUTLINE

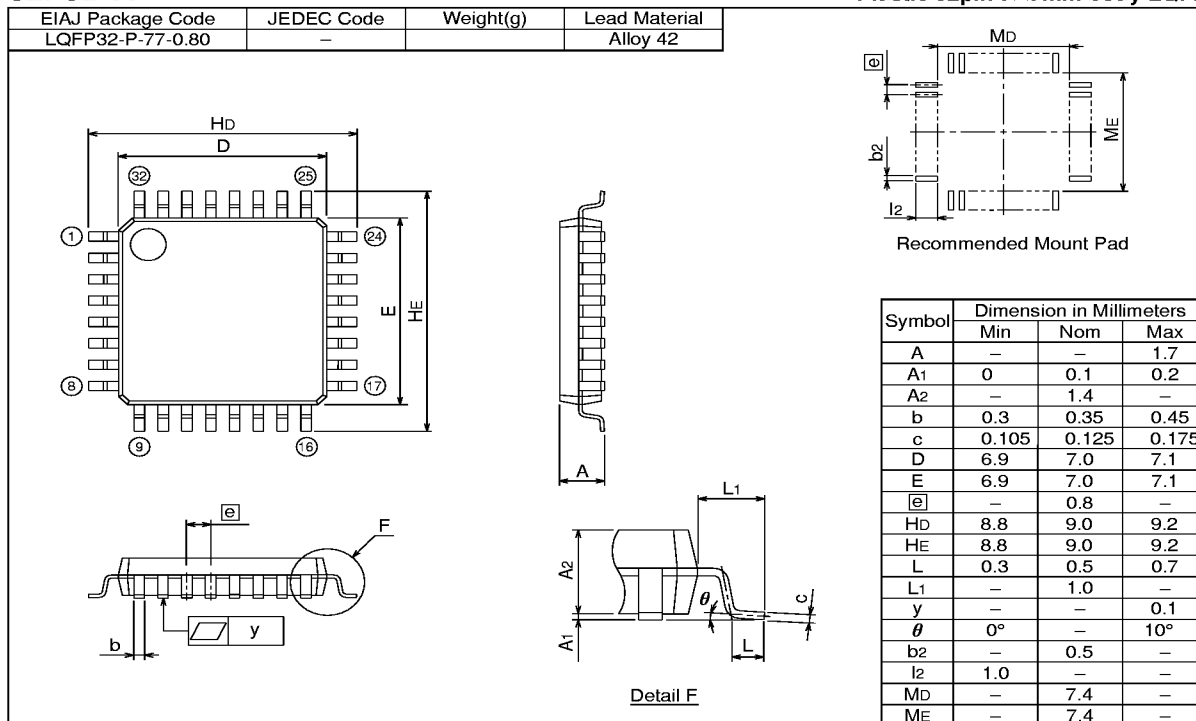
32P4B

Plastic 32pin 400mil SDIP



32P6B-A

Plastic 32pin 7x7mm body LQFP





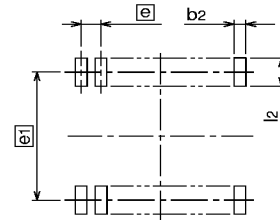
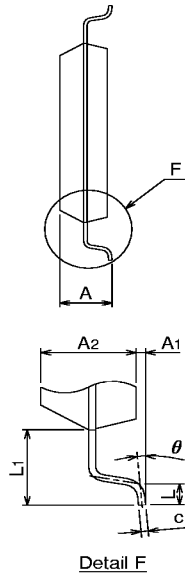
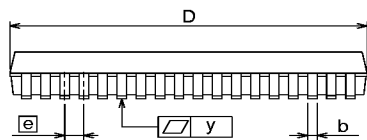
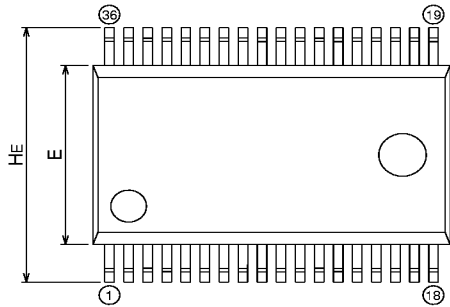
MITSUBISHI MICROCOMPUTERS  
**7531 Group**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

**36P2R-A**

Plastic 36pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP36-P-450-0.80	-	0.53	Alloy 42



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	2.4
A1	0.05	-	-
A2	-	2.0	-
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	14.8	15.0	15.2
E	8.2	8.4	8.6
e	-	0.8	-
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	-	1.765	-
y	-	-	0.15
$\theta$	0°	-	10°
b2	-	0.5	-
e1	-	11.43	-
l2	1.27	-	-

MITSUBISHI MICROCOMPUTERS  
**7531 Group**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

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**Keep safety first in your circuit designs!**

- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

**Notes regarding these materials**

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REVISION DESCRIPTION LIST

7531 Group DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	970822
2.0	<p>Page 1; <b>FEATURES</b>                      In Programmable I/O ports, the pin number of 32-pin version is added.                      In Power source voltage, two conditions are added and two are revised.</p> <p>Page 8; <b>Central Processing Unit (CPU)</b>                      The name of manual, 740 Family Software Manual, is revised.                      Fig. 11; Note is added.</p> <p>Page 11; <b>[Direction registers] PiD</b>                      The sentences are revised: Pins set to input are floating, and permit reading pin values.                      Fig. 12; Bit function and the initial value are added.                      Fig. 13; The figure name is revised: port P1P3 control register.</p> <p>Page 15; <b>Interrupt operation</b>                      The order of No. 3 and 4 is revised.                      Fig. 17; Four bit names are revised: Serial I/O1.</p> <p>Page 21; <b>[Serial I/O1 status register] SIO1STS</b>                      Explanations are partly revised.                      Fig. 25; Bits 6 and 7 explanations of serial I/O1 control register are revised.</p> <p>Page 23; <b>[Serial I/O2 control register] SIO2CON</b>                      Explanations are partly revised.                      Fig. 26; Bit 3 explanations are revised. Note is partly revised.</p> <p>Page 27; <b>Reset Circuit</b>                      Explanations are partly revised: In the case of f(<math>\phi</math>)...</p> <p>Fig. 35; The waveform of clock from built-in ring oscillator is revised. Note 1 is revised.                      Fig. 36; (6) Port P1P3 control register is added.</p> <p>Page 32; <b>A-D Converter</b>                      Explanations are partly revised: The <b>WIT</b> instruction is eliminated.</p> <p>Page 33; <b>DATA REQUIRED FOR ROM PROGRAMMING ORDERS</b>                      This clause is added.</p> <p>Table 7; Characteristics of Vcc is revised.                      Table 8; Characteristics of f(XIN) is revised.                      Table 9; Characteristics of Icc is revised.                      Table 12; Characteristics of tC(XIN), tWH(XIN), tWL(XIN), tC(CNTR), tWH(CNTR), tWL(CNTR), tC(SCLK), tWH(SCLK) and tWL(SCLK) are revised.</p> <p>Pages 42 to 45; <b>MASK ROM CONFIRMATION FORM</b>                      These are added.</p> <p>Pages 46 and 47; <b>ROM PROGRAMMING CONFIRMATION FORM</b>                      These are added.</p>	980220

REVISION DESCRIPTION LIST

7531 Group DATA SHEET

Rev. No.	Revision Description	Rev. date
2.0	<p>Pages 48 to 51; <b>MARK SPECIFICATION FORM</b> These are added.</p> <p>Pages 52 and 53; <b>PACKAGE OUTLINE</b> These are added.</p>	980220
2.1	<p>Pages 37, 46, 47; Some words are corrected.</p> <p>Pages 42 to 47; The numbers of Mask ROM and ROM Programming Confirmation Forms are revised.</p> <p>Page 49; 32P6B Mark Specification Form is revised.</p>	980702
3.0	<p>All pages; "PRELIMINARY Notice: This is ..." eliminated.</p> <p>All register structures; Initial values are added.</p> <p>Page 1; Explanations are partly revised.</p> <p>Page 1 and 2; Product names are added into the pin configurations.</p> <p>Page 3; Pin configuration of 42S1M is added.</p> <p>Page 8; Explanations of Figure 8 and Table 2 are partly revised.</p> <p>Page 9; Explanations of Figures 9 and 10 are partly revised.</p> <p>Page 11; The register name (Timer count source <u>set</u> register) is revised.</p> <p>Page 16; Table 4; The contents of "Remarks" is partly revised.</p> <p>Page 20; Explanation is revised.</p> <p>Page 21; The some word is added.</p> <p>Page 24; The some word is added. Explanation is revised.</p> <p>Page 26; Explanation is added.</p> <p>Page 27; Figure 34; Explanation is revised.</p> <p>Page 28; Period is added.</p> <p>Page 32; Figure titles of Figures 42 and 43 are revised.</p> <p>Page 33; Explanation is revised.</p> <p>Page 36 to 59; "ELECTRICAL CHARACTERISTICS" are all revised.  "Electrical Characteristics" of Extended operating temperature version is added.  "Electrical Characteristics" of Extended operating temperature 125 °C version is added.</p> <p>Page 60 to 71; "MASK ROM CONFIRMATION FORM" and "ROM PROGRAMMING CONFIRMATION FORM" are all revised.</p> <p>"SHRINK DIP MARK SPECIFICATION FORM" eliminated.</p>	990212