



ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748-5089

NTE5728 Powerblock Module

Description:

The NTE5728 uses high voltage power thyristors/diodes and is electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built. This device is intended for general purpose applications such as battery chargers, welders and plating equipment and where high voltage and high current are required.

Features:

- High Voltage
- Electrically Isolated Base Plate
- 3000V_{RMS} Isolating Voltage
- High Surge Capability
- Large Creepage Distances

Ratings and Characteristics:

Average Forward Current ($T_C = +85^\circ\text{C}$, 180° Conduction, Half Sine Wave), $I_{F(AV)}$	250A
Maximum RMS On-State Current (As AC Switch), $I_{T(RMS)}$	555A
Maximum Repetitive Peak Reverse and Off-State Blocking Voltage, V_{RRM} , V_{DRM}	1600V
Maximum Non-Repetitive Peak Reverse Voltage, V_{RSM}	1700V
Maximum Peak Reverse and Off-State Leakage Current ($T_J = +130^\circ\text{C}$), I_{RRM} , I_{DRM}	50mA
RMS Isolation Voltage (50Hz, Circuit to Base, All Terminals Shorted, $t = 1\text{s}$), V_{ISO}	3000V
Critical Rate of Rise of Off-State Voltage ($T_J = +130^\circ\text{C}$), dv/dt (Linear to 80% Rated V_{DRM})	500V/ μs
(Linear to 67% Rated V_{DRM})	1000V/ μs
Operating Junction Temperature Range, T_J	-40° to $+130^\circ\text{C}$
Storage Temperature Range, T_{stg}	-40° to $+150^\circ\text{C}$
Thermal Resistance, Junction-to-Case (Per Junction, DC Operation), R_{thJC}	0.125°C/W
Thermal Resistance, Case-to-Sink (Per Module, Note 1), R_{thCS}	0.02°C/W

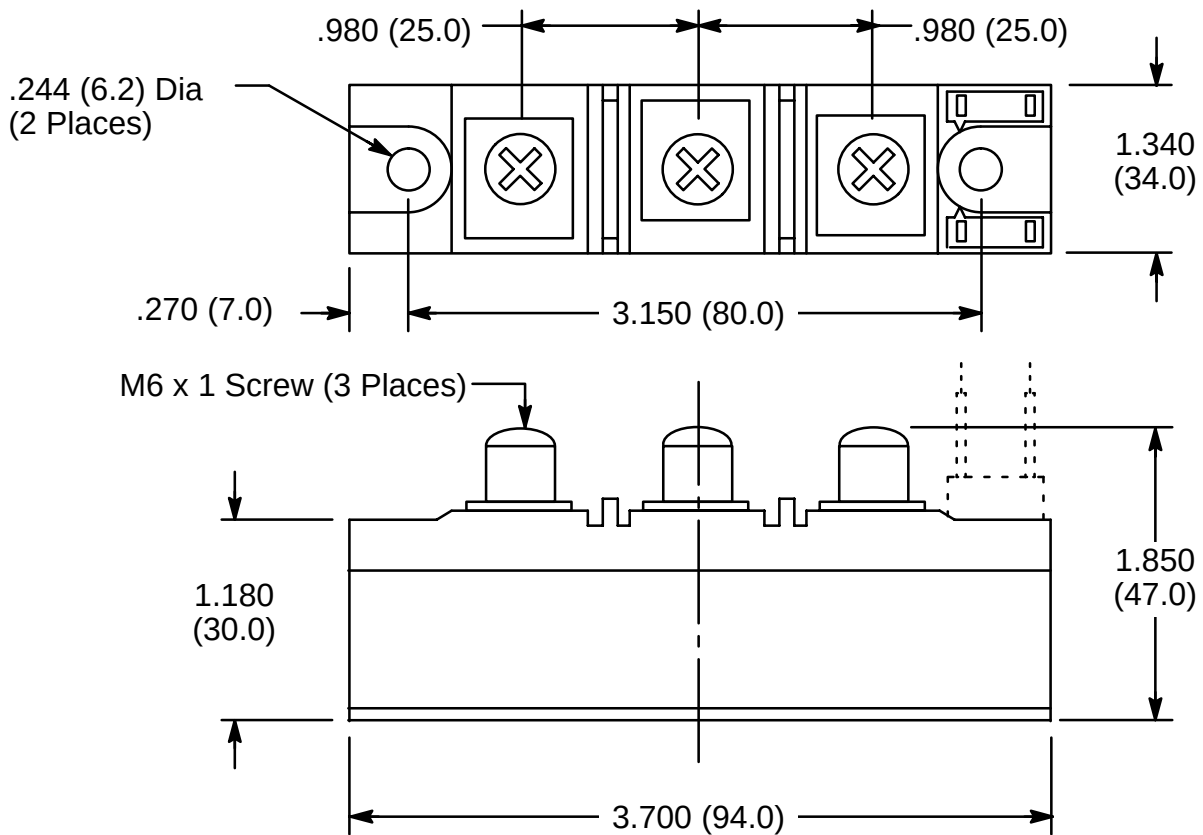
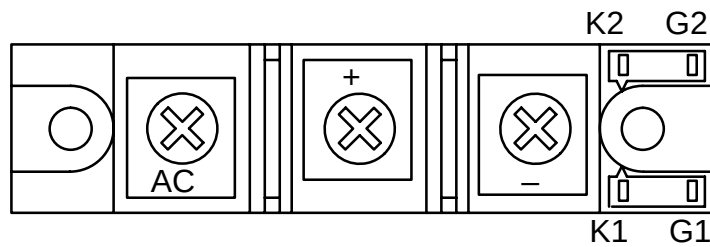
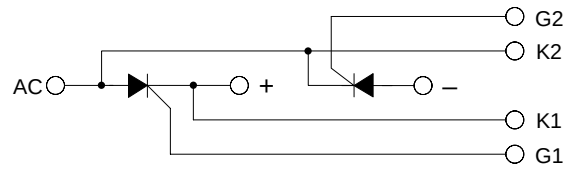
Note 1. Mounting surface flat, smooth and greased.



Electrical Specifications:

Parameter	Symbol	Test Conditions		Rating	Unit
Maximum Peak One–Cycle Non–Repetitive Surge Current	I _{FSM}	t = 10ms	Sinusoidal Half Wave, 100% V _{RRM} Reapplied, Initial T _J = +130°C	7150	A
		t = 8.3ms		7500	A
		t = 10ms	Sinusoidal Half Wave, No Voltage Reapplied, Initial T _J = +130°C	8500	A
		t = 8.3ms		8900	A
Maximum I ² t for Fusing	I ² t	t = 10ms	Sinusoidal Half Wave, 100% V _{RRM} Reapplied, Initial T _J = +130°C	255	A ² s
		t = 8.3ms		233	A ² s
		t = 10ms	Sinusoidal Half Wave, No Voltage Reapplied, Initial T _J = +130°C	361	A ² s
		t = 8.3ms		330	A ² s
Maximum I ² √t	I ² √t	t = 0.1 to 10ms, no voltage reapplied		3610	A ² √t
Threshold Voltage, Low level	V _{T(TO)1}	T _J = +130°C, (16.7% × π × I _{T(AV)}) < I < π × I _{T(AV)})		0.97	V
Threshold Voltage, High level	V _{T(TO)2}	T _J = +130°C, (π × I _{T(AV)}) < I < 20 × π × I _{T(AV)})		1.00	V
On–State Slope Resistance, Low Level	r _{t1}	T _J = +130°C, (16.7% × π × I _{T(AV)}) < I < π × I _{T(AV)})		0.60	mΩ
On–State Slope Resistance, High Level	r _{t2}	T _J = +130°C, (π × I _{T(AV)}) < I < 20 × π × I _{T(AV)})		0.57	mΩ
Maximum On–State Voltage Drop	V _{TM}	T _J = +130°C, I _{TM} = π × I _{T(AV)} , 180° Condition, Av. Power = V _{T(TO)} × I _{T(AV)} + r _t × (I _{T(RMS)}) ²		1.44	V
Maximum Holding Current	I _H	Anode Supply = 12V, Initial I _T = 30A, T _J = +25°C		500	mA
Maximum Latching Current	I _L	Anode Supply = 12V, Resistive Load = 1Ω, Gat Pulse: 10V, 100μs, T _J = +25°C		1000	mA
Maximum Peak Gate Power	P _{GM}	T _J = +130°C, t _p ≤ 5ms		10	W
Maximum Average Gate Power	P _{G(AV)}	T _J = +130°C, f = 50Hz		2.0	W
Maximum Peak Gate Current	+I _{GM}	T _J = +130°C, t _p ≤ 5ms		3.0	A
Maximum Peak Negative Gate Voltage	–V _{GT}	T _J = +130°C, t _p ≤ 5ms		5.0	V
Maximum Required DC Gate Trigger Voltage to Trigger	V _{GT}	T _J = –40°C	Anode Supply = 12V, Resistive Load: R _A = 1Ω	4.0	V
		T _J = +25°C		3.0	V
		T _J = +130°C		2.0	V
Maximum Required DC Gate Trigger Current to Trigger	I _{GT}	T _J = –40°C	Anode Supply = 12V, Resistive Load: R _A = 1Ω	350	mA
		T _J = +25°C		200	mA
		T _J = +130°C		100	mA
Maximum Gate Voltage that will not Trigger	V _{GD}	T _J = +130°C, Rated V _{DRM} Applied		0.25	V
Maximum Gate Current that will not Trigger	I _{GD}	T _J = +130°C, Rated V _{DRM} Applied		10	mA
Maximum Rate of Rise of Turned–On Current	di/dt	T _J = +130°C, I _{TM} = 400A, Rated V _{DRM} Applied		500	A/μs
Typical Delay Time	t _d	T _J = +25°C, Gate Current = 1A di _G /dt = 1A/μs, V _D = 0.67% V _{DRM}		1.0	μs
Typical Rise Time	t _r			2.0	μs
Typical Turn–Off Time	t _q	T _J = +25°C, I _{TM} = 300A, –di/dt = 15A/μs, V _R = 50V, dV/dt = 20V/μs, Gate 0V, 100Ω		50–150	μs

Circuit Diagram



NOTE: Can be used with Heat Sink NTE441A