7540 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 7540 Group is the 8-bit microcomputer based on the 740 family core technology.

The 7540 Group has a serial I/O, 8-bit timers, a 16-bit timer, and an A-D converter, and is useful for control of home electric appliances and office automation equipment.

FEATURES

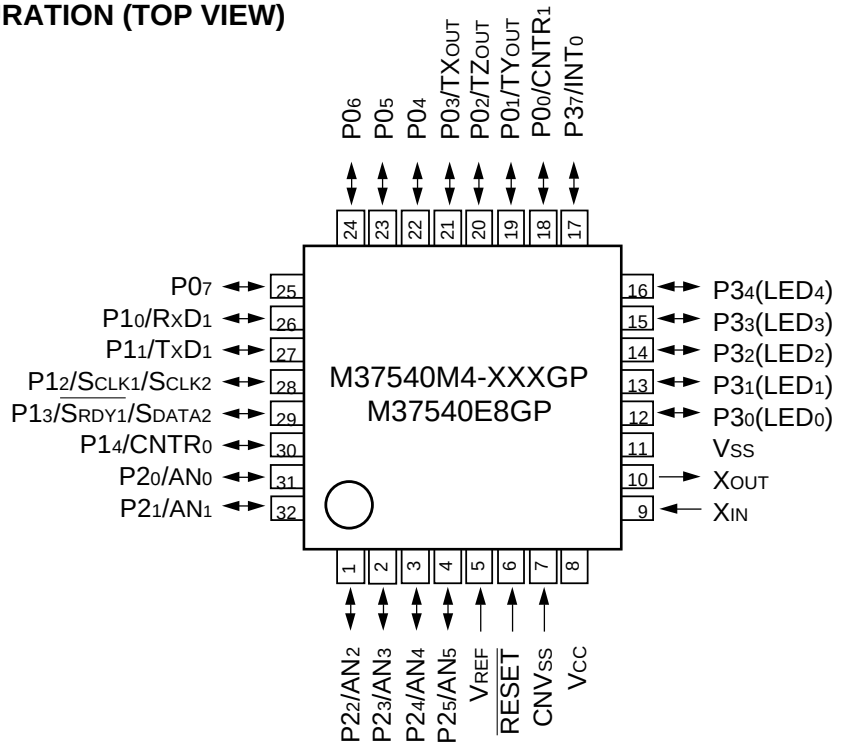
- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.50 µs
  (at 8 MHz oscillation frequency for the shortest instruction)
- Memory size ROM ..... 16K to 32K bytes
  RAM ..... 512 to 768 bytes
- Programmable I/O ports 29
  (25 in 32-pin version)
- Interrupts ..... 15 sources, 15 vectors
  (14 sources, 14 vectors for 32-pin version)
- Timers ..... 8-bit × 4
  16-bit × 1
- Serial I/O1 ..... 8-bit × 1
  (UART or Clock-synchronized)
- Serial I/O2 ..... 8-bit × 1
  (Clock-synchronized)
- A-D converter ..... 10-bit × 8 channels
  (6 channels for 32-pin version)
- Clock generating circuit ..... Built-in type
  (low-power dissipation by a ring oscillator enabled)
  (connect to external ceramic resonator or quartz-crystal oscillator permitting RC oscillation)
- Watchdog timer ..... 16-bit × 1
- Power source voltage
  X_{IN} oscillation frequency at ceramic oscillation, in high-speed mode
  At 8 MHz ..... 4.0 to 5.5 V
  At 4 MHz ..... 2.4 to 5.5 V
  At 2 MHz ..... 2.2 to 5.5 V
  X_{IN} oscillation frequency at RC oscillation
  At 4 MHz ..... 4.0 to 5.5 V
  At 2 MHz ..... 2.4 to 5.5 V
  At 1 MHz ..... 2.2 to 5.5 V
- Power dissipation ..... 25 mW (standard)
- Operating temperature range ..... –20 to 85 °C
  (–40 to 85 °C for extended operating temperature version)

APPLICATION

Office automation equipment, factory automation equipment, home electric appliances, consumer electronics, car, etc.

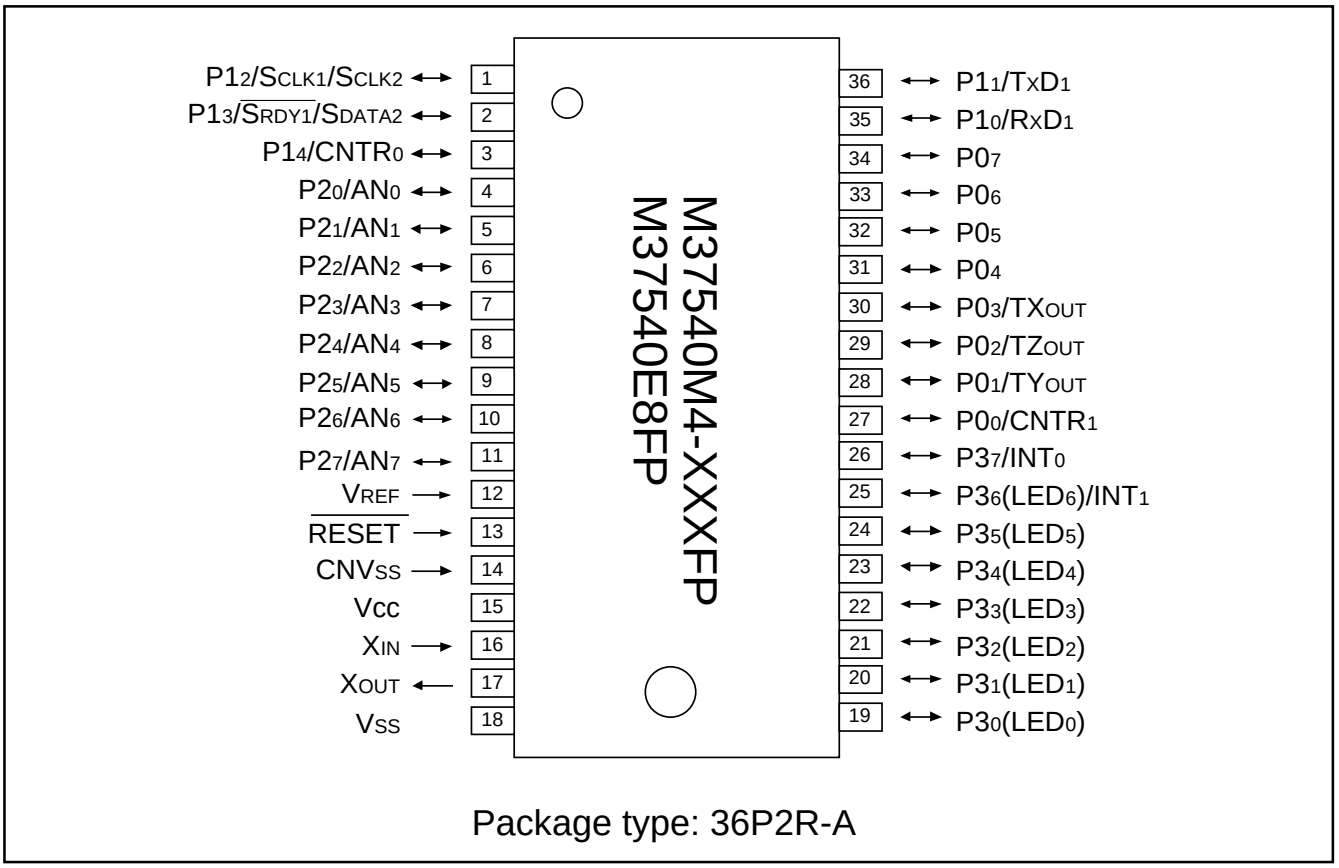
Note: Serial I/O2 can be used in the following cases;
(1) Serial I/O1 is not used,
(2) Serial I/O1 is used as UART and BRG output divided by 16 is selected as the synchronized clock.

PIN CONFIGURATION (TOP VIEW)



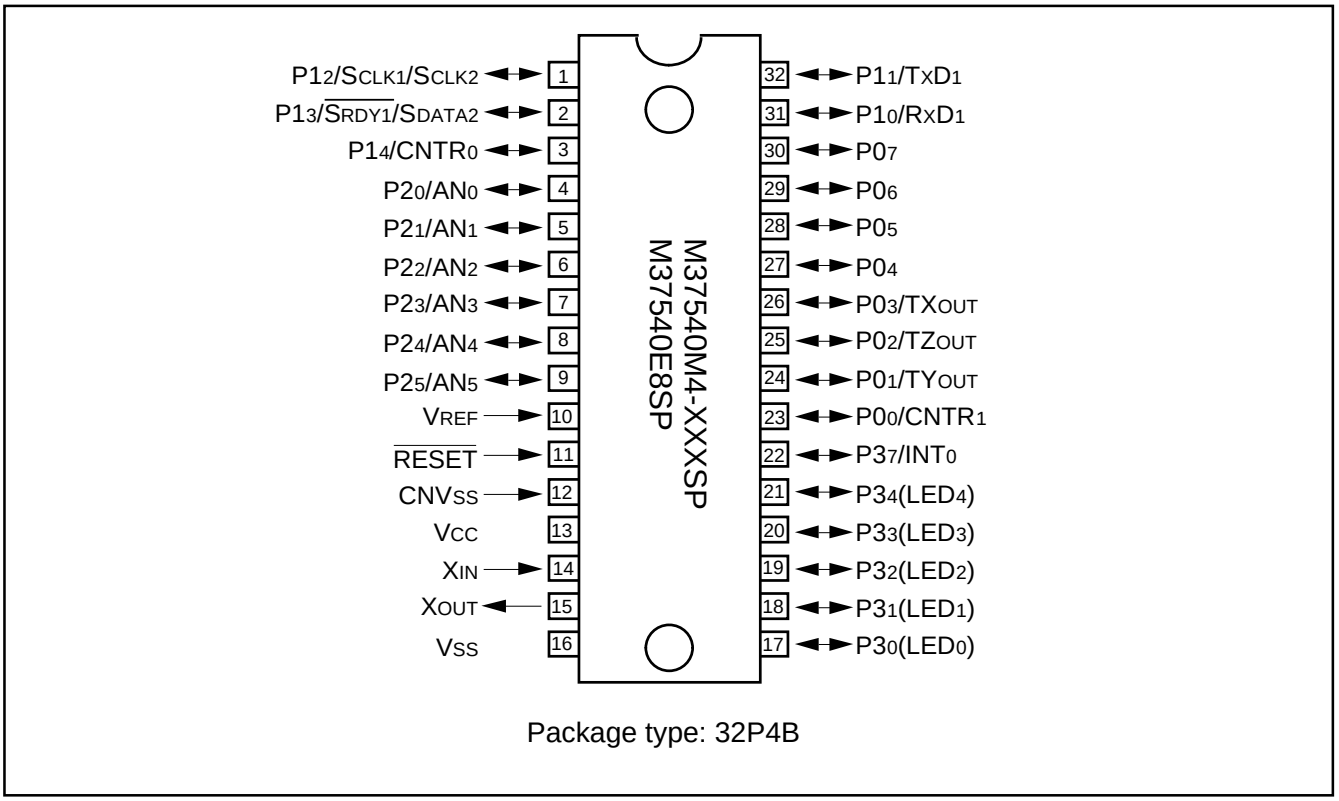
Package type: 32P6B-A

Fig. 1 M37540M4-XXXGP, M37540E8GP pin configuration



Package type: 36P2R-A

Fig. 2 M37540M4-XXXFP, M37540E8FP pin configuration



Package type: 32P4B

Fig. 3 M37540M4-XXXSP, M37540E8SP pin configuration

FUNCTIONAL BLOCK

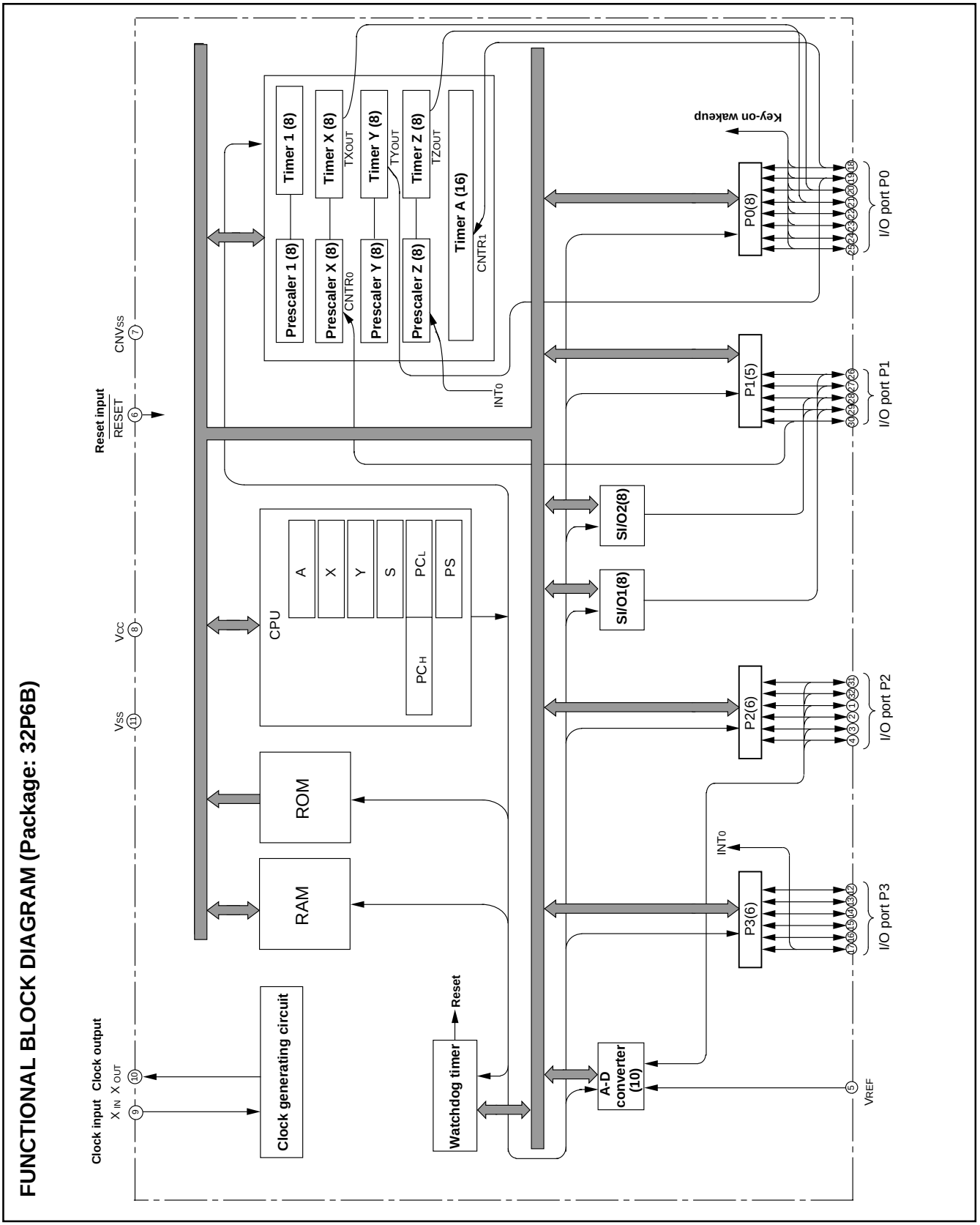


Fig. 4 Functional block diagram (32P6B package)

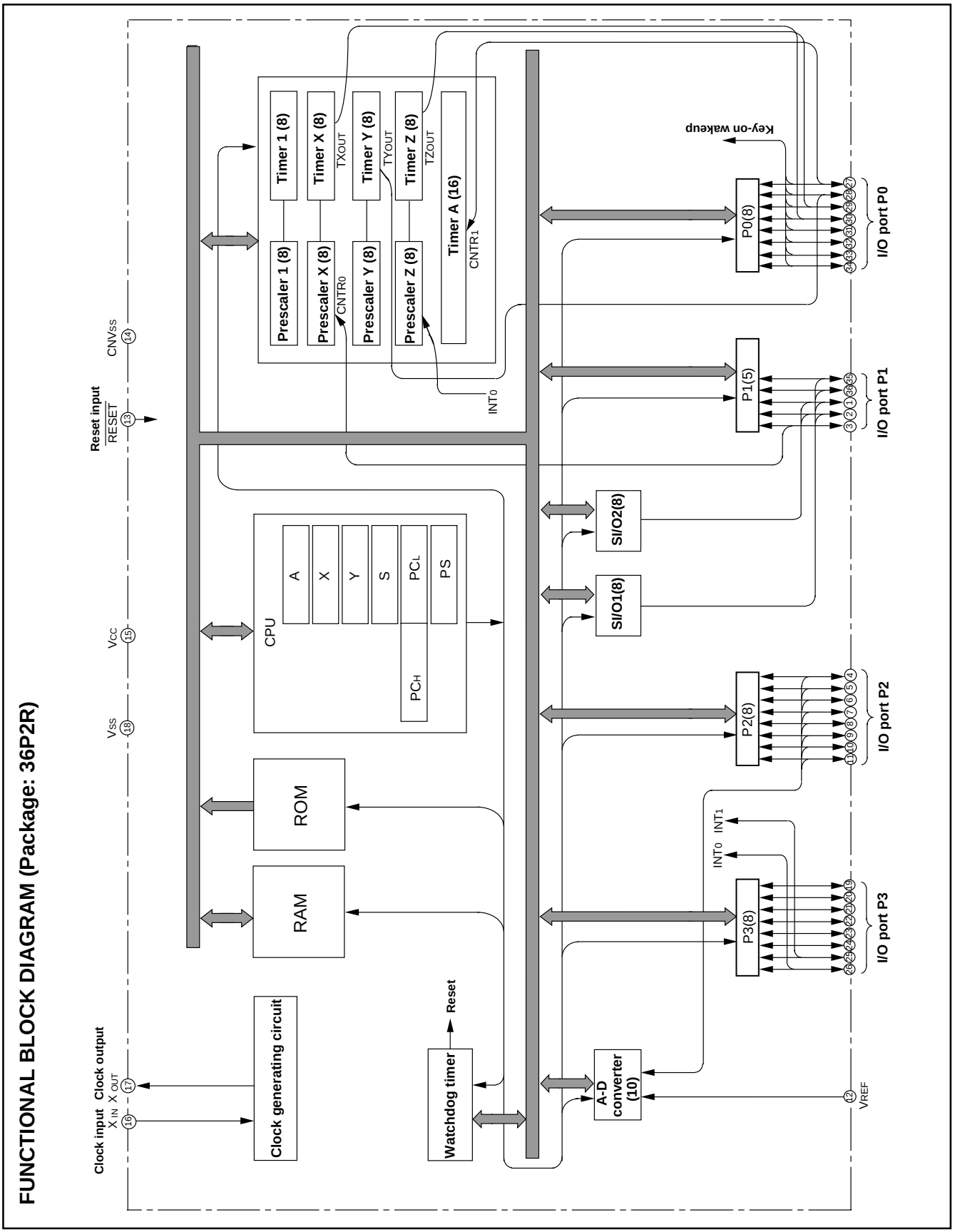


Fig. 5 Functional block diagram (36P2R package)

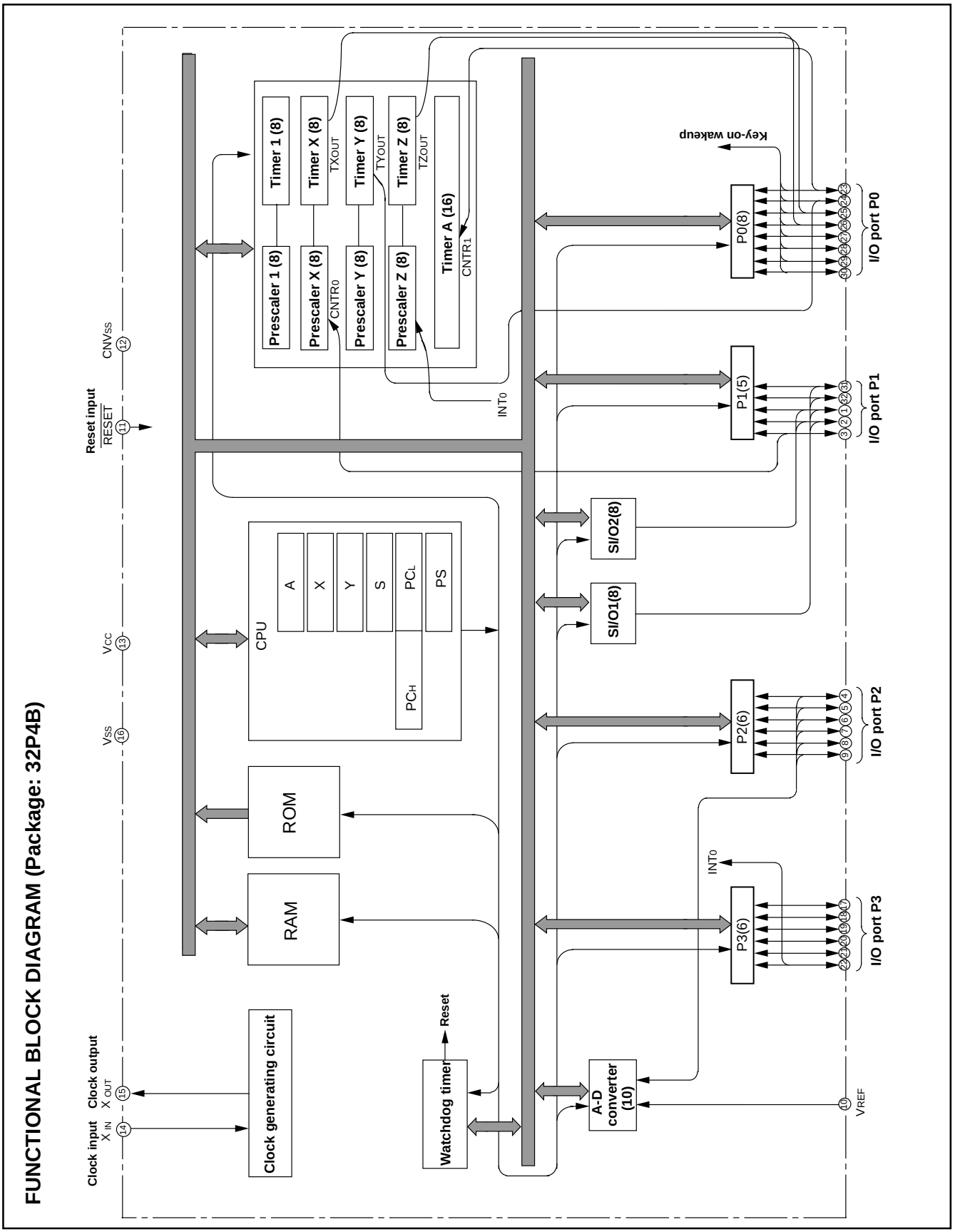


Fig. 6 Functional block diagram (32P4B package)

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	Function expect a port function
Vcc, Vss	Power source	•Apply voltage of 2.2–5.5 V to Vcc, and 0 V to Vss.	
V_{REF}	Analog reference voltage	•Reference voltage input pin for A-D converter	
CNVss	CNVss	•Chip operating mode control pin, which is always connected to Vss.	
$\overline{RESET}$	Reset input	•Reset input pin for active "L"	
X_{IN}	Clock input	•Input and output pins for main clock generating circuit •Connect a ceramic resonator or quartz crystal oscillator between the X_{IN} and X_{OUT} pins. •For using RC oscillator, short between the X_{IN} and X_{OUT} pins, and connect the capacitor and resistor. •If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
$P0_0$/$CNTR_1$ $P0_1$/TY_{OUT} $P0_2$/TZ_{OUT} $P0_3$/TX_{OUT} $P0_4$–$P0_7$	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •Whether a built-in pull-up resistor is to be used or not can be determined by program.	• Key-input (key-on wake up interrupt input) pins • Timer Y, timer Z, timer X and timer A function pin
$P1_0$/RxD_1 $P1_1$/TxD_1	I/O port P1	•5-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level •CMOS 3-state output structure •CMOS/TTL level can be switched for $P1_0$, $P1_2$ and $P1_3$	•Serial I/O1 function pin
$P1_2$/$\overline{SCLK1}$/$SCLK2$ $P1_3$/$\overline{SRDY1}$/$SDATA2$			•Serial I/O1 function pin •Serial I/O2 function pin
$P1_4$/$CNTR_0$			•Timer X function pin
$P2_0$/AN_0– $P2_7$/AN_7	I/O port P2	•8-bit I/O port having almost the same function as P0 •CMOS compatible input level •CMOS 3-state output structure	•Input pins for A-D converter
$P3_0$–$P3_5$	I/O port P3	•8-bit I/O port •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level (CMOS/TTL level can be switched for $P3_6$ and $P3_7$). •CMOS 3-state output structure •$P3_0$ to $P3_6$ can output a large current for driving LED.	
$P3_6$/INT_1 $P3_7$/INT_0		•Whether a built-in pull-up resistor is to be used or not can be determined by program.	•Interrupt input pins

GROUP EXPANSION

Mitsubishi plans to expand the 7540 group as follow:

Memory type

Support for Mask ROM version, One Time PROM version, and Emulator MCU .

Memory size

ROM/PROM size ..... 16 K to 32 K bytes
RAM size ..... 512 to 768 bytes

Package

32P4B ..... 32-pin shrink plastic molded DIP
32P6B-A ..... 0.8 mm-pitch plastic molded QFP
36P2R-A ..... 0.8 mm-pitch plastic molded SOP
42S1M ..... 42-pin shrink ceramic PIGGY BACK

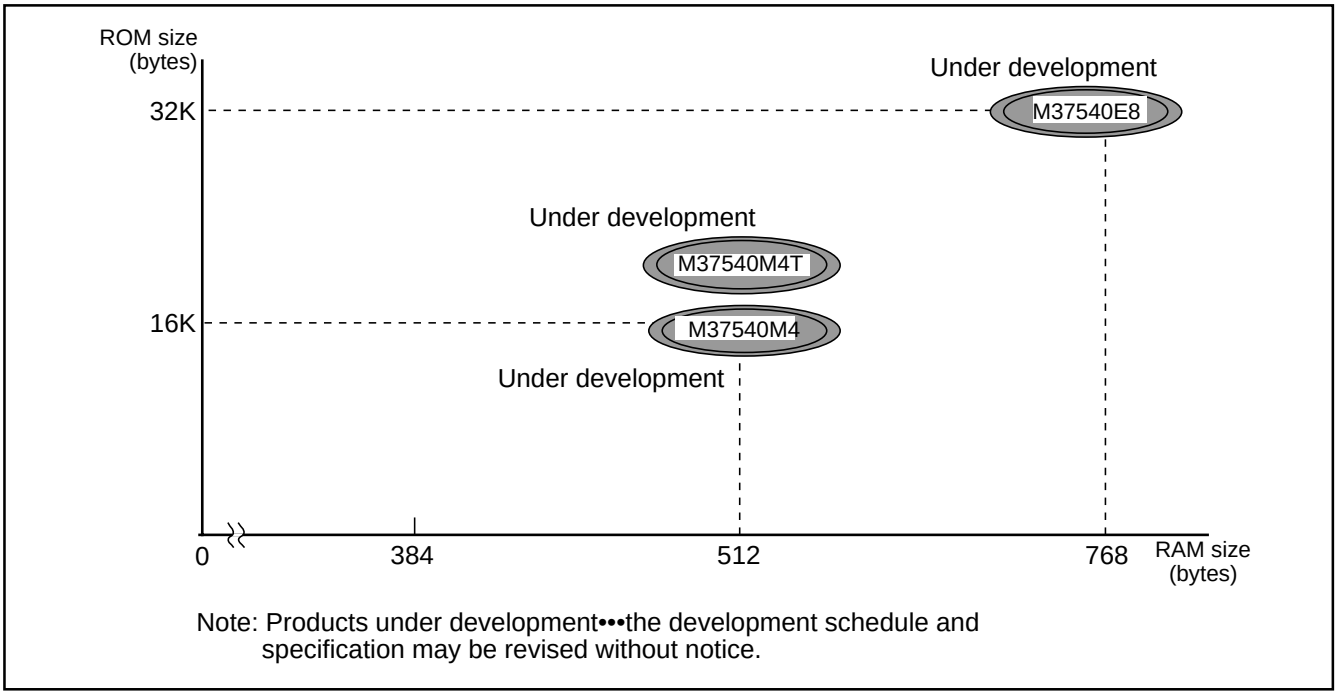


Fig. 7 Memory expansion plan

Currently supported products are listed below.

Table 2 List of supported products

Product	(P) ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M37540M4-XXXSP	16384 (16254)	512	32P4B	Mask ROM version
M37540M4-XXXFP			36P2R-A	Mask ROM version
M37540M4T-XXXFP				Mask ROM version (extended operating temperature version)
M37540M4-XXXGP			32P6B-A	Mask ROM version
M37540M4T-XXXGP				Mask ROM version (extended operating temperature version)
M37540E8SP	32768 (32638)	768	32P4B	One Time PROM version (blank)
M37540E8FP			36P2R-A	One Time PROM version (blank)
M37540E8GP			32P6B-A	One Time PROM version (blank)
M37540RSS	————	768	42S1M	Emulator MCU

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The 7540 Group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine-language instructions or the 740 Family Software MANUAL for details on each instruction set.

Machine-resident 740 family instructions are as follows:

1. The FST and SLW instructions cannot be used.
2. The MUL and DIV instructions can be used.
3. The WIT instruction can be used.
4. The STP instruction can be used.

(This instruction cannot be used while CPU operates by a ring oscillator.)

[CPU mode register] CPUM

The CPU mode register contains the stack page selection bit.
This register is allocated at address 003B16.

Switching method of CPU mode register

Switch the CPU mode register (CPUM) at the head of program after releasing Reset in the following method.

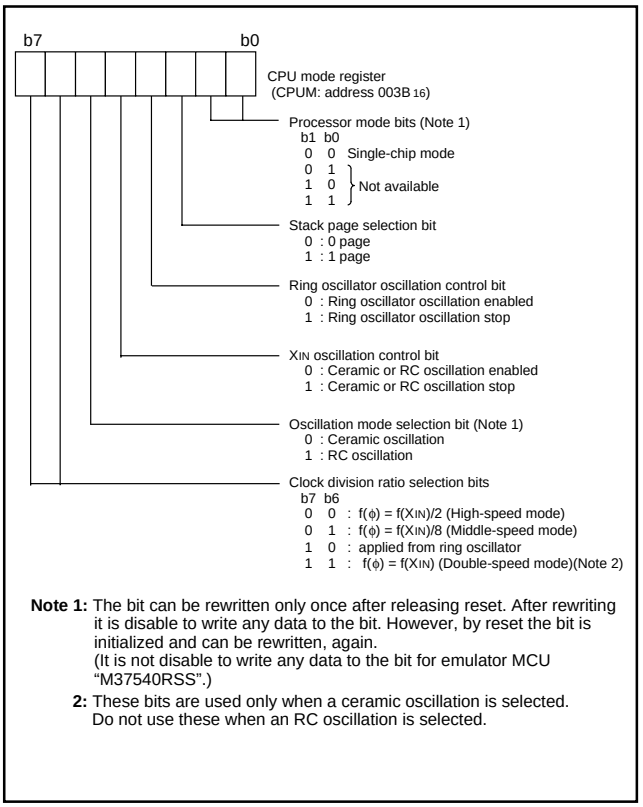


Fig. 8 Structure of CPU mode register

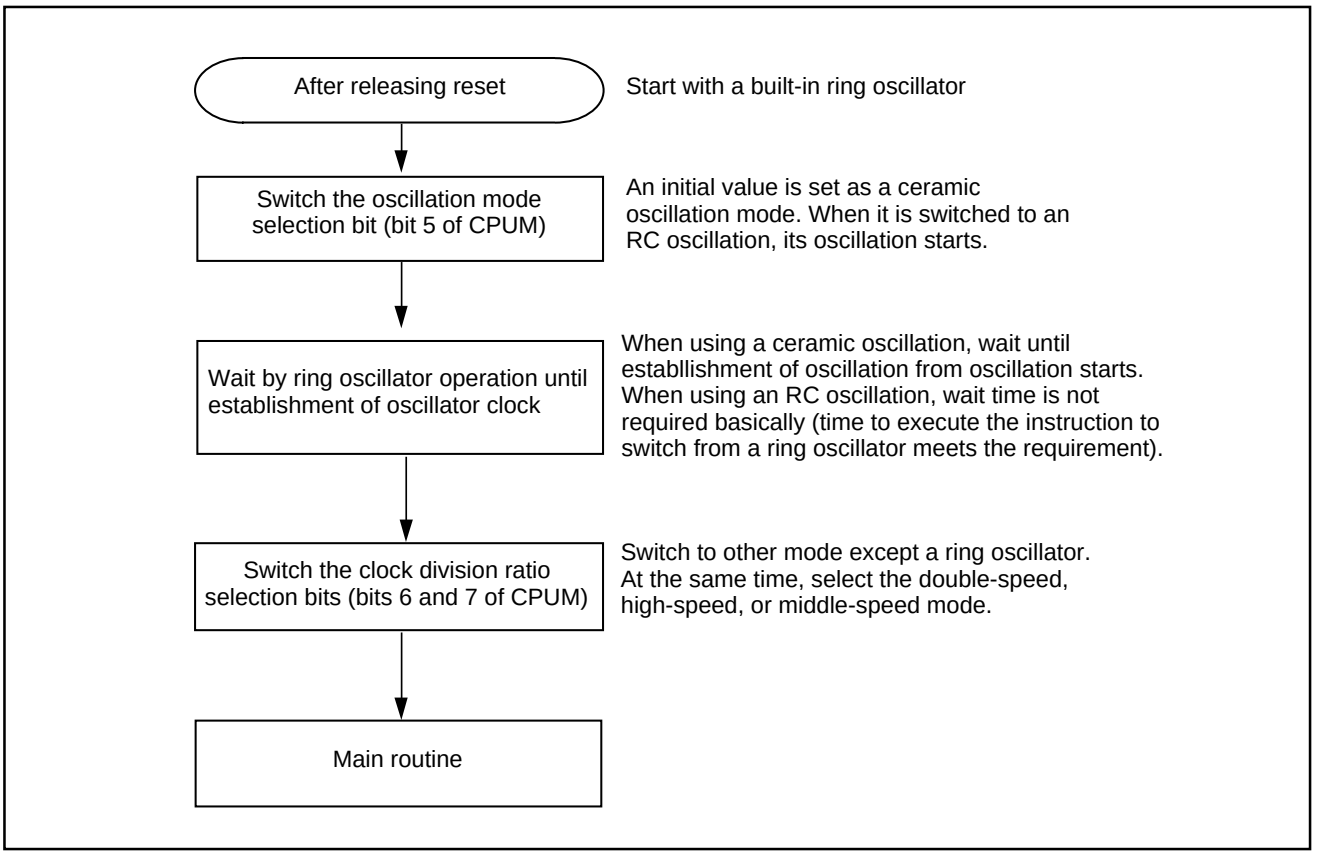


Fig. 9 Switching method of CPU mode register

Memory

Special function register (SFR) area

The SFR area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for a stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is a user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

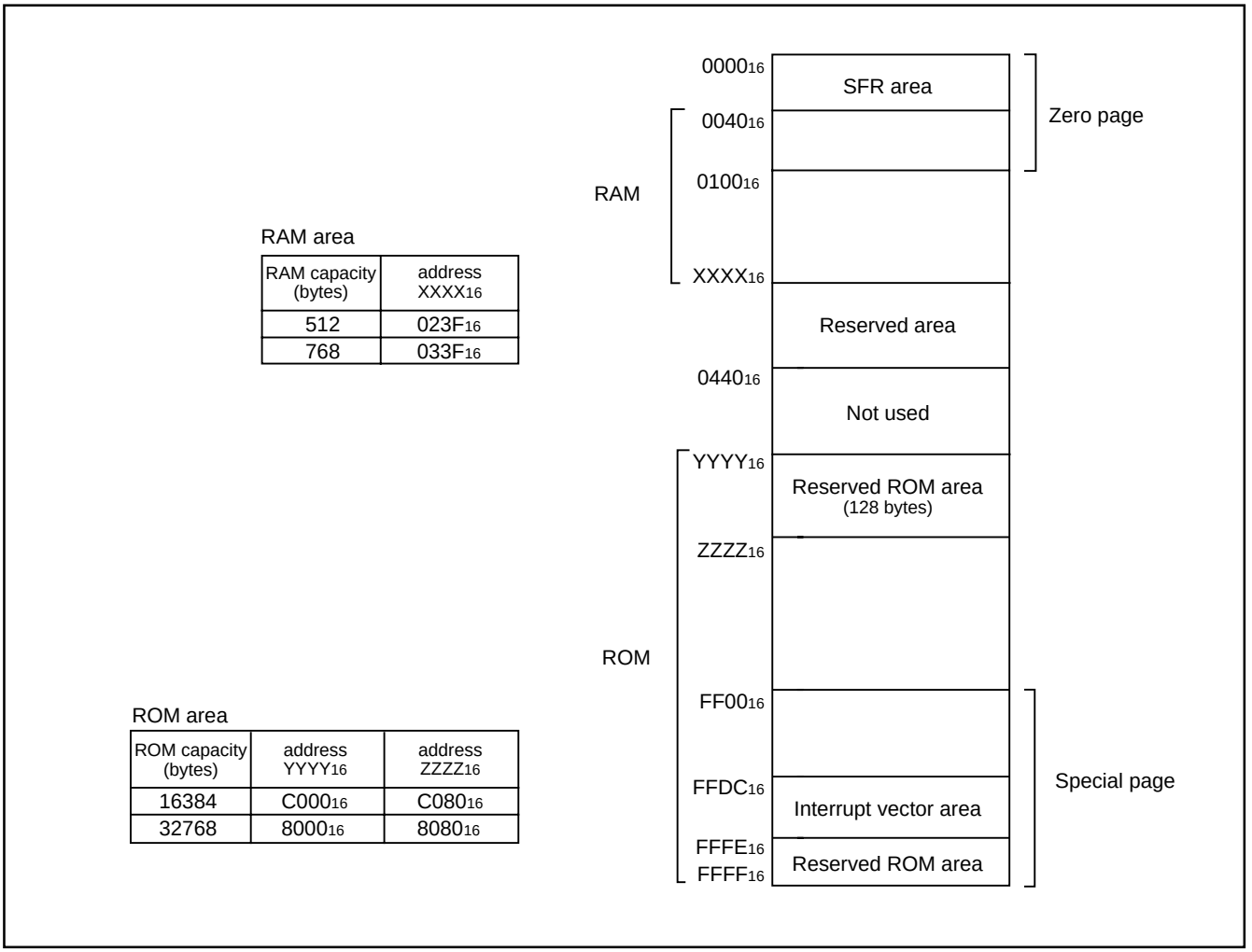
Zero page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.



RAM area

RAM capacity (bytes)	address XXXX16
512	023F16
768	033F16

ROM area

ROM capacity (bytes)	address YYYY16	address ZZZZ16
16384	C00016	C08016
32768	800016	808016

Fig. 10 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Timer Y, Z mode register (TYZM)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Prescaler Y (PREY)
0002_{16}	Port P1 (P1)	0022_{16}	Timer Y secondary (TYS)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Timer Y primary (TYP)
0004_{16}	Port P2 (P2)	0024_{16}	Timer Y, Z waveform output control register (PUM)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Prescaler Z (PREZ)
0006_{16}	Port P3 (P3)	0026_{16}	Timer Z secondary (TZS)
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Timer Z primary (TZP)
0008_{16}		0028_{16}	Prescaler 1 (PRE1)
0009_{16}		0029_{16}	Timer 1 (T1)
$000A_{16}$		$002A_{16}$	One-shot start register (ONS)
$000B_{16}$		$002B_{16}$	Timer X mode register (TXM)
$000C_{16}$		$002C_{16}$	Prescaler X (PREX)
$000D_{16}$		$002D_{16}$	Timer X (TX)
$000E_{16}$		$002E_{16}$	Timer count source set register (TCSS)
$000F_{16}$		$002F_{16}$	
0010_{16}		0030_{16}	Serial I/O2 control register (SIO2CON)
0011_{16}		0031_{16}	Serial I/O2 register (SIO2)
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	A-D control register (ADCON)
0015_{16}		0035_{16}	A-D conversion register (low-order) (ADL)
0016_{16}	Pull-up control register (PULL)	0036_{16}	A-D conversion register (high-order) (ADH)
0017_{16}	Port P1P3 control register (P1P3C)	0037_{16}	
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	MISRG
0019_{16}	Serial I/O1 status register (SIO1STS)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	Timer A mode register (TAM)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$	Timer A (low-order) (TAL)	$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	Timer A (high-order) (TAH)	$003F_{16}$	Interrupt control register 2 (ICON2)

Note : Do not access to the SFR area including nothing.

Fig. 11 Memory map of special function register (SFR)

I/O Ports

[Direction registers] PiD

The I/O ports have direction registers which determine the input/output direction of each pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input or output.

When "1" is set to the bit corresponding to a pin, this pin becomes an output port. When "0" is set to the bit, the pin becomes an input port. When data is read from a pin set to output, not the value of the pin itself but the value of port latch is read. Pins set to input are floating, and permit reading pin values.

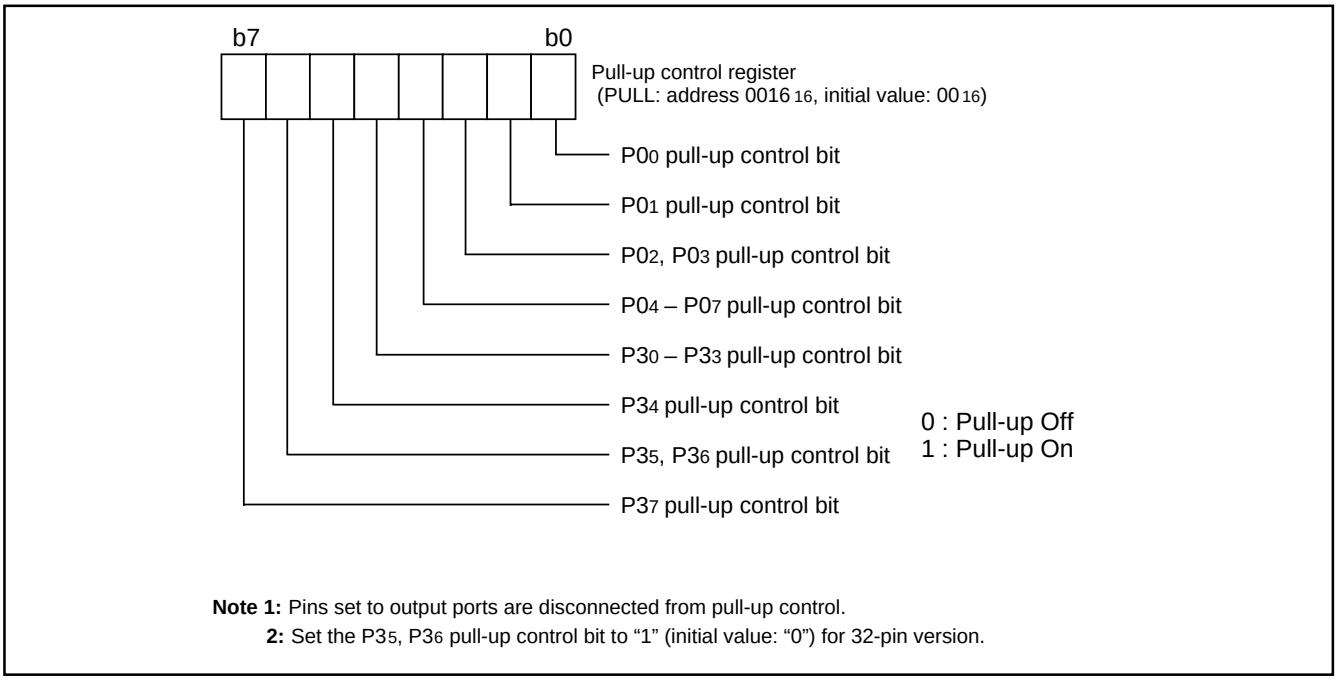
If a pin set to input is written to, only the port latch is written to and the pin remains floating.

[Pull-up control register] PULL

By setting the pull-up control register (address 0016_{16}), ports P0 and P3 can exert pull-up control by program. However, pins set to output are disconnected from this control and cannot exert pull-up control.

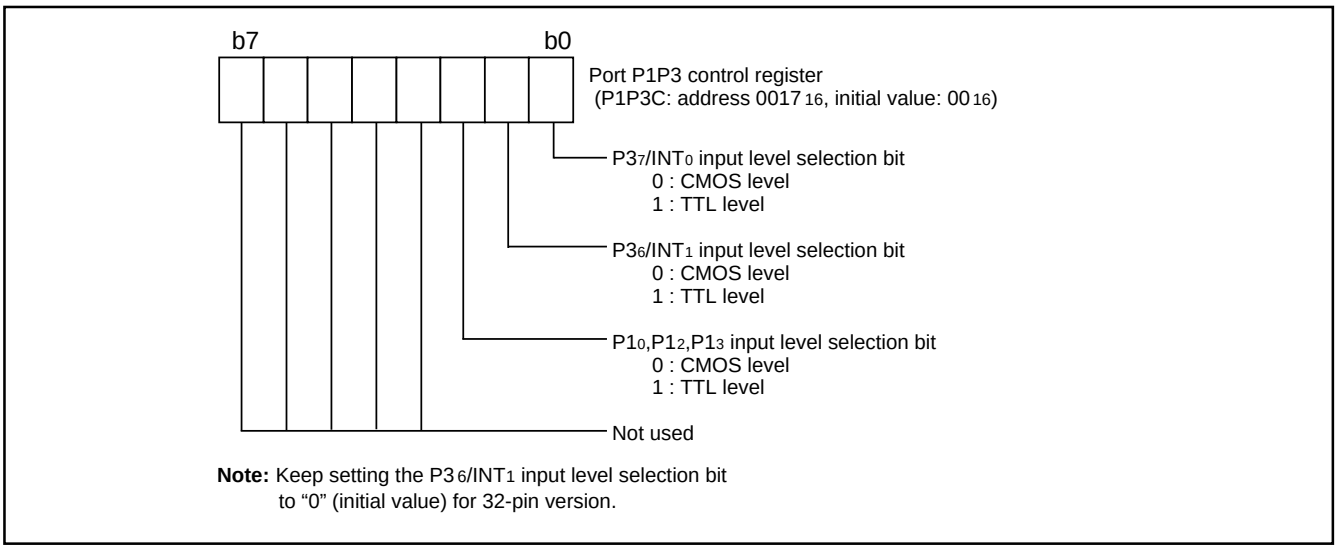
[Port P1P3 control register] P1P3C

By setting the port P1P3 control register (address 0017_{16}), a CMOS input level or a TTL input level can be selected for ports $P1_0$, $P1_2$, $P1_3$, $P3_6$, and $P3_7$ by program.



Note 1: Pins set to output ports are disconnected from pull-up control.
2: Set the $P3_5$, $P3_6$ pull-up control bit to "1" (initial value: "0") for 32-pin version.

Fig. 12 Structure of pull-up control register



Note: Keep setting the $P3_6$/INT_1 input level selection bit to "0" (initial value) for 32-pin version.

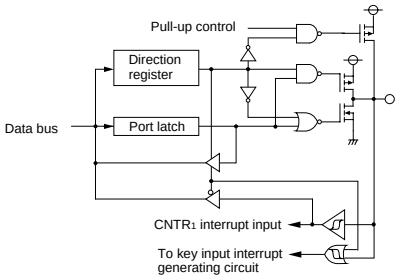
Fig. 13 Structure of port P1P3 control register

Table 3 I/O port function table

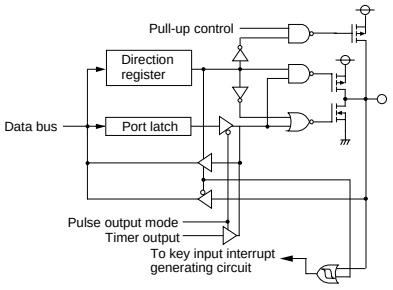
Pin	Name	Input/output	I/O format	Non-port function	Related SFRs	Diagram No.
$P0_0$/$CNTR_1$ $P0_1$/TY_{OUT} $P0_2$/TZ_{OUT} $P0_3$/TX_{OUT} $P0_4$–$P0_7$	I/O port P0	I/O individual bits	•CMOS compatible input level •CMOS 3-state output (Note)	Key input interrupt	Pull-up control register Timer Y mode register Timer Z mode register Timer X mode register Timer Y,Z waveform output control register Timer A mode register	(1) (2) (3) (4)
$P1_0$/RxD_1 $P1_1$/TxD_1	I/O port P1			Serial I/O1 function input/output	Serial I/O1 control register	(5) (6)
$P1_2$/S_{CLK1}/S_{CLK2} $P1_3$/$\overline{S_{RDY1}}$/S_{DATA2}				Serial I/O2 function input/output	Serial I/O1 control register Serial I/O2 control register	(7) (8)
$P1_4$/$CNTR_0$				Timer X function input/output	Timer X mode register	(9)
$P2_0$/AN_0–$P2_7$/AN_7	I/O port P2			A-D conversion input	A-D control register	(10)
$P3_0$–$P3_5$	I/O port P3					(11)
$P3_6$/INT_1 $P3_7$/INT_0				External interrupt input	Interrupt edge selection register	(12)

Note: Ports $P1_0$, $P1_2$, $P1_3$, $P3_6$, and $P3_7$ are CMOS/TTL level.

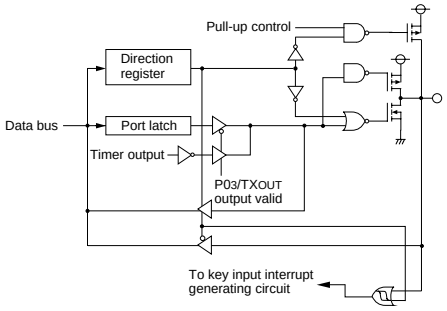
(1)Port $P0_0$



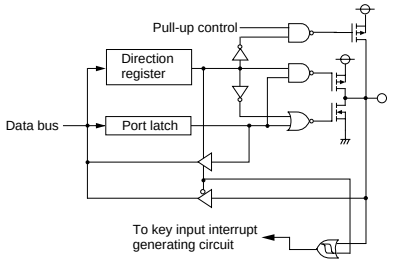
(2)Ports $P0_1$, $P0_2$



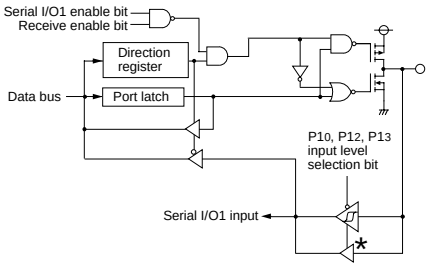
(3)Port $P0_3$



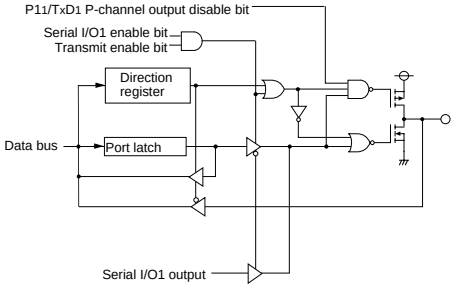
(4)Ports $P0_4$–$P0_7$



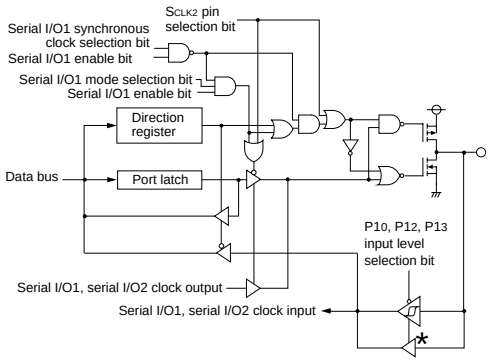
(5)Port $P1_0$



(6)Port $P1_1$



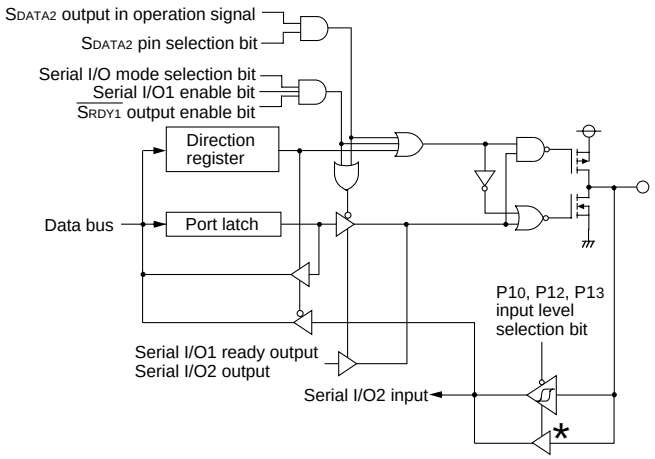
(7)Port $P1_2$



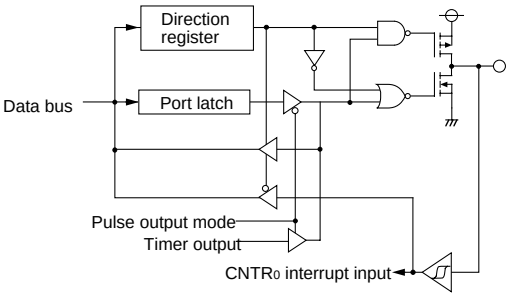
* $P1_0$, $P1_2$, $P1_3$, $P3_6$, and $P3_7$ input level are switched to the CMOS/TTL level by the port P1P3 control register.

Fig. 14 Block diagram of ports (1)

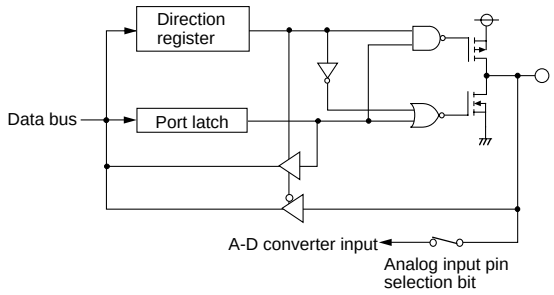
(8) Port P13



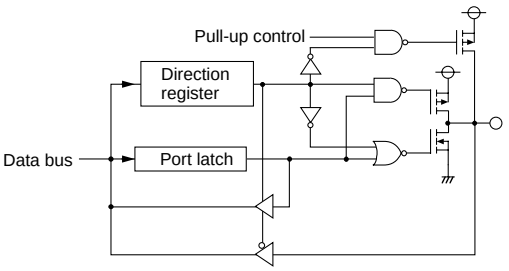
(9) Port P14



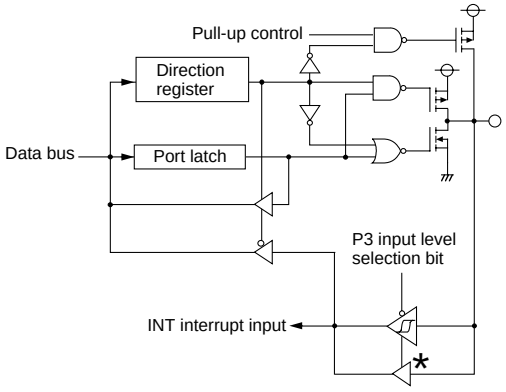
(10) Ports P20–P27



(11) Ports P30–P35



(12) Ports P36, P37



* P10, P12, P13, P36, and P37 input level are switched to the CMOS/TTL level by the port P1P3 control register.

Fig. 15 Block diagram of ports (2)

Interrupts

Interrupts occur by 15 different sources : 5 external sources, 9 internal sources and 1 software source.

Interrupt control

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit, and they are controlled by the interrupt disable flag. When the interrupt enable bit and the interrupt request bit are set to "1" and the interrupt disable flag is set to "0", an interrupt is accepted.

The interrupt request bit can be cleared by program but not be set.

The interrupt enable bit can be set and cleared by program.

The reset and BRK instruction interrupt can never be disabled with any flag or bit. All interrupts except these are disabled when the interrupt disable flag is set.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack.
3. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
4. Concurrently with the push operation, the interrupt destination address is read from the vector table into the program counter.

Notes on use

When the active edge of an external interrupt (INT_0, INT_1,$CNTR_0$) is set, the interrupt request bit may be set.

Therefore, please take following sequence:

1. Disable the external interrupt which is selected.
2. Change the active edge in interrupt edge selection register. (in case of $CNTR_0$: Timer X mode register, in case of $CNTR_1$: Timer A mode register)
3. Clear the set interrupt request bit to "0".
4. Enable the external interrupt which is selected.

Table 4 Interrupt vector address and priority

Interrupt source	Priority	Vector addresses (Note 1)		Interrupt request generating conditions	Remarks
		High-order	Low-order		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset input	Non-maskable
Serial I/O1 receive	2	$FFFB_{16}$	$FFFA_{16}$	At completion of serial I/O1 data receive	Valid only when serial I/O1 is selected
Serial I/O1 transmit	3	$FFF9_{16}$	$FFF8_{16}$	At completion of serial I/O1 transmit shift or when transmit buffer is empty	Valid only when serial I/O1 is selected
INT_0	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1 (Note 3)	5	$FFF5_{16}$	$FFF4_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Key-on wake-up	6	$FFF3_{16}$	$FFF2_{16}$	At falling of conjunction of input logical level for port P0 (at input)	External interrupt (valid at falling)
$CNTR_0$	7	$FFF1_{16}$	$FFF0_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	8	$FFEF_{16}$	$FFEE_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
Timer X	9	$FFED_{16}$	$FFEC_{16}$	At timer X underflow	
Timer Y	10	$FFEB_{16}$	$FFEA_{16}$	At timer Y underflow	
Timer Z	11	$FFE9_{16}$	$FFE8_{16}$	At timer Z underflow	
Timer A	12	$FFE7_{16}$	$FFE6_{16}$	At timer A underflow	
Serial I/O2	13	$FFE5_{16}$	$FFE4_{16}$	At completion of transmit/receive shift	
A-D conversion	14	$FFE3_{16}$	$FFE2_{16}$	At completion of A-D conversion	
Timer 1	15	$FFE1_{16}$	$FFE0_{16}$	At timer 1 underflow	STP release timer underflow
Reserved area	16	$FFDF_{16}$	$FFDE_{16}$	Not available	
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Note 1: Vector addressed contain internal jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

3: It is an interrupt which can use only for 36 pin version.

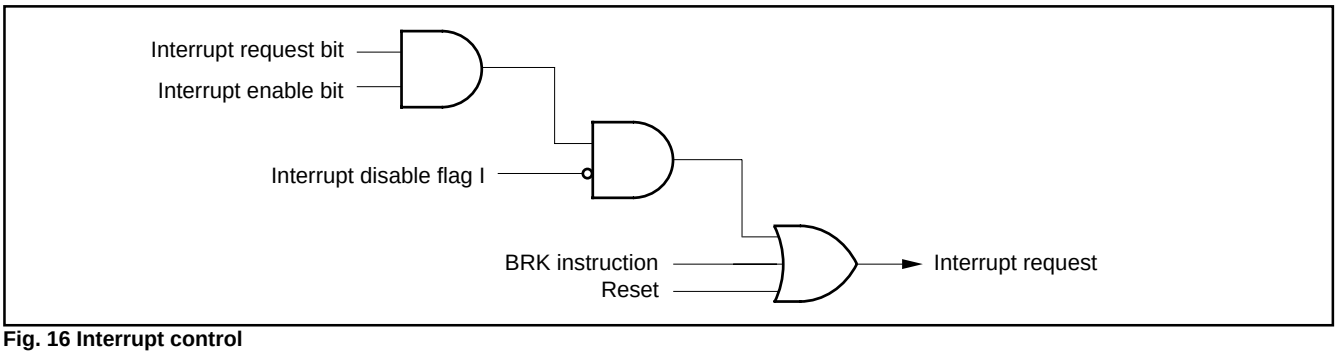


Fig. 16 Interrupt control

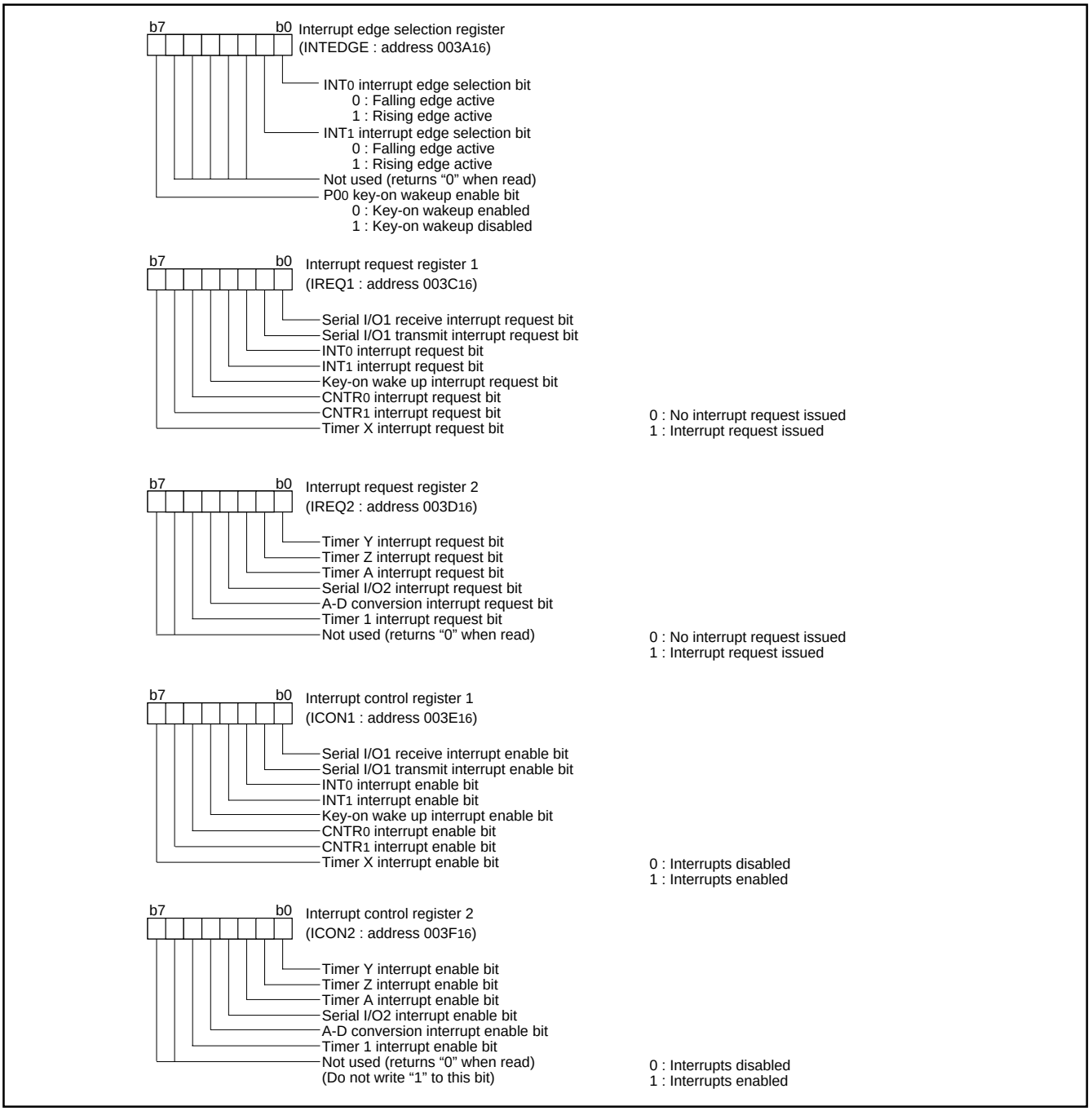


Fig. 17 Structure of Interrupt-related registers

Key Input Interrupt (Key-On Wake-Up)

A key-on wake-up interrupt request is generated by applying “L” level to any pin of port P0 that has been set to input mode.
In other words, it is generated when the AND of input level goes from “1” to “0”. An example of using a key input interrupt is shown in Figure 18, where an interrupt request is generated by pressing one of the keys provided as an active-low key matrix which uses ports P0$_0$ to P0$_3$ as input ports.

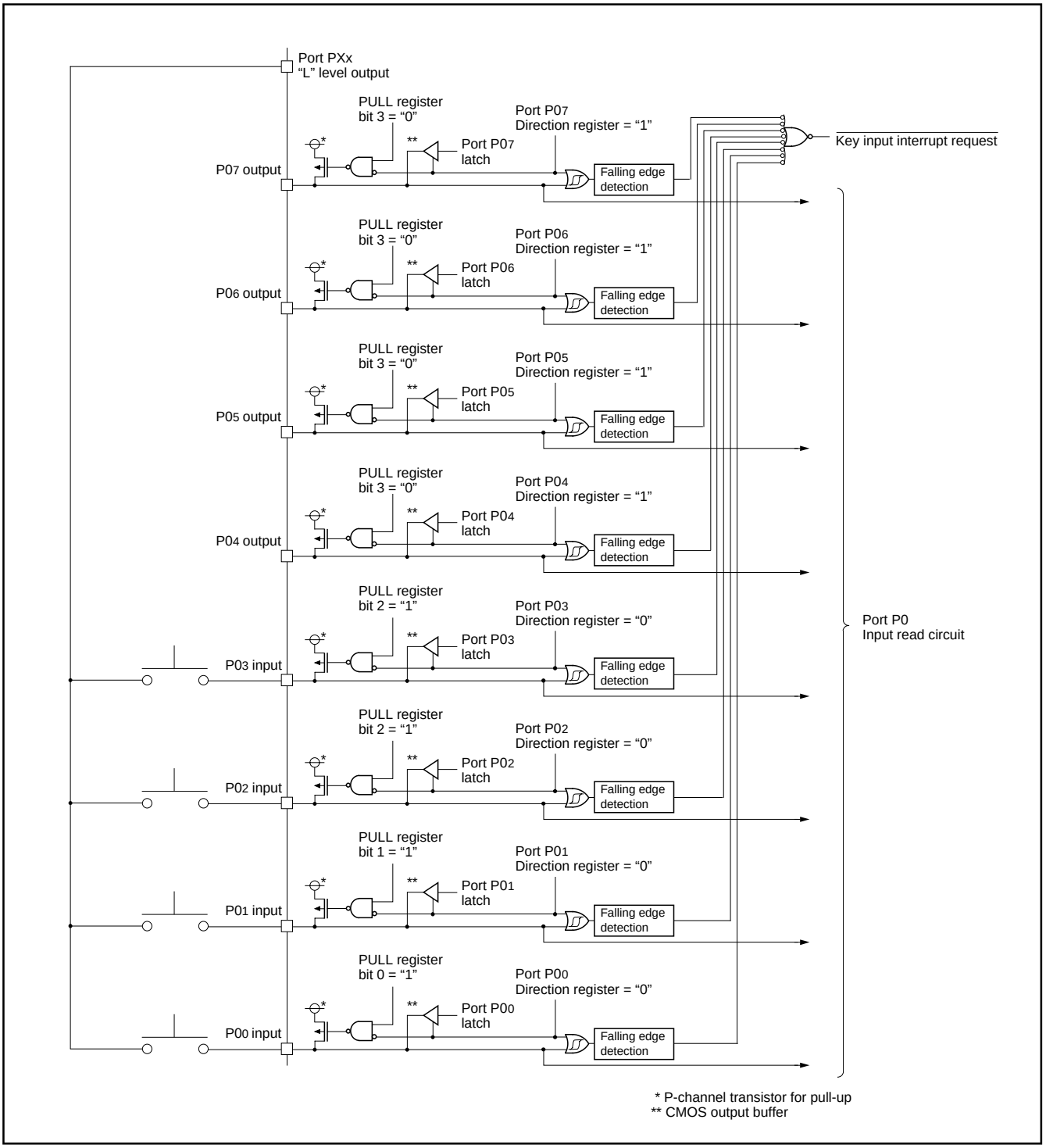


Fig. 18 Connection example when using key input interrupt and port P0 block diagram

Timers

The 7540 Group has 5 timers: timer 1, timer A, timer X, timer Y and timer Z.

The division ratio of every timer and prescaler is 1/(n+1) provided that the value of the timer latch or prescaler is n.

All the timers are down count timers. When a timer reaches "0", an underflow occurs at the next count pulse, and the corresponding timer latch is reloaded into the timer. When a timer underflows, the interrupt request bit corresponding to each timer is set to "1".

●Timer 1

Prescaler 1 always counts f(X_{IN})/16. Timer 1 always counts the prescaler 1 output and periodically sets the interrupt request bit.

●Timer A

Timer A is a 16-bit timer that can be selected in one of four modes.

• Timer Mode

The timer counts f(X_{IN})/16.

• Period Measurement Mode

$CNTR_1$ interrupt request is generated at rising/falling edge of $CNTR_1$ pin input signal. Simultaneously, the value in timer A latch is reloaded in timer A and timer A continues counting down. Except for the above-mentioned, the operation in period measurement mode is the same as in timer mode.

The timer value just before the reloading at rising/falling of $CNTR_1$ pin input signal is retained until the timer A is read once after the reload.

The rising/falling timing of $CNTR_1$ pin input signal is found by $CNTR_1$ interrupt.

• Event Counter Mode

The timer counts signals input through the $CNTR_1$ pin.

Except for this, the operation in event counter mode is the same as in timer mode.

• Pulse Width HL Continuously Measure-ment Mode

$CNTR_1$ interrupt request is generated at both rising and falling edges of $CNTR_1$ pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode.

■ **Note**

● **$CNTR_1$ interrupt active edge selection**

$CNTR_1$ interrupt active edge depends on the $CNTR_1$ active edge switch bit. However, in pulse width HL continuously measurement mode, $CNTR_1$ interrupt request is generated at both rising and falling edges of $CNTR_1$ pin input signal regardless of the setting of $CNTR_1$ active edge switch bit.

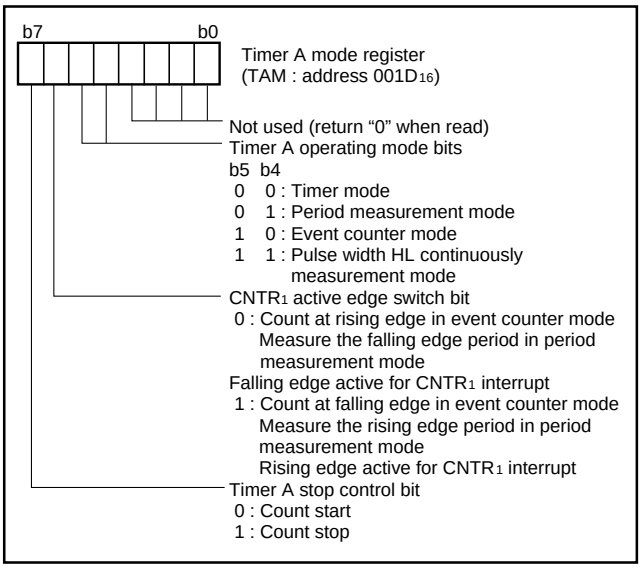


Fig. 19 Structure of timer A mode register

●Timer X

Timer X can be selected in one of 4 operating modes by setting the timer X mode register.

• Timer Mode

The timer counts the signal selected by the timer X count source selection bits.

• Pulse Output Mode

The timer counts the signal selected by the timer X count source selection bits, and outputs a signal whose polarity is inverted each time the timer value reaches "0", from the $CNTR_0$ pin.

When the $CNTR_0$ active edge switch bit is "0", the output of the $CNTR_0$ pin is started with an "H" output. At "1", this output is started with an "L" output. When using a timer in this mode, set the port $P1_4$ direction register to output mode. Also, in the pulse output mode, the inverted waveform of pulse output from $CNTR_0$ pin can be output from TX_{OUT} pin by setting the $P0_3/TX_{OUT}$ output valid bit to "1" . When using a timer in this mode, set the port $P0_3$ direction register to output mode.

• Event Counter Mode

The operation in the event counter mode is the same as that in the timer mode except that the timer counts the input signal from the $CNTR_0$ pin.

When the $CNTR_0$ active edge switch bit is "0", the timer counts the rising edge of the $CNTR_0$ pin. When this bit is "1", the timer counts the falling edge of the $CNTR_0$ pin.

• Pulse Width Measurement Mode

When the $CNTR_0$ active edge switch bit is "0", the timer counts the signal selected by the timer X count source selection bit while the $CNTR_0$ pin is "H". When this bit is "1", the timer counts the signal while the $CNTR_0$ pin is "L".

In any mode, the timer count can be stopped by setting the timer X count stop bit to "1". Each time the timer overflows, the interrupt request bit is set.

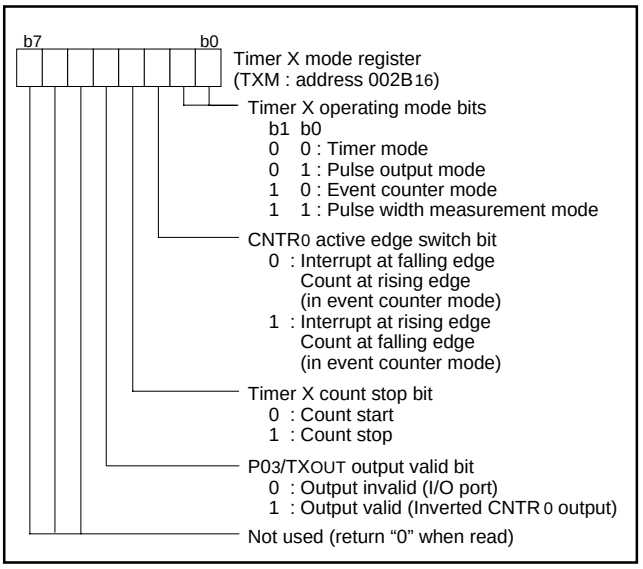


Fig. 20 Structure of timer X mode register

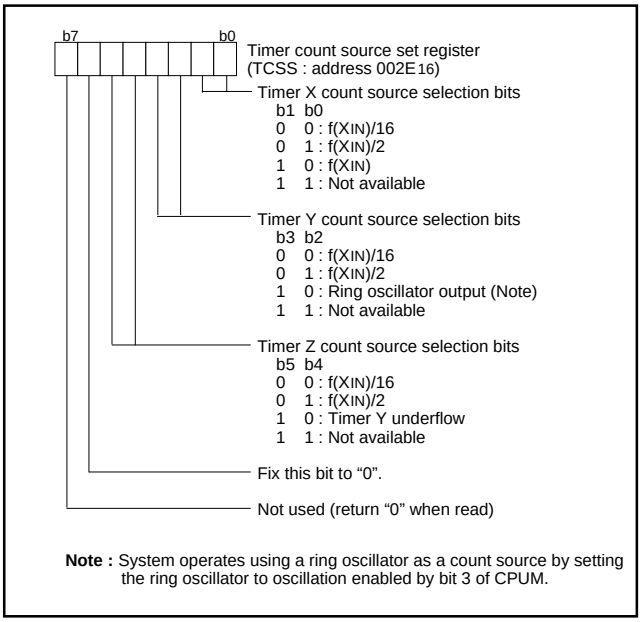


Fig. 21 Timer count source set register

●Timer Y

Timer Y is an 8-bit timer and can be selected in one of 2 operating modes by setting the timer Y, Z mode register (TYZM).

- Timer mode
- Programmable waveform generation mode

The division ratio of timer Y and prescaler Y is 1/(n+1) provided that the value of the timer latch or prescaler Y latch is n.

(1)Timer mode

- Mode select
  Timer mode is selected by setting timer Y operation mode bit (b0) of TYZM to "0".
- Count source select
  The count source is f(XIN)/2 or f(XIN)/16.
- Interrupt
  When an underflow occurs, timer Y interrupt request bit (b0) of IREQ2 is set to "1".
- Operation description
  After reset release, timer Y is operating because the timer Y count stop bit (b3) of TYZM is "0". Timer operation is stopped by setting b3 of TYZM to "1". In the timer mode, the timer count value is set by timer Y primary latch (TYP). When a value is set to TYP while timer is stopped, the setting value is written to latch and timer simultaneously.
  When timer Y reaches "00", an underflow occurs at the next count pulse, and the timer Y latch is reloaded into the timer and count continues. When timer value is changed during the count operation, either "writing to latch and timer simultaneously" or "writing to only latch" can be selected by setting the timer Y write control bit (b2) of TYZM. When selecting "writing to only latch", the timer count value is changed after the next underflow.

(2)Programmable waveform generation mode

- Mode select
  Timer mode is selected by setting timer Y operation mode bit (b0) of TYZM to "1".
  When this mode is selected, set timer Y write control bit (b2) of TYZM to "1" ("writing to only latch" selected).
- Count source select
  The count source is f(XIN)/2 or f(XIN)/16.
- Interrupt
  When an underflow occurs, timer Y interrupt request bit (b0) of IREQ is set to "1".
- Operation description
  After reset release, timer Y is operating because the timer Y count stop bit (b3) of TYZM is "0". MCU operates in the programmable waveform generation mode when timer Y operation mode bit (b0) of TYZM is set to "1" and b3 to "0" after timer Y operation is stopped by setting b3 of TYZM to "1".
  In the programmable waveform generation mode, timer counts the setting value of timer Y primary latch (TYP) and the setting value of timer Y secondary latch (TYS) alternately, the waveform inverted each time TYP and TYS underflow is output from TYOUT pin. The active edge of output waveform is set by the timer Y output level latch (b4) of the timer Y, Z waveform output control register (PUM). When "0" is set to b4 of PUM, the initial state of timer at stop is "L", and "H" interval by the setting value of TYP or "L" interval by the setting value of TYS is output alternately. When "1" is set to b4 of PUM, the initial state of timer at stop is "H", and "L" interval by the setting value of TYP or "H" interval by the setting value of TYS is output alternately.
  Also, in this mode, the primary interval and the secondary interval of the output waveform can be extended respectively for 0.5 cycle of timer count source clock by setting the timer Y primary waveform extension control bit (b0) and the timer Y secondary waveform extension control bit (b1) of PUM to "1". As a result, the waveforms of more accurate resolution can be output.
  When b0 and b1 of PUM are used, the frequency and duty of the output waveform are as follows;

Waveform frequency:

$$FTYOUT = (2 \times TMCL)/(2 \times (TYP+1) + 2 \times (TYS) + (EXPYP + EXPYS))$$

Duty:

$$DTYOUT = (2 \times (TYP + 1)) + EXPYP)/(2 \times (TYS + 1) + EXPYS))$$

TMCL: Timer Y count clock f(XIN)/2 or f(XIN)/16
TYP: Timer Y primary latch (8 bits)
TYS: Timer Y secondary latch (8 bits)
EXPYP: Timer Y primary waveform extension control bit (1 bit)
EXPYS: Timer Y secondary waveform extension control bit (1 bit)

When using the programmable waveform generation mode, note the following;

Notes on using the programmable waveform generation mode

- When setting and changing TYP, TYS, EXPYP and EXPYS, write to TYP at last because the setting to them is executed all at once by writing to TYP. Even when TYP is not changed, write the same value. The value is reloaded to timer at the beginning of the next primary interval.
- Set by software in order not to execute the writing to timer Y primary and the timing of timer underflow simultaneously. When reading the timer Y secondary, the undefined value is read out. However, while timer counts the setting value of the timer Y secondary, the count values at the secondary interval can be identified by reading the timer Y primary.
- In this mode, set port $P0_1$ which is also used as TYOUT pin to output.
- B0 and b1 of PUM can be used only when "00_{16}" is set to prescaler Y.

●Timer Z

Timer Z is an 8-bit timer and can be selected in one of 4 operating modes by setting the timer YZ mode register (TYZM).

- Timer mode
- Programmable waveform generation mode
- Programmable one-shot generation mode
- Programmable wait one-shot generation mode

The division ratio of timer Z and prescaler Z is 1/(n+1) provided that the value of the timer Z latch or prescaler Z latch is n.

(1)Timer mode

- Mode select
  Timer mode is selected by setting timer Z operation mode bits (b5,b4) of TYZM to “00”.
- Count source select
  The count source is f(XIN)/2, f(XIN)/16 or timer Y underflow.
- Interrupt
  When an underflow occurs, timer Z interrupt request bit (b1) of IREQ2 is set to “1”.
- Operation description
  After reset release, timer Z is operating because the timer Z count stop bit (b7) is “0”. Timer operation is stopped by setting b7 of TYZM to “1”. In the timer mode, the timer count value is set by timer Z primary latch (TZP). When a value is set to TZP while timer is stopped, the setting value is written to latch and timer simultaneously.
  When timer Z reaches “00”, an underflow occurs at the next count pulse, and the timer Z latch is reloaded into the timer and count continues. When timer value is changed during the count operation, either “writing to latch and timer simultaneously” or “writing to only latch” can be selected by setting the timer Z write control bit (b6) of TYZM. When selecting “writing to only latch”, the timer count value is changed after the next underflow.

(2)Programmable waveform generation mode

- Mode select
  Timer mode is selected by setting timer Z operation mode bits (b5,b4) of TYZM to “01”.
  When this mode is selected, set timer Z write control bit (b6) of TYZM to “1” (“writing to only latch” selected).
- Count source select
  The count source is f(XIN)/2, f(XIN)/16 or timer Y underflow.
- Interrupt
  When an underflow occurs, timer Z interrupt request bit (b1) of IREQ is set to “1”.
- Operation description
  After reset release, timer Z is operating because the timer Z count stop bit (b7) of TYZM is “0”. MCU operates in the programmable waveform generation mode when timer Z operation mode bits (b5, b4) of TYZM is set to “01” and b7 to “0” after timer Z operation is stopped by setting b7 of TYZM to “1”.

  In the programmable waveform generation mode, timer counts the setting value of timer Z primary latch (TZP) and the setting value of timer Z secondary latch (TZS) alternately, the waveform inverted each time TZP and TZS underflow is output from TZOUT pin. The active edge of output waveform is set by the timer Z output level latch (b5) of the timer Y, Z waveform output control register (PUM). When “0” is set to b5 of PUM, the initial state of timer at stop is “L”, and “H” interval by the setting value of TZP or “L” interval by the setting value of TZS is output alternately. When “1” is set to b5 of PUM, the initial state of timer at stop is “H”, and “L” interval by the setting value of TZP or “H” interval by the setting value of TZS is output alternately.
  Also, in this mode, the primary interval and the secondary interval of the output waveform can be extended respectively for 0.5 cycle of timer count source clock by setting the timer Z primary waveform extension control bit (b2) and the timer Z secondary waveform extension control bit (b3) of PUM to “1”. As a result, the waveforms of more accurate resolution can be output.
  When b2 and b3 of PUM are used, the frequency and duty of the output waveform are as follows;

Waveform frequency:

$FTZOUT = (2 \times TMCL)/(2 \times (TZP + 1)+2 \times (TZS) + (EXPZP + EXPZS))$

Duty:

$DTZOUT = (2 \times (TZP + 1)) + EXPZP)/(2 \times (TZS+1) + EXPZS))$

TMCL: Timer Z count clock f(XIN)/2 or f(XIN)/16
TZP: Timer Z primary latch (8 bits)
TZS: Timer Z secondary latch (8 bits)
EXPZP: Timer Z primary waveform extension control bit (1 bit)
EXPZS: Timer Z secondary waveform extension control bit (1 bit)

When using the programmable waveform generation mode, note the following;

Notes on using the programmable waveform generation mode

- When setting and changing TZP, TZS, EXPZP and EXPZS, write to TZP at last because the setting to them is executed all at once by writing to TZP. Even when TZP is not changed, write the same value. The value is reloaded to timer at the beginning of the next primary interval.
- Set by software in order not to execute the writing to timer Z primary and the timing of timer underflow simultaneously. When reading the timer Z secondary, the undefined value is read out. However, while timer counts the setting value of the timer Z secondary, the count values at the secondary interval can be identified by reading the timer Z primary.
- In this mode, set port P02 which is also used as TZOUT pin to output.
- B2 and b3 of PUM can be used only when “0016” is set to prescaler Z and f(XIN)/2 or f(XIN)/16 is selected as the timer Z count source.

(3)Programmable one-shot generation mode

- Mode select
  Timer mode is selected by setting timer Z operation mode bits (b5,b4) of TYZM to "10".
  When this mode is selected, set timer Z write control bit (b6) of TYZM to "1" ("writing to only latch" selected).
- Count source select
  The count source is f(XIN)/2, f(XIN)/16 or timer Y underflow.
- Interrupt
  When an underflow occurs, timer Z interrupt request bit (b1) of IREQ2 is set to "1".
- Operation description
  After reset release, timer Z is operating because the timer Z count stop bit (b7) of TYZM is "0". MCU operates in the programmable one-shot generation mode when timer Z operation mode bits (b5, b4) of TYZM is set to "10" after timer Z operation is stopped by setting b7 of TYZM to "1".
  Timer Z is enabled to accept the one-shot start trigger when "0" is written to b7 of TYZM after the timer count value is set to the timer Z primary latch (TZP). In this state, when "1" is written to the timer Z one-shot start bit (b0) of the one-shot start register (ONS), timer Z starts count operation, at the same time, the output of TZOUT pin is inverted. Timer Z counts down the value of TZP and stops after the output of TZOUT pin is inverted to the same level as the initial state when an underflow occurs. In this time, the next one-shot pulse can be output by writing b0 of ONS to "1" because this bit is initialized to "0".
  The active edge of the output waveform from TZOUT pin is set by the timer Z output level latch (b5) of PUM. When "0" is set to b5 of PUM, the initial level of timer at stop is "L" and "H" is output at the same time when timer starts. "H" is output in the count interval of TZP, and the output is inverted to "L" and stopped when an underflow occurs.
  Also, when "1" is set to b5 of PUM, the initial level of timer at stop is "H" and "L" is output at the same time when timer starts. "L" is output in the count interval of TZP, and the output is inverted to "H" and stopped when an underflow occurs.
  When the INT0 pin one-shot trigger control bit (b6) of PUM is set to "1", the one-shot pulse can be output by using the input of INT0 pin as a trigger. The active edge of the pulse input to INT0 pin as the trigger can be selected by the INT0 pin one-shot trigger active edge selection bit (b7) of PUM. The trigger is accepted and the one-shot pulse is generated by the falling edge of INT0 pin input when "0" is set to b7 of PUM or the rising edge of INT0 pin input when "1" is set to the b7 of PUM.
  Also, the INT0 interrupt occurs when the trigger is input from the INT0 pin by setting the INT0 interrupt edge selection bit (b0) of the interrupt edge selection register (INTEDGE) and the INT0 interrupt enable bit (b2) of the interrupt control register 1 (ICON1). Even when the trigger by the INT0 pin input is selected, the one-shot pulse can be output by writing to b0 of ONS.
  Also, in this mode, the waveform output interval of the one-shot pulse can be extended for 0.5 cycle of timer count source clock by setting the timer Z primary waveform extension control bit (b2) to "1". As a result, the waveforms of more accurate resolution can be output.

When using the programmable one-shot generation mode, note the following;

Notes on using the programmable one-shot generation mode

- When setting and changing TZP and EXPZS, write to TZP at last because the setting to them is executed all at once by writing to TZP. Even when TZP is not changed, write the same value. The value is reloaded to timer at the beginning of the next primary interval.
- Set by software in order not to execute the writing to timer Z primary and the timing of timer underflow simultaneously. When reading the timer Z secondary, the undefined value is read out. However, while timer counts the setting value of the timer Z secondary, the count values at the secondary interval can be identified by reading the timer Z primary.
- In this mode, set port P02 which is also used as TZOUT pin to output.
- B2 of PUM can be used only when "0016" is set to prescaler Z and f(XIN)/2 or f(XIN)/16 is selected as the timer Z count source.

(4)Programmable wait one-shot generation mode

- Mode select
  Timer mode is selected by setting timer Z operation mode bits (b5,b4) of TYZM to "11".
  When this mode is selected, set timer Z write control bit (b6) of TYZM to "1" ("writing to only latch" selected).
- Count source select
  The count source is f(XIN)/2, f(XIN)/16 or timer Y underflow.
- Interrupt
  When an underflow occurs, timer Z interrupt request bit (b1) of IREQ is set to "1".
- Operation description
  After reset release, timer Z is operating because the timer Z count stop bit (b7) of TYZM is "0". MCU operates in the programmable wait one-shot generation mode when timer Z operation mode bits (b5, b4) of TYZM is set to "11" after timer Z operation is stopped by setting b7 of TYZM to "1".
  Timer Z is enabled to accept the one-shot start trigger when "0" is written to b7 of TYZM after the timer count values are set to the timer Z primary latch (TZP) and the timer Z secondary latch (TZS). In this state, when "1" is written to the timer Z one-shot start bit (b0) of ONS, timer Z starts count operation. Unlike the programmable one-shot generation mode, the output of TZOUT pin is not changed until the timer counts TZP and an underflow occurs.
  When the timer Z counts TZP and an underflow occurs, TZS is reloaded to timer, at the same time, the output of the TZOUT pin is inverted.
  Timer Z counts down the value of TZP and stops after the output of TZOUT pin is inverted to the same level as the initial state when an underflow occurs. In this time, the next one-shot pulse can be output by writing b0 of ONS to "1" because this bit is initialized to "0".
  The active edge of the output waveform from TZOUT pin is set by the timer Z output level latch (b5) of PUM. When "0" is set to b5 of PUM, the initial level of timer at stop and the TZP count interval are "L" and inverted to "H" at the same time when an underflow occurs. "H" is output in the count interval of TZS, and the output is inverted to "L" and stopped when an underflow occurs.
  Also, when "1" is set to b5 of PUM, the initial level of timer at stop and the TZP count interval are "H" and inverted to "L" at the same time when an underflow occurs. "L" is output in the count interval of TZS, and the output is inverted to "H" and stopped when an underflow occurs.
  When the INT0 pin one-shot trigger control bit (b6) of PUM is set to "1", the one-shot pulse can be output by using the input of INT0 pin as a trigger. The active edge of the pulse input to INT0 pin as the trigger can be selected by the INT0 pin one-shot trigger active edge selection bit (b7) of PUM. The trigger is accepted and the one-shot pulse is generated by the falling edge of INT0 pin input when "0" is set to b7 of PUM or the rising edge of INT0 pin input when "1" is set to the b7 of PUM.
  Also, the INT0 interrupt occurs when the trigger is input from the INT0 pin by setting the INT0 interrupt edge selection bit (b0) of the interrupt edge selection register (INTEDGE) and the INT0 interrupt enable bit (b2) of the interrupt control register 1 (ICON1). Even when the trigger by the INT0 pin input is selected, the one-shot pulse can be output by writing to b0 of ONS.
  Also, in this mode, the waveform output interval of the one-shot pulse can be extended for 0.5 cycle of timer count source clock by setting the timer Z primary waveform extension control bit (b2) to "1". As a result, the waveforms of more accurate resolution can be output.

  When using the programmable wait one-shot generation mode, note the following;

Notes on using the programmable wait one-shot generation mode

- When setting and changing TZP, TZS, EXPZP and EXPZS, write to TZP at last because the setting to them is executed all at once by writing to TZP. Even when TZP is not changed, write the same value. The value is reloaded to timer at the beginning of the next primary interval.
- Set by software in order not to execute the writing to timer Z primary and the timing of timer underflow simultaneously. When reading the timer Z secondary, the undefined value is read out. However, while timer counts the setting value of the timer Z secondary, the count values at the secondary interval can be identified by reading the timer Z primary.
- In this mode, set port P02 which is also used as TZOUT pin to output.
- B2 of PUM can be used only when "0016" is set to prescaler Z and f(XIN)/2 or f(XIN)/16 is selected as the timer Z count source.

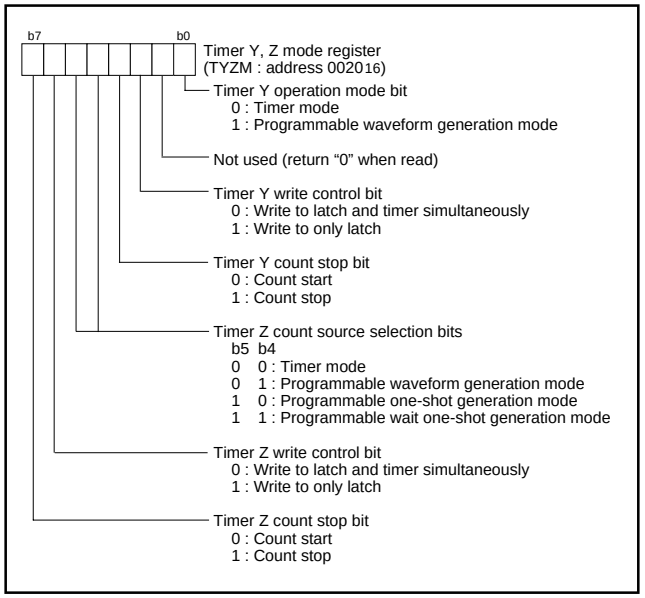


Fig. 22 Structure of timer Y, Z mode register

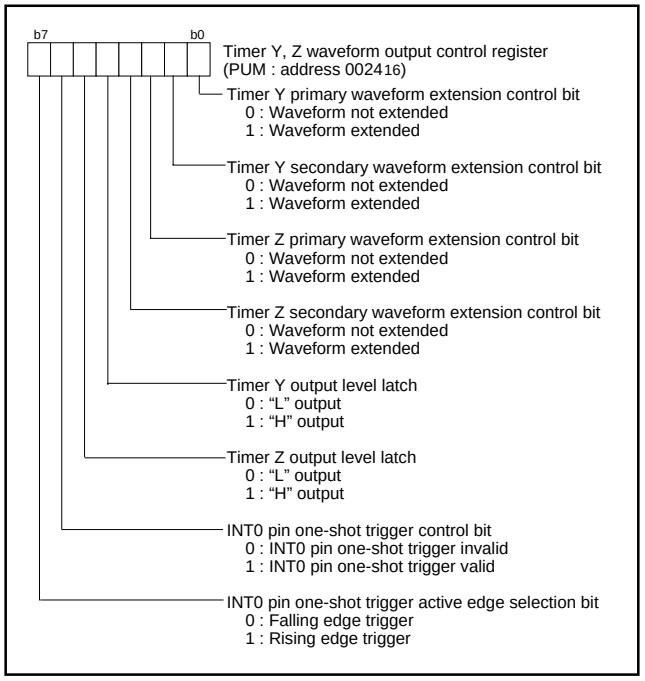


Fig. 23 Structure of timer YZ waveform output control register

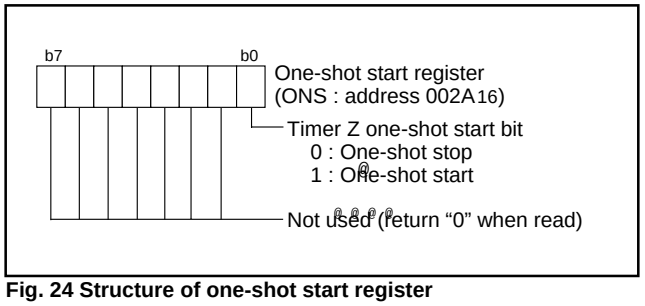


Fig. 24 Structure of one-shot start register

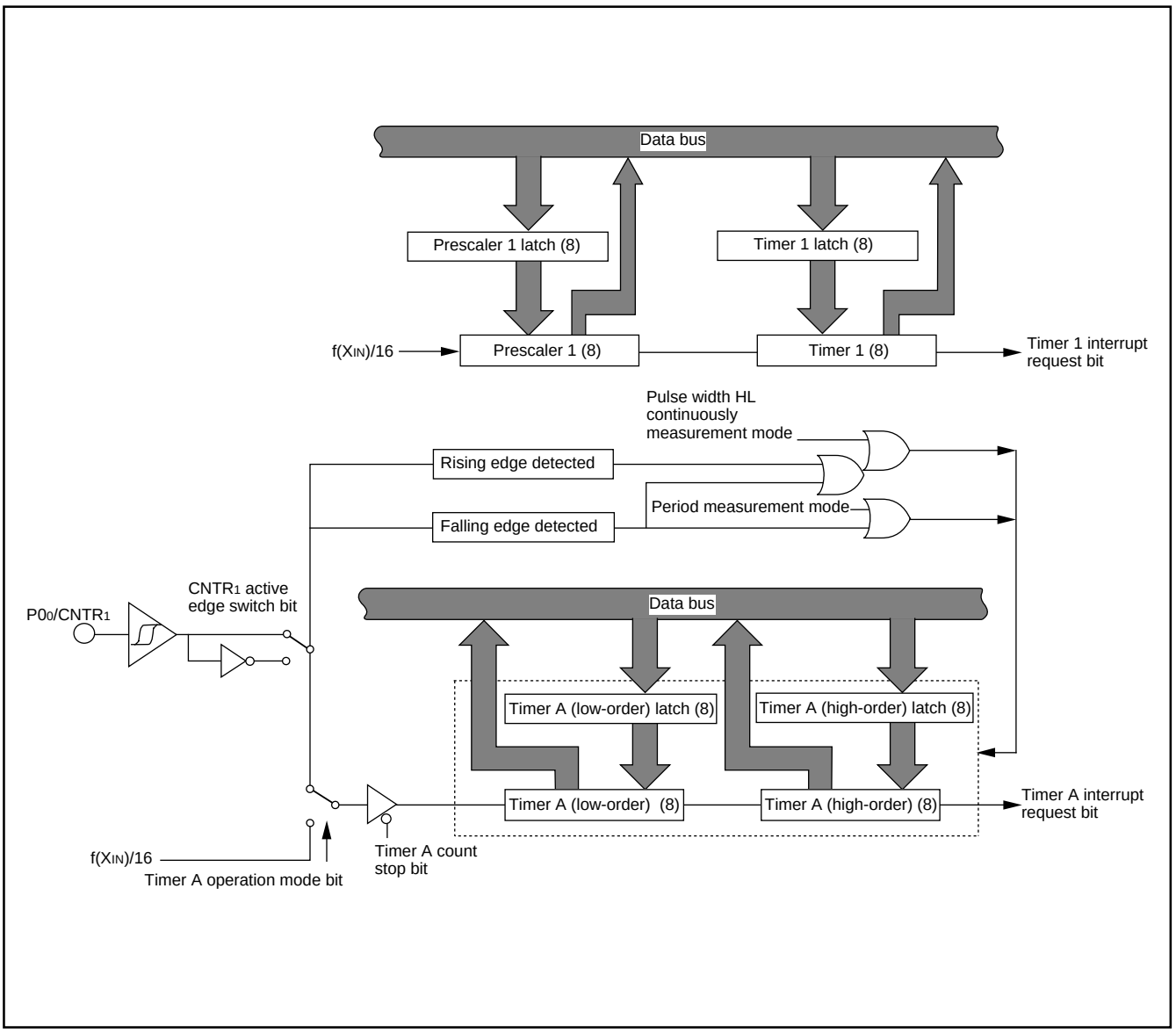


Fig. 25 Block diagram of timer 1 and timer A

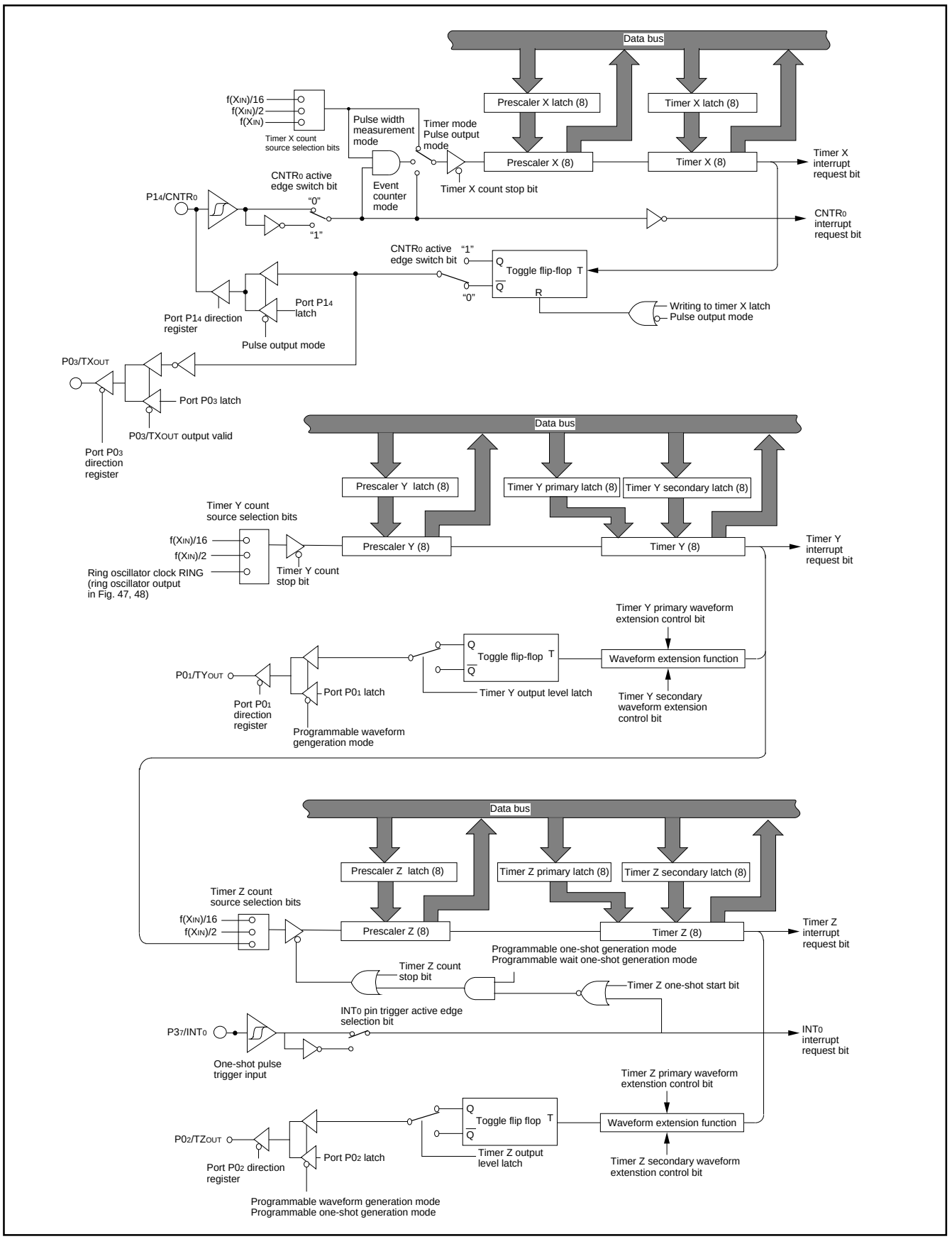


Fig. 26 Block diagram of timer X, timer Y and timer Z

Serial I/O

●Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6) to "1".

For clock synchronous serial I/O 1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

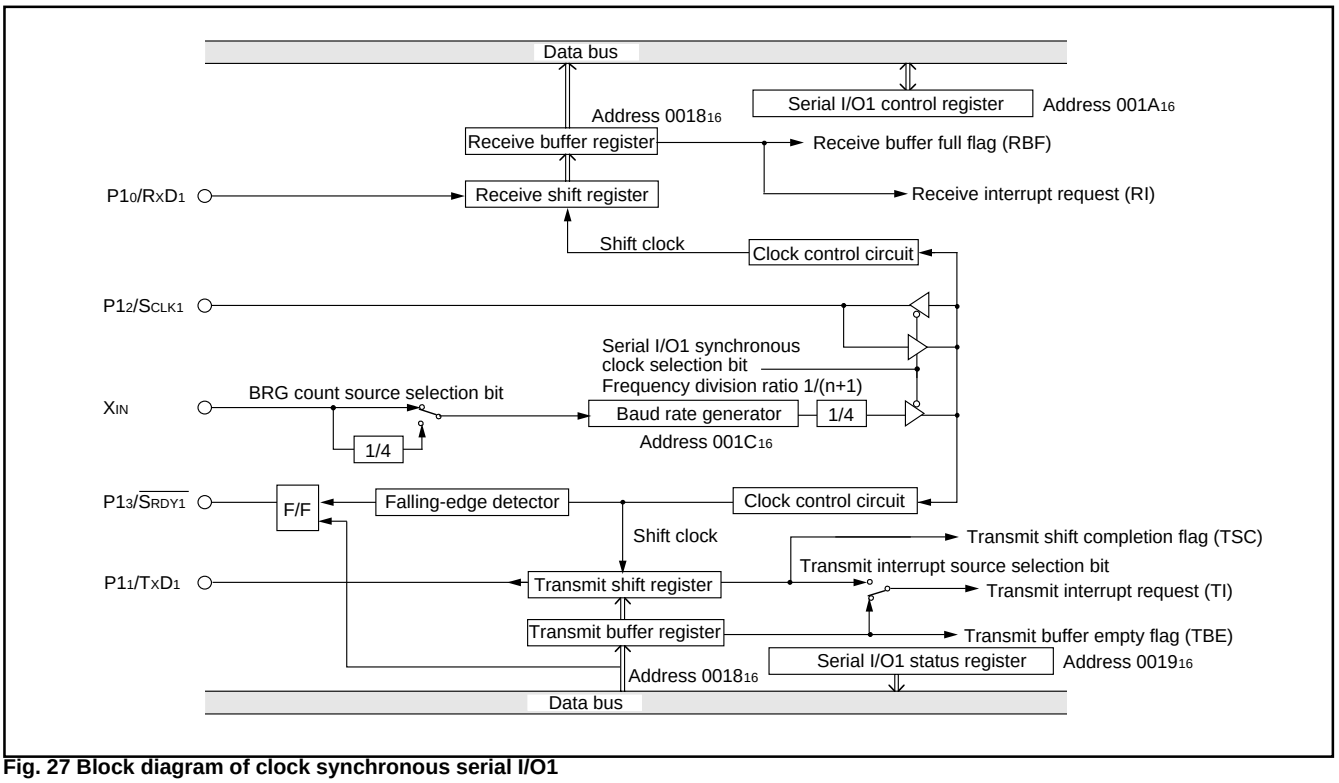
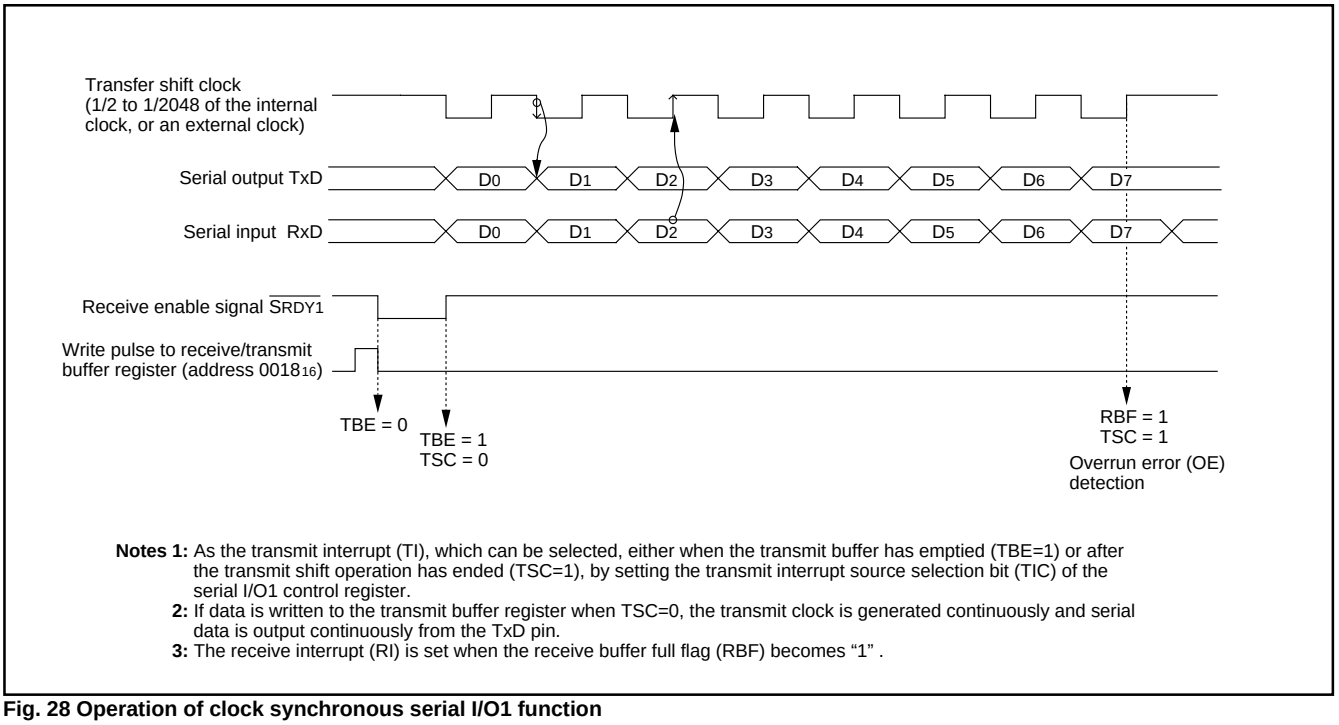


Fig. 27 Block diagram of clock synchronous serial I/O1



Notes 1: As the transmit interrupt (TI), which can be selected, either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig. 28 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit of the serial I/O1 control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

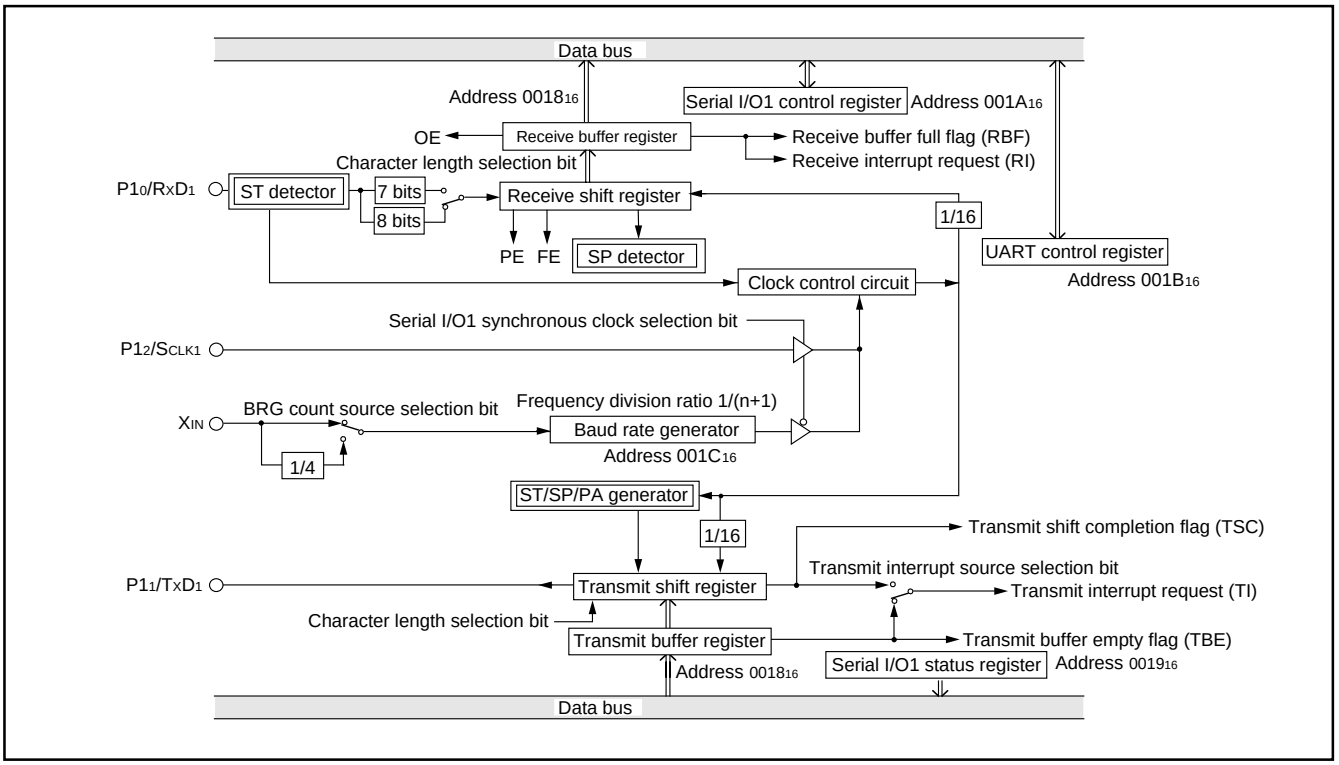
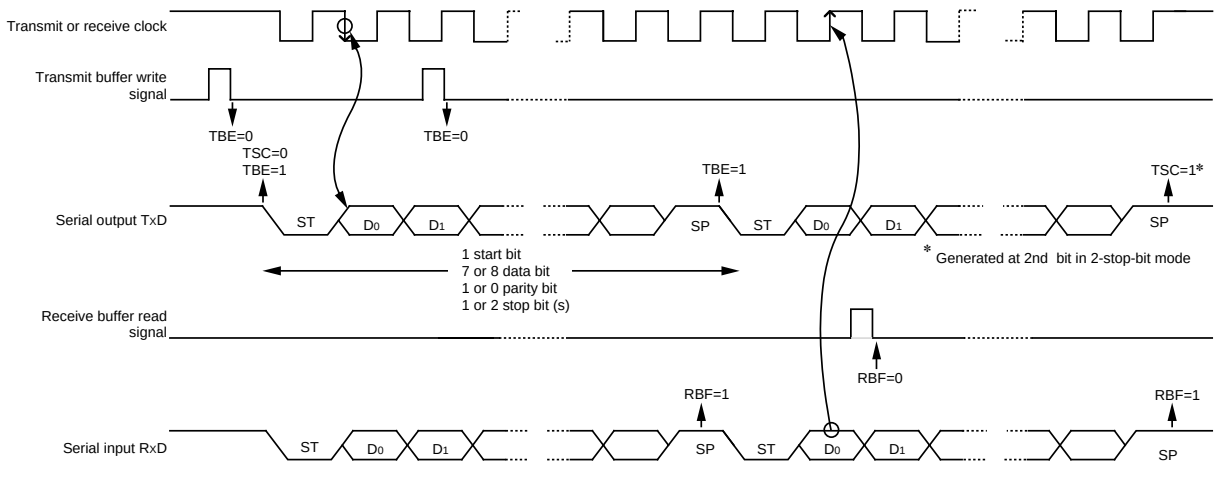


Fig. 29 Block diagram of UART serial I/O1



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes "1," can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes "1."
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 30 Operation of UART serial I/O1 function

[Transmit buffer register/receive buffer register (TB/RB)] 0018_{16}
The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O1 status register (SIO1STS)] 0019_{16}
The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.
Three of the flags (bits 4 to 6) are valid only in UART mode.
The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.
All bits of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O1 control register (SIO1CON)] $001A_{16}$
The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART control register (UARTCON)] $001B_{16}$
The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the $P1_1$/TXD_1, $P1_2$/S_{CLK1} pin.

[Baud rate generator (BRG)] $001C_{16}$
The baud rate generator determines the baud rate for serial transfer.
The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

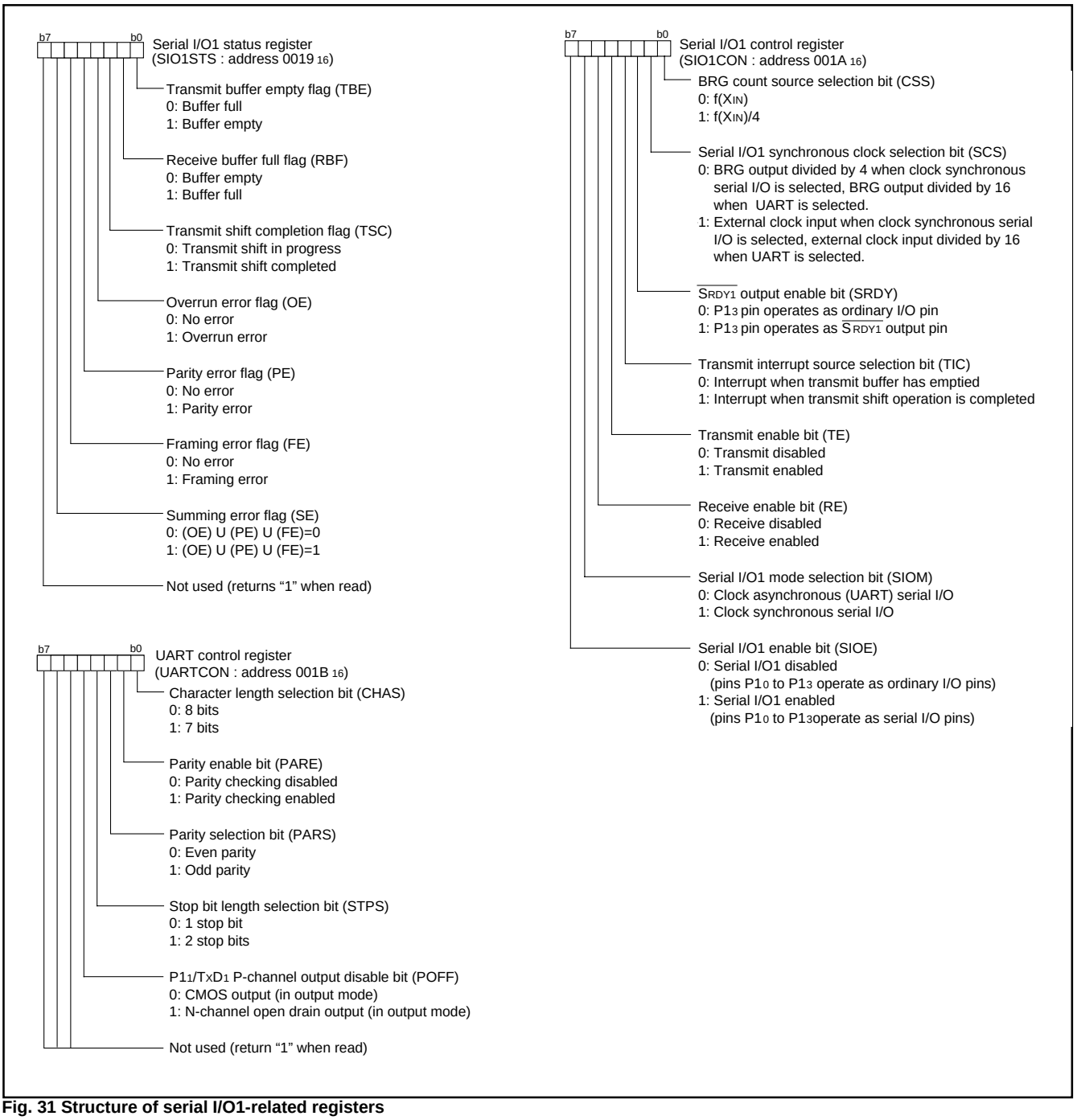


Fig. 31 Structure of serial I/O1-related registers

●Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O2 the transmitter and the receiver must use the same clock. When the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

Note: Serial I/O2 can be used in the following cases;
(1) Serial I/O1 is not used,
(2) Serial I/O1 is used as UART and BRG output divided by 16 is selected as the synchronized clock.

[Serial I/O2 control register] SIO2CON

The serial I/O2 control register contains 8 bits which control various serial I/O functions.

- Set "0" to bit 3 to receive.
- At reception, clear bit 7 to "0" by writing a dummy data to the serial I/O2 register after completion of shift.

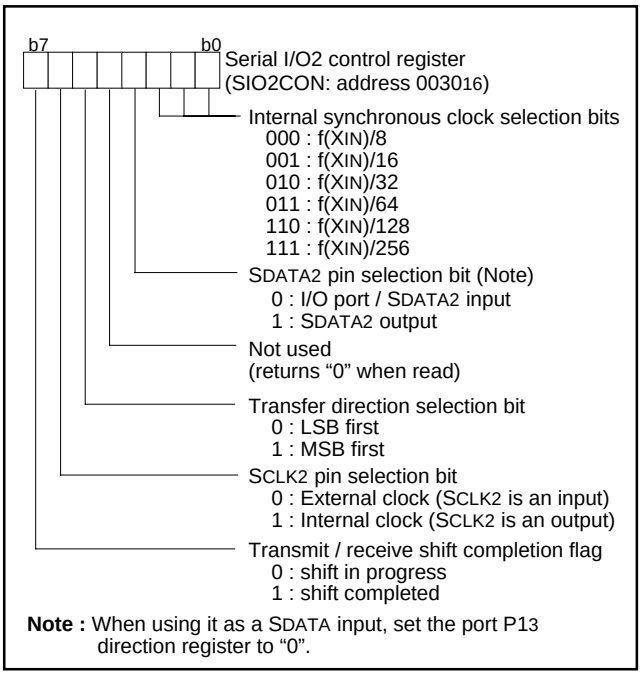


Fig. 32 Structure of serial I/O2 control registers

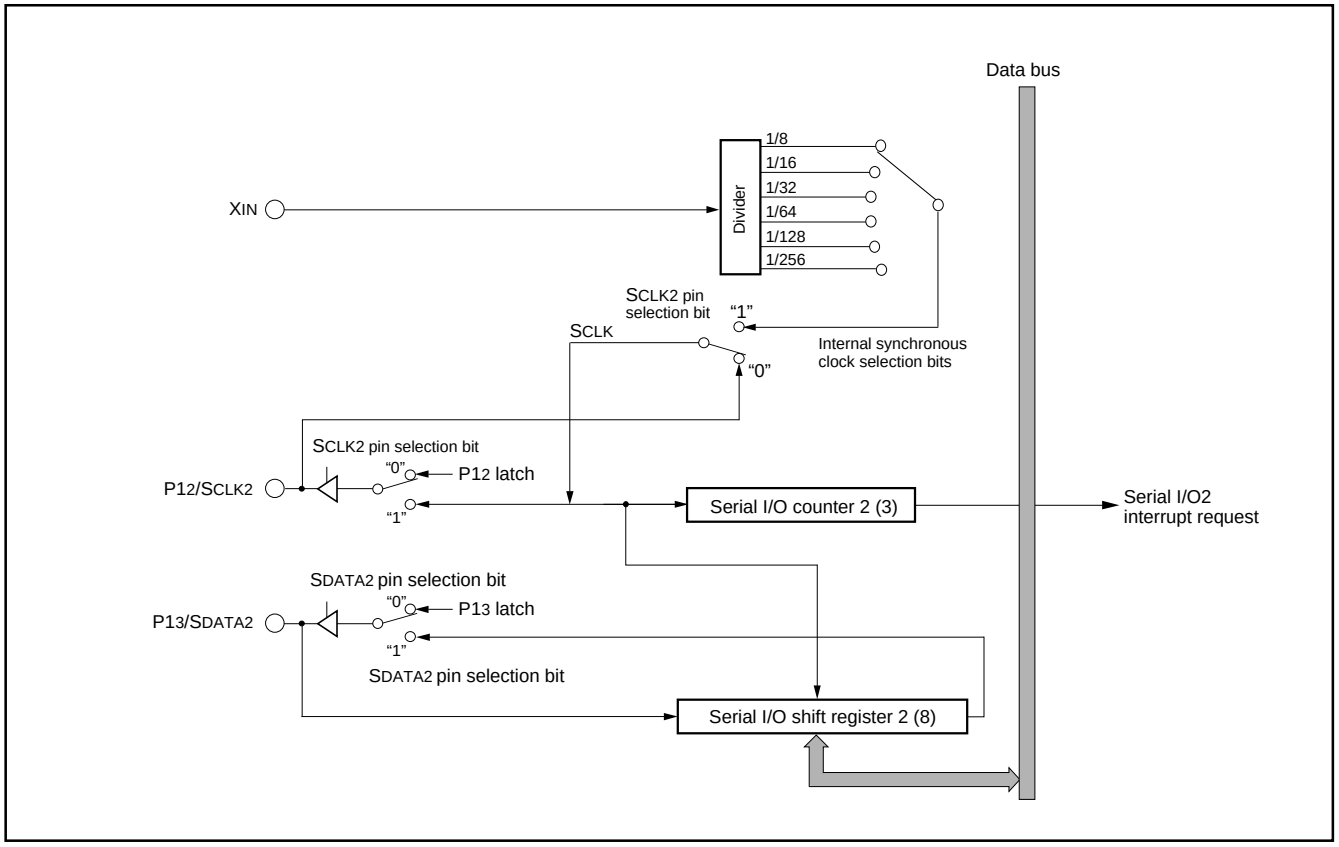


Fig. 33 Block diagram of serial I/O2

Serial I/O2 operation

By writing to the serial I/O2 register (address 0031_{16}) the serial I/O2 counter is set to "7".

After writing, the SDATA2 pin outputs data every time the transfer clock shifts from "H" to "L". And, as the transfer clock shifts from "L" to "H", the SDATA2 pin reads data, and at the same time the contents of the serial I/O2 register are shifted by 1 bit.

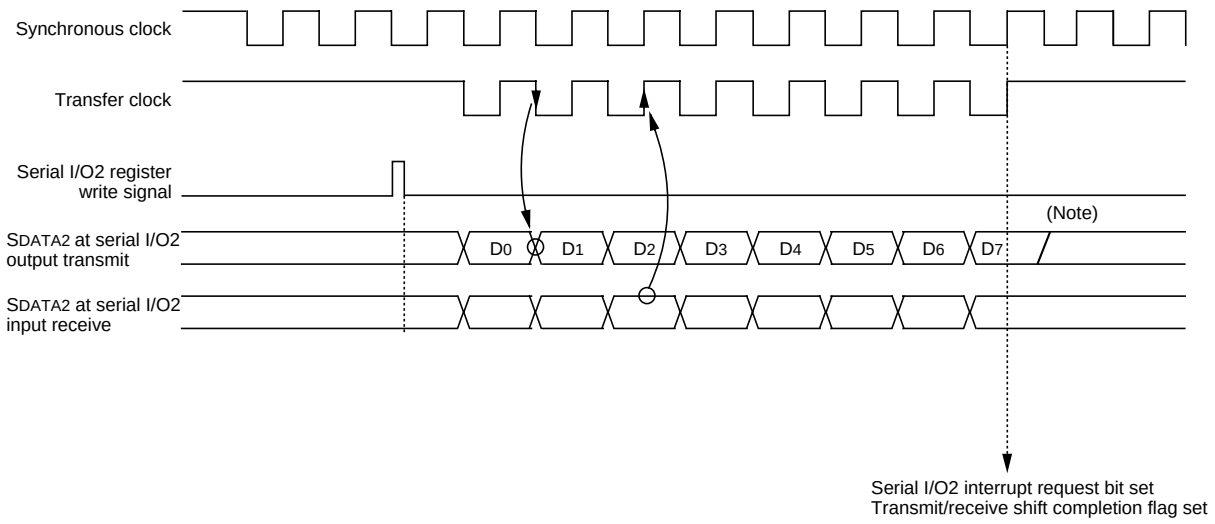
When the internal clock is selected as the transfer clock source, the following operations execute as the transfer clock counts up to 8.

- Serial I/O2 counter is cleared to "0".
- Transfer clock stops at an "H" level.
- Interrupt request bit is set.
- Shift completion flag is set.

Also, the SDATA2 pin is in a high impedance state after the data transfer is completed.

When the external clock is selected as the transfer clock source, the interrupt request bit is set as the transfer clock counts up to 8, but external control of the clock is required since it does not stop. Notice that the SDATA2 pin is not in a high impedance state on the completion of data transfer.

Also, after the receive operation is completed, the transmit/receive shift completion flag is cleared by reading the serial I/O2 register. At transmit, the transmit/receive shift completion flag is cleared and the transmit operation is started by writing to serial I/O2 register.



Note : When the internal clock is selected as the transfer, the SDATA2 pin is in a high impedance state after the data transfer is completed.

Fig. 34 Serial I/O2 timing (LSB first)

A-D Converter

The functional blocks of the A-D converter are described below.

[A-D conversion register] AD

The A-D conversion register is a read-only register that stores the result of A-D conversion. Do not read out this register during an A-D conversion.

[A-D control register] ADCON

The A-D control register controls the A-D converter. Bit 2 to 0 are analog input pin selection bits. Bit 4 is the AD conversion completion bit. The value of this bit remains at "0" during A-D conversion, and changes to "1" at completion of A-D conversion.
A-D conversion is started by setting this bit to "0".

[Comparison voltage generator]

The comparison voltage generator divides the voltage between AVSS and VREF by 1024, and outputs the divided voltages.

[Channel selector]

The channel selector selects one of ports P27/AN7 to P20/AN0, and inputs the voltage to the comparator.

[Comparator and control circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores its result into the A-D conversion register. When A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1". Because the comparator is constructed linked to a capacitor, set f(XIN) to 500 kHz or more during A-D conversion.

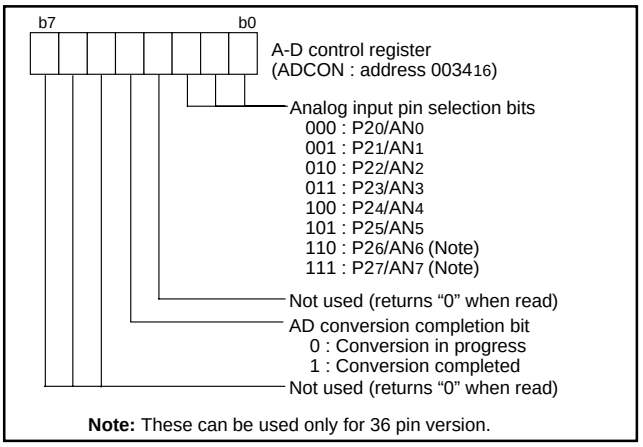


Fig. 35 Structure of A-D control register

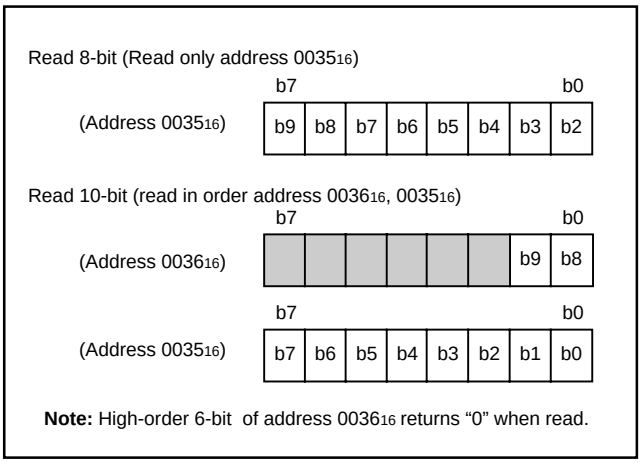


Fig. 36 Structure of A-D conversion register

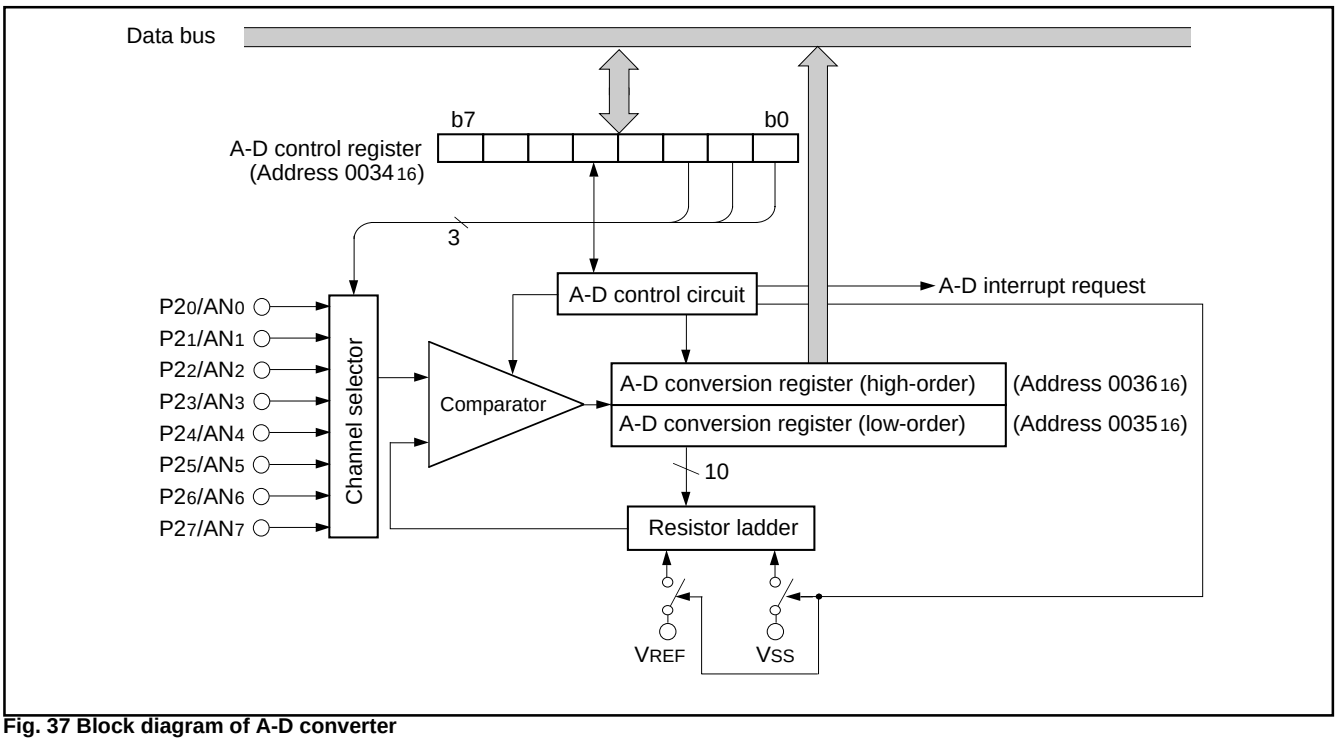


Fig. 37 Block diagram of A-D converter

Watchdog Timer

The watchdog timer gives a means for returning to a reset status when the program fails to run on its normal loop due to a runaway. The watchdog timer consists of an 8-bit watchdog timer H and an 8-bit watchdog timer L, being a 16-bit counter.

Standard operation of watchdog timer

The watchdog timer stops when the watchdog timer control register (address 0039_{16}) is not set after reset. Writing an optional value to the watchdog timer control register (address 0039_{16}) causes the watchdog timer to start to count down. When the watchdog timer H underflows, an internal reset occurs. Accordingly, it is programmed that the watchdog timer control register (address 0039_{16}) can be set before an underflow occurs.

When the watchdog timer control register (address 0039_{16}) is read, the values of the high-order 6-bit of the watchdog timer H, STP instruction disable bit and watchdog timer H count source selection bit are read.

Initial value of watchdog timer

By a reset or writing to the watchdog timer control register (address 0039_{16}), the watchdog timer H is set to "FF_{16}" and the watchdog timer L is set to "FF_{16}".

Operation of watchdog timer H count source selection bit

A watchdog timer H count source can be selected by bit 7 of the watchdog timer control register (address 0039_{16}). When this bit is "0", the count source becomes a watchdog timer L underflow signal. The detection time is 131.072 ms at f(XIN)=8 MHz.

When this bit is "1", the count source becomes f(XIN)/16. In this case, the detection time is 512 µs at f(XIN)=8 MHz.

This bit is cleared to "0" after reset.

Operation of STP instruction disable bit

When the watchdog timer is in operation, the STP instruction can be disabled by bit 6 of the watchdog timer control register (address 0039_{16}).

When this bit is "0", the STP instruction is enabled.

When this bit is "1", the STP instruction is disabled, and an internal reset occurs if the STP instruction is executed.

Once this bit is set to "1", it cannot be changed to "0" by program.

This bit is cleared to "0" after reset.

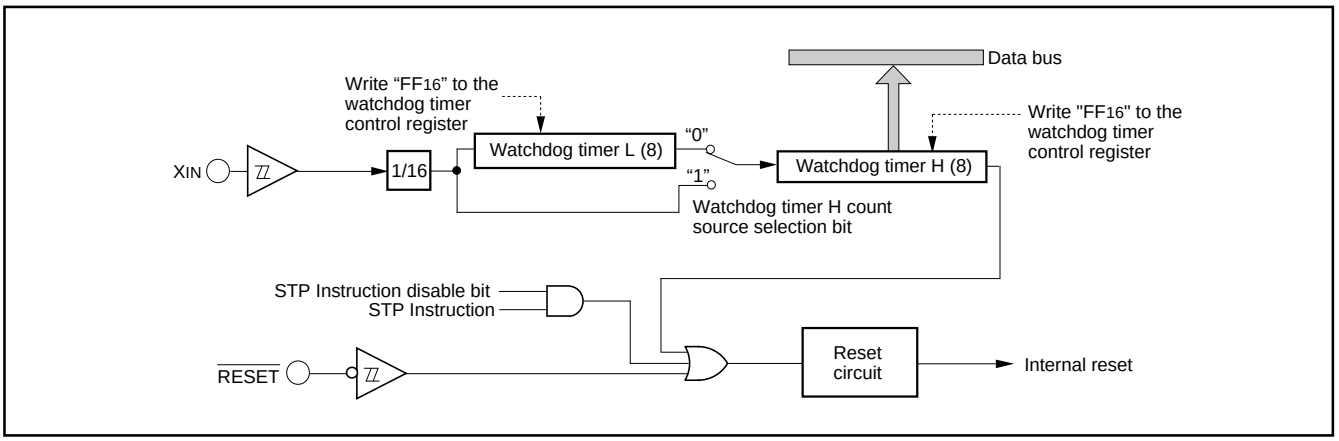


Fig. 38 Block diagram of watchdog timer

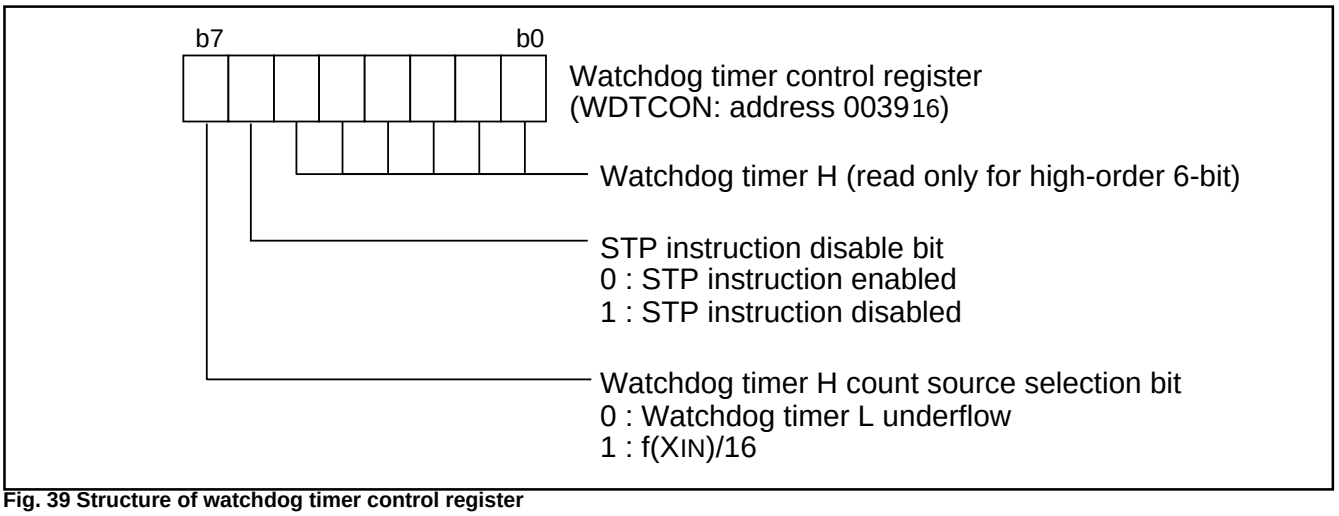


Fig. 39 Structure of watchdog timer control register

Reset Circuit

The microcomputer is put into a reset status by holding the $\overline{\text{RESET}}$ pin at the "L" level for 2 µs or more when the power source voltage is 2.2 to 5.5 V and X_{IN} is in stable oscillation.

After that, this reset status is released by returning the $\overline{\text{RESET}}$ pin to the "H" level. The program starts from the address having the contents of address $FFFD_{16}$ as high-order address and the contents of address $FFFC_{16}$ as low-order address.

In the case of $f(\phi) \leq 4$ MHz, the reset input voltage must be 0.8 V or less when the power source voltage passes 4.0 V.

In the case of $f(\phi) \leq 2$ MHz, the reset input voltage must be 0.48 V or less when the power source voltage passes 2.4 V.

In the case of $f(\phi) \leq 1$ MHz, the reset input voltage must be 0.44 V or less when the power source voltage passes 2.2 V.

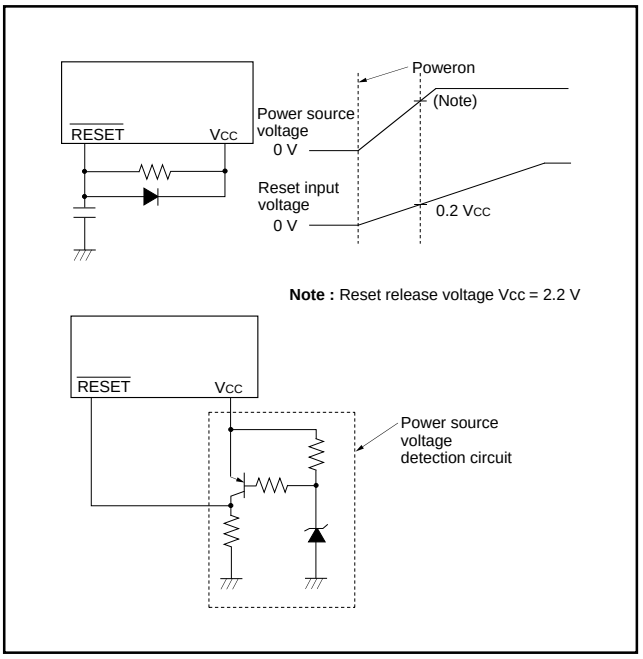


Fig. 40 Example of reset circuit

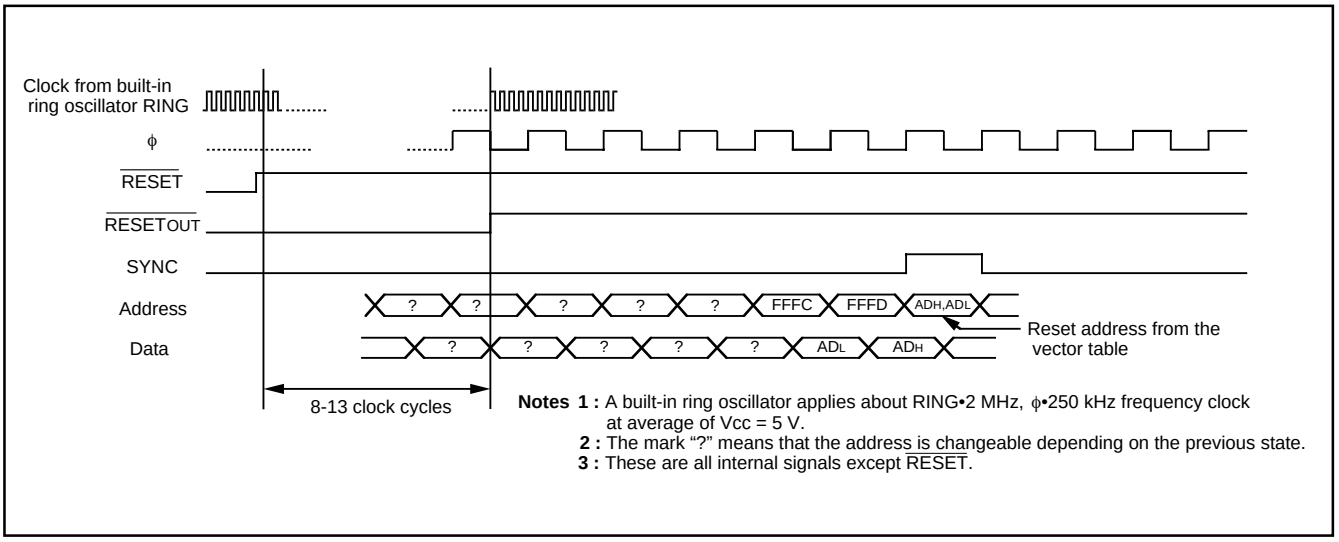


Fig. 41 Timing diagram at reset

	Address	Register contents
(1) Port P0 direction register	0001_{16}	00_{16}
(2) Port P1 direction register	0003_{16}	X X X 0 0 0 0 0
(3) Port P2 direction register	0005_{16}	00_{16}
(4) Port P3 direction register	0007_{16}	00_{16}
(5) Pull-up control register	0016_{16}	00_{16}
(6) Port P1P3 control register	0017_{16}	00_{16}
(7) Serial I/O1 status register	0019_{16}	1 0 0 0 0 0 0 1
(8) Serial I/O1 control register	$001A_{16}$	02_{16}
(9) UART control register	$001B_{16}$	1 1 1 0 0 0 0 0
(10) Timer A mode register	$001D_{16}$	00_{16}
(11) Timer A (low-order)	$001E_{16}$	FF_{16}
(12) Timer A (high-order)	$001F_{16}$	FF_{16}
(13) Timer Y, Z mode register	0020_{16}	00_{16}
(14) Prescaler Y	0021_{16}	FF_{16}
(15) Timer Y secondary	0022_{16}	FF_{16}
(16) Timer Y primary	0023_{16}	FF_{16}
(17) Timer Y, Z waveform output control register	0024_{16}	00_{16}
(18) Prescaler Z	0025_{16}	FF_{16}
(19) Timer Z secondary	0026_{16}	FF_{16}
(20) Timer Z primary	0027_{16}	FF_{16}
(21) Prescaler 1	0028_{16}	FF_{16}
(22) Timer 1	0029_{16}	01_{16}
(23) One-shot start register	$002A_{16}$	00_{16}
(24) Timer X mode register	$002B_{16}$	00_{16}
(25) Prescaler X	$002C_{16}$	FF_{16}
(26) Timer X	$002D_{16}$	FF_{16}
(27) Timer count source set register	$002E_{16}$	00_{16}
(28) Serial I/O2 control register	0030_{16}	00_{16}
(29) Serial I/O2 register	0031_{16}	00_{16}
(30) A-D control register	0034_{16}	10_{16}
(31) MISRG	0038_{16}	00_{16}
(32) Watchdog timer control register	0039_{16}	0 0 1 1 1 1 1 1
(33) Interrupt edge selection register	$003A_{16}$	00_{16}
(34) CPU mode register	$003B_{16}$	1 0 0 0 0 0 0 0
(35) Interrupt request register 1	$003C_{16}$	00_{16}
(36) Interrupt request register 2	$003D_{16}$	00_{16}
(37) Interrupt control register 1	$003E_{16}$	00_{16}
(38) Interrupt control register 2	$003F_{16}$	00_{16}
(39) Processor status register	(PS)	X X X X X 1 X X
(40) Program counter	(PC_H)	Contents of address $FFFD_{16}$
	(PC_L)	Contents of address $FFFC_{16}$

Note X : Undefined

Fig. 42 Internal status of microcomputer at reset

Clock Generating Circuit

An oscillation circuit can be formed by connecting a resonator between XIN and XOUT, and an RC oscillation circuit can be formed by connecting a resistor and a capacitor.

Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip.

Set the constants of the resistor and capacitor when an RC oscillator is used, so that a frequency variation due to LSI variation and resistor and capacitor variations may not exceed the standard input frequency.

●Oscillation control

• Stop mode

When the STP instruction is executed, the internal clock f stops at an "H" level and the XIN oscillator stops. At this time, timer 1 is set to "01_{16}" and prescaler 1 is set to "FF_{16}" when the oscillation stabilization time set bit after release of the STP instruction is "0". On the other hand, timer 1 and prescaler 1 are not set when the above bit is "1". Accordingly, set the wait time fit for the oscillation stabilization time of the oscillator to be used. f(XIN)/16 is forcibly connected to the input of prescaler 1. When an external interrupt is accepted, oscillation is restarted but the internal clock f remains at "H" until timer 1 underflows. As soon as timer 1 underflows, the internal clock f is supplied. This is because when a ceramic oscillator is used, some time is required until a start of oscillation. In case oscillation is restarted by reset, no wait time is generated. So apply an "L" level to the $\overline{\text{RESET}}$ pin while oscillation becomes stable.

Also, the STP instruction cannot be used while CPU is operating by a ring oscillator.

• Wait mode

If the WIT instruction is executed, the internal clock f stops at an "H" level, but the oscillator does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

When the STP status is released, prescaler 1 and timer 1 will start counting clock which is XIN divided by 16, so set the timer 1 interrupt enable bit to "0" before the STP instruction is executed.

Note

For use with the oscillation stabilization set bit after release of the STP instruction set to "1", set values in timer 1 and prescaler 1 after fully appreciating the oscillation stabilization time of the oscillator to be used.

●Switch of ceramic and RC oscillations

After releasing reset the operation starts by starting a built-in ring oscillator. Then, a ceramic oscillation or an RC oscillation is selected by setting bit 5 of the CPU mode register.

●Double-speed mode

When a ceramic oscillation is selected, a double-speed mode can be used. Do not use it when an RC oscillation is selected.

●CPU mode register

Bits 5, 1 and 0 of CPU mode register are used to select oscillation mode and to control operation modes of the microcomputer. In order to prevent the dead-lock by error-writing (ex. program run-away), these bits can be rewritten only once after releasing reset. After rewriting it is disable to write any data to the bit. (The emulator MCU "M37540RSS" is excluded.)

Also, when the read-modify-write instructions (SEB, CLB) are executed to bits 2 to 4, 6 and 7, bits 5, 1 and 0 are locked.

●Clock division ratio, XIN oscillation control, ring oscillator control

The state transition shown in Fig. 49 can be performed by setting the clock division ratio selection bits (bits 7 and 6), XIN oscillation control bit (bit 4), ring oscillator oscillation control bit (bit 3) of CPU mode register. Be careful of notes on use in Fig. 49.

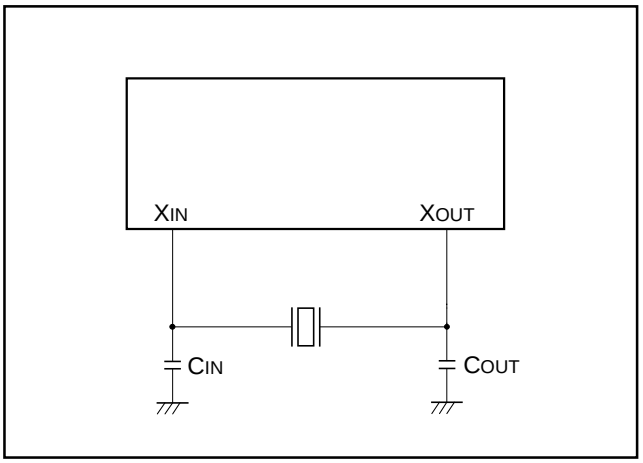


Fig. 43 External circuit of ceramic resonator

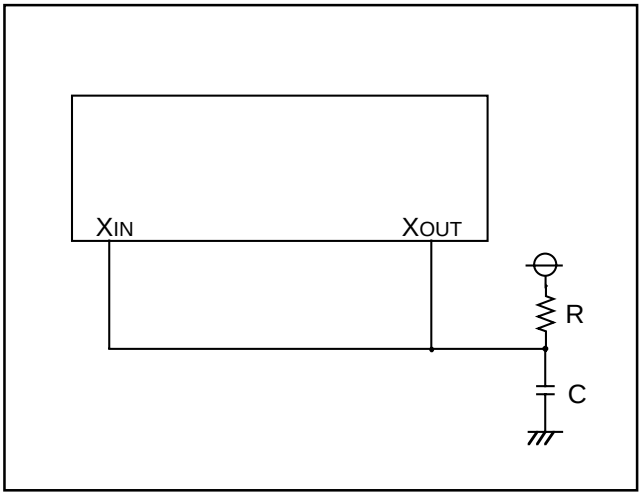


Fig. 44 External circuit of RC oscillation

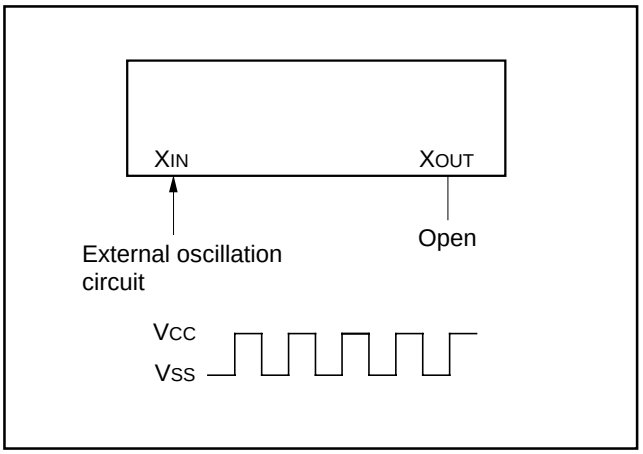


Fig. 45 External clock input circuit

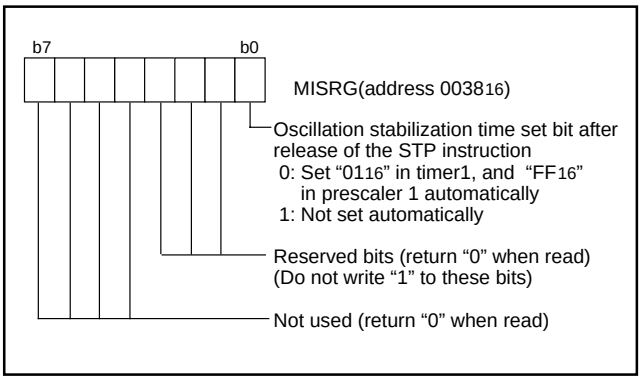


Fig. 46 Structure of MISRG

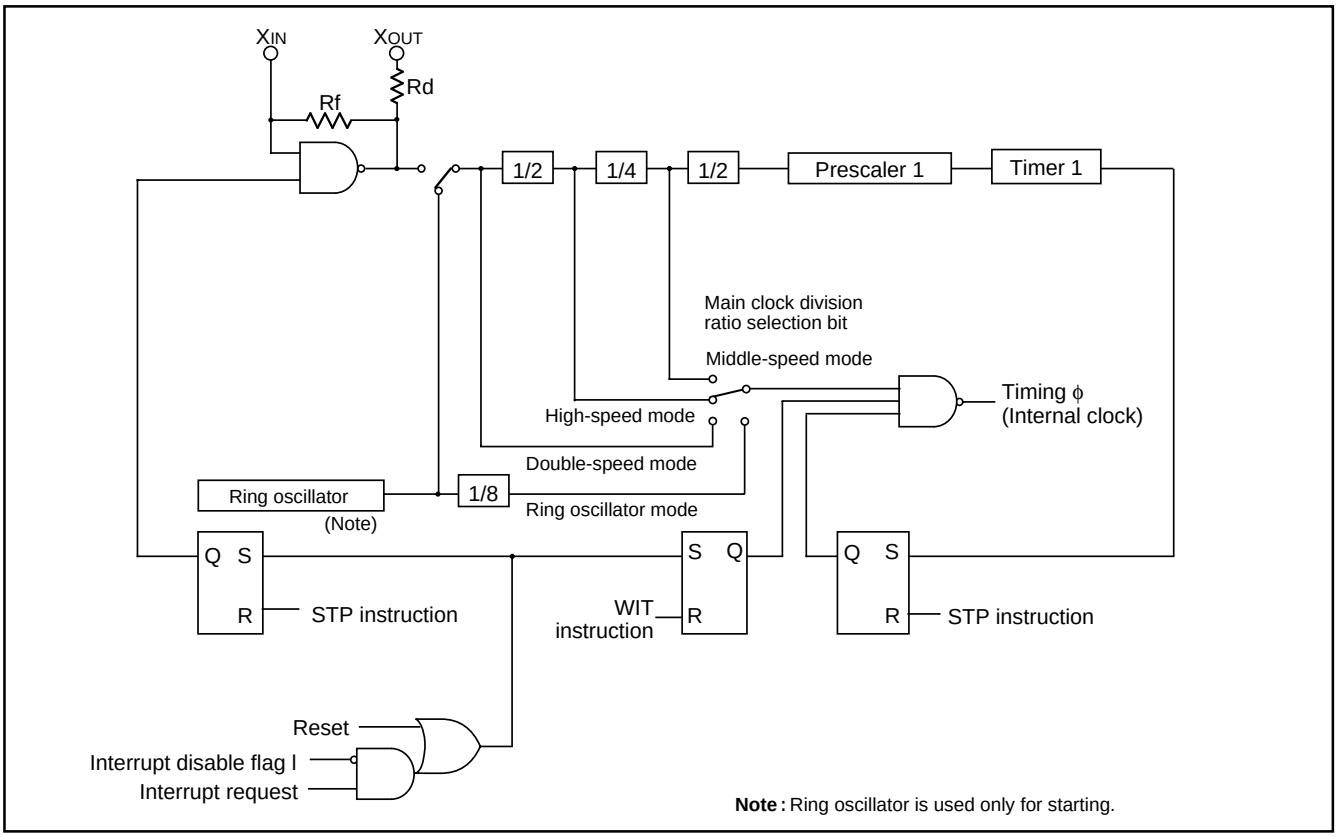


Fig. 47 Block diagram of internal clock generating circuit (for ceramic resonator)

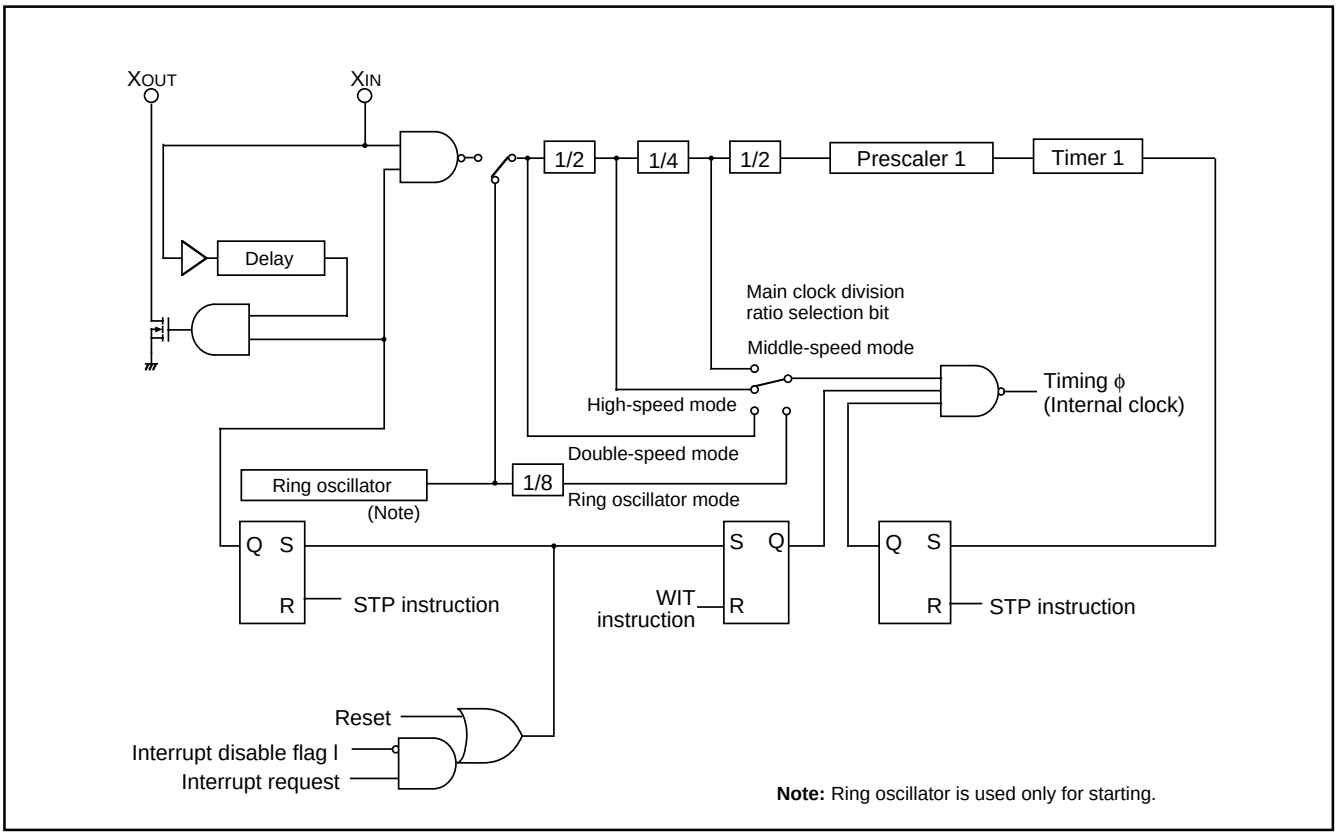
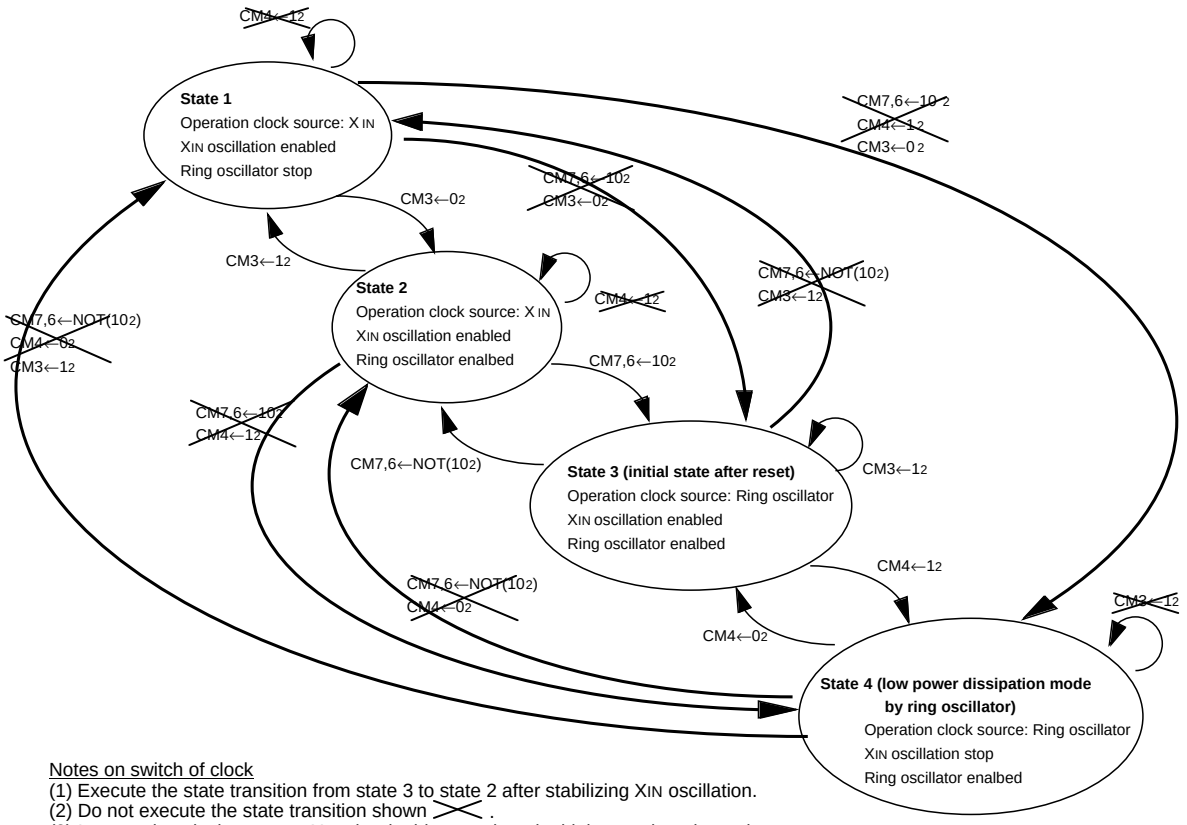


Fig. 48 Block diagram of internal clock generating circuit (for RC oscillation)



Notes on switch of clock
(1) Execute the state transition from state 3 to state 2 after stabilizing XIN oscillation.
(2) Do not execute the state transition shown ✕ .
(3) In operation clock source = XIN, the double-speed mode, high-speed mode, and middle-speed mode can be selected for the CPU clock division ratio.
(4) In operation clock source = ring oscillator, the middle-speed mode is selected for the CPU clock division ratio.
(5) Do not stop the clock selected as the operation clock because of setting of CM3, 4.

Fig. 49 State transition

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after reset are undefined except for the interrupt disable flag I which is "1". After reset, initialize flags which affect program execution. In particular, it is essential to initialize the T flag and the D flag because of their effect on calculations.

Interrupts

The contents of the interrupt request bit do not change even if the BBC or BBS instruction is executed immediately after they are changed by program because this instruction is executed for the previous contents. For executing the instruction for the changed contents, execute one instruction before executing the BBC or BBS instruction.

Decimal Calculations

- For calculations in decimal notation, set the decimal mode flag D to "1", then execute the ADC instruction or SBC instruction. In this case, execute SEC instruction, CLC instruction or CLD instruction after executing one instruction before the ADC instruction or SBC instruction.
- In the decimal mode, the values of the N (negative), V (overflow) and Z (zero) flags are invalid.

Timers

- When n (0 to 255) is written to a timer latch, the frequency division ratio is 1/(n+1).
- When a count source of timer X, timer Y or timer Z is switched, stop a count of timer X.

Ports

- The values of the port direction registers cannot be read.
  That is, it is impossible to use the LDA instruction, memory operation instruction when the T flag is "1", addressing mode using direction register values as qualifiers, and bit test instructions such as BBC and BBS.
  It is also impossible to use bit operation instructions such as CLB and SEB and read/modify/write instructions of direction registers for calculations such as ROR.
  For setting direction registers, use the LDM instruction, STA instruction, etc.
- $P2_6/AN_6$, $P2_7/AN_7$, $P3_5$ (LED_5), $P3_6/INT_1$ pins do not exist in the 32-pin version. Stabilize the internal level by setting the port direction registers of these ports to output or setting $P3_5$, $P3_6$ pull-up control bits of the pull-up control register (PULL) to ON by program.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Make sure that f(X_{IN}) is 500kHz or more during A-D conversion.
Do not execute the STP instruction during A-D conversion.

Instruction Execution Timing

The instruction execution time can be obtained by multiplying the frequency of the internal clock ϕ by the number of cycles mentioned in the machine-language instruction table.
The frequency of the internal clock ϕ is the same as that of the X_{IN} in double-speed mode, twice the X_{IN} cycle in high-speed mode and 8 times the X_{IN} cycle in middle-speed mode.

CPU Mode Register

The oscillation mode selection bit and processor mode bits can be rewritten only once after releasing reset. However, after rewriting it is disable to write any value to the bit. (Emulator MCU is excluded.)
When a ceramic oscillation is selected, a double-speed mode of the clock division ratio selection bits can be used. Do not use it when an RC oscillation is selected.

State transition

Do not stop the clock selected as the operation clock because of setting of CM3, 4.

NOTES ON USE

Handling of Power Source Pin

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (Vcc pin) and GND pin (Vss pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 µF to 0.1 µF is recommended.

One Time PROM Version

The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.
To improve the noise reduction, connect a track between CNVss pin and Vss pin with 1 to 10 kΩ resistance.
The mask ROM version track of CNVss pin has no operational interference even if it is connected via a resistor.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form
(three identical copies)

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 5 Special programming adapter

Package	Name of Programming Adapter
32P4B	PCA7435SPG02
32P6B-A	PCA7435GPG02
36P2R-A	PCA7435FPG02

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 50 is recommended to verify programming.

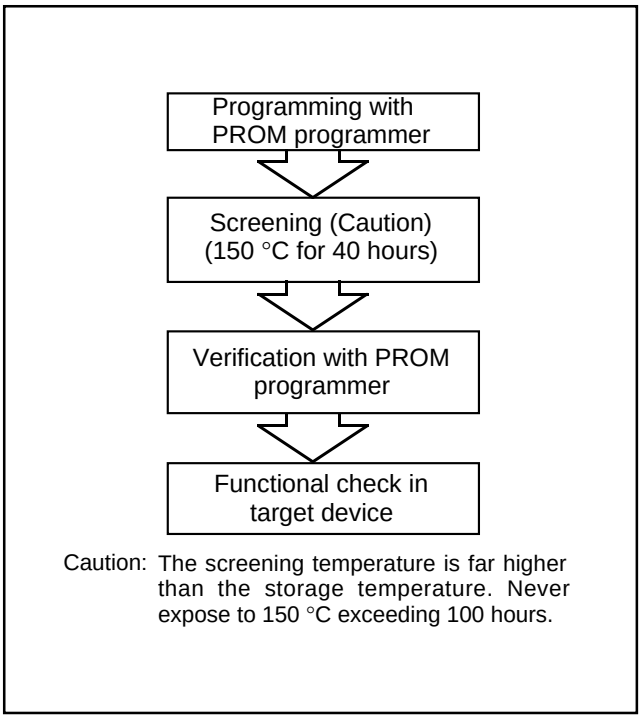


Fig. 50 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

1.7540Group (General purpose)

Applied to: M37540M4-XXXFP/SP/GP, M37540E8FP/SP/GP

Absolute Maximum Ratings (General purpose)

Table 6 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage		All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	CNV_{SS} (Note 1)		–0.3 to 13	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		Ta = 25°C	300 (Note 2)	mW
T_{opr}	Operating temperature			–20 to 85	°C
T_{stg}	Storage temperature			–40 to 125	°C

Note 1: It is a rating only for the One Time PROM version. Connect to V_{SS} for the mask ROM version.
2: 200 mW for the 32P6B package product.

Recommended Operating Conditions (General purpose)

Table 7 Recommended operating conditions (1) (V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (ceramic)	f(X_{IN}) = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 2 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
		f(X_{IN}) = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 1 MHz (Double-speed mode)	2.2	5.0	5.5	V
	Power source voltage (RC)	f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 1 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)	2.0		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	0		0.3V_{CC}	V
V_{IL}	“L” input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)	0		0.8	V
V_{IL}	“L” input voltage	$\overline{RESET}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}	0		0.16V_{CC}	V
$\Sigma I_{OH(peak)}$	“H” total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current (Note 2)	$P3_0$–$P3_6$			60	mA
$\Sigma I_{OH(avg)}$	“H” total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current (Note 2)	$P3_0$–$P3_6$			30	mA

Note 1: Vcc = 4.0 to 5.5V

2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Recommended Operating Conditions (General purpose)(continued)

Table 8 Recommended operating conditions (2) (V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P3_0$–$P3_6$			30	mA
$I_{OH(avg)}$	"H" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P3_0$–$P3_6$			15	mA
$f(X_{IN})$	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V Double-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V Double-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.2 to 5.5 V Double-speed mode			1	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.2 to 5.5 V High-, Middle-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at RC oscillation	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.2 to 5.5 V High-, Middle-speed mode			1	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50 %.

Electrical Characteristics (General purpose)

Table 9 Electrical characteristics (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ (Note 1)	I_{OH} = –5 mA V_{CC} = 4.0 to 5.5 V		V_{CC}–1.5			V
			I_{OH} = –1.0 mA V_{CC} = 2.2 to 5.5 V		V_{CC}–1.0			V
V_{OL}	"L" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$	I_{OL} = 5 mA V_{CC} = 4.0 to 5.5 V				1.5	V
			I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V				0.3	V
			I_{OL} = 1.0 mA V_{CC} = 2.2 to 5.5 V				1.0	V
V_{OL}	"L" output voltage	$P3_0$–$P3_6$	I_{OL} = 15 mA V_{CC} = 4.0 to 5.5 V				2.0	V
			I_{OL} = 1.5 mA V_{CC} = 4.0 to 5.5 V				0.3	V
			I_{OL} = 10 mA V_{CC} = 2.2 to 5.5 V				1.0	V
V_{T+}–V_{T-}	Hysteresis	$CNTR_0$, $CNTR_1$, INT_0, INT_1(Note 2) $P0_0$–$P0_7$ (Note 3)				0.4		V
V_{T+}–V_{T-}	Hysteresis	R_XD, S_{CLK1}, S_{CLK2}, S_{DATA2} (Note 2)				0.5		V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$				0.5		V
I_{IH}	"H" input current	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{CC} (Pin floating. Pull up transistors "off")				5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$	V_I = V_{CC}				5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}			4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pin floating. Pull up transistors "off")				–5.0	µA
I_{IL}	"L" input current	$\overline{RESET}$, CNV_{SS}	V_I = V_{SS}				–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}			–4.0		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pull up transistors "on")			–0.2	–0.5	mA
V_{RAM}	RAM hold voltage		When clock stopped		2.0		5.5	V
I_{CC}	Power source current	High-speed mode, f(X_{IN}) = 8 MHz Output transistors "off"				5.0	TBD	mA
		High-speed mode, f(X_{IN}) = 2 MHz, V_{CC} = 2.2 V Output transistors "off"				TBD	TBD	mA
		Double-speed mode, f(X_{IN}) = 4 MHz Output transistors "off"				5.0	TBD	mA
		Middle-speed mode, f(X_{IN}) = 8 MHz Output transistors "off"				2.0	TBD	mA
		f(X_{IN}) = 8 MHz (in WIT state), functions except timer 1 disabled, Output transistors "off"				1.6		mA
		f(X_{IN}) = 2 MHz, V_{CC} = 2.2 V (in WIT state) Output transistors "off"				TBD		mA
		Increment when A-D conversion is executed f(X_{IN}) = 8 MHz, V_{CC} = 5 V				0.7		mA
		All oscillation stopped (in STP state) Output transistors "off"		Ta = 25 °C		0.1	1.0	µA
				Ta = 85 °C			10	µA

Notes 1: $P1_1$ is measured when the $P1_1$/T_XD_1 P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: R_XD1, S_{CLK1}, S_{CLK2}, S_{DATA2}, INT_0, and INT_1 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake up.

A-D Converter Characteristics (General purpose)

Table 10 A-D Converter characteristics (1) (V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±0.9	LSB
V_{OT}	Zero transition voltage	V_{CC} = V_{REF} = 5.12 V	0	5	20	mV
		V_{CC} = V_{REF} = 3.072 V	0	3	15	mV
V_{FST}	Full scale transition voltage	V_{CC} = V_{REF} = 5.12 V	5105	5115	5125	mV
		V_{CC} = V_{REF} = 3.072 V	3060	3069	3075	mV
t_{CONV}	Conversion time				122	$t_{c(XIN)}$
R_{LADDER}	Ladder resistor			35		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	150	200	µA
		V_{REF} = 3.0 V	30	90	120	
$I_{I(AD)}$	A-D port input current				5.0	µA

Timing Requirements (General purpose)

Table 11 Timing requirements (1) (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	External clock input cycle time	125			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	50			ns
$t_{C(CNTR0)}$	$CNTR_0$ input cycle time	200			ns
$t_{WH(CNTR0)}$	$CNTR_0$, INT_0, INT_1, input “H” pulse width	80			ns
$t_{WL(CNTR0)}$	$CNTR_0$, INT_0, INT_1, input “L” pulse width	80			ns
$t_{C(CNTR1)}$	$CNTR_1$ input cycle time	200			ns
$t_{WH(CNTR1)}$	$CNTR_1$ input “H” pulse width	80			ns
$t_{WL(CNTR1)}$	$CNTR_1$ input “L” pulse width	80			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time (Note)	2000			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width (Note)	950			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width (Note)	950			ns
$t_{su(RxD1–SCLK1)}$	Serial I/O1 input set up time	400			ns
$t_{h(RxD1–SCLK1)}$	Serial I/O1 input hold time	200			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(SDATA2–SCLK2)}$	Serial I/O2 input set up time	200			ns
$t_{h(SCLK2–SDATA2)}$	Serial I/O2 input hold time	200			ns

Note: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O1 is selected).
When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.

Table 12 Timing requirements (2) (V_{CC} = 2.2 to 5.5 V or 2.4 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width		2			µs
$t_{C(XIN)}$	External clock input cycle time	V_{CC} = 2.2 to 5.5 V	500			ns
		V_{CC} = 2.4 to 5.5 V	250			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	V_{CC} = 2.2 to 5.5 V	200			ns
		V_{CC} = 2.4 to 5.5 V	100			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	V_{CC} = 2.2 to 5.5 V	200			ns
		V_{CC} = 2.4 to 5.5 V	100			ns
$t_{C(CNTR0)}$	$CNTR_0$ input cycle time	V_{CC} = 2.2 to 5.5 V	1000			ns
		V_{CC} = 2.4 to 5.5 V	500			ns
$t_{WH(CNTR0)}$	$CNTR_0$, INT_0, INT_1, input “H” pulse width	V_{CC} = 2.2 to 5.5 V	460			ns
		V_{CC} = 2.4 to 5.5 V	230			ns
$t_{WL(CNTR0)}$	$CNTR_0$, INT_0, INT_1, input “L” pulse width	V_{CC} = 2.2 to 5.5 V	460			ns
		V_{CC} = 2.4 to 5.5 V	230			ns
$t_{C(CNTR1)}$	$CNTR_1$ input cycle time	V_{CC} = 2.2 to 5.5 V	TBD			ns
		V_{CC} = 2.4 to 5.5 V	TBD			ns
$t_{WH(CNTR1)}$	$CNTR_1$ input “H” pulse width	V_{CC} = 2.2 to 5.5 V	TBD			ns
		V_{CC} = 2.4 to 5.5 V	TBD			ns
$t_{WL(CNTR1)}$	$CNTR_1$ input “L” pulse width	V_{CC} = 2.2 to 5.5 V	TBD			ns
		V_{CC} = 2.4 to 5.5 V	TBD			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time	V_{CC} = 2.2 to 5.5 V	TBD			ns
		V_{CC} = 2.4 to 5.5 V	TBD			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width	V_{CC} = 2.2 to 5.5 V	TBD			ns
		V_{CC} = 2.4 to 5.5 V	TBD			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width	V_{CC} = 2.2 to 5.5 V	TBD			ns
		V_{CC} = 2.4 to 5.5 V	TBD			ns
$t_{su(SDATA1–SCLK1)}$	Serial I/O1 input set up time		TBD			ns
$t_{h(SCLK1–SDATA1)}$	Serial I/O1 input hold time		TBD			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	V_{CC} = 2.2 to 5.5 V	4000			ns
		V_{CC} = 2.4 to 5.5 V	2000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	V_{CC} = 2.2 to 5.5 V	1900			ns
		V_{CC} = 2.4 to 5.5 V	950			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	V_{CC} = 2.2 to 5.5 V	1900			ns
		V_{CC} = 2.4 to 5.5 V	950			ns
$t_{su(SDATA2–SCLK2)}$	Serial I/O2 input set up time		400			ns
$t_{h(SCLK2–SDATA2)}$	Serial I/O2 input hold time		400			ns

Switching Characteristics (General purpose)

Table 13 Switching characteristics (1) (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

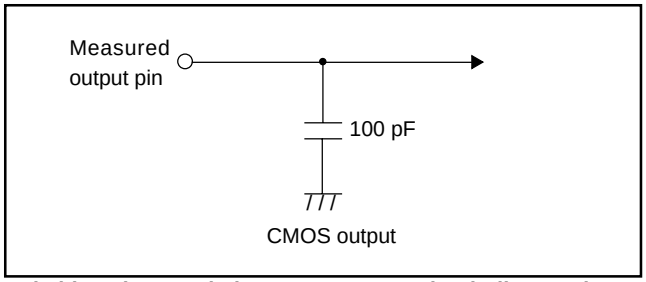
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK1)}$	Serial I/O1 clock output “H” pulse width	$t_{C(SCLK1)}$/2–30			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock output “L” pulse width	$t_{C(SCLK1)}$/2–30			ns
$t_{d(SCLK1–TxD1)}$	Serial I/O1 output delay time			140	ns
$t_{v(SCLK1–TxD1)}$	Serial I/O1 output valid time	–30			ns
$t_{r(SCLK1)}$	Serial I/O1 clock output rising time			30	ns
$t_{f(SCLK1)}$	Serial I/O1 clock output falling time			30	ns
$t_{WH(SCLK2)}$	Serial I/O2 clock output “H” pulse width	$t_{C(SCLK2)}$/2–30			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock output “L” pulse width	$t_{C(SCLK2)}$/2–30			ns
$t_{d(SCLK2–SDATA2)}$	Serial I/O2 output delay time			140	ns
$t_{v(SCLK2–SDATA2)}$	Serial I/O2 output valid time	0			ns
$t_{r(SCLK2)}$	Serial I/O2 clock output rising time			30	ns
$t_{f(SCLK2)}$	Serial I/O2 clock output falling time			30	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 1)		10	30	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 1)		10	30	ns

Note 1: Pin X_{OUT} is excluded.

Table 14 Switching characteristics (2) (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK1)}$	Serial I/O1 clock output “H” pulse width	TBD			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock output “L” pulse width	TBD			ns
$t_{d(SCLK1–TxD1)}$	Serial I/O1 output delay time			TBD	ns
$t_{v(SCLK1–TxD1)}$	Serial I/O1 output valid time	TBD			ns
$t_{r(SCLK1)}$	Serial I/O1 clock output rising time			TBD	ns
$t_{f(SCLK1)}$	Serial I/O1 clock output falling time			TBD	ns
$t_{WH(SCLK2)}$	Serial I/O2 clock output “H” pulse width	$t_{C(SCLK2)}$/2–50			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock output “L” pulse width	$t_{C(SCLK2)}$/2–50			ns
$t_{d(SCLK2–SDATA2)}$	Serial I/O2 output delay time			350	ns
$t_{v(SCLK2–SDATA2)}$	Serial I/O2 output valid time	0			ns
$t_{r(SCLK2)}$	Serial I/O2 clock output rising time			50	ns
$t_{f(SCLK2)}$	Serial I/O2 clock output falling time			50	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 1)		20	50	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 1)		20	50	ns

Note 1: Pin X_{OUT} is excluded.



Switching characteristics measurement circuit diagram (General purpose)

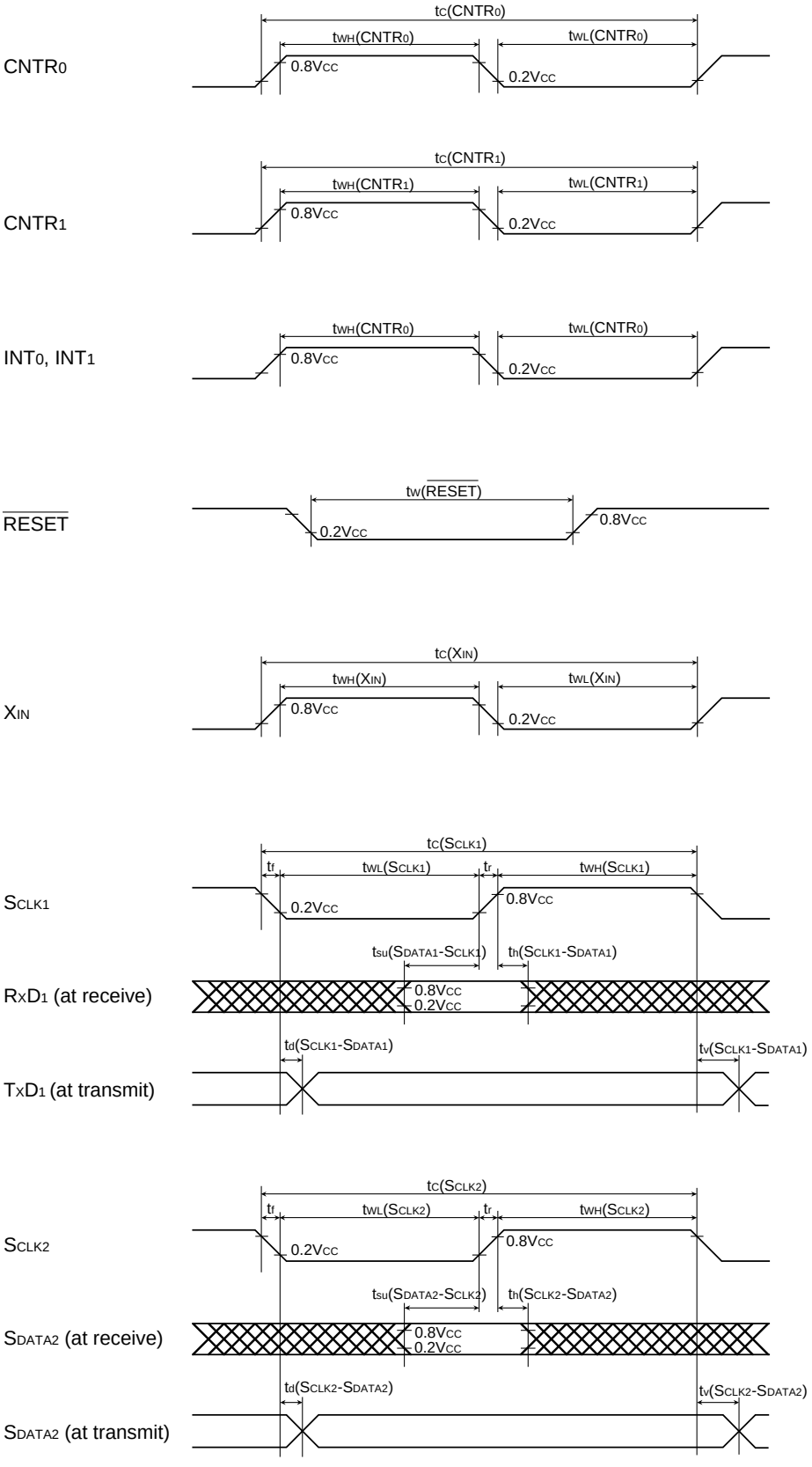


Fig. 51 Timing chart (General purpose)

ELECTRICAL CHARACTERISTICS

2.7540Group (Extended operating temperature version)

Applied to: M37540M4T-XXXFP/GP

Absolute Maximum Ratings (Extended operating temperature version)

Table 15 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage		All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}, CNV_{SS}		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		Ta = 25°C	300 (Note)	mW
T_{opr}	Operating temperature			–40 to 85	°C
T_{stg}	Storage temperature			–65 to 150	°C

Note : 200 mW for the 32P6B package product.

Recommended Operating Conditions (Extended operating temperature version)

Table 16 Recommended operating conditions (1) (V_{CC} = 2.2 to 5.5 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (ceramic)	f(X_{IN}) = 8 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
		f(X_{IN}) = 2 MHz (High-, Middle-speed mode)	2.2	5.0	5.5	V
		f(X_{IN}) = 4 MHz (Double-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (Double-speed mode)	2.4	5.0	5.5	V
	Power source voltage (RC)	f(X_{IN}) = 4 MHz (High-, Middle-speed mode)	4.0	5.0	5.5	V
		f(X_{IN}) = 2 MHz (High-, Middle-speed mode)	2.4	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	Analog reference voltage		2.0		V_{CC}	V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)	2.0		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	0		0.3V_{CC}	V
V_{IL}	“L” input voltage (TTL input level selected)	$P1_0$, $P1_2$, $P1_3$, $P3_6$, $P3_7$ (Note 1)	0		0.8	V
V_{IL}	“L” input voltage	$\overline{RESET}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}	0		0.16V_{CC}	V
$\sum I_{OH(peak)}$	“H” total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–80	mA
$\sum I_{OL(peak)}$	“L” total peak output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			80	mA
$\sum I_{OL(peak)}$	“L” total peak output current (Note 2)	$P3_0$–$P3_6$			60	mA
$\sum I_{OH(avg)}$	“H” total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–40	mA
$\sum I_{OL(avg)}$	“L” total average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			40	mA
$\sum I_{OL(avg)}$	“L” total average output current (Note 2)	$P3_0$–$P3_6$			30	mA

Note 1: Vcc = 4.0 to 5.5V

2: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Recommended Operating Conditions (Extended operating temperature version)

Table 17 Recommended operating conditions (2) (V_{CC} = 2.2 to 5.5 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P3_0$–$P3_6$			30	mA
$I_{OH(avg)}$	"H" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$			–5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$			5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P3_0$–$P3_6$			15	mA
$f(X_{IN})$	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V Double-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V Double-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			8	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at ceramic oscillation or external clock input	V_{CC} = 2.2 to 5.5 V High-, Middle-speed mode			2	MHz
	Internal clock oscillation frequency (Note 3) at RC oscillation	V_{CC} = 4.0 to 5.5 V High-, Middle-speed mode			4	MHz
	Internal clock oscillation frequency (Note 3) at RC oscillation	V_{CC} = 2.4 to 5.5 V High-, Middle-speed mode			2	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50 %.

Electrical Characteristics (Extended operating temperature version)

Table 18 Electrical characteristics (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$ (Note 1)	I_{OH} = –5 mA, V_{CC} = 4.0 to 5.5 V	V_{CC}–1.5			V
		I_{OH} = –1.0 mA, V_{CC} = 2.2 to 5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_7$	I_{OL} = 5 mA, V_{CC} = 4.0 to 5.5 V			1.5	V
		I_{OL} = 1.5 mA, V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 1.0 mA, V_{CC} = 2.2 to 5.5 V			1.0	V
V_{OL}	"L" output voltage $P3_0$–$P3_6$	I_{OL} = 15 mA, V_{CC} = 4.0 to 5.5 V			2.0	V
		I_{OL} = 1.5 mA, V_{CC} = 4.0 to 5.5 V			0.3	V
		I_{OL} = 10 mA, V_{CC} = 2.2 to 5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis $CNTR_0$, $CNTR_1$, INT_0, INT_1(Note 2) $P0_0$–$P0_7$ (Note 3)			0.4		V
V_{T+}–V_{T-}	Hysteresis R_XD_1, S_{CLK1}, S_{CLK2}, S_{DATA2} (Note 2)			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{CC} (Pin floating. Pull up transistors "off")			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_4$, $P2_0$–$P2_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pin floating. Pull up transistors "off")			–5.0	µA
I_{IL}	"L" input current $\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P3_0$–$P3_7$	V_I = V_{SS} (Pull up transistors "on")		–0.2	–0.5	mA
V_{RAM}	RAM hold voltage	When clock stopped	2.0		5.5	V
I_{CC}	Power source current — High-speed mode, f(X_{IN}) = 8 MHz, Output transistors "off"			5.0	TBD	mA
	High-speed mode, f(X_{IN}) = 2 MHz, V_{CC} = 2.2 V, Output transistors "off"			TBD	TBD	mA
	Double-speed mode, f(X_{IN}) = 4 MHz, Output transistors "off"			5.0	TBD	mA
	Middle-speed mode, f(X_{IN}) = 8 MHz, Output transistors "off"			2.0	TBD	mA
	f(X_{IN}) = 8 MHz (in WIT state), functions except timer 1 disabled, Output transistors "off"			1.6		mA
	f(X_{IN}) = 2 MHz, V_{CC} = 2.2 V (in WIT state), Output transistors "off"			TBD		mA
	Increment when A-D conversion is executed, f(X_{IN}) = 8 MHz, V_{CC} = 5 V			0.7		mA
	All oscillation stopped (in STP state), Output transistors "off"	Ta = 25 °C		0.1	1.0	µA
		Ta = 85 °C			10	µA

Notes 1: $P1_1$ is measured when the $P1_1$/T_XD_1 P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: R_XD_1, S_{CLK1}, S_{CLK2}, S_{DATA2}, INT_0, and INT_1 have hysteresises only when bits 0 to 2 of the port P1P3 control register are set to "0" (CMOS level).
3: It is available only when operating key-on wake up.

A-D Converter Characteristics (Extended operating temperature version)

Table 19 A-D Converter characteristics (1) (V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Linearity error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±3	LSB
—	Differential nonlinear error	V_{CC} = 2.7 to 5.5 V Ta = 25 °C			±0.9	LSB
V_{OT}	Zero transition voltage	V_{CC} = V_{REF} = 5.12 V	0	5	20	mV
		V_{CC} = V_{REF} = 3.072 V	0	3	15	mV
V_{FST}	Full scale transition voltage	V_{CC} = V_{REF} = 5.12 V	5105	5115	5125	mV
		V_{CC} = V_{REF} = 3.072 V	3060	3069	3075	mV
t_{CONV}	Conversion time				122	$t_{c(XIN)}$
R_{LADDER}	Ladder resistor			35		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	150	200	µA
		V_{REF} = 3.0 V	30	90	120	
$I_{I(AD)}$	A-D port input current				5.0	µA

Timing Requirements (Extended operating temperature version)

Table 20 Timing requirements (1) (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	External clock input cycle time	125			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	50			ns
$t_{C(CNTR0)}$	CNTR0 input cycle time	200			ns
$t_{WH(CNTR0)}$	CNTR0, INT0, INT1, input “H” pulse width	80			ns
$t_{WL(CNTR0)}$	CNTR0, INT0, INT1, input “L” pulse width	80			ns
$t_{C(CNTR1)}$	CNTR1 input cycle time	200			ns
$t_{WH(CNTR1)}$	CNTR1 input “H” pulse width	80			ns
$t_{WL(CNTR1)}$	CNTR1 input “L” pulse width	80			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time (Note)	2000			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width (Note)	950			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width (Note)	950			ns
$t_{su(RxD1–SCLK1)}$	Serial I/O1 input set up time	400			ns
$t_{h(RxD1–SCLK1)}$	Serial I/O1 input hold time	200			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(SDATA2–SCLK2)}$	Serial I/O2 input set up time	200			ns
$t_{h(SCLK2–SDATA2)}$	Serial I/O2 input hold time	200			ns

Note: In this time, bit 6 of the serial I/O1 control register (address $001A_{16}$) is set to “1” (clock synchronous serial I/O1 is selected).
When bit 6 of the serial I/O1 control register is “0” (clock asynchronous serial I/O1 is selected), the rating values are divided by 4.

Table 21 Timing requirements (2) (Vcc = 2.2 to 5.5 V or 2.4 to 5.5 V, Vss = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width		2			µs
$t_{C(XIN)}$	External clock input cycle time	Vcc = 2.2 to 5.5 V	500			ns
		Vcc = 2.4 to 5.5 V	250			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	Vcc = 2.2 to 5.5 V	200			ns
		Vcc = 2.4 to 5.5 V	100			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	Vcc = 2.2 to 5.5 V	200			ns
		Vcc = 2.4 to 5.5 V	100			ns
$t_{C(CNTR0)}$	CNTR0 input cycle time	Vcc = 2.2 to 5.5 V	1000			ns
		Vcc = 2.4 to 5.5 V	500			ns
$t_{WH(CNTR0)}$	CNTR0, INT0, INT1, input “H” pulse width	Vcc = 2.2 to 5.5 V	460			ns
		Vcc = 2.4 to 5.5 V	230			ns
$t_{WL(CNTR0)}$	CNTR0, INT0, INT1, input “L” pulse width	Vcc = 2.2 to 5.5 V	460			ns
		Vcc = 2.4 to 5.5 V	230			ns
$t_{C(CNTR1)}$	CNTR1 input cycle time	Vcc = 2.2 to 5.5 V	TBD			ns
		Vcc = 2.4 to 5.5 V	TBD			ns
$t_{WH(CNTR1)}$	CNTR1 input “H” pulse width	Vcc = 2.2 to 5.5 V	TBD			ns
		Vcc = 2.4 to 5.5 V	TBD			ns
$t_{WL(CNTR1)}$	CNTR1 input “L” pulse width	Vcc = 2.2 to 5.5 V	TBD			ns
		Vcc = 2.4 to 5.5 V	TBD			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time	Vcc = 2.2 to 5.5 V	TBD			ns
		Vcc = 2.4 to 5.5 V	TBD			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width	Vcc = 2.2 to 5.5 V	TBD			ns
		Vcc = 2.4 to 5.5 V	TBD			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width	Vcc = 2.2 to 5.5 V	TBD			ns
		Vcc = 2.4 to 5.5 V	TBD			ns
$t_{su(SDATA1–SCLK1)}$	Serial I/O1 input set up time		TBD			ns
$t_{h(SCLK1–SDATA1)}$	Serial I/O1 input hold time		TBD			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	Vcc = 2.2 to 5.5 V	4000			ns
		Vcc = 2.4 to 5.5 V	2000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	Vcc = 2.2 to 5.5 V	1900			ns
		Vcc = 2.4 to 5.5 V	950			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	Vcc = 2.2 to 5.5 V	1900			ns
		Vcc = 2.4 to 5.5 V	950			ns
$t_{su(SDATA2–SCLK2)}$	Serial I/O2 input set up time		400			ns
$t_{h(SCLK2–SDATA2)}$	Serial I/O2 input hold time		400			ns

Switching Characteristics (Extended operating temperature version)

Table 22 Switching characteristics (1) (V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

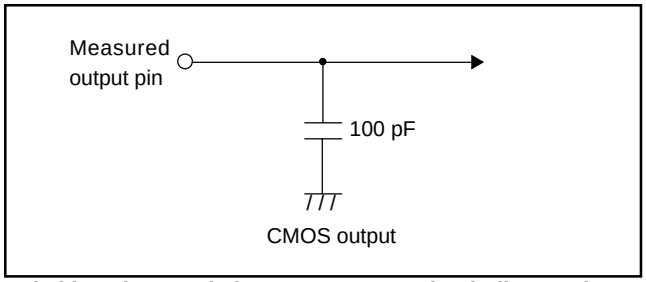
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH}(SCLK1)	Serial I/O1 clock output “H” pulse width	t_C(SCLK1)/2–30			ns
t_{WL}(SCLK1)	Serial I/O1 clock output “L” pulse width	t_C(SCLK1)/2–30			ns
t_d(SCLK1–TxD1)	Serial I/O1 output delay time			140	ns
t_v(SCLK1–TxD1)	Serial I/O1 output valid time	–30			ns
t_r(SCLK1)	Serial I/O1 clock output rising time			30	ns
t_f(SCLK1)	Serial I/O1 clock output falling time			30	ns
t_{WH}(SCLK2)	Serial I/O2 clock output “H” pulse width	t_C(SCLK2)/2–30			ns
t_{WL}(SCLK2)	Serial I/O2 clock output “L” pulse width	t_C(SCLK2)/2–30			ns
t_d(SCLK2–SDATA2)	Serial I/O2 output delay time			140	ns
t_v(SCLK2–SDATA2)	Serial I/O2 output valid time	0			ns
t_r(SCLK2)	Serial I/O2 clock output rising time			30	ns
t_f(SCLK2)	Serial I/O2 clock output falling time			30	ns
t_r(CMOS)	CMOS output rising time (Note 1)		10	30	ns
t_f(CMOS)	CMOS output falling time (Note 1)		10	30	ns

Note 1: Pin XOUT is excluded.

Table 23 Switching characteristics (2) (V_{CC} = 2.2 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH}(SCLK1)	Serial I/O1 clock output “H” pulse width	TBD			ns
t_{WL}(SCLK1)	Serial I/O1 clock output “L” pulse width	TBD			ns
t_d(SCLK1–TxD1)	Serial I/O1 output delay time			TBD	ns
t_v(SCLK1–TxD1)	Serial I/O1 output valid time	TBD			ns
t_r(SCLK1)	Serial I/O1 clock output rising time			TBD	ns
t_f(SCLK1)	Serial I/O1 clock output falling time			TBD	ns
t_{WH}(SCLK2)	Serial I/O2 clock output “H” pulse width	t_C(SCLK2)/2–50			ns
t_{WL}(SCLK2)	Serial I/O2 clock output “L” pulse width	t_C(SCLK2)/2–50			ns
t_d(SCLK2–SDATA2)	Serial I/O2 output delay time			350	ns
t_v(SCLK2–SDATA2)	Serial I/O2 output valid time	0			ns
t_r(SCLK2)	Serial I/O2 clock output rising time			50	ns
t_f(SCLK2)	Serial I/O2 clock output falling time			50	ns
t_r(CMOS)	CMOS output rising time (Note 1)		20	50	ns
t_f(CMOS)	CMOS output falling time (Note 1)		20	50	ns

Note 1: Pin XOUT is excluded.



Switching characteristics measurement circuit diagram (General purpose)

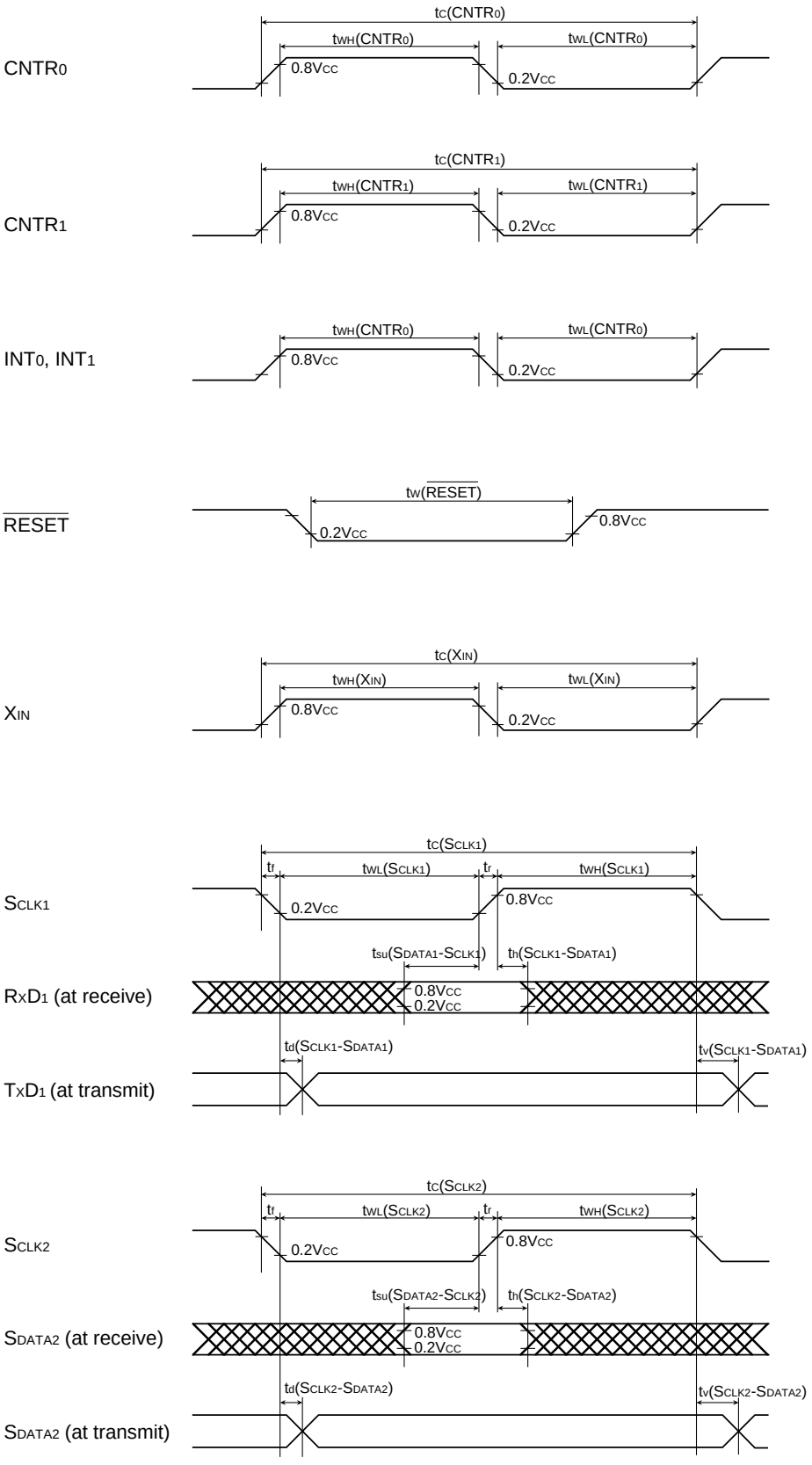


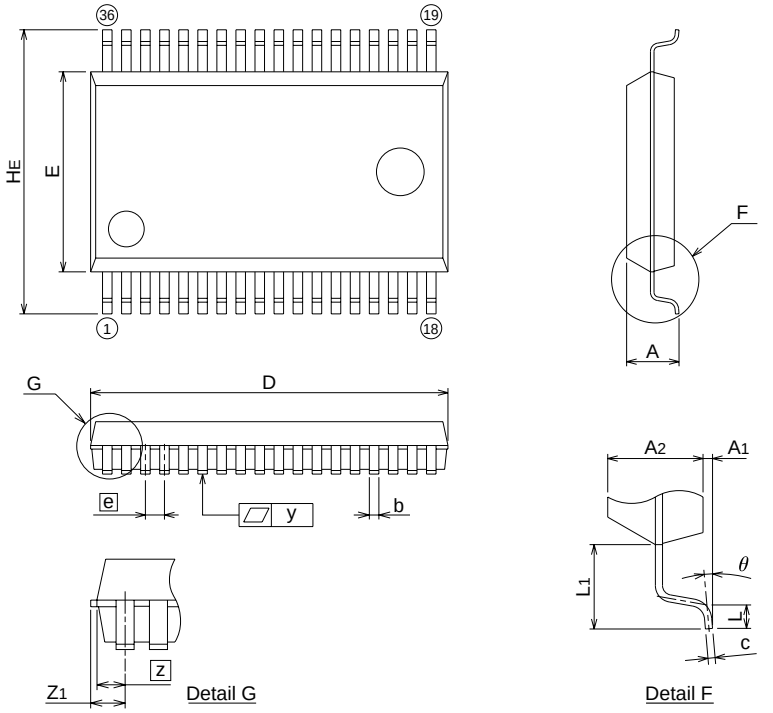
Fig. 52 Timing chart (Extended operating temperature version)

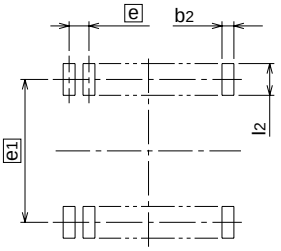
PACKAGE OUTLINE

36P2R-A

Plastic 36pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP36-P-450-0.80	–	0.53	Alloy 42





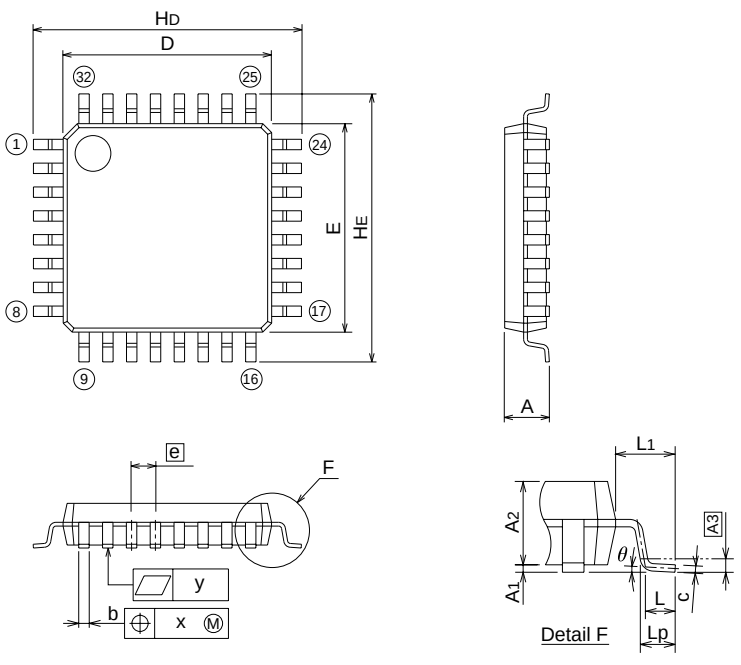
Recommended Mount Pad

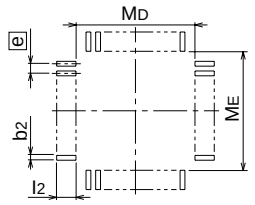
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A1	0.05	–	–
A2	–	2.0	–
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	14.8	15.0	15.2
E	8.2	8.4	8.6
e	–	0.8	–
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	–	1.765	–
z	–	0.7	–
Z1	–	–	0.85
y	–	–	0.15
θ	0°	–	10°
b2	–	0.5	–
e1	–	11.43	–
I2	1.27	–	–

32P6B-A

Plastic 32pin 7×7mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP32-P-77-0.80	–	0.17	Alloy 42





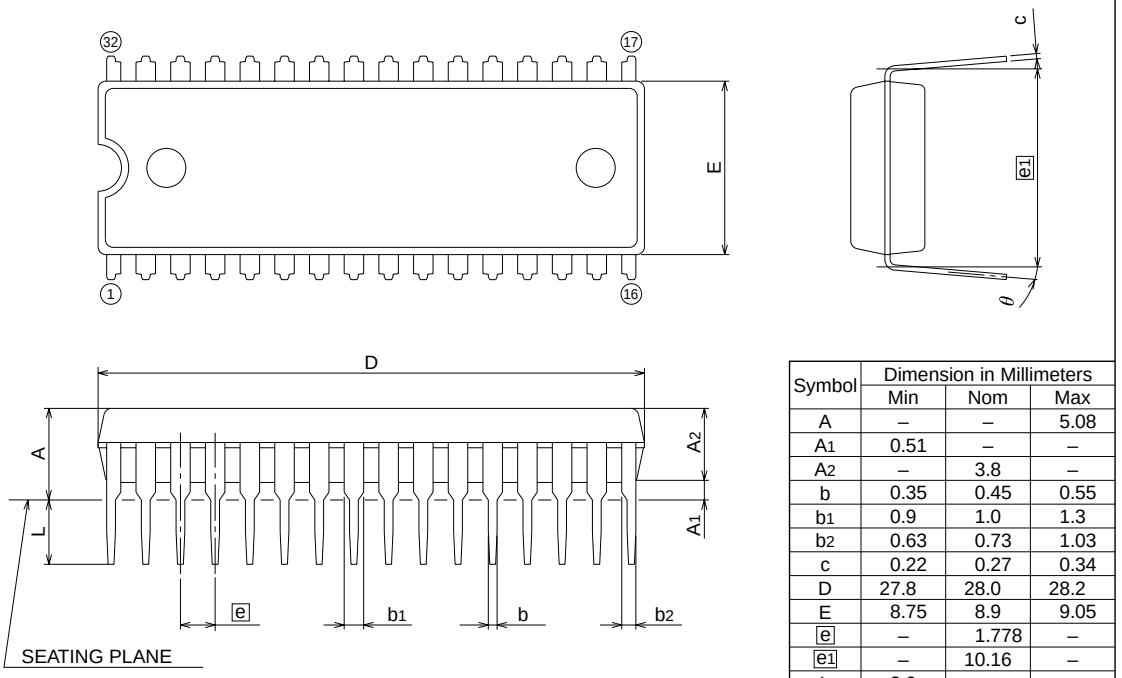
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.3	0.35	0.45
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.8	–
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.2
y	–	–	0.1
θ	0°	–	10°
b2	–	0.5	–
I2	1.0	–	–
MD	–	7.4	–
ME	–	7.4	–

32P4B

Plastic 32pin 400mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP32-P-400-1.78	–	2.2	Alloy 42/Cu Alloy



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.08
A_1	0.51	–	–
A_2	–	3.8	–
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	27.8	28.0	28.2
E	8.75	8.9	9.05
e	–	1.778	–
e1	–	10.16	–
L	3.0	–	–
θ	0°	–	15°

7540 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

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MITSUBISHI ELECTRIC

REVISION HISTORY	7540 Group DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	991122