

# **±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

## **General Description**

The MAX3372E–MAX3379E and MAX3390E–MAX3393E ±15kV ESD-protected level translators provide the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, V<sub>CC</sub> and V<sub>L</sub>, set the logic levels on either side of the device. A low-voltage logic signal present on the V<sub>L</sub> side of the device appears as a high-voltage logic signal on the V<sub>CC</sub> side of the device, and vice-versa. The MAX3374E/MAX3375E/MAX3376E/MAX3379E and MAX3390E–MAX3393E unidirectional level translators level shift data in one direction (V<sub>L</sub> → V<sub>CC</sub> or V<sub>CC</sub> → V<sub>L</sub>) on any single data line. The MAX3372E/MAX3373E and MAX3377E/MAX3378E bidirectional level translators utilize a transmission-gate-based design (Figure 2) to allow data translation in either direction (V<sub>L</sub> ↔ V<sub>CC</sub>) on any single data line. The MAX3372E–MAX3379E and MAX3390E–MAX3393E accept V<sub>L</sub> from +1.2V to +5.5V and V<sub>CC</sub> from +1.65V to +5.5V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

All devices in the MAX3372E–MAX3379E, MAX3390E–MAX3393E family feature a three-state output mode that reduces supply current to less than 1µA, thermal short-circuit protection, and ±15kV ESD protection on the V<sub>CC</sub> side for greater protection in applications that route signals externally. The MAX3372E/MAX3377E operate at a guaranteed data rate of 230kbps. Slew-rate limiting reduces EMI emissions in all 230kbps devices. The MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E operate at a guaranteed data rate of 8Mbps over the entire specified operating voltage range. Within specific voltage domains, higher data rates are possible. (See *Timing Characteristics*.)

The MAX3372E–MAX3376E are dual level shifters available in 3 × 3 UCSP™ and 8-pin SOT23-8 packages. The MAX3377E/MAX3378E/MAX3379E and MAX3390E–MAX3393E are quad level shifters available in 3 × 4 UCSP and 14-pin TSSOP packages.

## **Applications**

- SPI™, MICROWIRE™, and I<sup>2</sup>C™ Level Translation
- Low-Voltage ASIC Level Translation
- Smart Card Readers
- Cell-Phone Cradles
- Portable POS Systems
- Portable Communication Devices
- Low-Cost Serial Interfaces
- Cell Phones
- GPS
- Telecommunications Equipment



## **Features**

- ♦ Guaranteed Data Rate Options  
230kbps  
8Mbps (+1.2V ≤ V<sub>L</sub> ≤ V<sub>CC</sub> ≤ +5.5V)  
10Mbps (+1.2V ≤ V<sub>L</sub> ≤ V<sub>CC</sub> ≤ +3.3V)  
16Mbps (+1.8V ≤ V<sub>L</sub> ≤ V<sub>CC</sub> ≤ +2.5V and +2.5V ≤ V<sub>L</sub> ≤ V<sub>CC</sub> ≤ +3.3V)
- ♦ Bidirectional Level Translation  
(MAX3372E/MAX3373E and  
MAX3377E/MAX3378E)
- ♦ Operation Down to +1.2V on V<sub>L</sub>
- ♦ ±15kV ESD Protection on I/O V<sub>CC</sub> Lines
- ♦ Ultra-Low 1µA Supply Current in Three-State Output Mode
- ♦ Low-Quiescent Current (130µA typ)
- ♦ UCSP, SOT, and TSSOP Packages
- ♦ Thermal Short-Circuit Protection

## **Ordering Information**

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX3372EEKA-T	-40°C to +85°C	8 SOT23-8

*Ordering Information continued at end of data sheet.  
Selector Guide appears at end of data sheet.*

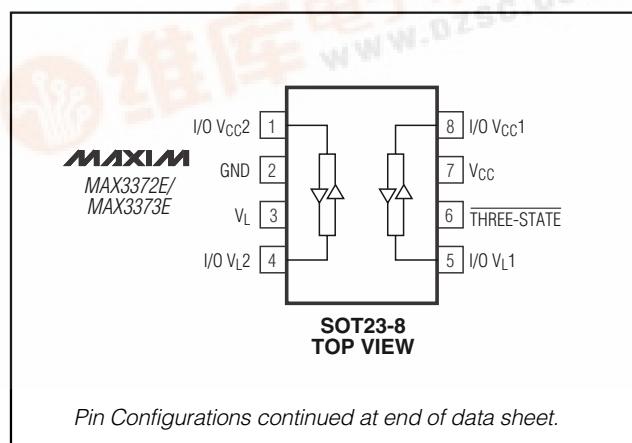
UCSP is a trademark of Maxim Integrated Products, Inc.

SPI is a trademark of Motorola, Inc.

I<sup>2</sup>C is a trademark of Phillips Corp.

MICROWIRE is a trademark of National Semiconductor Corp.

## **Pin Configurations**



*Pin Configurations continued at end of data sheet.*

**MAX3372E-MAX3379E/MAX3390E-MAX3393E**

# ***±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP***

## **ABSOLUTE MAXIMUM RATINGS**

All Voltages Referenced to GND

V <sub>CC</sub>	.....	-0.3V to +6V
I/O V <sub>CC</sub> _	.....	-0.3V to (V <sub>CC</sub> + 0.3V)
I/O V <sub>L</sub> _	.....	-0.3V to (V <sub>L</sub> + 0.3V)
THREE-STATE	.....	-0.3V to (V <sub>L</sub> + 0.3V)
Short-Circuit Duration I/O V <sub>L</sub> , I/O V <sub>CC</sub> to GND	.....	Continuous
Short-Circuit Duration I/O V <sub>L</sub> or I/O V <sub>CC</sub> to GND Driven from 40mA Source (except MAX3372E and MAX3377E)	.....	Continuous

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

8-Pin SOT23 (derate 8.9mW/°C above +70°C)	.....	714mW
3 x 3 UCSP (derate 4.7mW/°C above +70°C)	.....	379mW
3 x 4 UCSP (derate 6.5mW/°C above +70°C)	.....	579mW
14-Pin TSSOP (derate 9.1mW/°C above +70°C)	.....	727mW

Operating Temperature Range ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## **ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub> = +1.65V to +5.5V, V<sub>L</sub> = +1.2V to (V<sub>CC</sub> + 0.3V), GND = 0, I/O V<sub>L</sub>\_ and I/O V<sub>CC</sub>\_ unconnected, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V<sub>CC</sub> = +3.3V, V<sub>L</sub> = +1.8V, T<sub>A</sub> = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLIES</b>						
V <sub>L</sub> Supply Range	V <sub>L</sub>		1.2	5.5		V
V <sub>CC</sub> Supply Range	V <sub>CC</sub>		1.65	5.50		V
Supply Current from V <sub>CC</sub>	I <sub>QVCC</sub>		130	300		µA
Supply Current from V <sub>L</sub>	I <sub>QVL</sub>		16	100		µA
V <sub>CC</sub> Three-State Output Mode Supply Current	I <sub>THREE-STATE-VCC</sub>	T <sub>A</sub> = +25°C, THREE-STATE = GND	0.03	1		µA
V <sub>L</sub> Three-State Output Mode Supply Current	I <sub>THREE-STATE-VL</sub>	T <sub>A</sub> = +25°C, THREE-STATE = GND	0.03	1		µA
Three-State Output Mode Leakage Current I/O V <sub>L</sub> _ and I/O V <sub>CC</sub> _	I <sub>THREE-STATE-LKG</sub>	T <sub>A</sub> = +25°C, THREE-STATE = GND	0.02	1		µA
THREE-STATE Pin Input Leakage		T <sub>A</sub> = +25°C	0.02	1		µA
<b>ESD PROTECTION</b>						
I/O V <sub>CC</sub> (Note 3)		IEC 1000-4-2 Air-Gap Discharge	±8	kV		
		IEC 1000-4-2 Contact Discharge	±8			
		Human Body Model	±15			
<b>LOGIC-LEVEL THRESHOLDS (MAX3372E/MAX3377E)</b>						
I/O V <sub>L</sub> _ Input Voltage High	V <sub>IHL</sub>		V <sub>L</sub> - 0.2		V	
I/O V <sub>L</sub> _ Input Voltage Low	V <sub>ILL</sub>		0.15		V	

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## **ELECTRICAL CHARACTERISTICS (continued)**

( $V_{CC} = +1.65V$  to  $+5.5V$ ,  $V_L = +1.2V$  to  $(V_{CC} + 0.3V)$ , GND = 0, I/O  $V_{L\_}$  and I/O  $V_{CC\_}$  unconnected,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = +3.3V$ ,  $V_L = +1.8V$ ,  $T_A = +25^\circ C$ .) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Input Voltage High	$V_{IHC}$		$V_{CC} - 0.4$			V
I/O $V_{CC\_}$ Input Voltage Low	$V_{ILC}$			0.15		V
I/O $V_{L\_}$ Output Voltage High	$V_{OHL}$	I/O $V_{L\_}$ source current = 20 $\mu A$ , I/O $V_{CC\_} \geq V_{CC} - 0.4V$	0.67 $\times V_L$			V
I/O $V_{L\_}$ Output Voltage Low	$V_{OLL}$	I/O $V_{L\_}$ sink current = 20 $\mu A$ , I/O $V_{CC\_} \leq 0.15V$		0.4		V
I/O $V_{CC\_}$ Output Voltage High	$V_{OHC}$	I/O $V_{CC\_}$ source current = 20 $\mu A$ , I/O $V_{L\_} \geq V_L - 0.2V$	0.67 $\times V_{CC}$			V
I/O $V_{CC\_}$ Output Voltage Low	$V_{OLC}$	I/O $V_{CC\_}$ sink current = 20 $\mu A$ , I/O $V_{L\_} \leq 0.15V$		0.4		V
THREE-STATE Input Voltage High	$V_{IL-THREE-STATE}$		$V_L - 0.2$			V
THREE-STATE Input Voltage Low	$V_{IL-THREE-STATE}$			0.15		V

## **LOGIC-LEVEL THRESHOLDS (MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E)**

I/O $V_{L\_}$ Input Voltage High	$V_{IHL}$		$V_L - 0.2$		V
I/O $V_{L\_}$ Input Voltage Low	$V_{ILL}$			0.15	V
I/O $V_{CC\_}$ Input Voltage High	$V_{IHC}$		$V_{CC} - 0.4$		V
I/O $V_{CC\_}$ Input Voltage Low	$V_{ILC}$			0.15	V
I/O $V_{L\_}$ Output Voltage High	$V_{OHL}$	I/O $V_{L\_}$ source current = 20 $\mu A$ , I/O $V_{CC\_} \geq V_{CC} - 0.4V$	0.67 $\times V_L$		V
I/O $V_{L\_}$ Output Voltage Low	$V_{OLL}$	I/O $V_{L\_}$ sink current = 1mA, I/O $V_{CC\_} \leq 0.15V$		0.4	V
I/O $V_{CC\_}$ Output Voltage High	$V_{OHC}$	I/O $V_{CC\_}$ source current = 20 $\mu A$ , I/O $V_{L\_} \geq V_L - 0.2V$	0.67 $\times V_{CC}$		V
I/O $V_{CC\_}$ Output Voltage Low	$V_{OLC}$	I/O $V_{CC\_}$ sink current = 1mA, I/O $V_{L\_} \leq 0.15V$		0.4	V
THREE-STATE Input Voltage High	$V_{IH-THREE-STATE}$		$V_L - 0.2$		V
THREE-STATE Input Voltage Low	$V_{IL-THREE-STATE}$			0.15	V

## ***±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP***

### **TIMING CHARACTERISTICS**

( $V_{CC} = +1.65V$  to  $+5.5V$ ,  $V_L = +1.2V$  to  $(V_{CC} + 0.3V)$ , GND = 0,  $R_{LOAD} = 1M\Omega$ , I/O test signal of Figure 1,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = +3.3V$ ,  $V_L = +1.8V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>MAX3372E/MAX3377E (<math>C_{LOAD} = 50pF</math>)</b>						
I/O $V_{CC\_}$ Rise Time (Note 4)	$t_{RVCC}$		1100			ns
I/O $V_{CC\_}$ Fall Time (Note 5)	$t_{FVCC}$		1000			ns
I/O $V_{L\_}$ Rise Time (Note 4)	$t_{RVL}$		600			ns
I/O $V_{L\_}$ Fall Time (Note 5)	$t_{FVL}$		1100			ns
Propagation Delay	I/O $V_{L\_}$ - $V_{CC}$	Driving I/O $V_{L\_}$		1.6		$\mu s$
	I/O $V_{CC\_}$ - $V_L$	Driving I/O $V_{CC\_}$		1.6		
Channel-to-Channel Skew	$t_{SKEW}$	Each translator equally loaded	500			ns
Maximum Data Rate		$C_L = 25pF$	230			kbps
<b>MAX3373E-MAX3376E/MAX3378E/MAX3379E and MAX3390E-MAX3393E (<math>C_{LOAD} = 15pF</math>, Driver Output Impedance <math>\leq 50\Omega</math>)</b>						
<b>+1.2V <math>\leq V_L \leq V_{CC} \leq +5.5V</math></b>						
I/O $V_{CC\_}$ Rise Time (Note 4)	$t_{RVCC}$		7	25		ns
		Open-drain driving	170	400		
I/O $V_{CC\_}$ Fall Time (Note 5)	$t_{FVCC}$		6	37		ns
		Open-drain driving	20	50		
I/O $V_{L\_}$ Rise Time (Note 4)	$t_{RVL}$		8	30		ns
		Open-drain driving	180	400		
I/O $V_{L\_}$ Fall Time (Note 5)	$t_{LFV}$		3	30		ns
		Open-drain driving	30	60		
Propagation Delay	I/O $V_{L\_}$ - $V_{CC}$	Driving I/O $V_{L\_}$	5	30		ns
			210	1000		
	I/O $V_{CC\_}$ - $V_L$	Driving I/O $V_{CC\_}$	4	30		
Channel-to-Channel Skew	$t_{SKEW}$	Each translator equally loaded	190	1000		ns
			20			
Maximum Data Rate			50			ns
		Open-drain driving	8			
			500			Mbps
						kbps

# **$\pm 15\text{kV}$ ESD-Protected, $1\mu\text{A}$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

## **TIMING CHARACTERISTICS (continued)**

( $V_{CC} = +1.65\text{V}$  to  $+5.5\text{V}$ ,  $V_L = +1.2\text{V}$  to  $(V_{CC} + 0.3\text{V})$ ,  $GND = 0$ ,  $R_{LOAD} = 1\text{M}\Omega$ , I/O test signal of Figure 1,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{CC} = +3.3\text{V}$ ,  $V_L = +1.8\text{V}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b><math>+1.2\text{V} \leq V_L \leq V_{CC} \leq +3.3\text{V}</math></b>						
I/O $V_{CC\_}$ Rise Time (Note 4)	$t_{RVCC}$			25		ns
I/O $V_{CC\_}$ Fall Time (Note 5)	$t_{FVCC}$			30		ns
I/O $V_L\_$ Rise Time (Note 4)	$t_{RVL}$			30		ns
I/O $V_L\_$ Fall Time (Note 5)	$t_{FVL}$			30		ns
Propagation Delay	I/OVL-VCC	Driving I/O $V_L\_$		20		ns
	I/OVCC-VL	Driving I/O $V_{CC\_}$		20		
Channel-to-Channel Skew	$t_{SKEW}$	Each translator equally loaded		10		ns
Maximum Data Rate			10			Mbps
<b><math>+2.5\text{V} \leq V_L \leq V_{CC} \leq +3.3\text{V}</math></b>						
I/O $V_{CC\_}$ Rise Time (Note 4)	$t_{RVCC}$			15		ns
I/O $V_{CC\_}$ Fall Time (Note 5)	$t_{FVCC}$			15		ns
I/O $V_L\_$ Rise Time (Note 4)	$t_{RVL}$			15		ns
I/O $V_L\_$ Fall Time (Note 5)	$t_{FVL}$			15		ns
Propagation Delay	I/OVL-VCC	Driving I/O $V_L\_$		15		ns
	I/OVCC-VL	Driving I/O $V_{CC\_}$		15		
Channel-to-Channel Skew	$t_{SKEW}$	Each translator equally loaded		10		ns
Maximum Data Rate			16			Mbps
<b><math>+1.8\text{V} \leq V_L \leq V_{CC} \leq +2.5\text{V}</math></b>						
I/O $V_{CC\_}$ Rise Time (Note 4)	$t_{RVCC}$			15		ns
I/O $V_{CC\_}$ Fall Time (Note 5)	$t_{FVCC}$			15		ns
I/O $V_L\_$ Rise Time (Note 4)	$t_{RVL}$			15		ns
I/O $V_L\_$ Fall Time (Note 5)	$t_{FVL}$			15		ns
Propagation Delay	I/OVL-VCC	Driving I/O $V_L\_$		15		ns
	I/OVCC-VL	Driving I/O $V_{CC\_}$		15		
Channel-to-Channel Skew	$t_{SKEW}$	Each translator equally loaded		10		ns
Maximum Data Rate			16			Mbps

**Note 1:** All units are 100% production tested at  $T_A = +25^\circ\text{C}$ . Limits over the operating temperature range are guaranteed by design and not production tested.

**Note 2:** For normal operation, ensure  $V_L < (V_{CC} + 0.3\text{V})$ . During power-up,  $V_L > (V_{CC} + 0.3\text{V})$  will not damage the device.

**Note 3:** To ensure maximum ESD protection, place a  $1\mu\text{F}$  capacitor between  $V_{CC}$  and GND. See *Applications Circuits*.

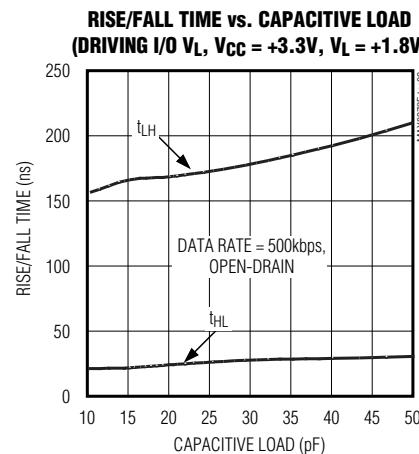
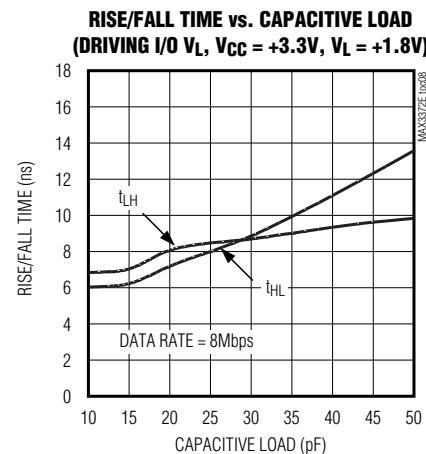
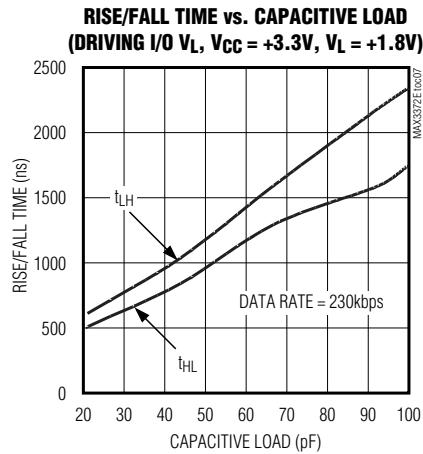
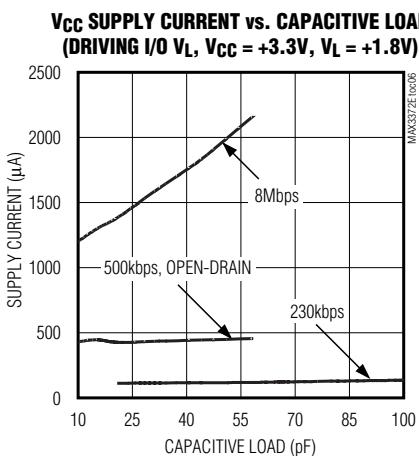
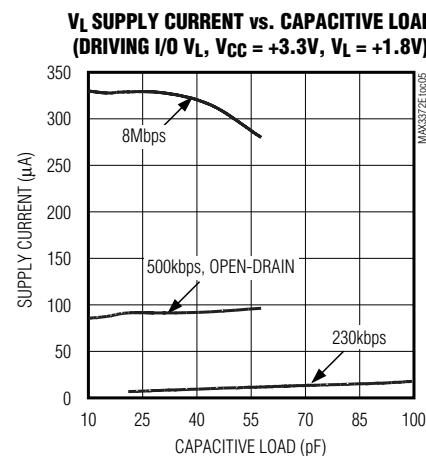
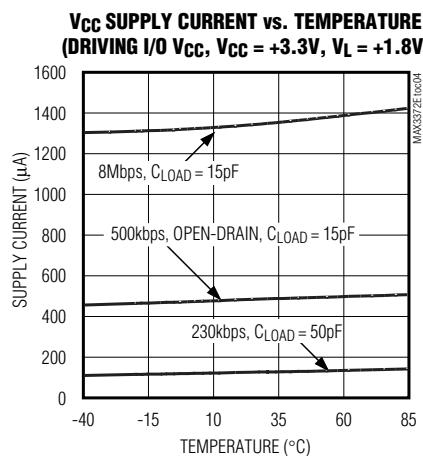
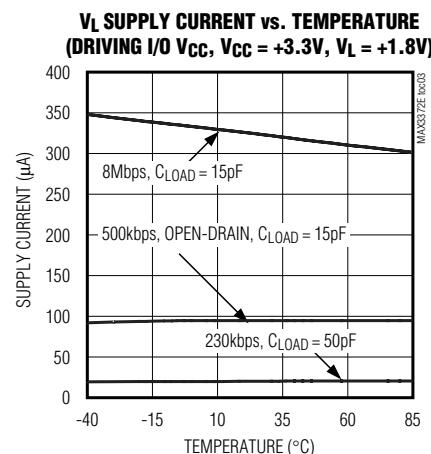
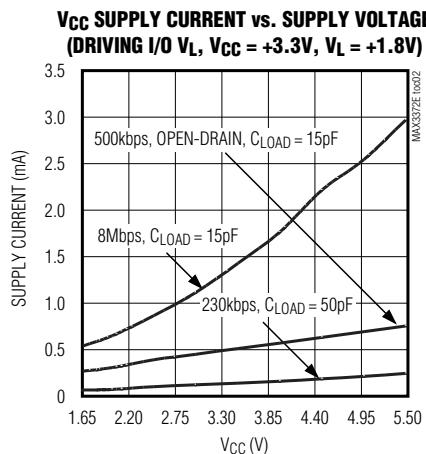
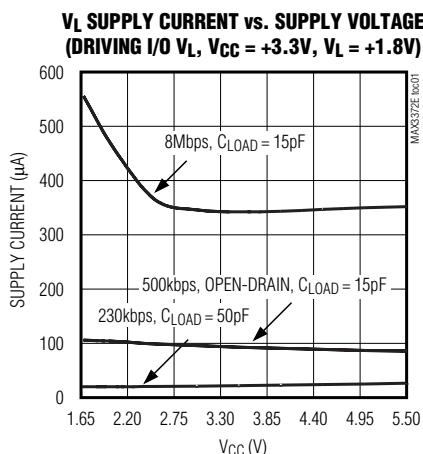
**Note 4:** 10% to 90%

**Note 5:** 90% to 10%

## **$\pm 15kV$ ESD-Protected, $1\mu A$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

### **Typical Operating Characteristics**

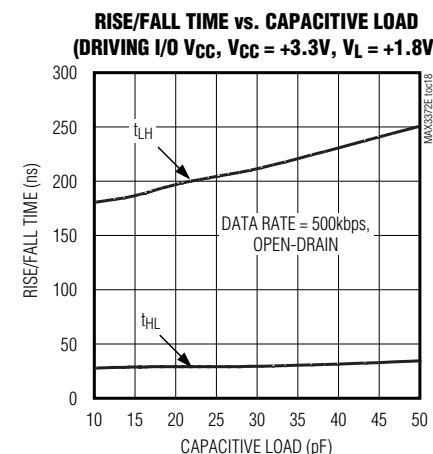
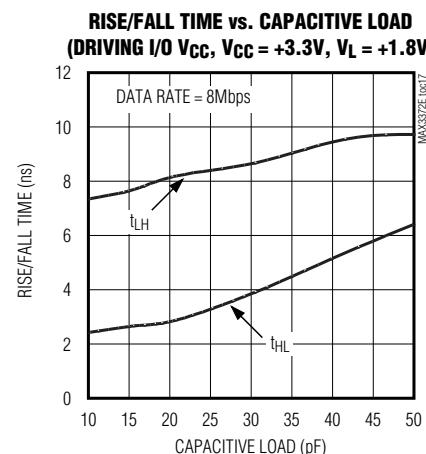
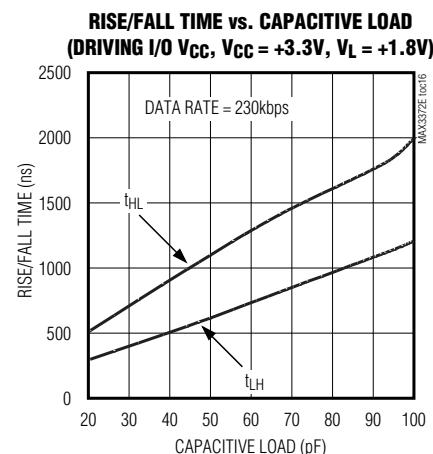
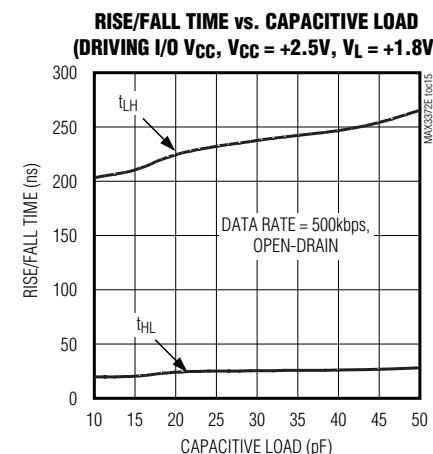
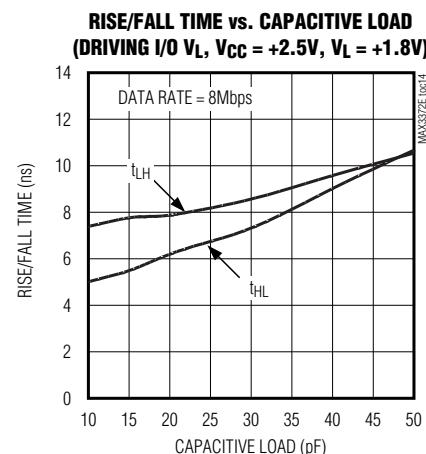
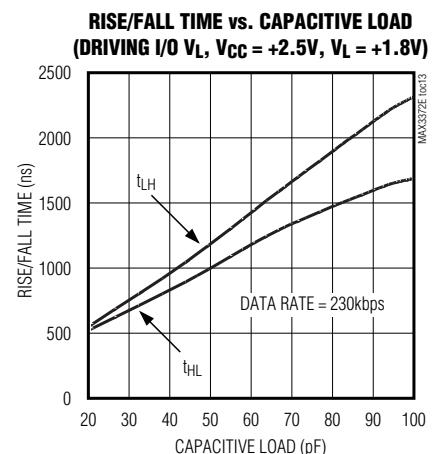
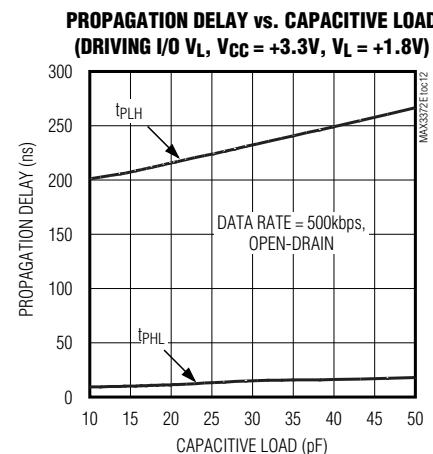
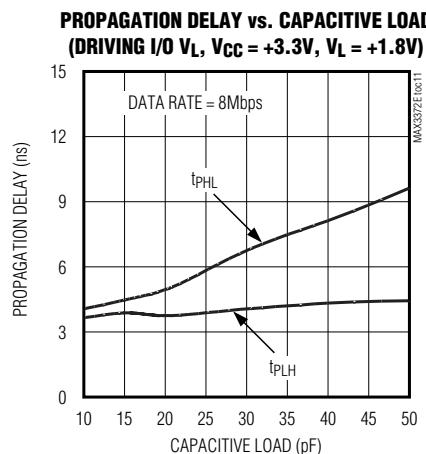
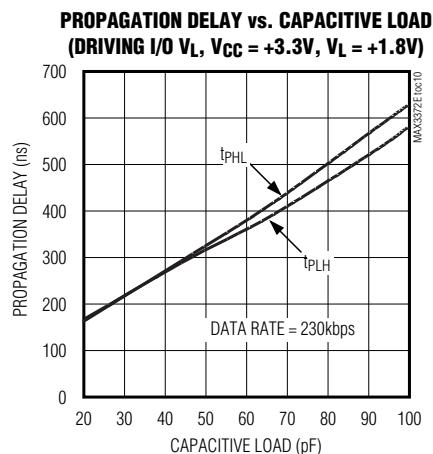
( $R_L = 1M\Omega$ ,  $T_A = +25^\circ C$ , unless otherwise noted. All 230kbps TOCs apply to MAX3372E/MAX3377E only. All 8Mbps and 500kbps TOCs apply to MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E only.)



# **$\pm 15kV$ ESD-Protected, $1\mu A$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

## **Typical Operating Characteristics (continued)**

( $R_L = 1M\Omega$ ,  $T_A = +25^\circ C$ , unless otherwise noted. All 230kbps TOCs apply to MAX3372E/MAX3377E only. All 8Mbps and 500kbps TOCs apply to MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E only.)

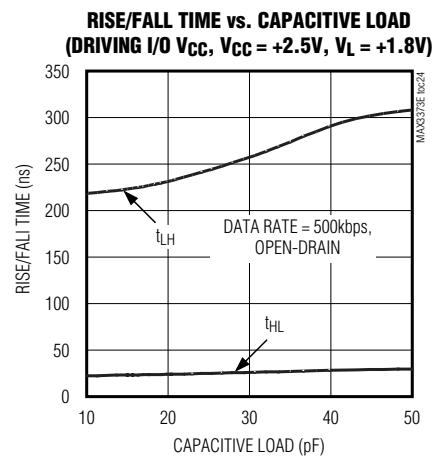
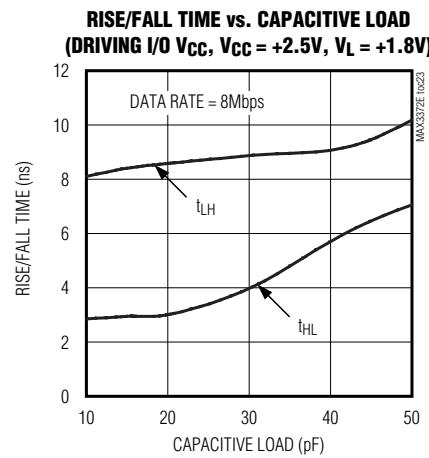
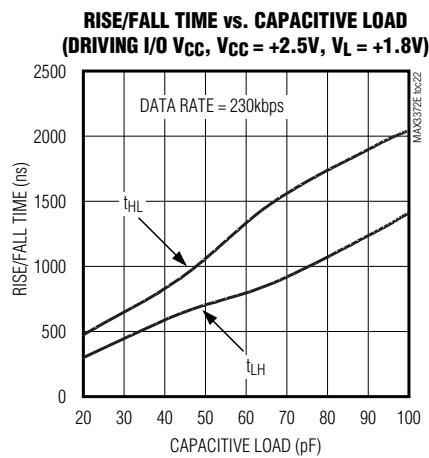
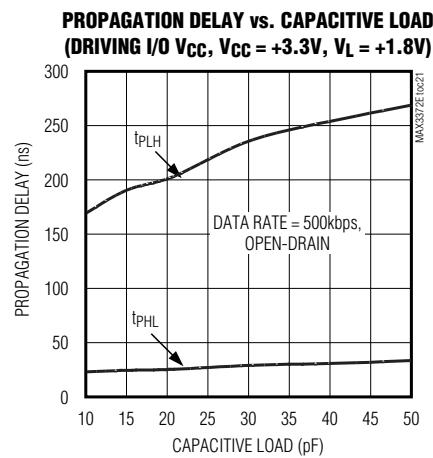
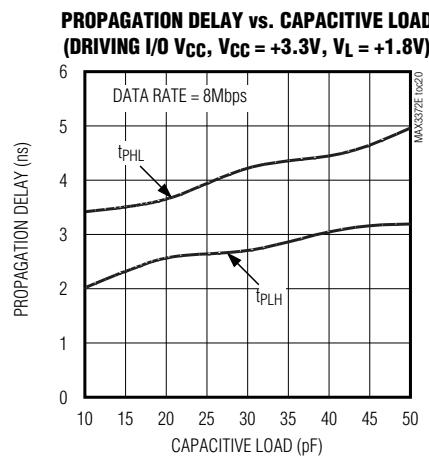
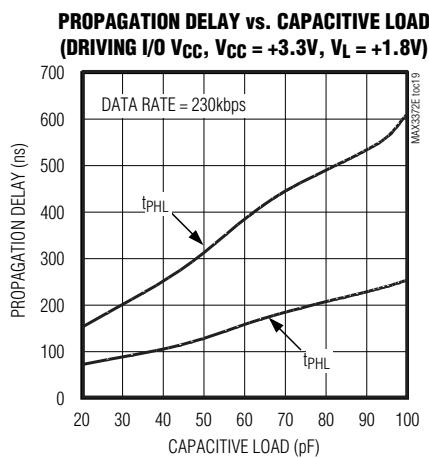


**MAX3372E-MAX3379E/MAX3390E-MAX3393E**

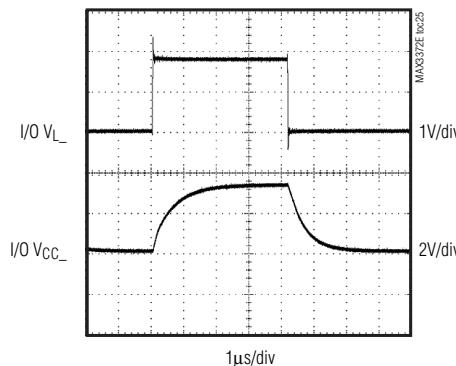
## **$\pm 15kV$ ESD-Protected, $1\mu A$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

### **Typical Operating Characteristics (continued)**

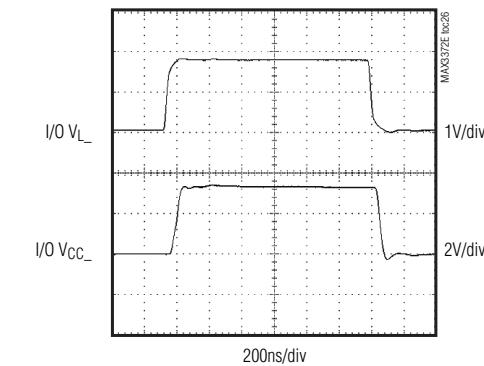
( $R_L = 1M\Omega$ ,  $T_A = +25^\circ C$ , unless otherwise noted. All 230kbps TOCs apply to MAX3372E/MAX3377E only. All 8Mbps and 500kbps TOCs apply to MAX3373E-MAX3376E/MAX3378E/MAX3379E and MAX3390E-MAX3393E only.)



**RAIL-TO-RAIL DRIVING  
(DRIVING I/O  $V_L$ ,  $V_{CC} = +3.3V$ ,  $V_L = +1.8V$ ,  
 $C_L = 50pF$ , DATA RATE = 230kbps)**



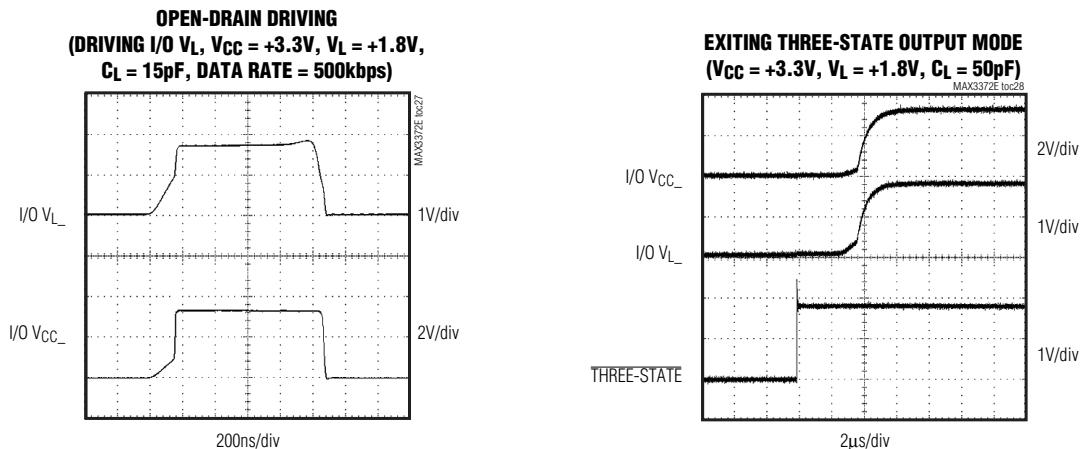
**RAIL-TO-RAIL DRIVING  
(DRIVING I/O  $V_L$ ,  $V_{CC} = +3.3V$ ,  $V_L = +1.8V$ ,  
 $C_L = 15pF$ , DATA RATE = 8Mbps)**



# **$\pm 15kV$ ESD-Protected, $1\mu A$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

## **Typical Operating Characteristics (continued)**

( $R_L = 1M\Omega$ ,  $T_A = +25^\circ C$ , unless otherwise noted. All 230kbps TOCs apply to MAX3372E/MAX3377E only. All 8Mbps and 500kbps TOCs apply to MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E only.)



## **Pin Description**

<b>PIN</b>				<b>NAME</b>	<b>FUNCTION</b>
<b>3 x 4 UCSP</b>	<b>TSSOP</b>	<b>SOT23-8</b>	<b>3 x 3 UCSP</b>		
A1	2	5	C2	I/O $V_{L1}$	Input/Output 1. Referenced to $V_L$ . (Note 6)
A2	3	4	C3	I/O $V_{L2}$	Input/Output 2. Referenced to $V_L$ . (Note 6)
A3	4	—	—	I/O $V_{L3}$	Input/Output 3. Referenced to $V_L$ . (Note 6)
A4	5	—	—	I/O $V_{L4}$	Input/Output 4. Referenced to $V_L$ . (Note 6)
B1	14	7	A1	$V_{CC}$	$V_{CC}$ Input Voltage $+1.65V \leq V_{CC} \leq +5.5V$ .
B2	1	3	C1	$V_L$	Logic Input Voltage $+1.2V \leq V_L \leq (V_{CC} + 0.3V)$
B3	8	6	B1	THREE-STATE	Three-State Output Mode Enable. Pull THREE-STATE low to place device in three-state output mode. I/O $V_{CC}$ and I/O $V_L$ are high impedance in three-state output mode. NOTE: Logic referenced to $V_L$ (for logic thresholds see Electrical Characteristics).
B4	7	2	B3	GND	Ground
C1	13	8	A2	I/O $V_{CC1}$	Input/Output 1. Referenced to $V_{CC}$ . (Note 6)
C2	12	1	A3	I/O $V_{CC2}$	Input/Output 2. Referenced to $V_{CC}$ . (Note 6)
C3	11	—	—	I/O $V_{CC3}$	Input/Output 3. Referenced to $V_{CC}$ . (Note 6)
C4	10	—	—	I/O $V_{CC4}$	Input/Output 4. Referenced to $V_{CC}$ . (Note 6)
—	6, 9	—	B2	N.C.	No Connection. Not internally connected.

**Note 6:** For unidirectional devices (MAX3374E/MAX3375E/MAX3376E/MAX3379E and MAX3390E–MAX3393E) see *Pin Configurations* for input/output configurations.

## ***±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP***

### **Detailed Description**

The MAX3372E–MAX3379E and MAX3390E–MAX3393E ESD-protected level translators provide the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, V<sub>CC</sub> and V<sub>L</sub>, set the logic levels on either side of the device. A low-voltage logic signal present on the V<sub>L</sub> side of the device appears as a high-voltage logic signal on the V<sub>CC</sub> side of the device, and vice-versa. The MAX3374E/MAX3375E/MAX3376E/MAX3379E and MAX3390E–MAX3393E unidirectional level translators level shift data in one direction (V<sub>L</sub> → V<sub>CC</sub> or V<sub>CC</sub> → V<sub>L</sub>) on any single data line. The MAX3372E/MAX3373E and MAX3377E/MAX3378E bidirectional level translators utilize a transmission-gate-based design (see Figure 2) to allow data translation in either direction (V<sub>L</sub> ↔ V<sub>CC</sub>) on any single data line. The MAX3372E–MAX3379E and MAX3390E–MAX3393E accept V<sub>L</sub> from +1.2V to +5.5V and V<sub>CC</sub> from +1.65V to +5.5V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

All devices in the MAX3372E–MAX3379E, MAX3390E–MAX3393E family feature a three-state output mode that reduces supply current to less than 1µA, thermal short-circuit protection, and ±15kV ESD protection on the V<sub>CC</sub> side for greater protection in applications that route signals externally. The MAX3372E/MAX3377E operate at a guaranteed data rate of 230kbps. Slew-rate limiting reduces EMI emissions in all 230kbps devices. The MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E operate at a guaranteed data rate of 8Mbps over the entire specified operating voltage range. Within specific voltage domains, higher data rates are possible. (See *Timing Characteristics*.)

### **Level Translation**

For proper operation ensure that  $+1.65V \leq V_{CC} \leq +5.5V$ ,  $+1.2V \leq V_L \leq +5.5V$ , and  $V_L \leq (V_{CC} + 0.3V)$ . During power-up sequencing,  $V_L \geq (V_{CC} + 0.3V)$  will not damage the device. During power-supply sequencing, when V<sub>CC</sub> is floating and V<sub>L</sub> is powering up, a current may be sourced, yet the device will not latch up. The speed-up

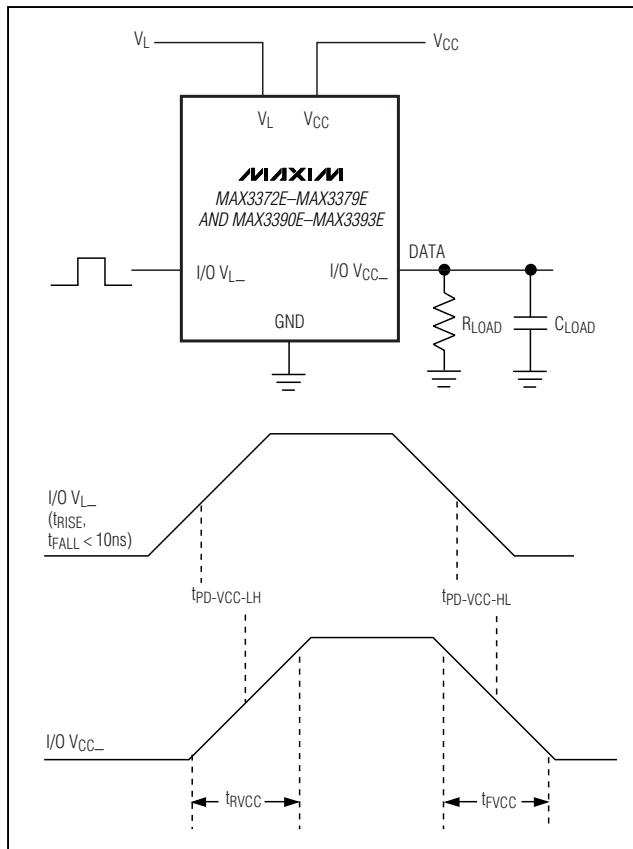


Figure 1a. Rail-to-Rail Driving I/O V<sub>L</sub>

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

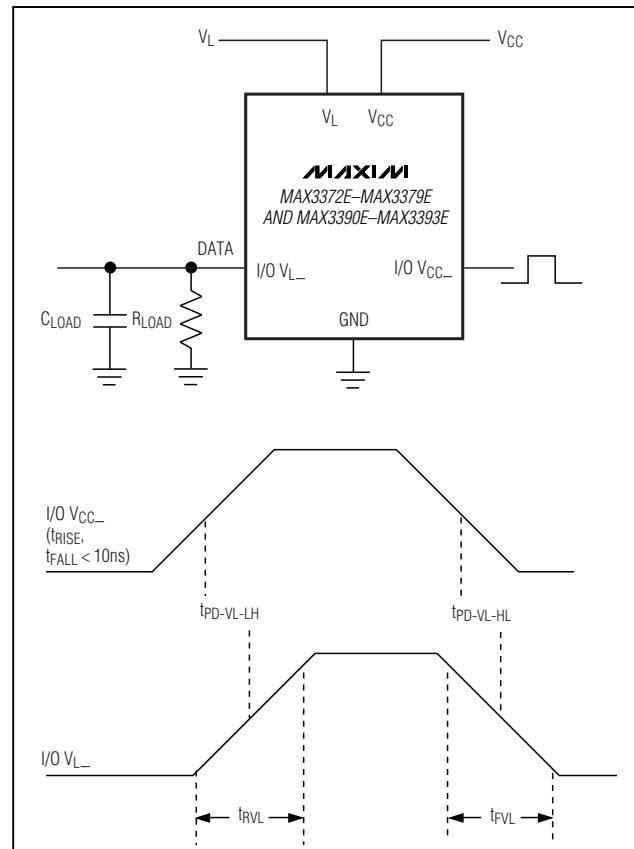


Figure 1b. Rail-to-Rail Driving I/O V<sub>CC</sub>

## **$\pm 15\text{kV}$ ESD-Protected, $1\mu\text{A}$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

circuitry limits the maximum data rate for devices in the MAX3372E–MAX3379E, MAX3390E–MAX3393E family to 16Mbps. The maximum data rate also depends heavily on the load capacitance (see *Typical Operating Characteristics*), output impedance of the driver, and the operational voltage range (see *Timing Characteristics*).

### **Speed-Up Circuitry**

The MAX3373E–MAX3376E/MAX3378E/MAX3379E and MAX3390E–MAX3393E feature a one-shot generator that decreases the rise time of the output. When triggered, MOSFETs PU1 and PU2 turn on for a short time to pull up I/O  $V_{L\_}$  and I/O  $V_{CC\_}$  to their respective supplies (see Figure 2b). This greatly reduces the rise time and propagation delay for the low-to-high transition. The scope photo of Rail-to-Rail Driving for 8Mbps Operation in the *Typical Operating Characteristics* shows the speed-up circuitry in operation.

### **Three-State Output Mode**

Pull THREE-STATE low to place the MAX3372E–MAX3379E and MAX3390E–MAX3393E in three-state out-

put mode. Connect THREE-STATE to  $V_L$  (logic high) for normal operation. Activating the three-state output mode disconnects the internal  $10\text{k}\Omega$  pullup resistors on the I/O  $V_{CC}$  and I/O  $V_{L\_}$  lines. This forces the I/O lines to a high-impedance state, and decreases the supply current to less than  $1\mu\text{A}$ . The high-impedance I/O lines in three-state output mode allow for use in a multidrop network. When in three-state output mode, do not allow the voltage at I/O  $V_{L\_}$  to exceed ( $V_L + 0.3\text{V}$ ), or the voltage at I/O  $V_{CC\_}$  to exceed ( $V_{CC} + 0.3\text{V}$ ).

### **Thermal Short-Circuit Protection**

Thermal overload detection protects the MAX3372E–MAX3379E and MAX3390E–MAX3393E from short-circuit fault conditions. In the event of a short-circuit fault, when the junction temperature ( $T_J$ ) reaches  $+152^\circ\text{C}$ , a thermal sensor signals the three-state output mode logic to force the device into three-state output mode. When  $T_J$  has cooled to  $+142^\circ\text{C}$ , normal operation resumes.

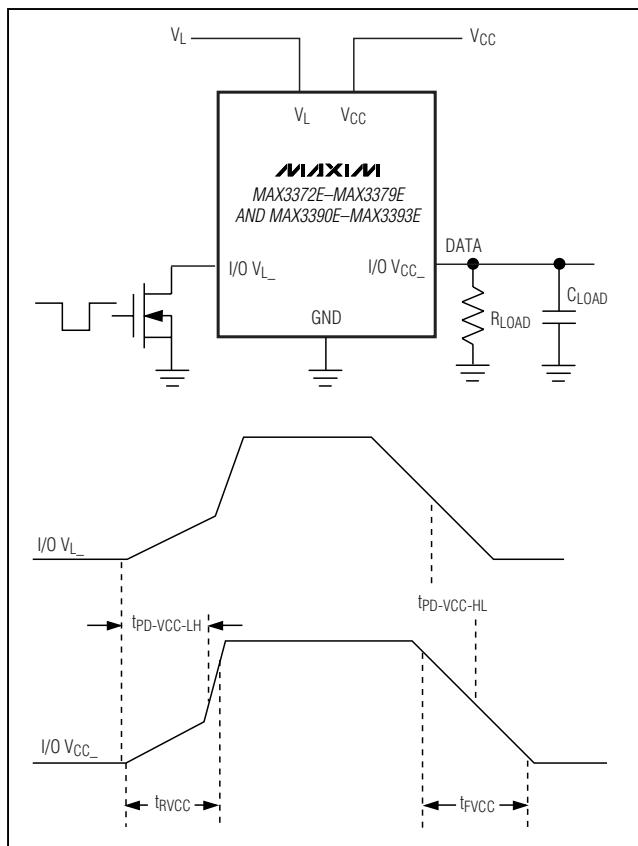


Figure 1c. Open-Drain Driving I/O  $V_{CC}$

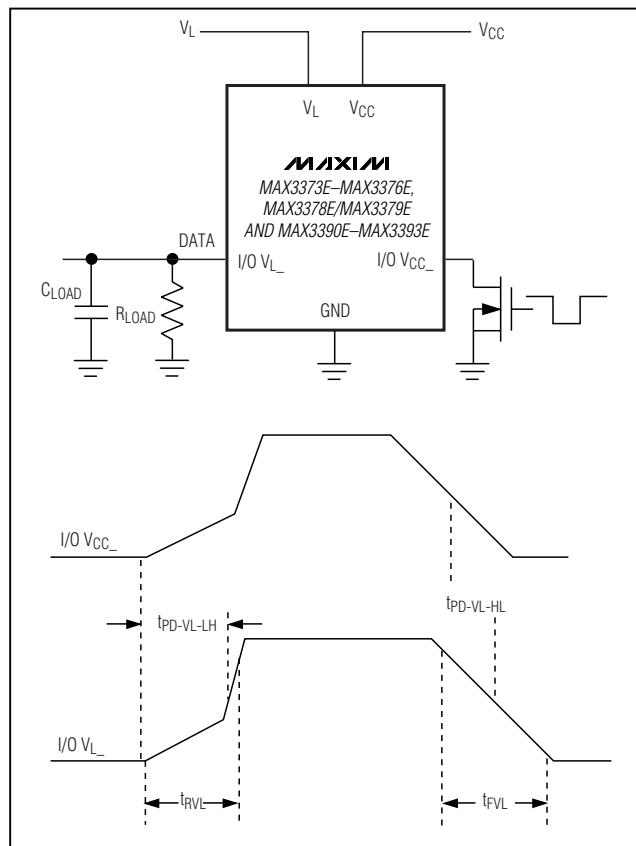


Figure 1d. Open-Drain Driving I/O  $V_L$

***±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP***

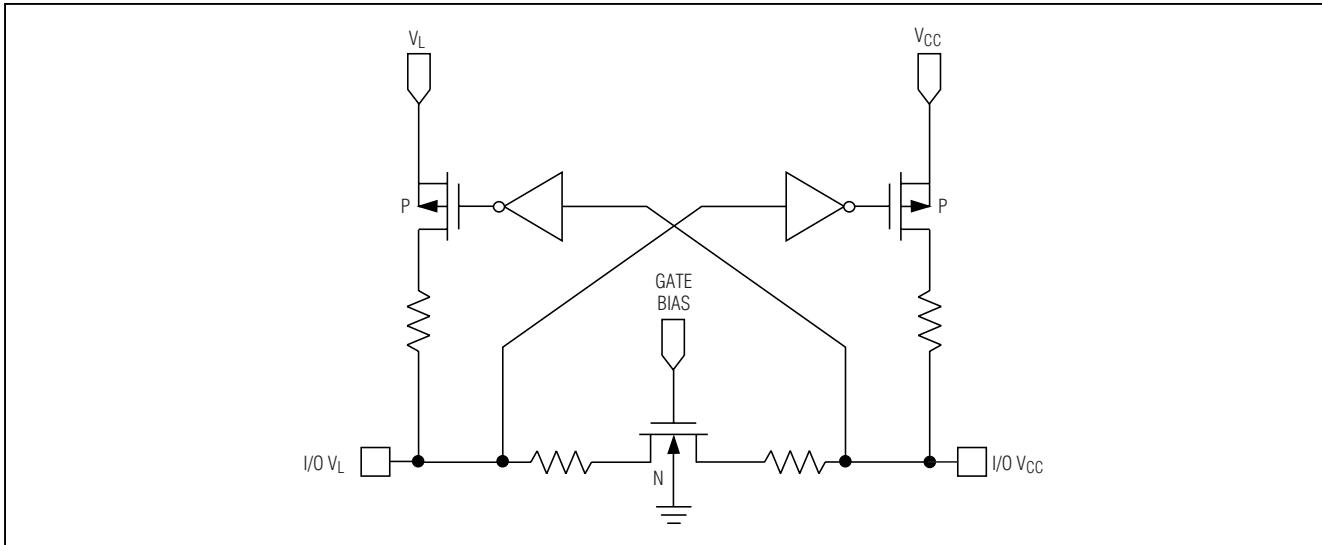


Figure 2a. Functional Diagram, MAX3372E/MAX3377E (1I/O line)

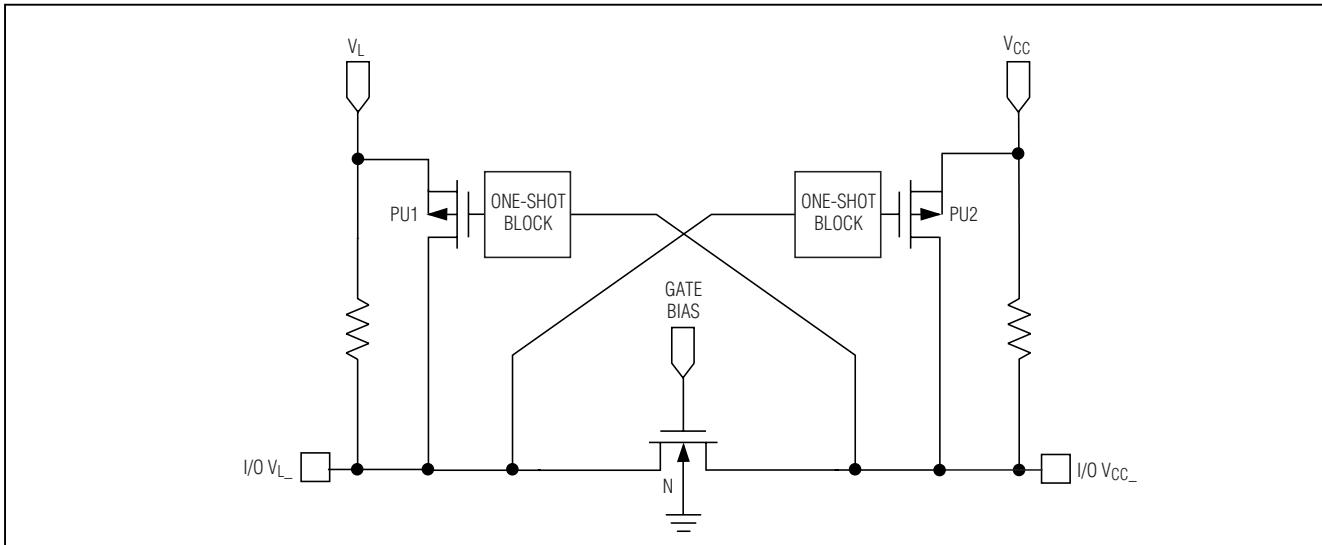


Figure 2b. Functional Diagram, MAX3373E/MAX3378E (1I/O line)

# **$\pm 15\text{kV}$ ESD-Protected, $1\mu\text{A}$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

## **$\pm 15\text{kV}$ ESD Protection**

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The I/O VCC lines have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of  $\pm 15\text{kV}$  without damage. The ESD structures withstand high ESD in all states: normal operation, three-state output mode, and powered down. After an ESD event, Maxim's E versions keep working without latchup, whereas competing products can latch and must be powered down to remove latchup.

ESD protection can be tested in various ways. The I/O VCC lines of this product family are characterized for protection to the following limits:

- 1)  $\pm 15\text{kV}$  using the Human Body Model
- 2)  $\pm 8\text{kV}$  using the Contact Discharge method specified in IEC 1000-4-2
- 3)  $\pm 10\text{kV}$  using IEC 1000-4-2's Air-Gap Discharge method

## **ESD Test Conditions**

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

## **Human Body Model**

Figure 3a shows the Human Body Model and Figure 3b shows the current waveform it generates when discharged into a low impedance. This model consists of a  $100\text{pF}$  capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a  $1.5\text{k}\Omega$  resistor.

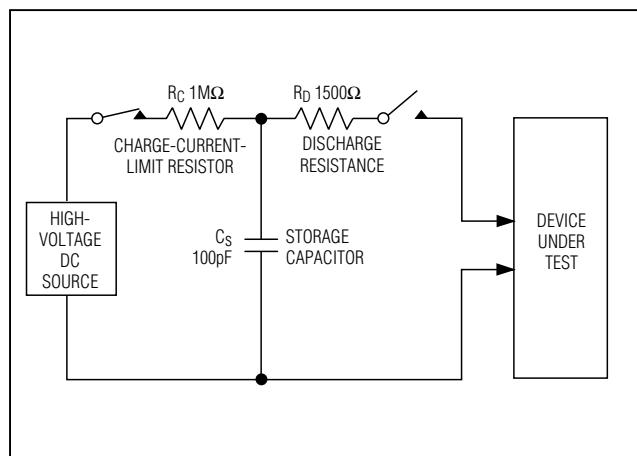


Figure 3a. Human Body ESD Test Model

## **IEC 1000-4-2**

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3372E-MAX3379E and MAX3390E-MAX3393E help to design equipment that meets Level 3 of IEC 1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2, because series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD withstand voltage measured to IEC 1000-4-2 is generally lower than that measured using the Human Body Model. Figure 4a shows the IEC 1000-4-2 model, and Figure 4b shows the current waveform for the  $\pm 8\text{kV}$ , IEC 1000-4-2, Level 4, ESD contact-discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

## **Machine Model**

The Machine Model for ESD tests all pins using a  $200\text{pF}$  storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

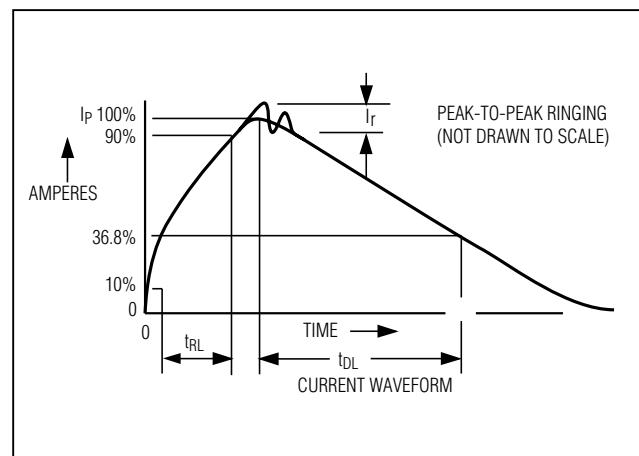


Figure 3b. Human Body Current Waveform

**MAX3372E-MAX3379E/MAX3390E-MAX3393E**

## **$\pm 15kV$ ESD-Protected, $1\mu A$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

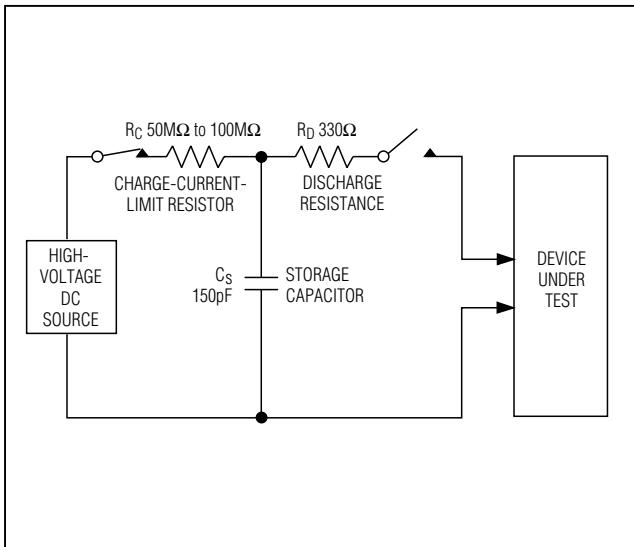


Figure 4a. IEC 1000-4-2 ESD Test Model

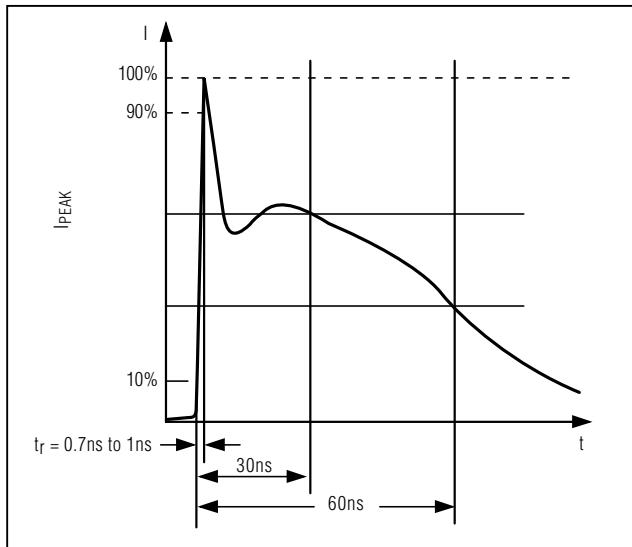


Figure 4b. IEC 1000-4-2 ESD Generator Current Waveform

### **Applications Information**

#### **Power-Supply Decoupling**

To reduce ripple and the chance of transmitting incorrect data, bypass  $V_L$  and  $V_{CC}$  to ground with a  $0.1\mu F$  capacitor. See *Typical Operating Circuit*. To ensure full  $\pm 15kV$  ESD protection, bypass  $V_{CC}$  to ground with a  $1\mu F$  capacitor. Place all capacitors as close to the power-supply inputs as possible.

#### **I<sup>2</sup>C Level Translation**

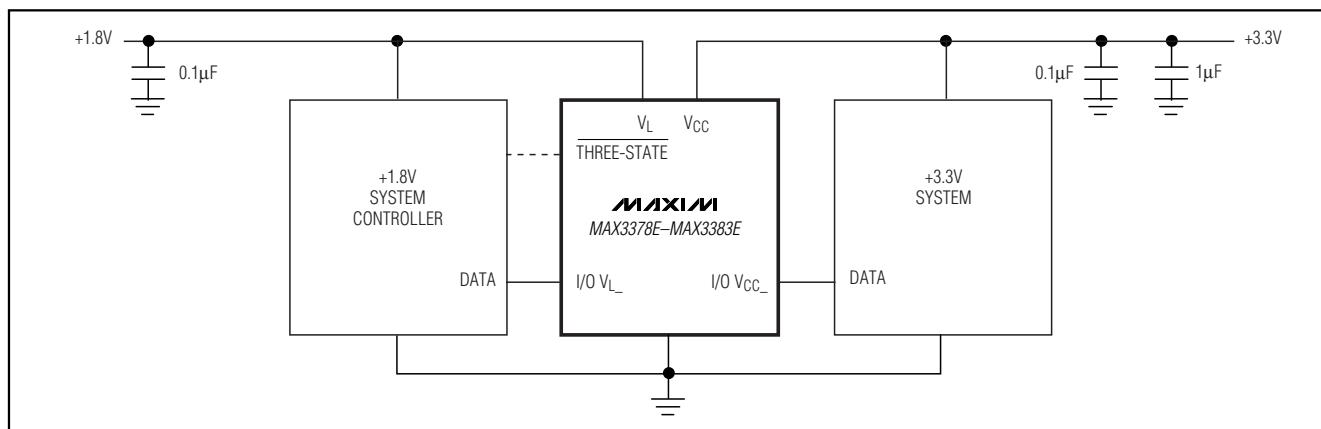
The MAX3373E-MAX3376E, MAX3378E/MAX3379E and MAX3390E-MAX3393E level-shift the data present on the I/O lines between +1.2V and +5.5V, making them ideal for level translation between a low-voltage

ASIC and an I<sup>2</sup>C device. A typical application involves interfacing a low-voltage microprocessor to a 3V or 5V D/A converter, such as the MAX517.

#### **Push-Pull vs. Open-Drain Driving**

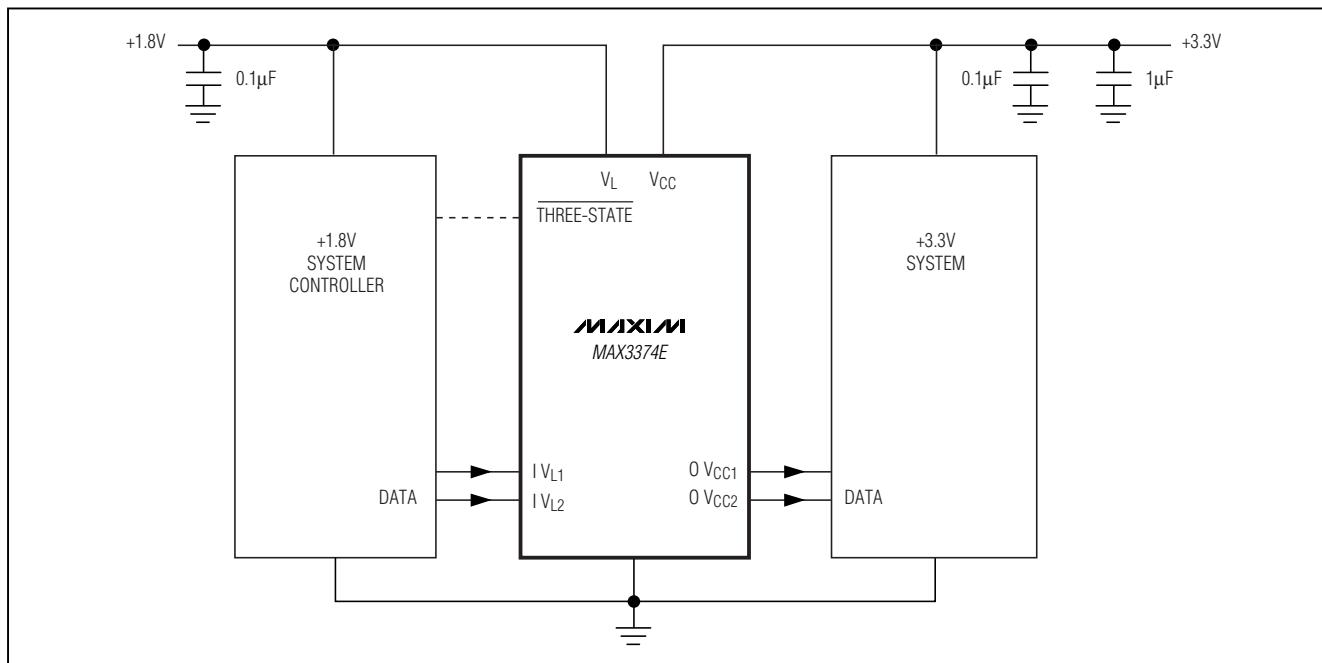
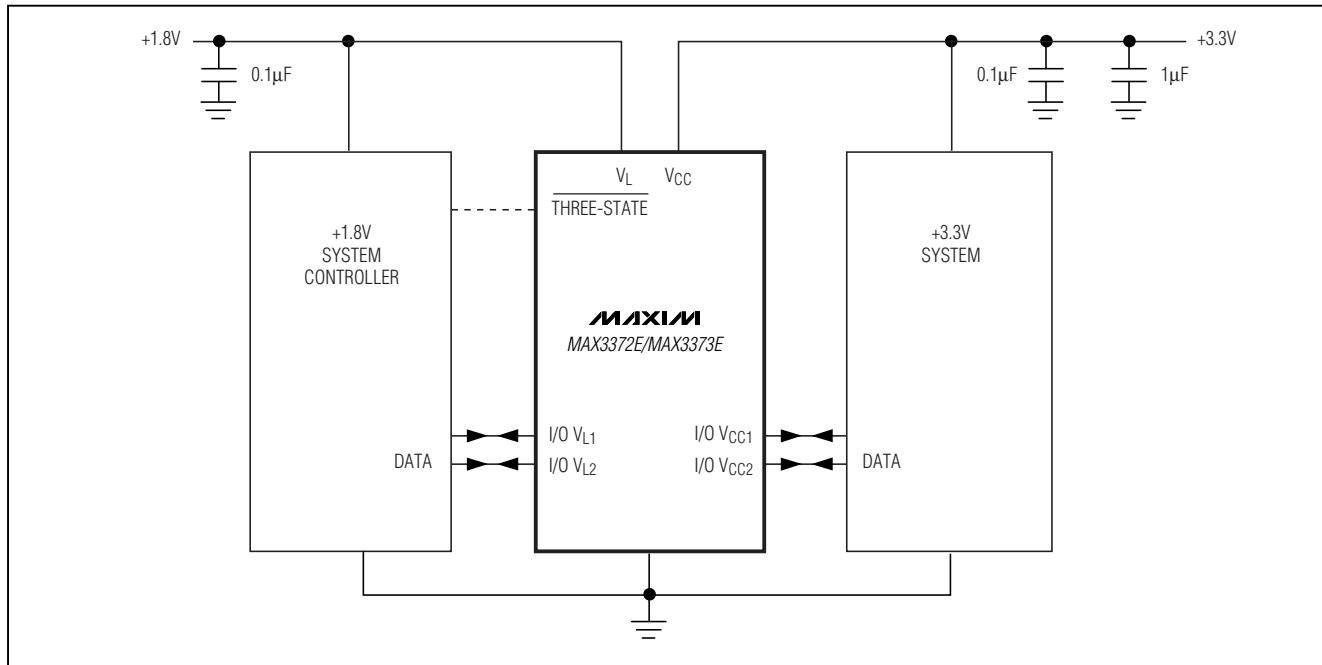
All devices in the MAX3372E-MAX3379E and MAX3390E-MAX3393E family may be driven in a push-pull configuration. The MAX3373E-MAX3376E/MAX3378E/MAX3379E and MAX3390E-MAX3393E include internal  $10k\Omega$  resistors that pull up I/O  $V_L$  and I/O  $V_{CC}$  to their respective power supplies, allowing operation of the I/O lines with open-drain devices. See *Timing Characteristics* for maximum data rates when using open-drain drivers.

### **Typical Operating Circuit**



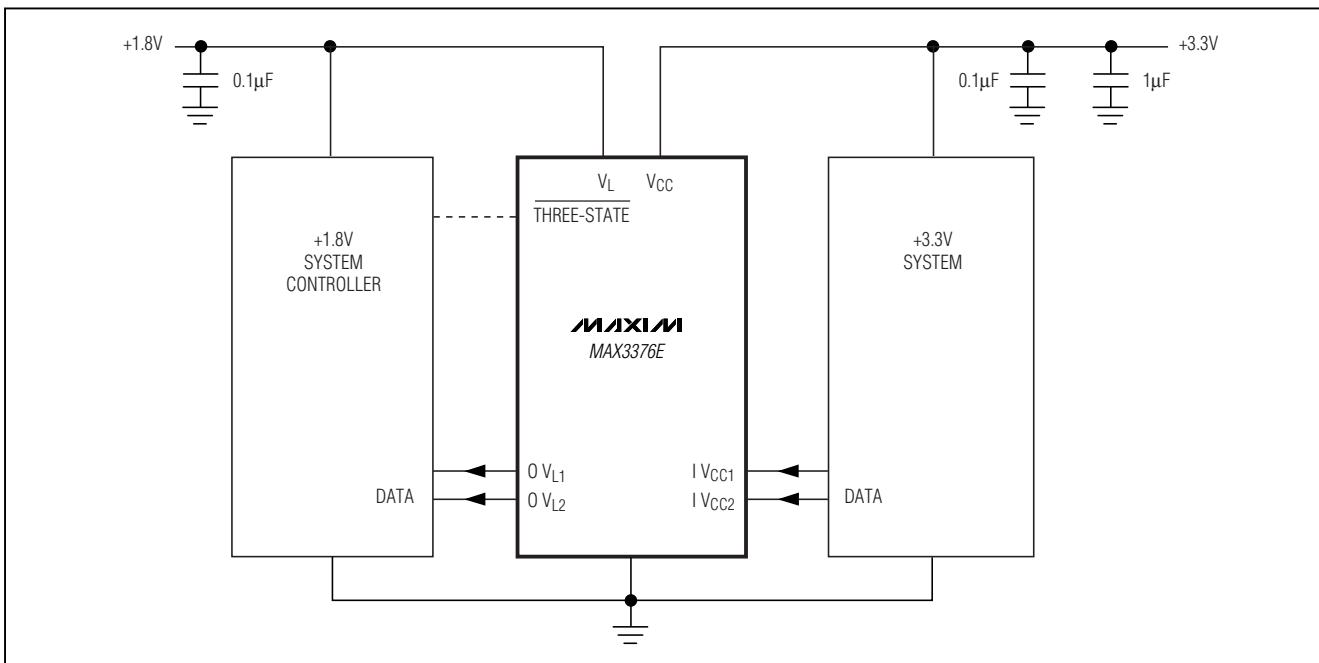
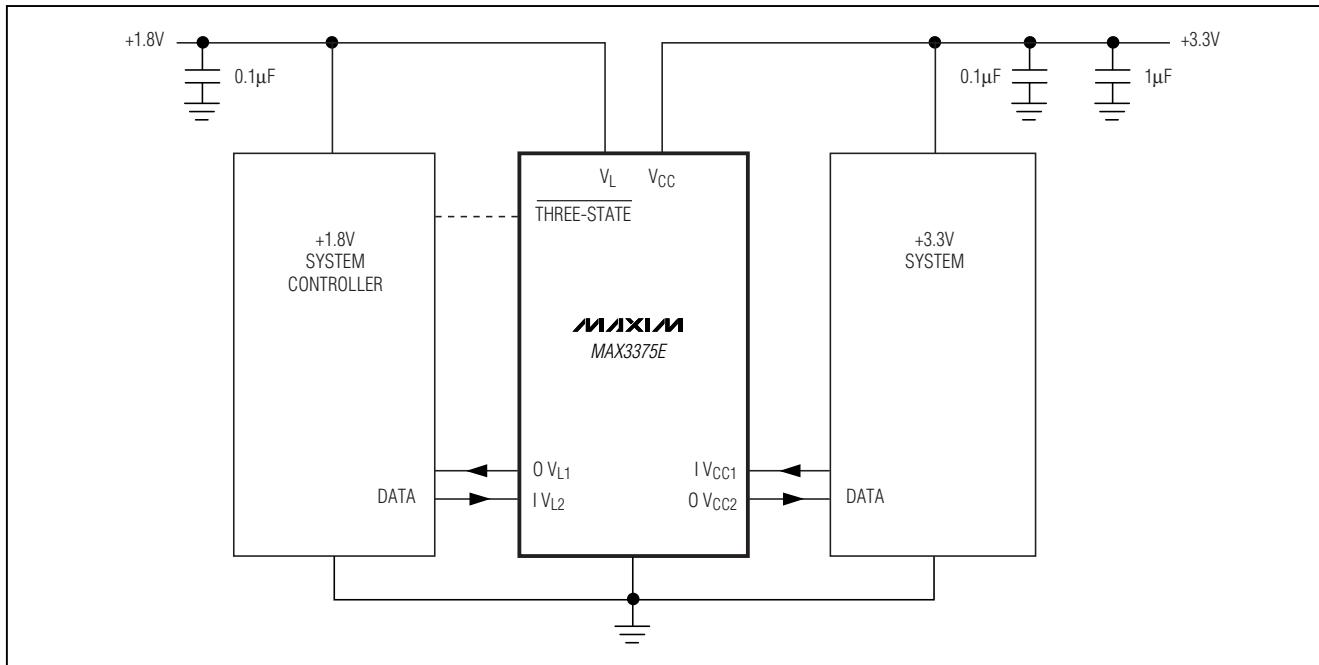
## **$\pm 15kV$ ESD-Protected, $1\mu A$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

### **Applications Circuits**



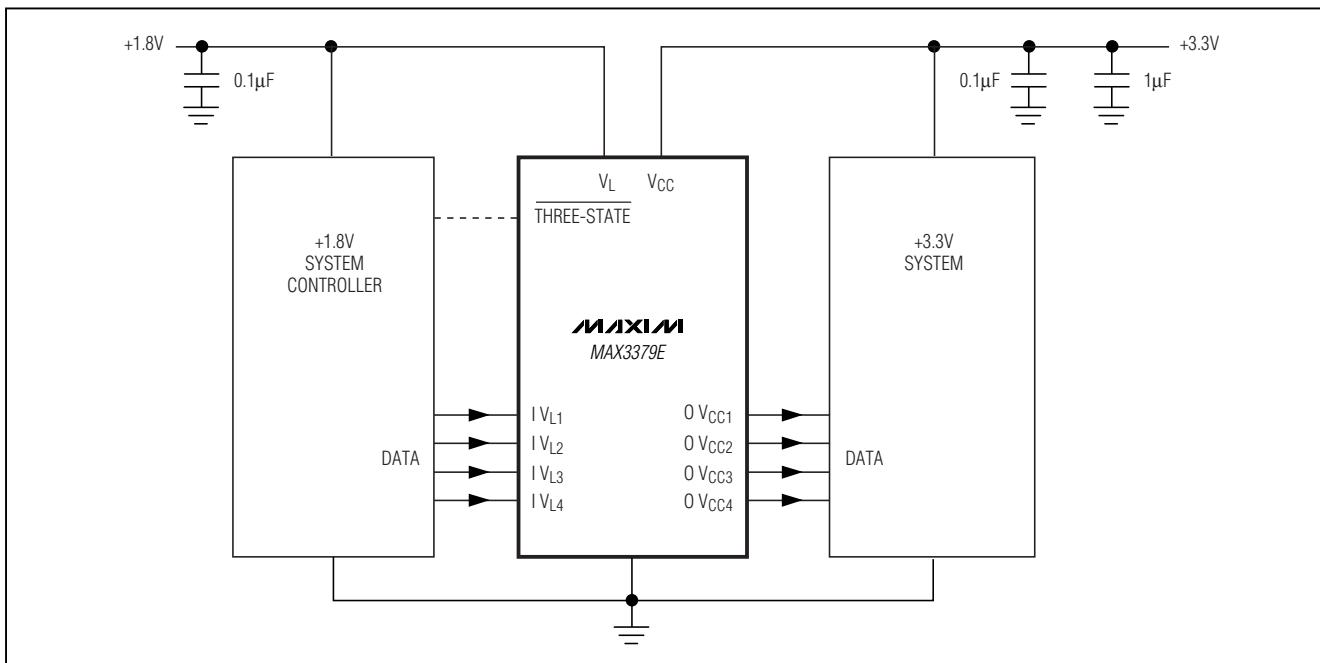
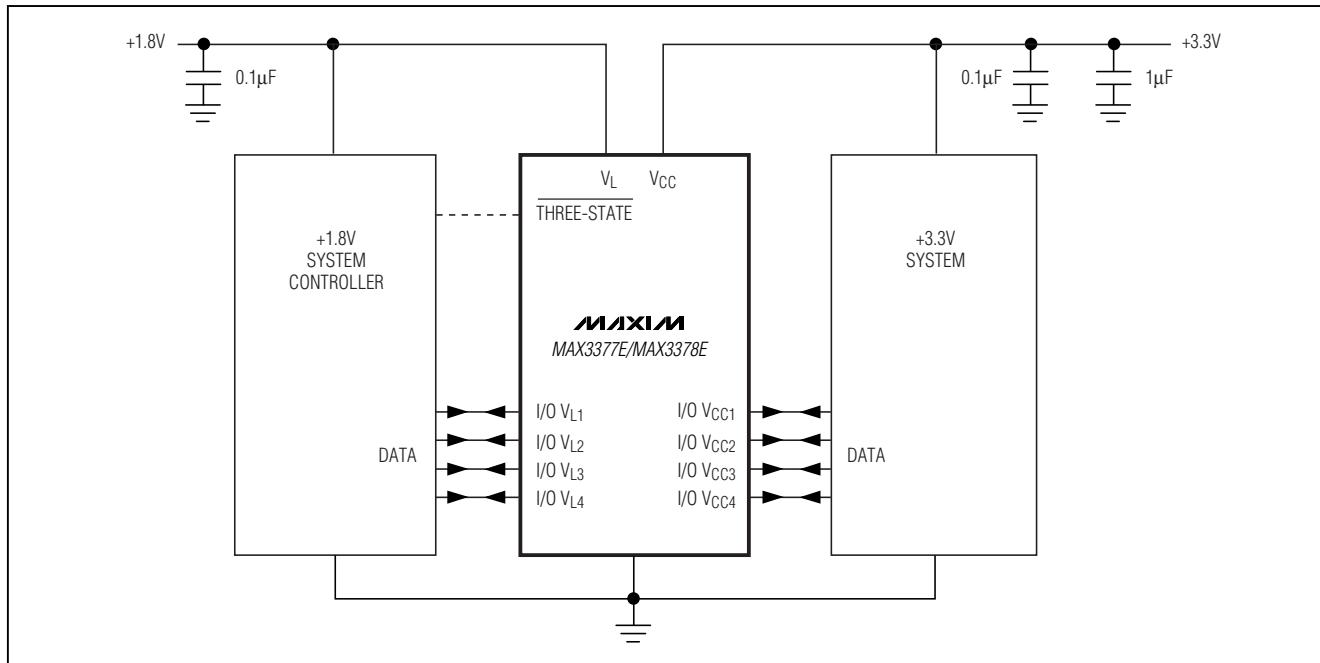
**$\pm 15kV$  ESD-Protected, 1 $\mu$ A, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

**Applications Circuits (continued)**



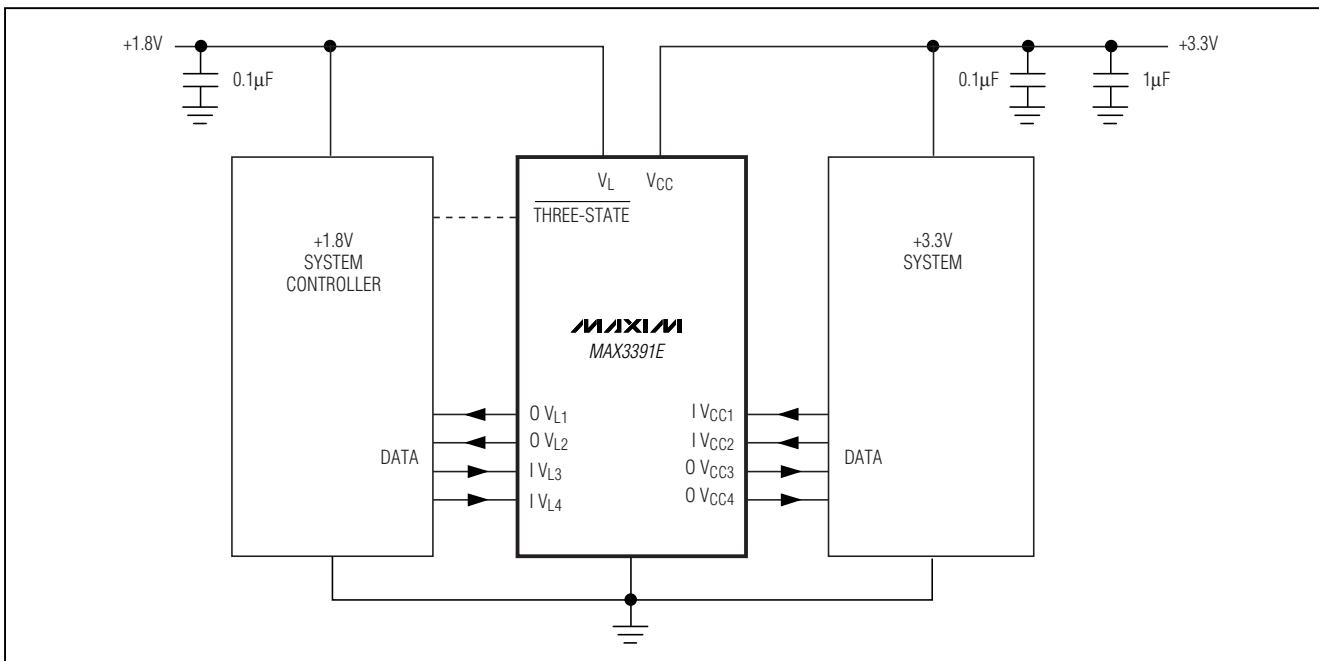
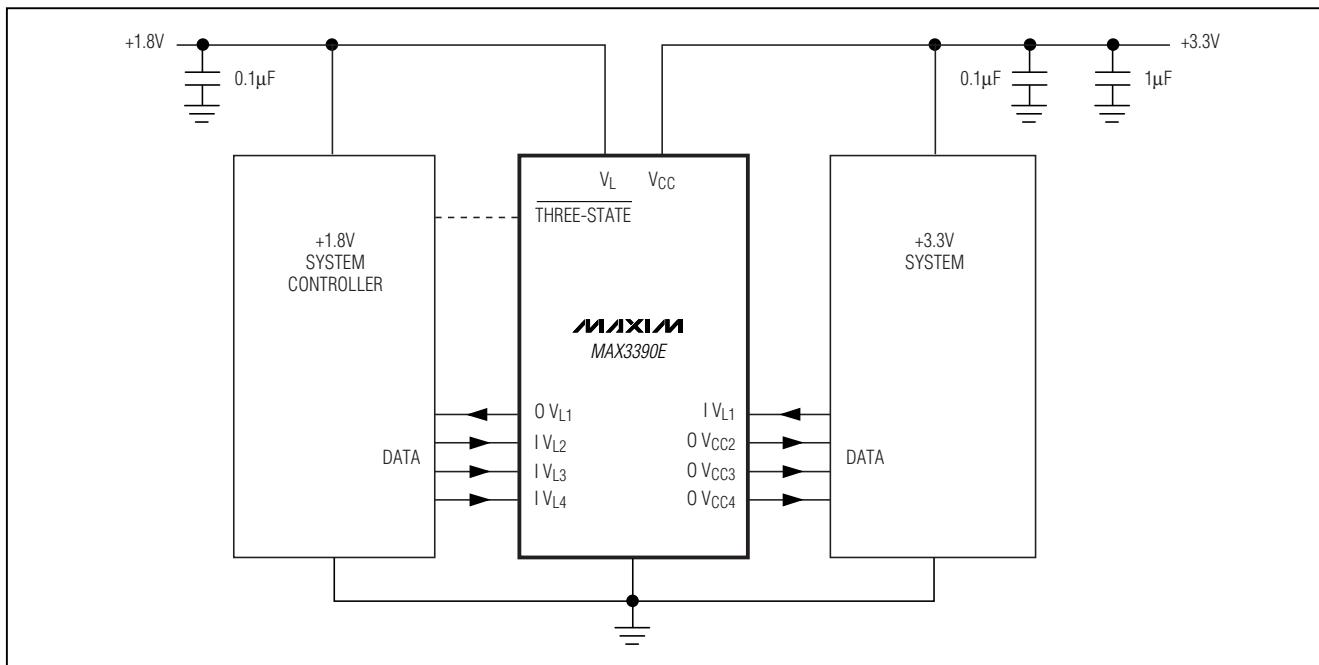
**$\pm 15kV$  ESD-Protected,  $1\mu A$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

**Applications Circuits (continued)**



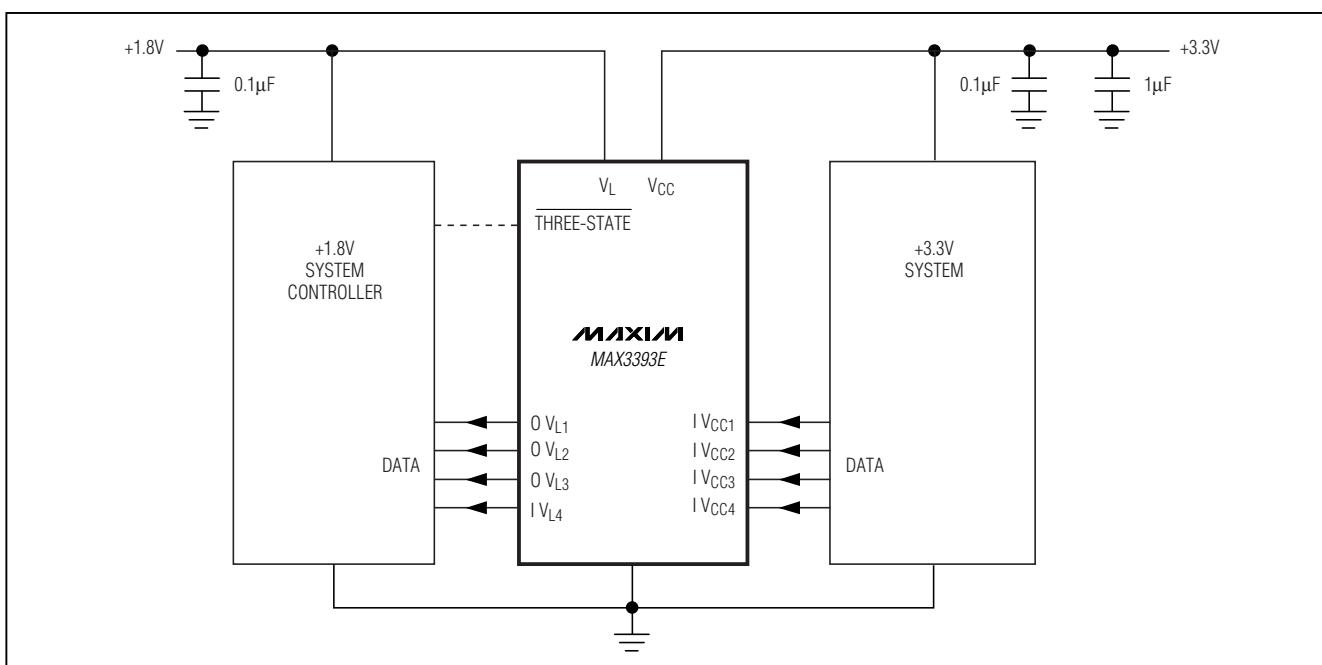
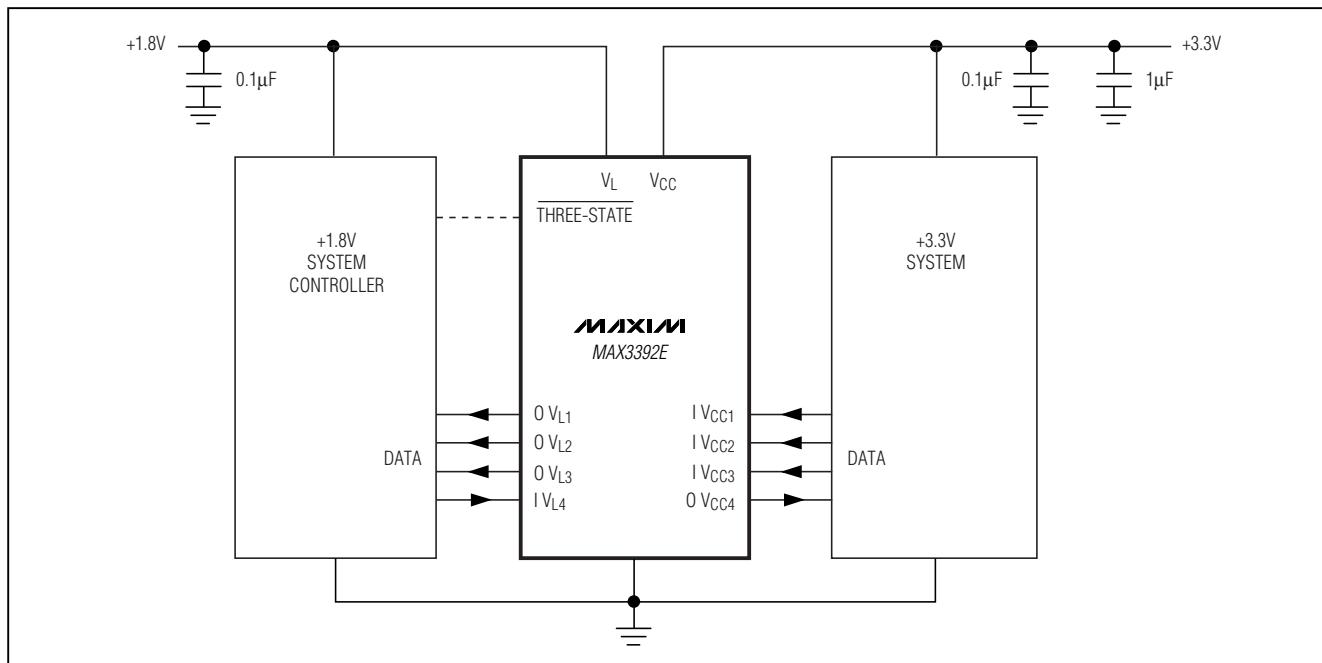
***±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP***

***Applications Circuits (continued)***



## **$\pm 15kV$ ESD-Protected, $1\mu A$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

### **Applications Circuits (continued)**



**±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

**Selector Guide**

PART NUMBER	LEVEL TRANSLATION	Tx/ Rx <sup>†</sup>	DATA RATE	TOP MARK	
MAX3372EEKA-T	✓ Bi	2/2	230kbps  8Mbps*	AAKO	
MAX3372EEBL-T	✓ Bi	2/2		AAR	
MAX3373EEKA-T	✓ Bi	2/2		AAKS	
MAX3373EEBL-T	✓ Bi	2/2		AAZ	
MAX3374EEKA-T	Uni	2/0		AALH	
MAX3374EEBL-T	Uni	2/0		ABA	
MAX3375EEKA-T	Uni	1/1		AALI	
MAX3375EEBL-T	Uni	1/1		ABB	
MAX3376EEKA-T	Uni	0/2		AALG	
MAX3376EEBL-T	Uni	0/2		AAV	
MAX3377EEUD	✓ Bi	4/4		230kbps  8Mbps*	—
MAX3377EEBC-T	✓ Bi	4/4			AAX
MAX3378EEUD	✓ Bi	4/4			—
MAX3378EEBC-T	✓ Bi	4/4			AAY
MAX3379EEUD	Uni	4/0			—
MAX3379EEBC-T	Uni	4/0			AAZ
MAX3390EEUD	Uni	3/1	—		
MAX3390EEBC-T	Uni	3/1	ABA		
MAX3391EEUD	Uni	2/2	—		
MAX3391EEBC-T	Uni	2/2	ABB		
MAX3392EEUD	Uni	1/3	—		
MAX3392EEBC-T	Uni	1/3	ABC		
MAX3393EEUD	Uni	0/4	—		
MAX3393EEBC-T	Uni	0/4	ABD		

<sup>†</sup>Tx =  $V_L \rightarrow V_{CC}$ , Rx =  $V_{CC} \rightarrow V_L$

\*Higher data rates are possible (see Timing Characteristics).

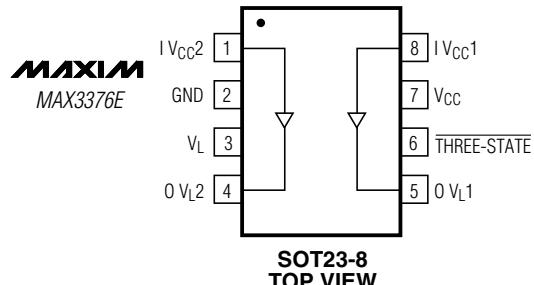
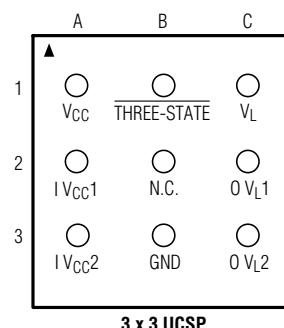
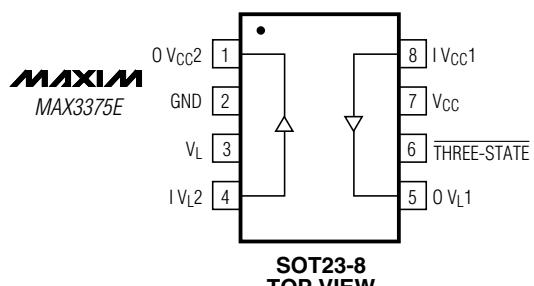
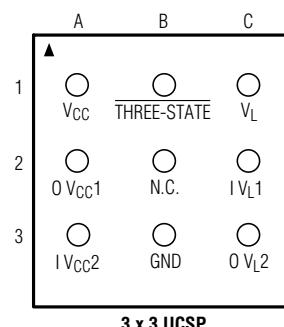
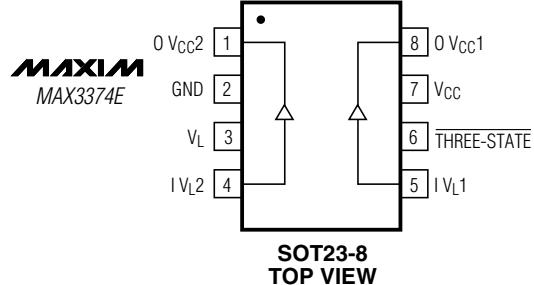
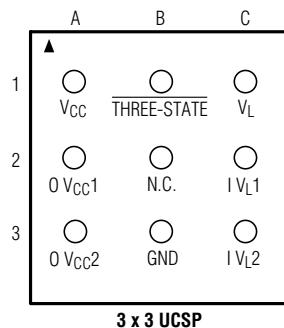
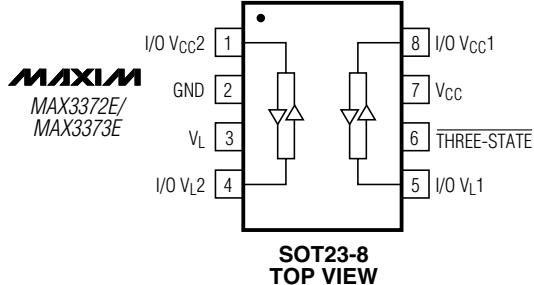
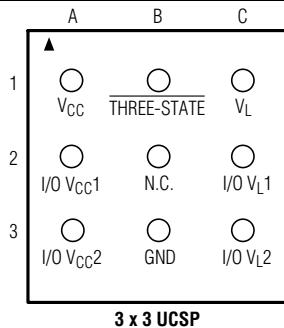
**Ordering Information (continued)**

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX3372EEBL-T	-40°C to +85°C	3 × 3 UCSP
<b>MAX3373EEKA-T</b>	-40°C to +85°C	8 SOT23-8
MAX3373EEBL-T	-40°C to +85°C	3 × 3 UCSP
<b>MAX3374EEKA-T</b>	-40°C to +85°C	8 SOT23-8
MAX3374EEBL-T	-40°C to +85°C	3 × 3 UCSP
<b>MAX3375EEKA-T</b>	-40°C to +85°C	8 SOT23-8
MAX3375EEBL-T	-40°C to +85°C	3 × 3 UCSP
<b>MAX3376EEKA-T</b>	-40°C to +85°C	8 SOT23-8
MAX3376EEBL-T	-40°C to +85°C	3 × 3 UCSP
<b>MAX3377EEUD</b>	-40°C to +85°C	14 TSSOP
MAX3377EEBC-T	-40°C to +85°C	3 × 4 UCSP
<b>MAX3378EEUD</b>	-40°C to +85°C	14 TSSOP
MAX3378EEBC-T	-40°C to +85°C	3 × 4 UCSP
<b>MAX3379EEUD*</b>	-40°C to +85°C	14 TSSOP
MAX3379EEBC-T*	-40°C to +85°C	3 × 4 UCSP
<b>MAX3390EEUD*</b>	-40°C to +85°C	14 TSSOP
MAX3390EEBC-T*	-40°C to +85°C	3 × 4 UCSP
<b>MAX3391EEUD*</b>	-40°C to +85°C	14 TSSOP
MAX3391EEBC-T*	-40°C to +85°C	3 × 4 UCSP
<b>MAX3392EEUD*</b>	-40°C to +85°C	14 TSSOP
MAX3392EEBC-T*	-40°C to +85°C	3 × 4 UCSP
<b>MAX3393EEUD*</b>	-40°C to +85°C	14 TSSOP
MAX3393EEBC-T*	-40°C to +85°C	3 × 4 UCSP

\*Future product—contact factory for availability.

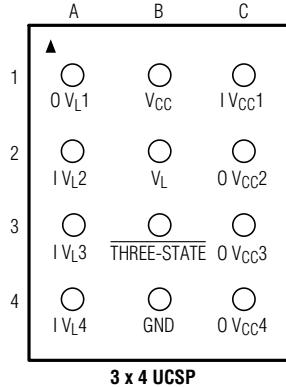
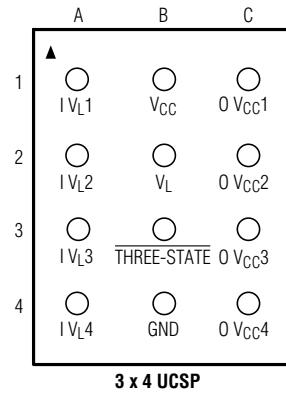
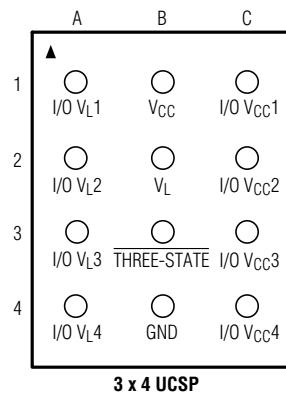
## **$\pm 15kV$ ESD-Protected, $1\mu A$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

### **Pin Configurations (continued)**

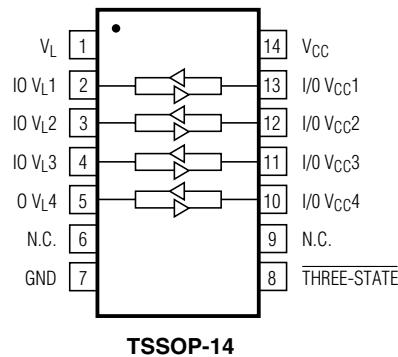


**$\pm 15kV$  ESD-Protected,  $1\mu A$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

**Pin Configurations (continued)**

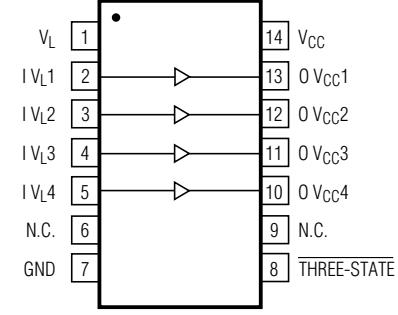


**MAXIM**  
MAX3377E/  
MAX3378E



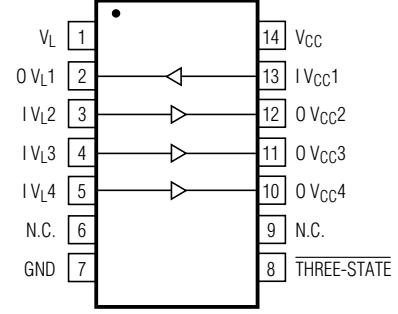
TSSOP-14

**MAXIM**  
MAX3379E



TSSOP-14

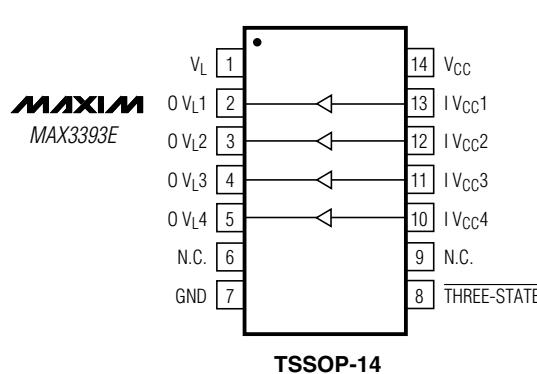
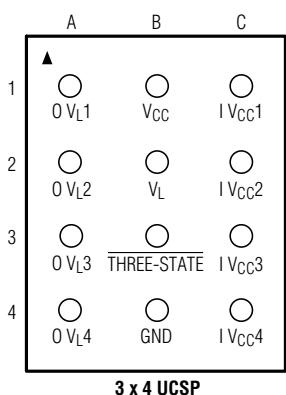
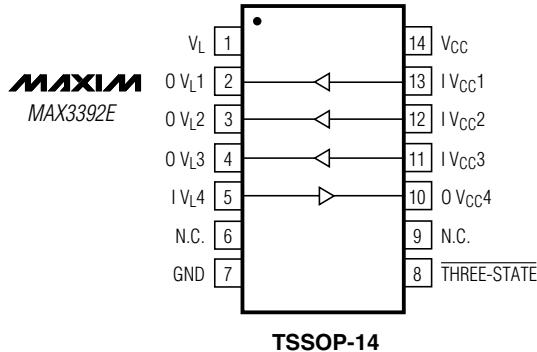
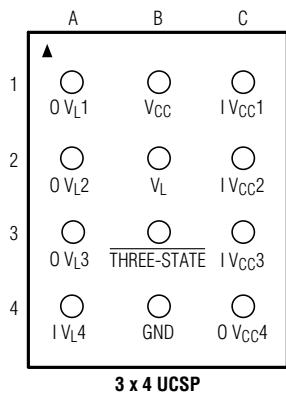
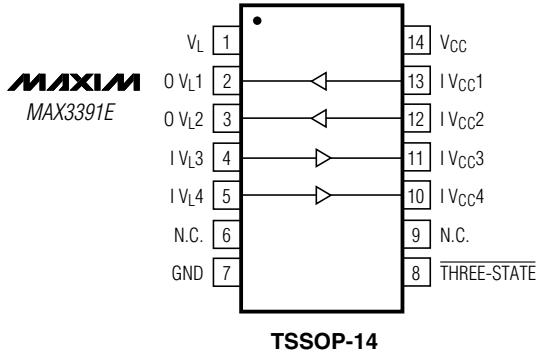
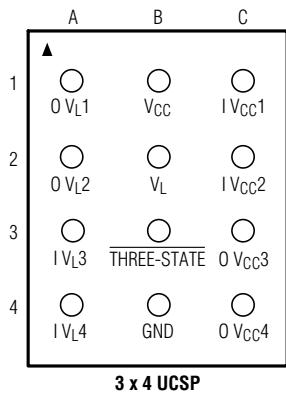
**MAXIM**  
MAX3390E



TSSOP-14

## ***±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP***

### ***Pin Configurations (continued)***



# ***±15kV ESD-Protected, 1µA, 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP***

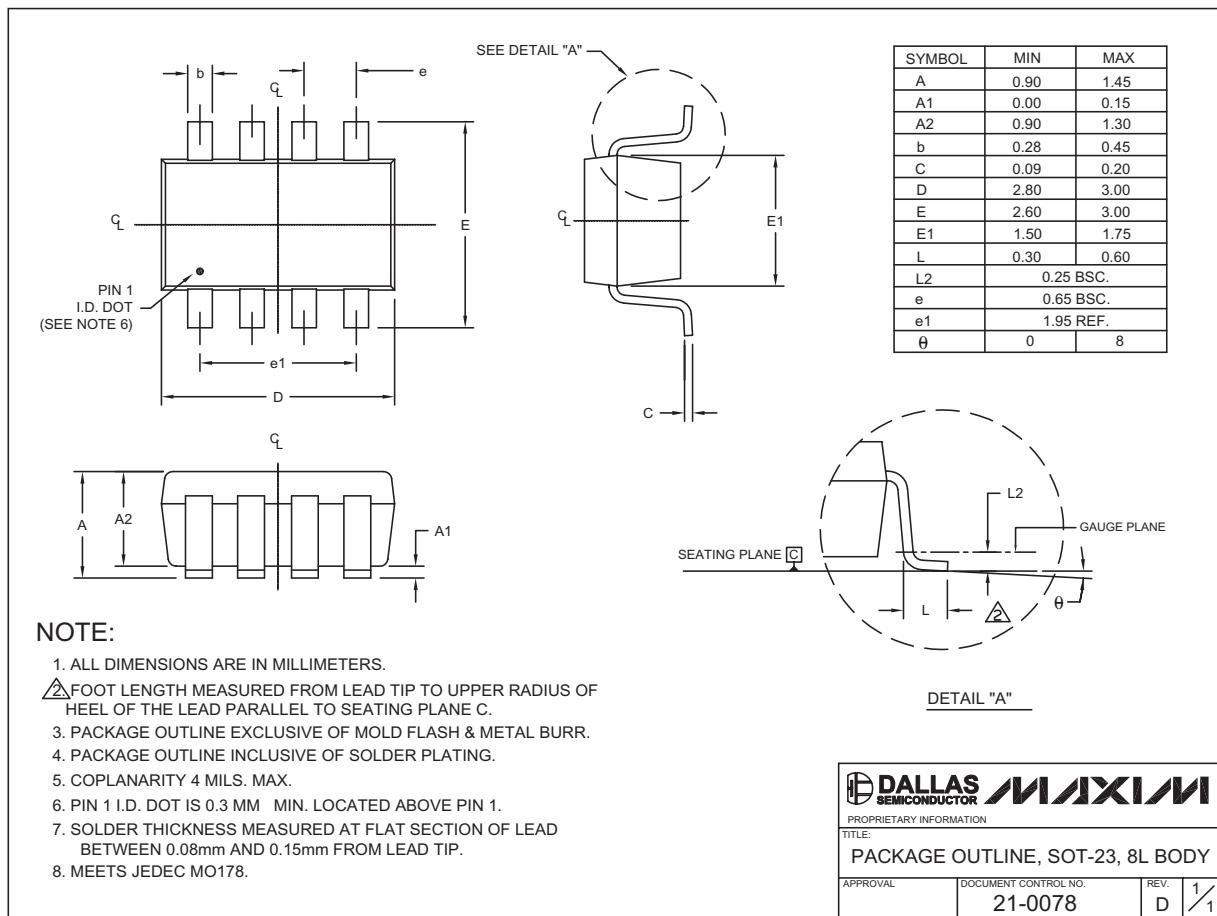
## ***Chip Information***

TRANSISTOR COUNT: MAX3372E–MAX3376E: 189  
 MAX3377E–MAX3379E,  
 MAX3390E–MAX3393E: 295

PROCESS: BiCMOS

## ***Package Information***

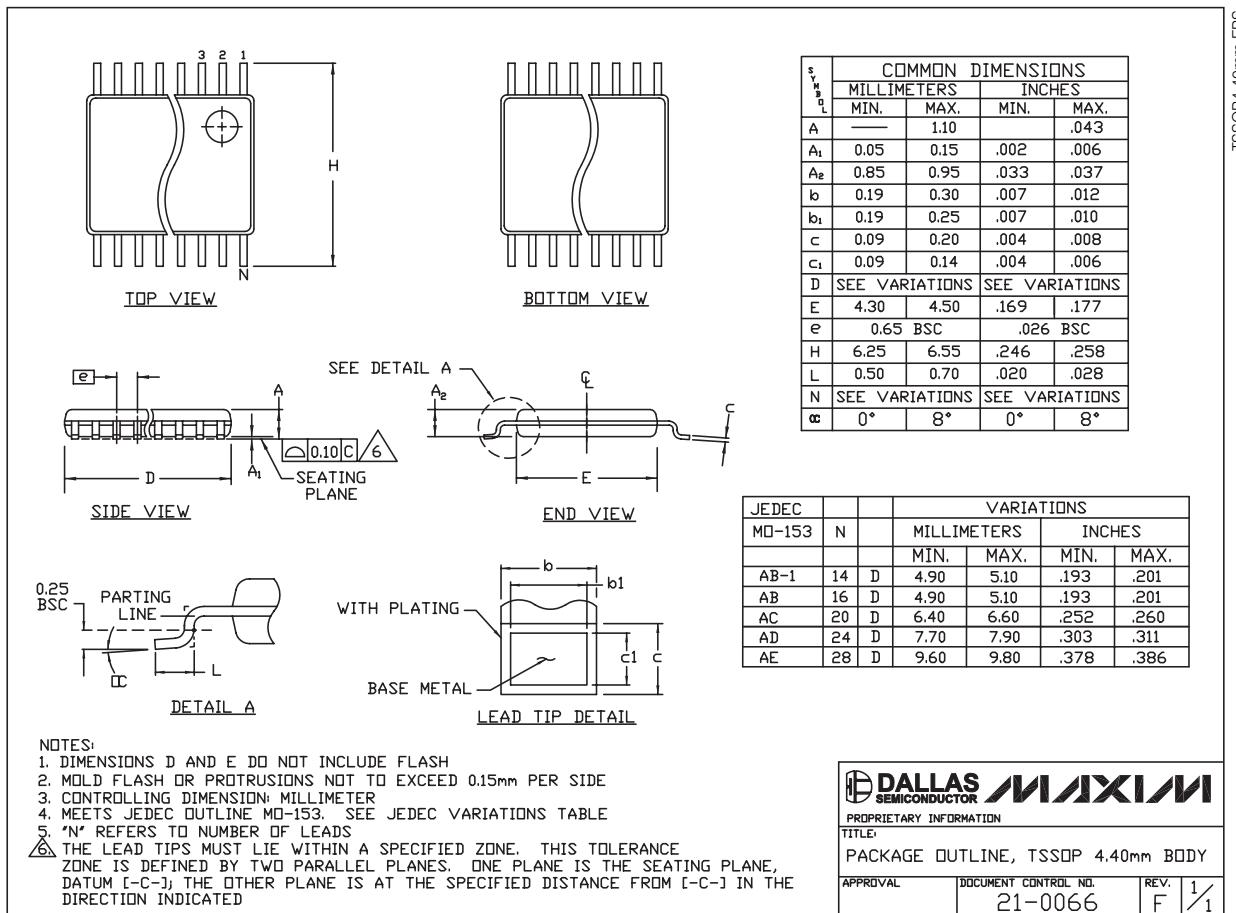
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



# **$\pm 15kV$ ESD-Protected, $1\mu A$ , 16Mbps, Dual/Quad Low-Voltage Level Translators in UCSP**

## **Package Information (continued)**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



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**Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600**

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**MAX3372E-MAX3379E/MAX3390E-MAX3393E**