19-2672; Rev 1; 10/03

MAXIM

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

General Description

The MAX3000E/MAX3001E/MAX3002–MAX3012 8-channel level translators provide the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a higher voltage logic signal on the V_{CC} side of the device, and vice-versa.

The MAX3000E/MAX3001E/MAX3002/MAX3004–MAX3012 feature an EN input that, when low, reduces the V_{CC} and V_L supply currents to <2µA. The MAX3000E/MAX3001E also have ±15kV ESD protection on the I/O V_{CC} side for greater protection in applications that route signals externally. The MAX3000E operates at a guaranteed data rate of 230kbps. The MAX3001E operates at a guaranteed data rate of 4Mbps. The MAX3002–MAX3012 operate at a guaranteed data rate of 20Mbps over the entire specified operating voltage range.

The MAX3000E/MAX3001E/MAX3002–MAX3012 accept V_L voltages from +1.2V to +5.5V and V_{CC} voltages from +1.65V to +5.5V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. The MAX3000E/MAX3001E/MAX3002–MAX3012 are available in 20-pin UCSP™ and 20-pin TSSOP packages.

Applications

Cellphones

SPI™ and MICROWIRE™ Level Translation

Low-Voltage ASIC Level Translation

Smart Card Readers

Cellphone Cradles

Portable POS Systems

Portable Communication Devices

Low-Cost Serial Interfaces

GPS

Telecommunications Equipment

UCSP is a trademark of Maxim Integrated Products, Inc.

SPI is a trademark of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor.

Features

- **Guaranteed Data Rate Options**
  230kbps (MAX3000E)
  4Mbps (MAX3001E)
  20Mbps (MAX3002–MAX3012)
- **Bidirectional Level Translation (MAX3000E/MAX3001E/MAX3002/MAX3003)**
- **Unidirectional Level Translation (MAX3004–MAX3012)**
- **Operation Down to +1.2V on V_L**
- **±15kV ESD Protection on I/O V_{CC} Lines (MAX3000E/MAX3001E)**
- **Ultra-Low 0.1µA Supply Current in Shutdown**
- **Low Quiescent Current (<10µA)**
- **UCSP and TSSOP Packages**

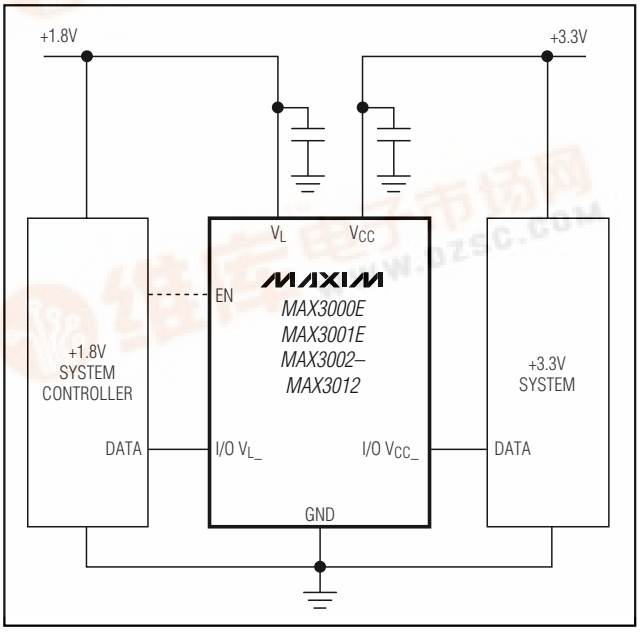
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3000EEUP	-40°C to +85°C	20 TSSOP
MAX3000EEBP-T*	-40°C to +85°C	4 x 5 UCSP

**Future product—contact factory for availability.*

Ordering Information continued at end of data sheet.

Typical Operating Circuit



Pin Configurations and Functional Diagrams appear at end of data sheet.

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

ABSOLUTE MAXIMUM RATINGS

All Voltages Referenced to GND
V_{CC} .....-0.3V to +6V
V_L .....-0.3V to +6V
I/O $V_{CC\_}$ .....-0.3V to (V_{CC} + 0.3V)
I/O $V_{L\_}$ .....-0.3V to (V_L + 0.3V)
EN, EN A/B .....-0.3V to +6V
Short-Circuit Duration I/O $V_{L\_}$, I/O $V_{CC\_}$ to GND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 7.0mW/°C above +70°C) 559mW
20-Pin UCSP (derate 10mW/°C above +70°C) 800mW

Operating Temperature Ranges
MAX3001EAUP .....-40°C to +125°C
MAX300_EE_P .....-40°C to +85°C
MAX30_ _E_P .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to V_{CC}, EN = V_L (MAX3000E/MAX3001E/MAX3002/MAX3004–MAX3012), EN A/B = V_L or 0 (MAX3003), T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = +1.65V, V_L = +1.2V, and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_L Supply Range	V_L		1.2		5.5	V
V_{CC} Supply Range	V_{CC}		1.65		5.50	V
Supply Current from V_{CC}	I_{QVCC}	I/O $V_{CC\_}$ = 0, I/O $V_{L\_}$ = 0 or I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L, MAX3000E/MAX3002–MAX3012		0.1	10	µA
		I/O $V_{CC\_}$ = 0, I/O $V_{L\_}$ = 0 or I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L, MAX3001E		0.1	50	
Supply Current from V_L	I_{QVL}	I/O $V_{CC\_}$ = 0, I/O $V_{L\_}$ = 0 or I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L, MAX3000E/MAX3002–MAX3012		0.1	10	µA
		I/O $V_{CC\_}$ = 0, I/O $V_{L\_}$ = 0 or I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L, MAX3001E		0.1	50	
V_{CC} Shutdown Supply Current	$I_{SHDN-VCC}$	T_A = +25°C, EN = 0, MAX3000E/MAX3001E/MAX3002/ MAX3004–MAX3012		0.1	2	µA
		T_A = +25°C, EN A/B = 0, MAX3003		0.1	2	
V_L Shutdown Supply Current	$I_{SHDN-VL}$	T_A = +25°C, EN = 0, MAX3000E/MAX3001E/MAX3002/ MAX3004–MAX3012		0.1	2	µA
		T_A = +25°C, EN A/B = 0, MAX3003		0.1	2	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to V_{CC}, EN = V_L (MAX3000E/MAX3001E/MAX3002/MAX3004–MAX3012), EN A/B = V_L or 0 (MAX3003), T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = +1.65V, V_L = +1.2V, and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Three-State Output Leakage Current		T_A = +25°C, EN = 0, MAX3000E/MAX3001E/MAX3002/ MAX3004–MAX3012		0.1	2	µA
		T_A = +25°C, EN A/B = 0, MAX3003		0.1	2	
I/O $V_{L\_}$ Three-State Output Leakage Current		EN A/B = 0, MAX3003		0.1	2	µA
I/O $V_{L\_}$ Pulldown Resistance During Shutdown		EN = 0, MAX3000E/MAX3001E/MAX3002/ MAX3004–MAX3012	4.59		8.30	kΩ
EN or EN A/B Input Leakage Current		T_A = +25°C			1	µA
LOGIC-LEVEL THRESHOLDS						
I/O $V_{L\_}$ Input Voltage High Threshold	V_{IHL}				V_L - 0.4	V
I/O $V_{L\_}$ Input Voltage Low Threshold	V_{ILL}		0.4			V
I/O $V_{CC\_}$ Input Voltage High Threshold	V_{IHC}				V_{CC} - 0.4	V
I/O $V_{CC\_}$ Input Voltage Low Threshold	V_{ILC}		0.4			V
EN, EN A/B Input Voltage High Threshold	V_{IH}				V_L - 0.4	V
EN, EN A/B Input Voltage Low Threshold	V_{IL}		0.4			V
I/O $V_{L\_}$ Output Voltage High	V_{OHL}	I/O $V_{L\_}$ source current = 20µA, I/O $V_{CC\_} \geq V_{CC}$ - 0.4V	V_L - 0.4			V
I/O $V_{L\_}$ Output Voltage Low	V_{OLL}	I/O $V_{L\_}$ sink current = 20µA, I/O $V_{CC\_} \leq$ 0.4V			0.4	V
I/O $V_{CC\_}$ Output Voltage High	V_{OHC}	I/O $V_{CC\_}$ source current = 20µA, I/O $V_{L\_} \geq V_L$ - 0.4V	V_{CC} - 0.4			V
I/O $V_{CC\_}$ Output Voltage Low	V_{OLC}	I/O V_{CC} sink current = 20µA, I/O $V_{L\_} \leq$ 0.4V			0.4	V
ESD PROTECTION						
I/O $V_{CC\_}$		Human Body Model, MAX3000E/MAX3001E		±15		kV

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

TIMING CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to V_{CC}, EN = V_L (MAX3000E/MAX3001E/MAX3002/MAX3004–MAX3012), EN A/B = V_L or 0 (MAX3003), T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = +1.65V, V_L = +1.2V, and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Rise Time	t_{RVCC}	R_S = 50Ω, C_{VCC} = 50pF, MAX3000E, Figures 1a, 1b	400	800	1200	ns
		R_S = 50Ω, C_{VCC} = 50pF, MAX3001E, Figures 1a, 1b		25	50	
		R_S = 50Ω, C_{VCC} = 50pF, MAX3002–MAX3012, Figures 1a, 1b			15	
I/O $V_{CC\_}$ Fall Time	t_{FVCC}	R_S = 50Ω, C_{VCC} = 50pF, MAX3000E, Figures 1a, 1b	400	800	1200	ns
		R_S = 50Ω, C_{VCC} = 50pF, MAX3001E, Figures 1a, 1b		25	50	
		R_S = 50Ω, C_{VCC} = 50pF, MAX3002–MAX3012, Figures 1a, 1b			15	
I/O $V_{L\_}$ Rise Time	t_{RVL}	R_S = 50Ω, C_{VL} = 50pF, MAX3000E, Figures 2a, 2b	400	800	1200	ns
		R_S = 50Ω, C_{VL} = 50pF, MAX3001E, Figures 2a, 2b		25	50	
		R_S = 50Ω, C_{VL} = 15pF, MAX3002–MAX3012, Figures 2a, 2b			15	
I/O $V_{L\_}$ Fall Time	t_{FVL}	R_S = 50Ω, C_{VL} = 50pF, MAX3000E, Figures 2a, 2b	400	800	1200	ns
		R_S = 50Ω, C_{VL} = 50pF, MAX3001E, Figures 2a, 2b		25	65	
		R_S = 50Ω, C_{VL} = 15pF, MAX3002–MAX3012, Figures 2a, 2b			15	
Propagation Delay (Driving I/O $V_{L\_}$)	I/O_{VL-VCC}	R_S = 50Ω, C_{VCC} = 50pF, MAX3000E, Figures 1a, 1b			1000	ns
		R_S = 50Ω, C_{VCC} = 50pF, MAX3001E, Figures 1a, 1b			50	
		R_S = 50Ω, C_{VCC} = 50pF, MAX3002–MAX3012, Figures 1a, 1b			20	
Propagation Delay (Driving I/O $V_{CC\_}$)	I/O_{VCC-VL}	R_S = 50Ω, C_{VL} = 50pF, MAX3000E, Figures 2a, 2b			1000	ns
		R_S = 50Ω, C_{VL} = 50pF, MAX3001E, Figures 2a, 2b			50	
		R_S = 50Ω, C_{VL} = 15pF, MAX3002–MAX3012, Figures 2a, 2b			20	

Note 1: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 2: For normal operation, ensure that V_L < (V_{CC} + 0.3V). During power-up, V_L > (V_{CC} + 0.3V) does not damage the device.

TIMING CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to V_{CC}, EN = V_L (MAX3000E/MAX3001E/MAX3002/MAX3004–MAX3012), EN A/B = V_L or 0 (MAX3003), T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = +1.65V, V_L = +1.2V, and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Channel-to-Channel Skew	t_{SKEW}	R_S = 50Ω, C_{VCC} = 50pF, C_{VL} = 50pF, MAX3000E			500	ns
		R_S = 50Ω, C_{VCC} = 50pF, C_{VL} = 50pF, MAX3001E			10	
		R_S = 50Ω, C_{VCC} = 50pF, C_{VL} = 15pF, MAX3002–MAX3012			5	
Part-to-Part Skew	t_{PPSKEW}	R_S = 50Ω, C_{VCC} = 50pF, C_{VL} = 50pF, ΔT_A = +20°C, MAX3000E (Note 3)			800	ns
		R_S = 50Ω, C_{VCC} = 50pF, C_{VL} = 50pF, ΔT_A = +20°C, MAX3001E (Note 3)			30	
		R_S = 50Ω, C_{VCC} = 50pF, C_{VL} = 15pF, ΔT_A = +20°C, MAX3002–MAX3012 (Note 3)			10	
Propagation Delay from I/O $V_{L\_}$ to I/O $V_{CC\_}$ after EN	t_{EN-VCC}	C_{VCC} = 50pF, MAX3000E/MAX3001E, MAX3002–MAX3012, Figure 3				µs
Propagation Delay from I/O $V_{CC\_}$ to I/O $V_{L\_}$ after EN	t_{EN-VL}	C_{VL} = 50pF, MAX3000E/MAX3001E/ MAX3002/MAX3004–MAX3012, Figure 4			2	µs
		C_{VL} = 15pF, MAX3003, Figure 4			2	
Maximum Data Rate		R_S = 50Ω, C_{VCC} = 50pF, C_{VL} = 50pF, MAX3000E	230			kbps
		R_S = 50Ω, C_{VCC} = 50pF, C_{VL} = 50pF, MAX3001E	4			Mbps
		R_S = 50Ω, C_{VCC} = 50pF, C_{VL} = 15pF, MAX3002–MAX3012	20			

Note 3: V_{CC} from device 1 must equal V_{CC} of device 2; V_L from device 1 must equal V_L of device 2.

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

TIMING CHARACTERISTICS—MAX3002–MAX3012

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to V_{CC}, EN = V_L (MAX3002/MAX3004–MAX3012), EN A/B = V_L or 0 (MAX3003), T_A = T_{MIN} to T_{MAX}.) (Notes 1, 2)

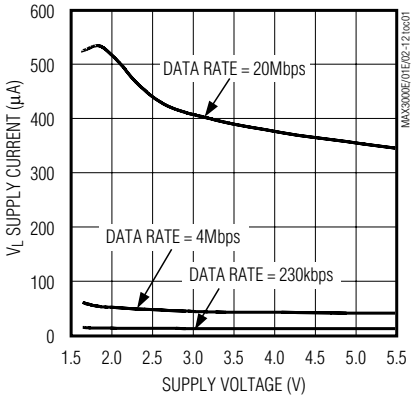
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
+1.2V ≤ V_L ≤ V_{CC} ≤ +3.3V						
I/O $V_{CC\_}$ Rise Time	t_{RVCC}				15	ns
I/O $V_{CC\_}$ Fall Time	t_{FVCC}				15	ns
I/O $V_{L\_}$ Rise Time	t_{RVL}				15	ns
I/O $V_{L\_}$ Fall Time	t_{FVL}				15	ns
Propagation Delay	I/O_{VL-VCC}	Driving I/O $V_{L\_}$			15	ns
	I/O_{VCC-VL}	Driving I/O $V_{CC\_}$			15	
Channel-to-Channel Skew	t_{SKEW}	Each translator equally loaded			5	ns
Maximum Data Rate			20			Mbps
+2.5V ≤ V_L ≤ V_{CC} ≤ +3.3V						
I/O $V_{CC\_}$ Rise Time	t_{RVCC}				8.5	ns
I/O $V_{CC\_}$ Fall Time	t_{FVCC}				8.5	ns
I/O $V_{L\_}$ Rise Time	t_{RVL}				8.5	ns
I/O $V_{L\_}$ Fall Time	t_{FVL}				8.5	ns
Propagation Delay	I/O_{VL-VCC}	Driving I/O $V_{L\_}$			8.5	ns
	I/O_{VCC-VL}	Driving I/O $V_{CC\_}$			8.5	
Channel-to-Channel Skew	t_{SKEW}	Each translator equally loaded			10	ns
Maximum Data Rate			35			Mbps
+1.8V ≤ V_L ≤ V_{CC} ≤ +2.5V						
I/O $V_{CC\_}$ Rise Time	t_{RVCC}				10	ns
I/O $V_{CC\_}$ Fall Time	t_{FVCC}				10	ns
I/O $V_{L\_}$ Rise Time	t_{RVL}				10	ns
I/O $V_{L\_}$ Fall Time	t_{FVL}				10	ns
Propagation Delay	I/O_{VL-VCC}	Driving I/O $V_{L\_}$			15	ns
	I/O_{VCC-VL}	Driving I/O $V_{CC\_}$			10	
Channel-to-Channel Skew	t_{SKEW}	Each translator equally loaded			5	ns
Maximum Data Rate			30			Mbps

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

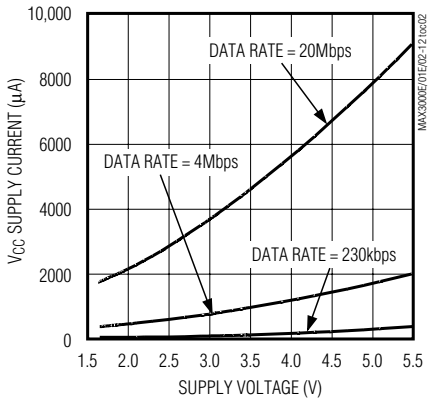
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

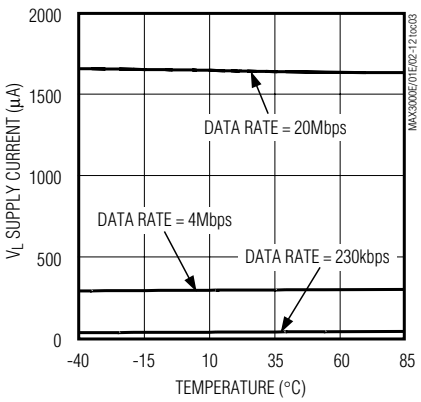
V_L SUPPLY CURRENT vs. SUPPLY VOLTAGE (DRIVING I/O V_L, V_L = 1.8V)



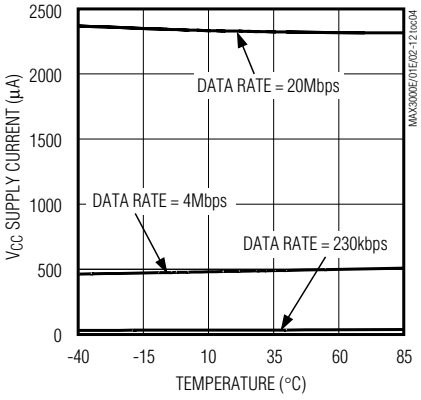
V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE (DRIVING I/O V_L, V_L = 1.8V)



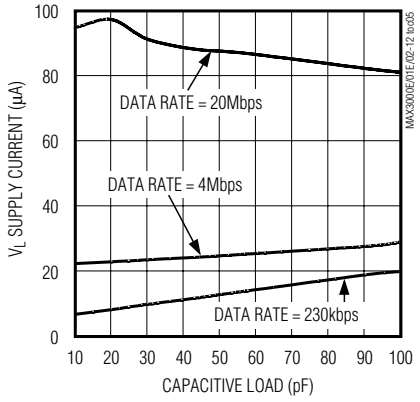
V_L SUPPLY CURRENT vs. TEMPERATURE (DRIVING I/O V_{CC}, V_{CC} = 3.3V, V_L = 1.8V)



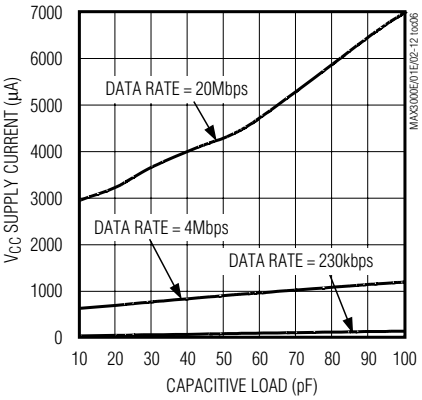
V_{CC} SUPPLY CURRENT vs. TEMPERATURE (DRIVING I/O V_{CC}, V_{CC} = 3.3V, V_L = 1.8V)



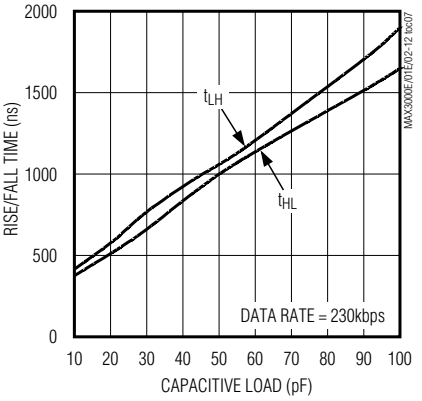
V_L SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING I/O V_L, V_{CC} = 3.3V, V_L = 1.8V)



V_{CC} SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING I/O V_L, V_{CC} = 3.3V, V_L = 1.8V)



MAX3000E RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING I/O V_L, V_{CC} = 3.3V, V_L = 1.8V)

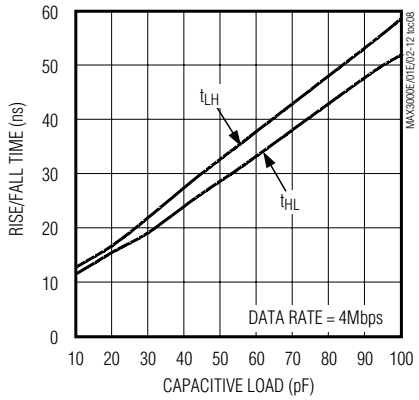


+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

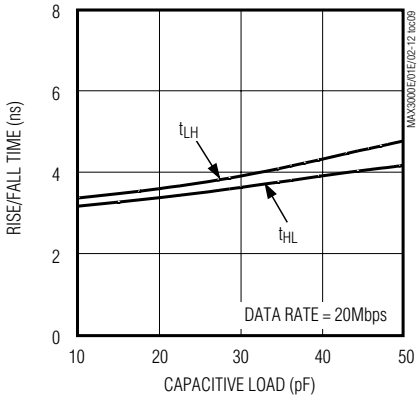
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

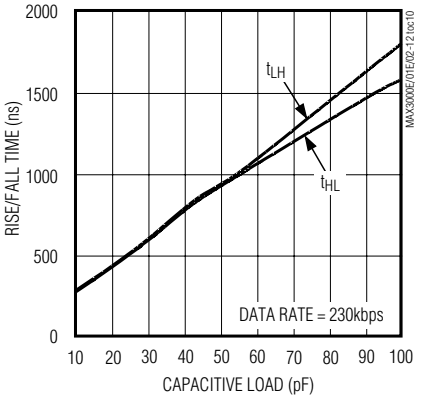
MAX3001E
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING I/O V_L, V_{CC} = 3.3V, V_L = 1.8V)



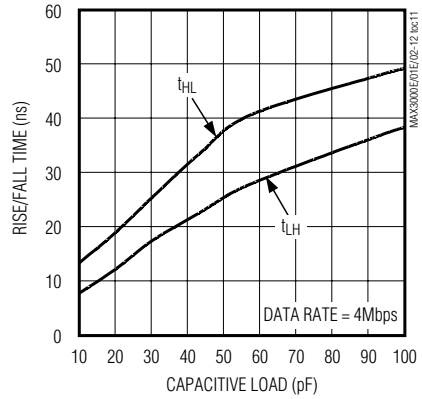
MAX3002–MAX3012
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING I/O V_L, V_{CC} = 3.3V, V_L = 1.8V)



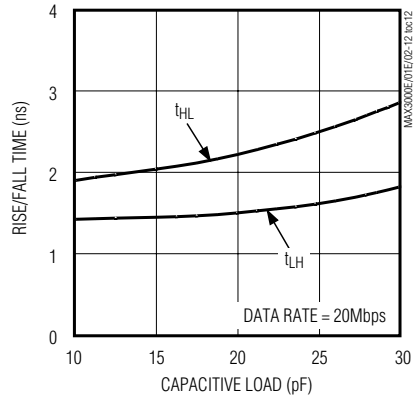
MAX3000E
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_L (DRIVING I/O V_{CC}, V_{CC} = 3.3V, V_L = 1.8V)



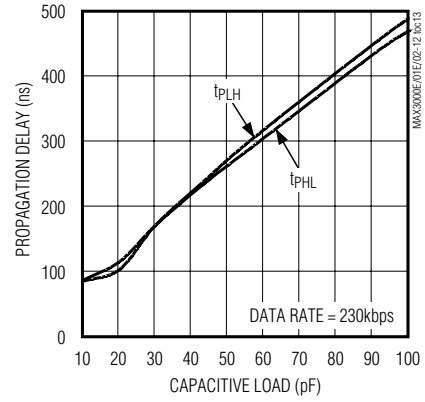
MAX3001E
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_L (DRIVING I/O V_{CC}, V_{CC} = 3.3V, V_L = 1.8V)



MAX3002–MAX3012
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_L (DRIVING I/O V_{CC}, V_{CC} = 3.3V, V_L = 1.8V)



MAX3000E
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING I/O V_L, V_{CC} = 3.3V, V_L = 1.8V)

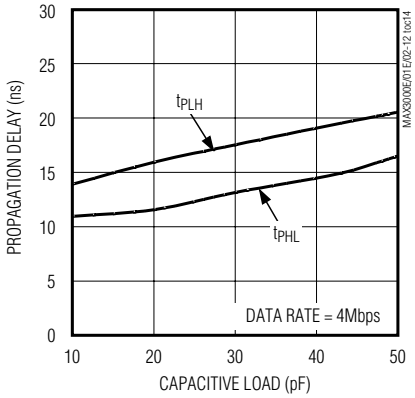


+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

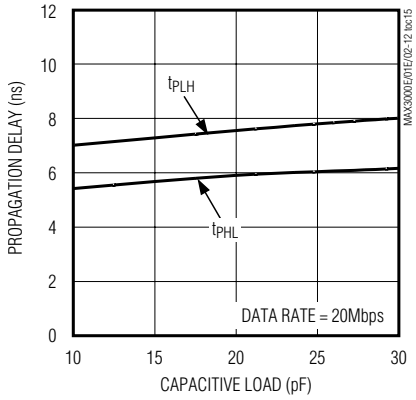
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

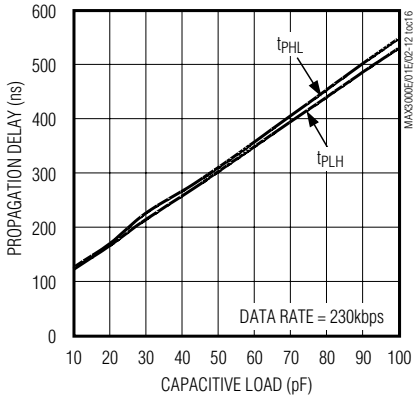
MAX3001E
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING I/O V_L, V_{CC} = 3.3V, V_L = 1.8V)



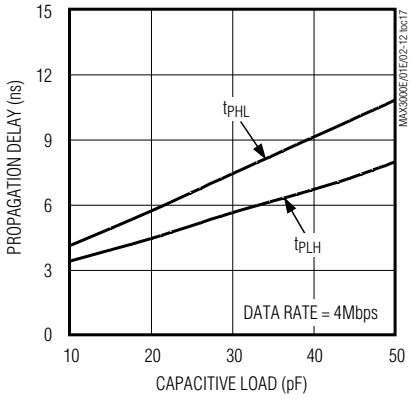
MAX3002–MAX3012
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_{CC} (DRIVING I/O V_L, V_{CC} = 3.3V, V_L = 1.8V)



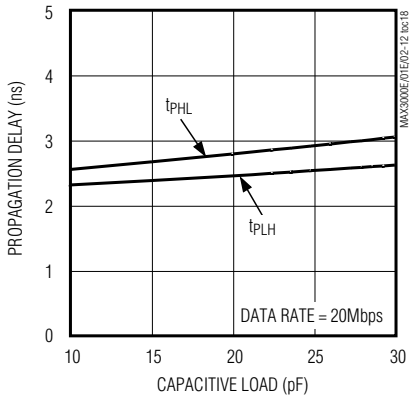
MAX3000E
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_L (DRIVING I/O V_{CC}, V_{CC} = 3.3V, V_L = 1.8V)



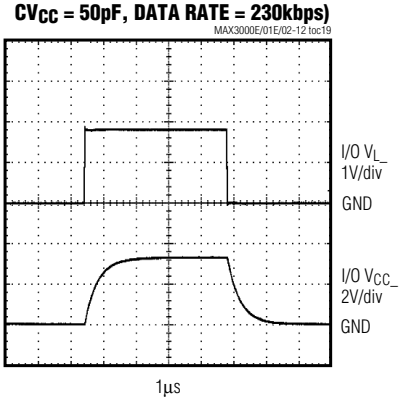
MAX3001E
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_L (DRIVING I/O V_{CC}, V_{CC} = 3.3V, V_L = 1.8V)



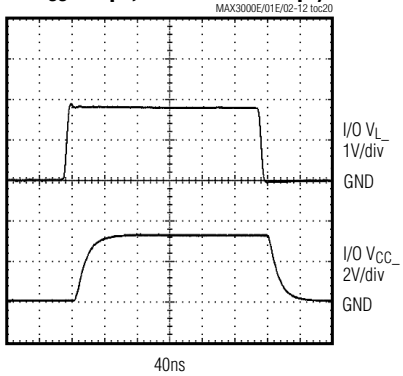
MAX3002–MAX3012
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O V_L (DRIVING I/O V_{CC}, V_{CC} = 3.3V, V_L = 1.8V)



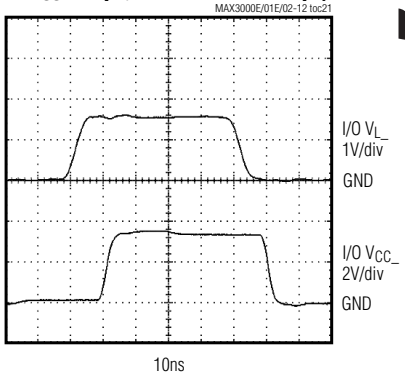
MAX3000E RAIL-TO-RAIL DRIVING (DRIVING I/O V_L, V_{CC} = 3.3V, V_L = 1.8V, CV_{CC} = 50pF, DATA RATE = 230kbps)



MAX3001E RAIL-TO-RAIL DRIVING (DRIVING I/O V_L, V_{CC} = 3.3V, V_L = 1.8V, CV_{CC} = 50pF, DATA RATE = 4Mbps)



MAX3002–MAX3012 RAIL-TO-RAIL DRIVING (DRIVING I/O V_L, V_{CC} = 3.3V, V_L = 1.8V, CV_{CC} = 50pF, DATA RATE = 20Mbps)



+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

Pin Description

MAX3000E/MAX3001E/MAX3002

PIN		NAME	FUNCTION
TSSOP	UCSP		
1	B1	I/O V_L1	Input/Output 1, Referenced to V_L
2	A1	V_L	Logic Input Voltage, +1.2V ≤ V_L ≤ V_{CC}. Bypass V_L to GND with a 0.1µF capacitor.
3	A2	I/O V_L2	Input/Output 2, Referenced to V_L
4	B2	I/O V_L3	Input/Output 3, Referenced to V_L
5	A3	I/O V_L4	Input/Output 4, Referenced to V_L
6	B3	I/O V_L5	Input/Output 5, Referenced to V_L
7	A4	I/O V_L6	Input/Output 6, Referenced to V_L
8	B4	I/O V_L7	Input/Output 7, Referenced to V_L
9	A5	I/O V_L8	Input/Output 8, Referenced to V_L
10	B5	EN	Enable Input. If EN is pulled low, I/O V_{CC}1 to I/O V_{CC}8 are in three-state, while I/O V_L1 to I/O V_L8 have internal 6kΩ pulldown resistors. Drive EN high (V_L) for normal operation.
11	C5	GND	Ground
12	D5	I/O V_{CC}8	Input/Output 8, Referenced to V_{CC}
13	C4	I/O V_{CC}7	Input/Output 7, Referenced to V_{CC}
14	D4	I/O V_{CC}6	Input/Output 6, Referenced to V_{CC}
15	C3	I/O V_{CC}5	Input/Output 5, Referenced to V_{CC}
16	D3	I/O V_{CC}4	Input/Output 4, Referenced to V_{CC}
17	C2	I/O V_{CC}3	Input/Output 3, Referenced to V_{CC}
18	D2	I/O V_{CC}2	Input/Output 2, Referenced to V_{CC}
19	D1	V_{CC}	V_{CC} Input Voltage, +1.65V ≤ V_{CC} ≤ +5.5V. Bypass V_{CC} to GND with a 0.1µF capacitor.
20	C1	I/O V_{CC}1	Input/Output 1, Referenced to V_{CC}

Pin Description (continued)

MAX3003

PIN		NAME	FUNCTION
TSSOP	UCSP		
1	B1	I/O V_L1A	Input/Output 1A, Referenced to V_L
2	A1	V_L	Logic Input Voltage, +1.2V ≤ V_L ≤ V_{CC}. Bypass V_L to GND with a 0.1µF capacitor.
3	A2	I/O V_L2A	Input/Output 2A, Referenced to V_L
4	B2	I/O V_L3A	Input/Output 3A, Referenced to V_L
5	A3	I/O V_L4A	Input/Output 4A, Referenced to V_L
6	B3	I/O V_L1B	Input/Output 1B, Referenced to V_L
7	A4	I/O V_L2B	Input/Output 2B, Referenced to V_L
8	B4	I/O V_L3B	Input/Output 3B, Referenced to V_L
9	A5	I/O V_L4B	Input/Output 4B, Referenced to V_L
10	B5	EN A/B	Enable Input. If EN A/B is pulled low, channels 1B through 4B are active, and channels 1A through 4A are in three-state. If EN A/B is driven high to V_L, channels 1A through 4A are active, and channels 1B through 4B are in three-state.
11	C5	GND	Ground
12	D5	I/O V_{CC}4B	Input/Output 4B, Referenced to V_{CC}
13	C4	I/O V_{CC}3B	Input/Output 3B, Referenced to V_{CC}
14	D4	I/O V_{CC}2B	Input/Output 2B, Referenced to V_{CC}
15	C3	I/O V_{CC}1B	Input/Output 1B, Referenced to V_{CC}
16	D3	I/O V_{CC}4A	Input/Output 4A, Referenced to V_{CC}
17	C2	I/O V_{CC}3A	Input/Output 3A, Referenced to V_{CC}
18	D2	I/O V_{CC}2A	Input/Output 2A, Referenced to V_{CC}
19	D1	V_{CC}	V_{CC} Input Voltage, +1.65V ≤ V_{CC} ≤ +5.5V. Bypass V_{CC} to GND with a 0.1µF capacitor.
20	C1	I/O V_{CC}1A	Input/Output 1A, Referenced to V_{CC}

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

Pin Description (continued)

MAX3004–MAX3012

NAME	FUNCTION (Note 1)
V_{CC}	V_{CC} Input Voltage, +1.65V < V_{CC} < +5.5V. Bypass V_{CC} to GND with a 0.1µF capacitor.
V_L	Logic Input Voltage, +1.2V ≤ V_L ≤ V_{CC}. Bypass V_L to GND with a 0.1µF capacitor.
GND	Ground
EN (MAX3004)	Enable Input. If EN is pulled low, $OV_{CC}1$–$OV_{CC}8$ are in three-state, while IV_L1–IV_L8 have 6kΩ pulldown resistors. Drive EN high (V_L) for normal operation.
EN (MAX3005)	Enable Input. If EN is pulled low, $IV_{CC}1$ and $OV_{CC}2$–$OV_{CC}8$ are in three-state, while OV_L1 and IV_L2–IV_L8 have 6kΩ pulldown resistors. Drive EN high (V_L) for normal operation.
EN (MAX3006)	Enable Input. If EN is pulled low, $IV_{CC}1$, $IV_{CC}2$, and $OV_{CC}3$–$OV_{CC}8$ are in three-state, while OV_L1, OV_L2, and IV_L3–IV_L8 have 6kΩ pulldown resistors. Drive EN high (V_L) for normal operation.
EN (MAX3007)	Enable Input. If EN is pulled low, $IV_{CC}1$, $IV_{CC}2$, $IV_{CC}3$, and $OV_{CC}4$–$OV_{CC}8$ are in three-state, while OV_L1, OV_L2, OV_L3, and IV_L4–IV_L8 have 6kΩ pulldown resistors. Drive EN high (V_L) for normal operation.
EN (MAX3008)	Enable Input. If EN is pulled low, $IV_{CC}1$–$IV_{CC}4$ and $OV_{CC}5$–$OV_{CC}8$ are in three-state, while OV_L1–OV_L4 and IV_L5–IV_L8 have 6kΩ pulldown resistors. Drive EN high (V_L) for normal operation.
EN (MAX3009)	Enable Input. If EN is pulled low, $IV_{CC}1$–$IV_{CC}5$, $OV_{CC}6$, $OV_{CC}7$, and $OV_{CC}8$ are in three-state, while OV_L1–OV_L5, IV_L6, IV_L7, and IV_L8 have 6kΩ pulldown resistors. Drive EN high (V_L) for normal operation.
EN (MAX3010)	Enable Input. If EN is pulled low, $IV_{CC}1$–$IV_{CC}6$, $OV_{CC}7$, and $OV_{CC}8$ are in three-state, while OV_L1–OV_L6, IV_L7, and IV_L8 have 6kΩ pulldown resistors. Drive EN high (V_L) for normal operation.
EN (MAX3011)	Enable Input. If EN is pulled low, $IV_{CC}1$–$IV_{CC}7$ and $OV_{CC}8$ are in three-state, while OV_L1–OV_L7 and IV_L8 have 6kΩ pulldown resistors. Drive EN high (V_L) for normal operation.
EN (MAX3012)	Enable Input. If EN is pulled low, $IV_{CC}1$–$IV_{CC}8$ are in three-state, while OV_L1–OV_L8 have 6kΩ pulldown resistors. Drive EN high (V_L) for normal operation.
IV_L1–IV_L8	Inputs Referenced to V_L, Numbers 1 to 8
OV_L1–OV_L8	Outputs Referenced to V_L, Numbers 1 to 8
$IV_{CC}1$–$IV_{CC}8$	Inputs Referenced to V_{CC}, Numbers 1 to 8
$OV_{CC}1$–$OV_{CC}8$	Outputs Referenced to V_{CC}, Numbers 1 to 8

Note 1: For specific pin numbers, see the *Pin Configurations*.

Test Circuits/Timing Diagrams

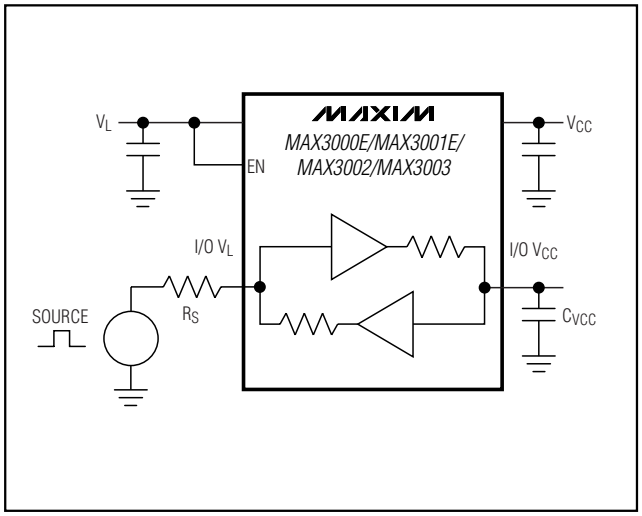


Figure 1a. Driving I/O V_L

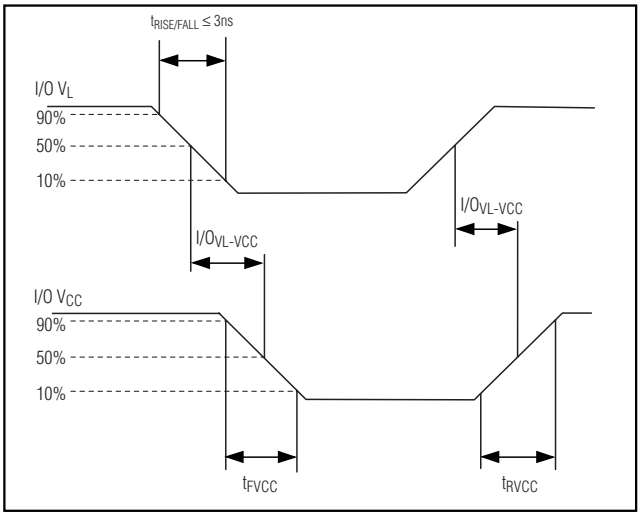


Figure 1b. Timing for Driving I/O V_L

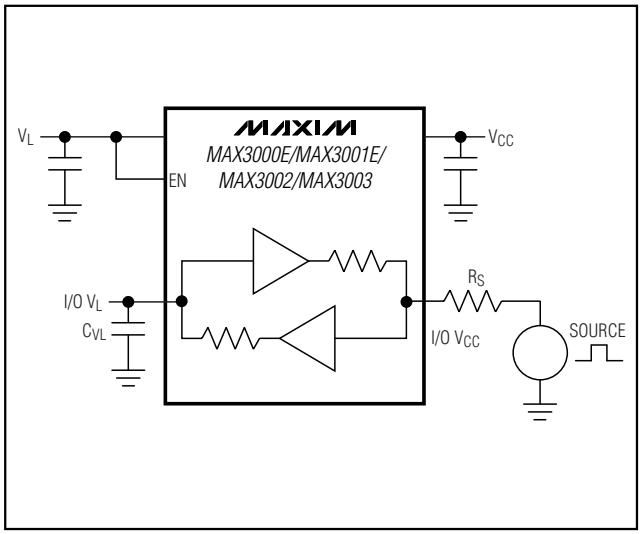


Figure 2a. Driving I/O V_{CC}

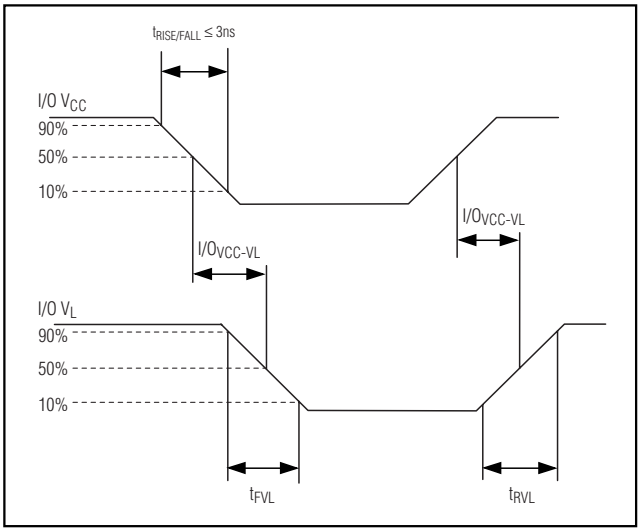


Figure 2b. Timing for Driving I/O V_{CC}

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

Test Circuits/Timing Diagrams (continued)

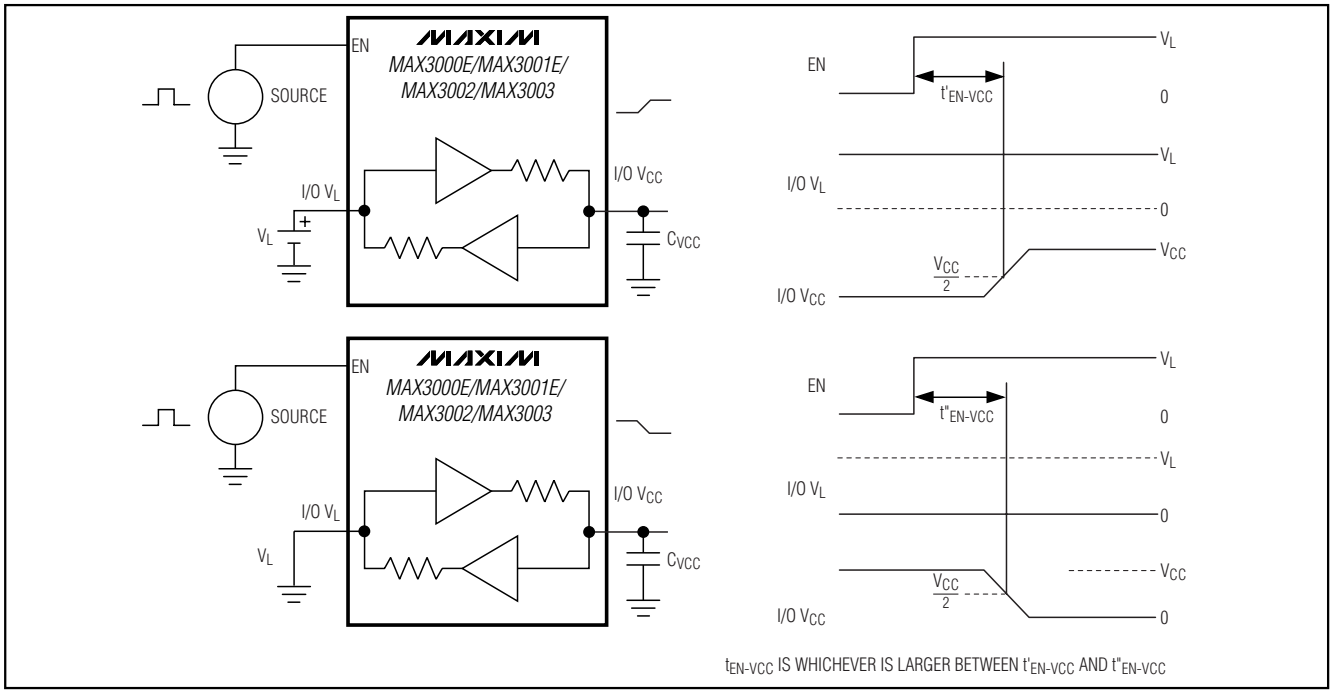


Figure 3. Propagation Delay from I/O V_L to I/O V_{CC} After EN

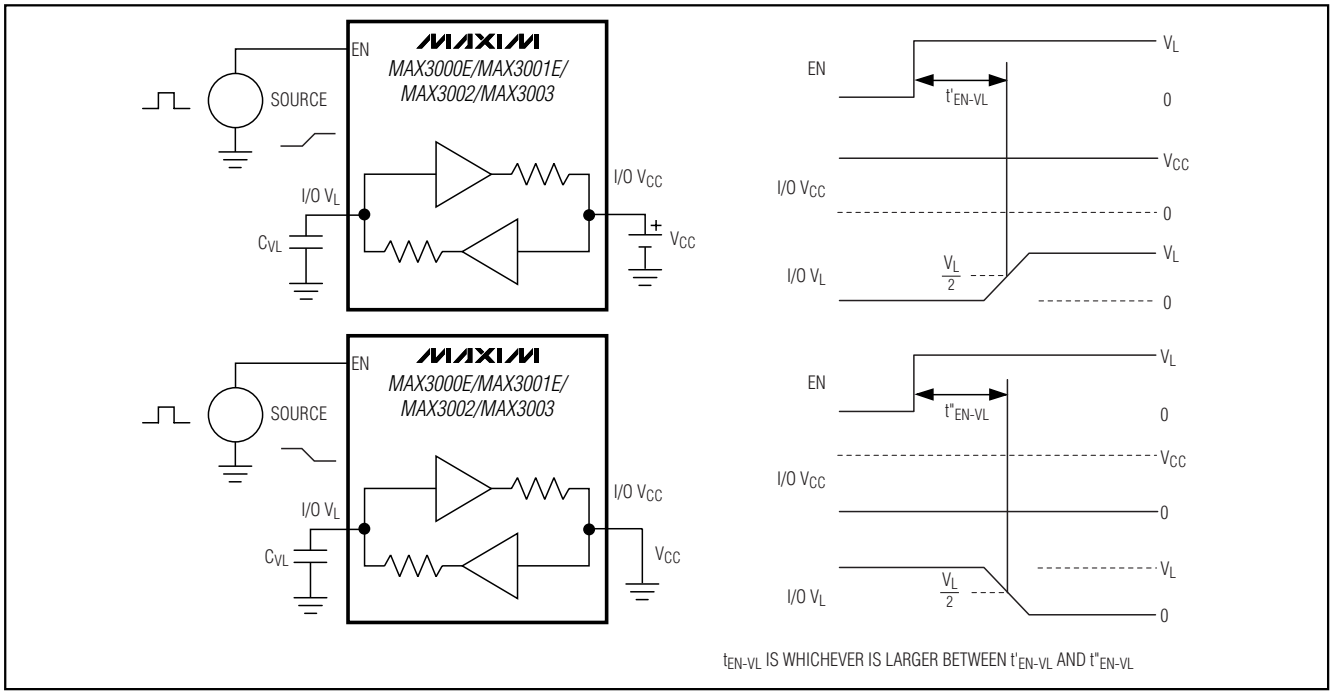


Figure 4. Propagation Delay from I/O V_{CC} to I/O V_L After EN

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

Detailed Description

The MAX3000E/MAX3001E/MAX3002–MAX3012 logic-level translators provide the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a higher voltage logic signal on the V_{CC} side of the device, and vice-versa. The MAX3000E/MAX3001E/MAX3002/MAX3003 are bidirectional level translators allowing data translation in either direction ($V_L \leftrightarrow V_{CC}$) on any single data line. The MAX3004–MAX3012 unidirectional level translators level shift data in one direction ($V_L \rightarrow V_{CC}$ or $V_{CC} \rightarrow V_L$) on any single data line. The MAX3000E/MAX3001E/MAX3002–MAX3012 accept V_L from +1.2V to +5.5V. All devices have V_{CC} ranging from +1.65V to +5.5V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The MAX3000E/MAX3001E/MAX3002/MAX3004–MAX3012 feature an output enable mode that reduces V_{CC} supply current to less than 2µA, and V_L supply current to less than 2µA when in shutdown. The MAX3000E/MAX3001E have ±15kV ESD protection on the V_{CC} side for greater protection in applications that route signals externally. The MAX3000E operates at a guaranteed data rate of 230kbps; the MAX3001E operates at a guaranteed data rate of 4Mbps and the MAX3002–MAX3012 are guaranteed with a data rate of 20Mbps of operation over the entire specified operating voltage range.

Level Translation

For proper operation, ensure that $+1.65V \le V_{CC} \le +5.5V$, $+1.2V \le V_L \le +5.5V$, and $V_L \le V_{CC}$. During power-up sequencing, $V_L \ge V_{CC}$ does not damage the device. During power-supply sequencing, when V_{CC} is floating and V_L is powering up, up to 10mA current can be sourced to each load on the V_L side, yet the device does not latch up.

The maximum data rate also depends heavily on the load capacitance (see the *Typical Operating Characteristics*), output impedance of the driver, and the operational voltage range (see the *Timing Characteristics*).

Input Driver Requirements

The MAX3001E/MAX3002–MAX3012 architecture is based on a one-shot accelerator output stage. See Figure 5. Accelerator output stages are always in three-state except when there is a transition on any of the translators on the input side, either I/O V_L or I/O V_{CC}.

Then, a short pulse is generated during which the accelerator output stages become active and charge/discharge the capacitances at the I/Os. Due to its bidirectional nature, both input stages become active during the one-shot pulse. This can lead to some current feeding into the external source that is driving the translator. However, this behavior helps to speed up the transition on the driven side.

For proper operation, the driver has to meet the following conditions: 50Ω maximum output impedance and 20mA minimum output current (for 20Mbps versions), 400Ω maximum output impedance and 4mA minimum output current (for 4Mbps versions), 1kΩ maximum output impedance and 1mA minimum output current (for 230kbps versions). Figure 6 shows a typical input current vs. input voltage.

Enable Output Mode (EN, EN A/B)

The MAX3000E/MAX3001E/MAX3002 and the MAX3004–MAX3012 feature an EN input, and the MAX3003 has an EN A/B input. Pull EN low to set the MAX3000E/MAX3001E/MAX3002/MAX3004–MAX3012s' I/O $V_{CC}1$ through I/O $V_{CC}8$ in three-state output mode, while I/O V_L1 through I/O V_L8 have internal 6kΩ pulldown resistors. Drive EN to logic high (V_L) for normal operation. For the MAX3003, pull EN A/B low to place channels 1B through 4B in active mode, while channels 1A through 4A are in three-state mode. Drive EN A/B to logic high (V_L) to enable channels 1A through 4A, while channels 1B through 4B remain in three-state mode.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The I/O V_{CC} lines have extra protection against static discharge. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, three-state output mode, and powered down. After an ESD event, Maxim's E versions keep working without latchup, whereas competing products can latch and must be powered down to remove latchup.

ESD protection can be tested in various ways. The I/O V_{CC} lines of the MAX3000E/MAX3001E are characterized for protection to ±15kV using the Human Body Model.

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

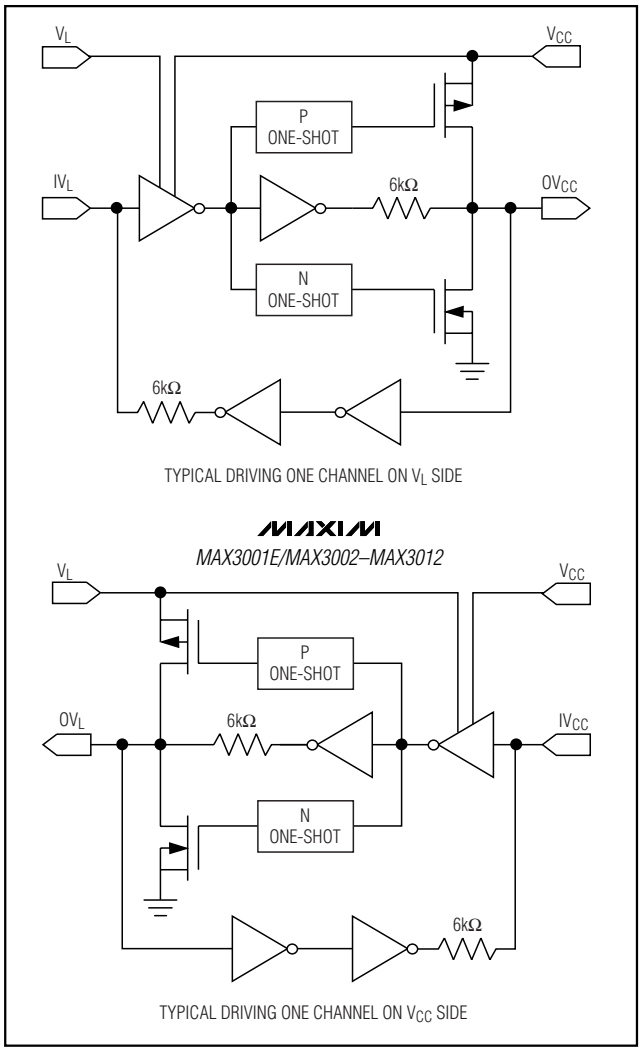


Figure 5. MAX3001E/MAX3002–MAX3012 Simplified Functional Diagram (1 I/O Line)

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 7a shows the Human Body Model and Figure 7b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

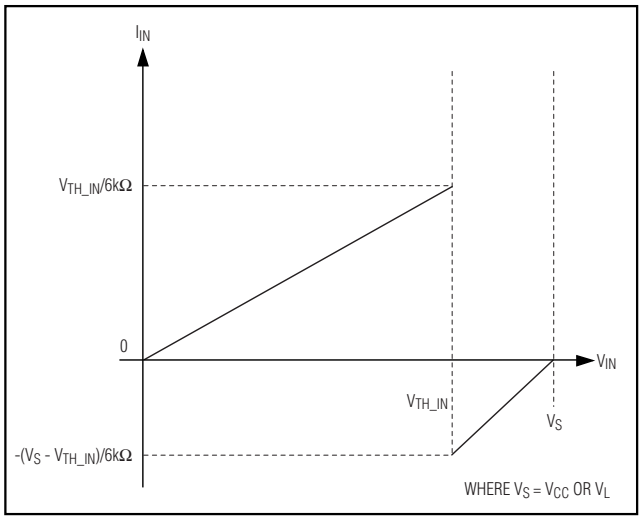


Figure 6. Typical I_{IN} vs. V_{IN}

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing, not just inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

Power-Supply Decoupling

To reduce ripple and the chance of transmitting incorrect data, bypass V_L and V_{CC} to ground with a 0.1µF capacitor. To ensure full ±15kV ESD protection, bypass V_{CC} to ground with a 1µF capacitor. Place all capacitors as close to the power-supply inputs as possible.

I²C Level Translation

For I²C level translation for I²C applications, please refer to the MAX3372E–MAX3379E/MAX3390E–MAX3393E datasheet.

Unidirectional vs. Bidirectional Level Translator

The MAX3000E/MAX3001E/MAX3002/MAX3003 can also be used to translate signals without inversion. These devices provide the smallest solution (UCSP package) for unidirectional level translation without inversion.

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

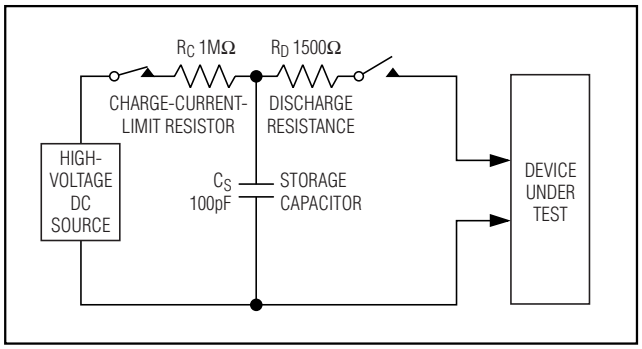


Figure 7a. Human Body ESD Test Model

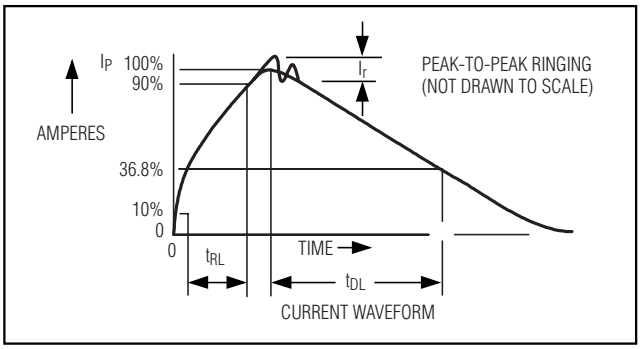


Figure 7b. Human Body Current Waveform

Selector Guide

PART	EN	EN A/B	Tx/Rx*	DATA RATE	ESD PROTECTION (kV)
MAX3000E	√	—	8/8	230kbps	±15
MAX3001E	√	—	8/8	4Mbps	±15
MAX3002	√	—	8/8	**	±2
MAX3003	—	√	8/8	**	±2
MAX3004	√	—	8/0	**	±2
MAX3005	√	—	7/1	**	±2
MAX3006	√	—	6/2	**	±2
MAX3007	√	—	5/3	**	±2
MAX3008	√	—	4/4	**	±2
MAX3009	√	—	3/5	**	±2
MAX3010	√	—	2/6	**	±2
MAX3011	√	—	1/7	**	±2
MAX3012	√	—	0/8	**	±2

**Tx = $V_L \rightarrow V_{CC}$; Rx = $V_{CC} \rightarrow V_L$*

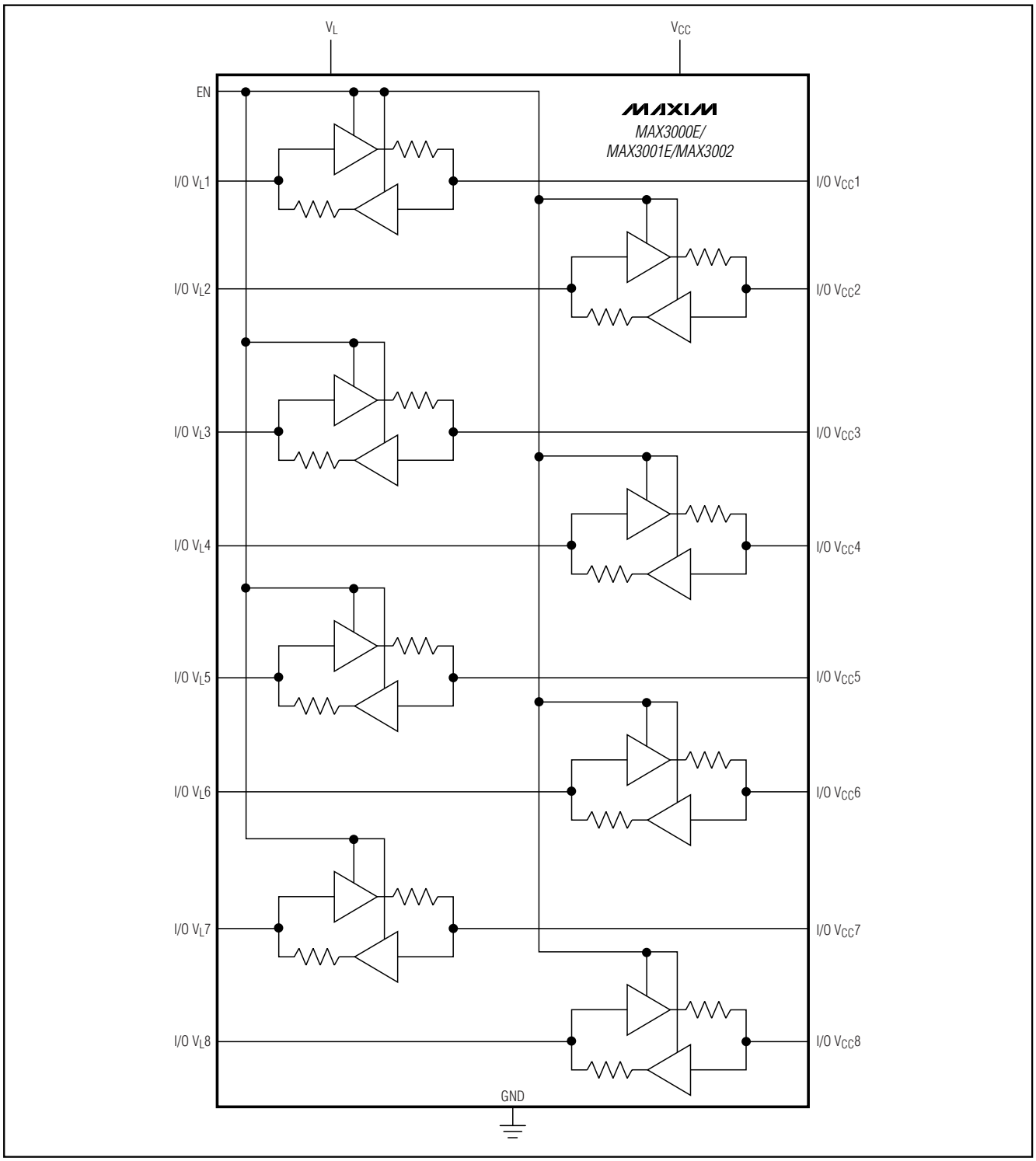
***See Table 1.*

Table 1. Data Rate

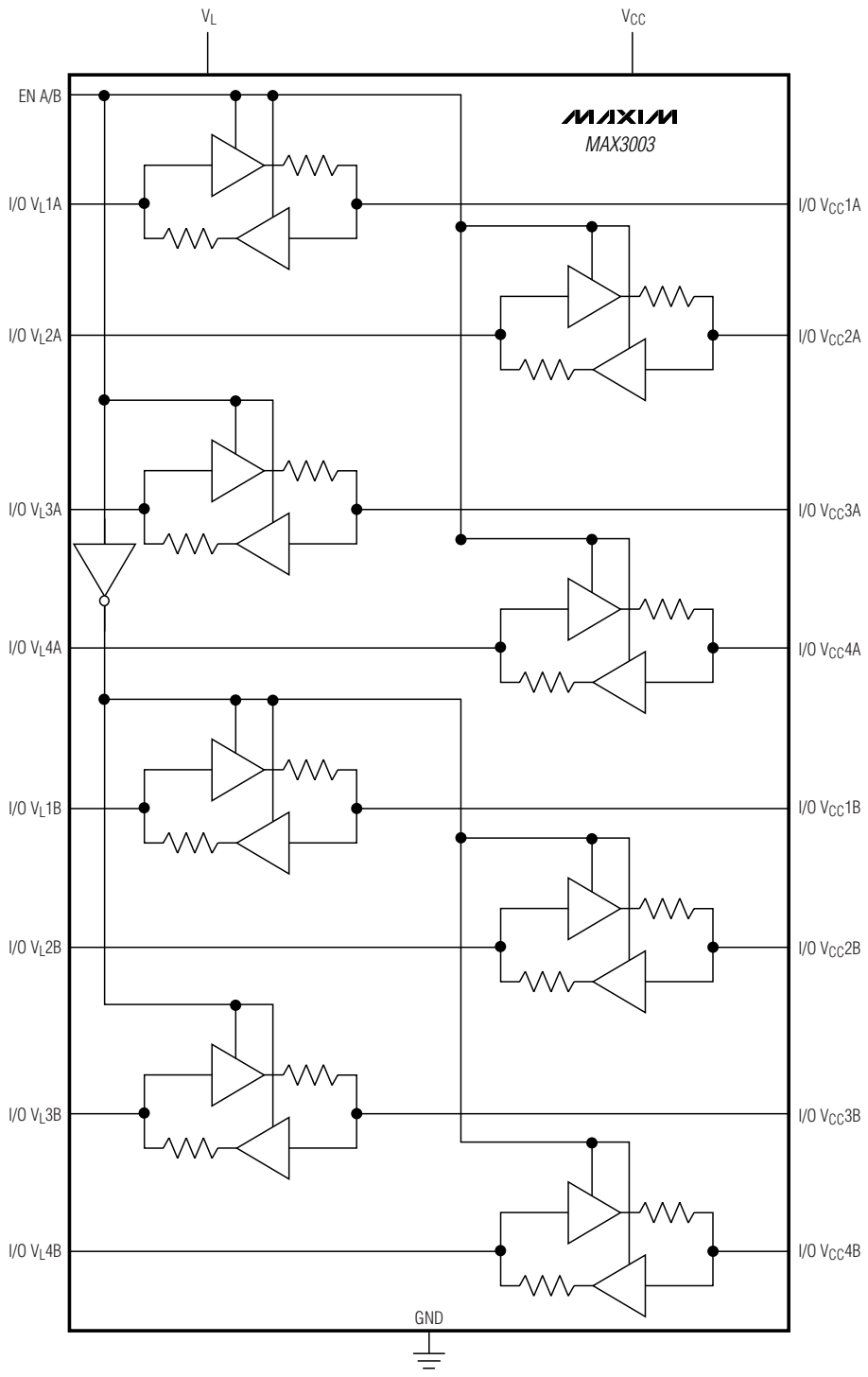
$V_L \leftrightarrow V_{CC}$ (V)	MAX3002–MAX3012 GUARANTEED DATA RATE (Mbps)
1.2 ↔ 5.5	40
1.2 ↔ 3.3	20
2.5 ↔ 3.3	35
1.8 ↔ 2.5	30
1.2 ↔ 2.5	20
1.2 ↔ 1.8	20

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

MAX3000E/MAX3001E/MAX3002 Functional Diagram



MAX3003 Functional Diagram

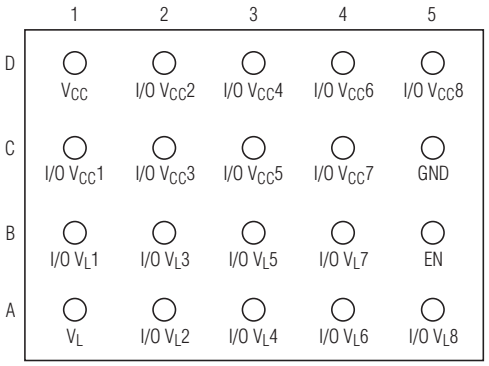


+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

Pin Configurations

MAXIM

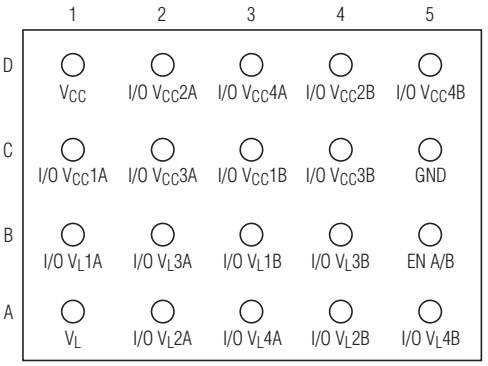
MAX3000E/MAX3001E/MAX3002
MAX3004–MAX3012



20 UCSP
(Bottom View)

MAXIM

MAX3003

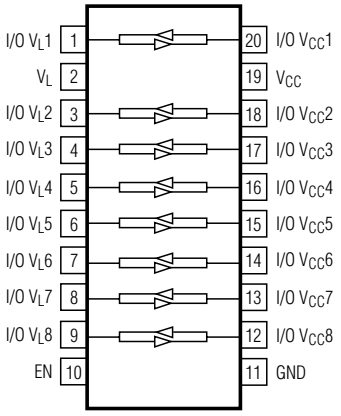


20 UCSP
(Bottom View)

MAXIM

MAX3000E/MAX3001E/
MAX3002

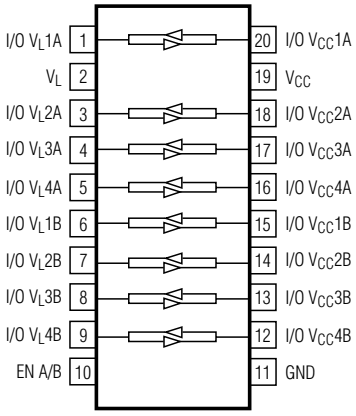
TOP VIEW



TSSOP

MAXIM

MAX3003



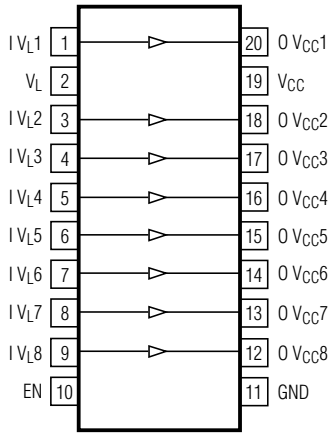
TSSOP

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

Pin Configurations (continued)

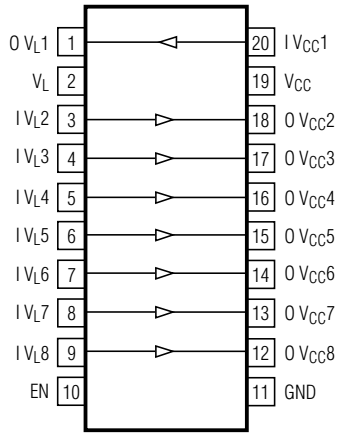
TOP VIEW

MAX3004



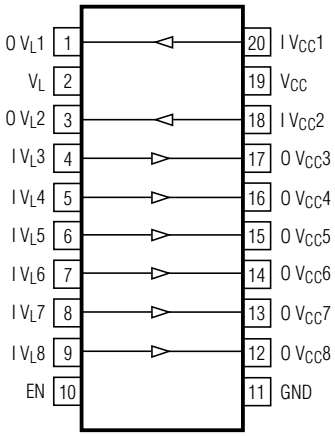
TSSOP

MAX3005



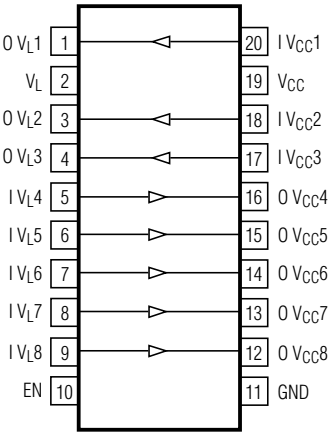
TSSOP

MAX3006



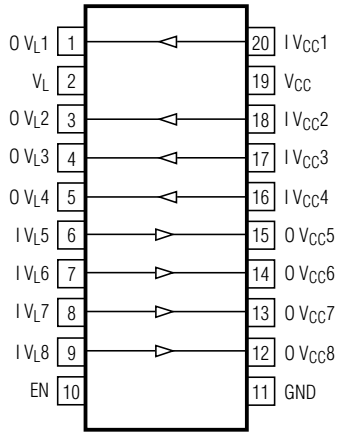
TSSOP

MAX3007



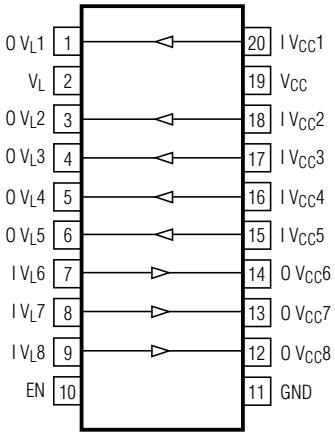
TSSOP

MAX3008



TSSOP

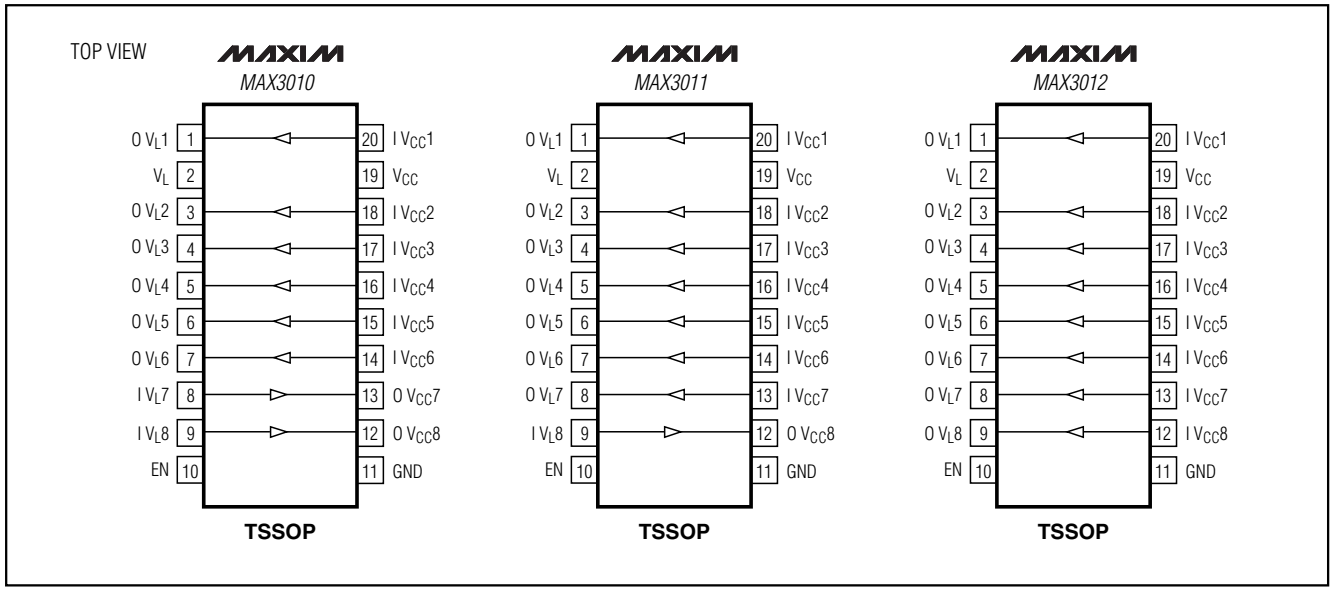
MAX3009



TSSOP

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

Pin Configurations (continued)



Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX3001EEUP	-40°C to +85°C	20 TSSOP
MAX3001EEBP-T*	-40°C to +85°C	4 x 5 UCSP
MAX3001EAUP	-40°C to +125°C	20 TSSOP
MAX3002EUP	-40°C to +85°C	20 TSSOP
MAX3002EBP-T*	-40°C to +85°C	4 x 5 UCSP
MAX3003EUP	-40°C to +85°C	20 TSSOP
MAX3003EBP-T*	-40°C to +85°C	4 x 5 UCSP
MAX3004EUP*	-40°C to +85°C	20 TSSOP
MAX3004EBP-T*	-40°C to +85°C	4 x 5 UCSP
MAX3005EUP*	-40°C to +85°C	20 TSSOP
MAX3005EBP-T*	-40°C to +85°C	4 x 5 UCSP
MAX3006EUP*	-40°C to +85°C	20 TSSOP
MAX3006EBP-T*	-40°C to +85°C	4 x 5 UCSP

PART	TEMP RANGE	PIN-PACKAGE
MAX3007EUP*	-40°C to +85°C	20 TSSOP
MAX3007EBP-T*	-40°C to +85°C	4 x 5 UCSP
MAX3008EUP*	-40°C to +85°C	20 TSSOP
MAX3008EBP-T*	-40°C to +85°C	4 x 5 UCSP
MAX3009EUP*	-40°C to +85°C	20 TSSOP
MAX3009EBP-T*	-40°C to +85°C	4 x 5 UCSP
MAX3010EUP*	-40°C to +85°C	20 TSSOP
MAX3010EBP-T*	-40°C to +85°C	4 x 5 UCSP
MAX3011EUP*	-40°C to +85°C	20 TSSOP
MAX3011EBP-T*	-40°C to +85°C	4 x 5 UCSP
MAX3012EUP*	-40°C to +85°C	20 TSSOP
MAX3012EBP-T*	-40°C to +85°C	4 x 5 UCSP

**Future product—contact factory for availability.*

Chip Information

TRANSISTOR COUNT: 1184

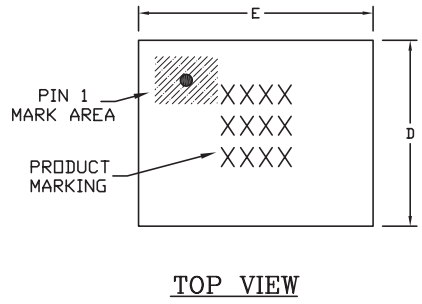
PROCESS: BiCMOS

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

5x4 UCSP EPS

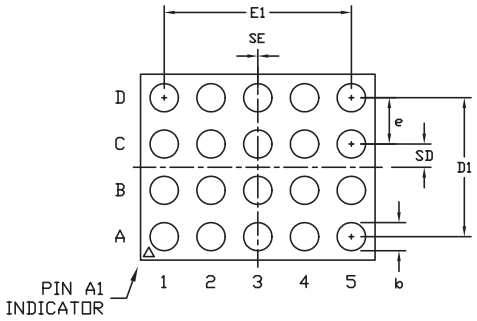


TOP VIEW

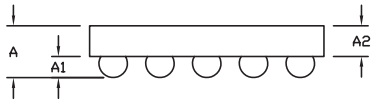
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.50 BASIC
E1	2.00 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B20-1	2.03±0.08	2.54±0.08	NONE
B20-2	2.03±0.08	2.54±0.08	B2, B3, B4
B20-4	2.03±0.08	2.54±0.08	B2, B3, B4, C2, C4
B20-5	2.03±0.08	2.54±0.08	B2, B3, B4, C2, C3, C4
B20-6	2.16±0.08	2.54±0.08	B2, B3, B4

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 5x4 UCSP

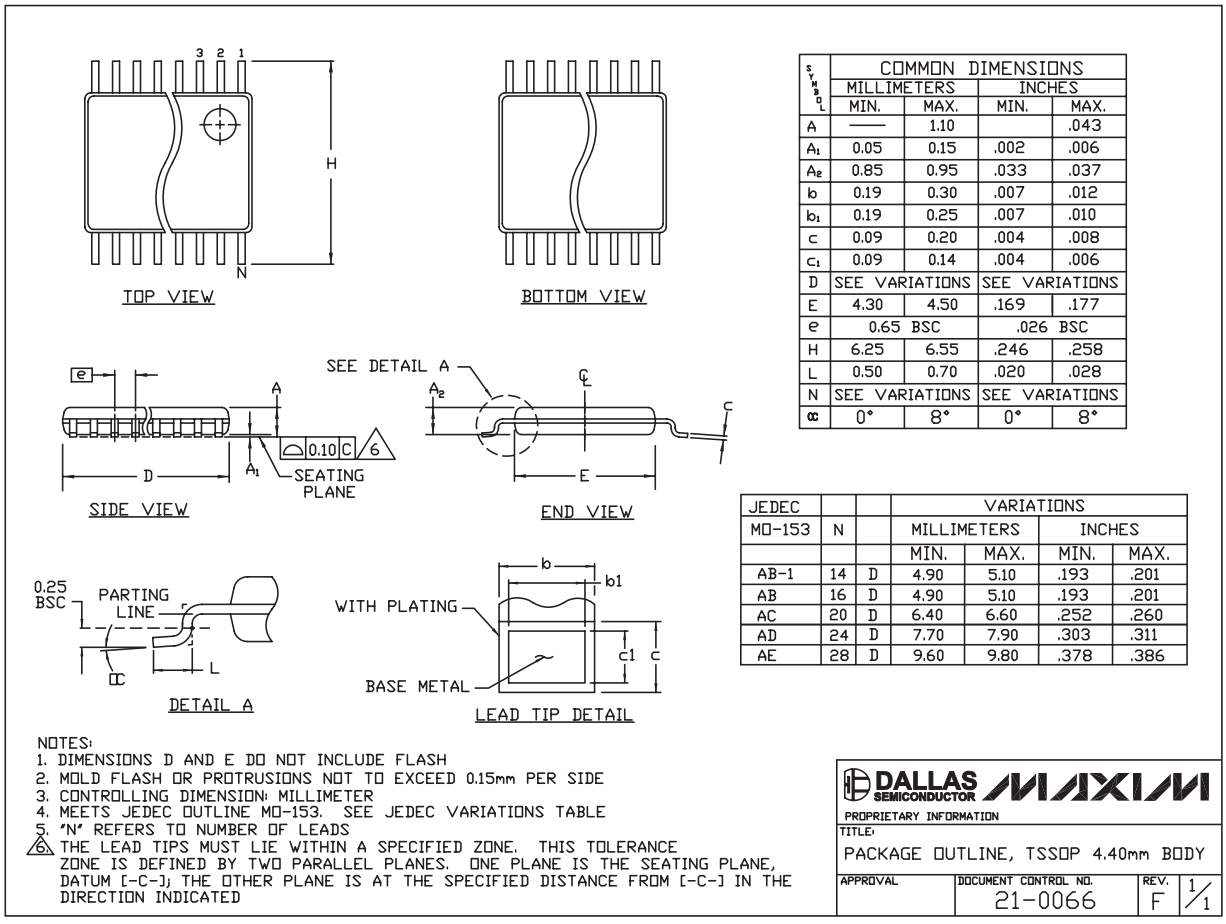
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0095	I	1/1

+1.2V to +5.5V, ±15kV ESD-Protected, 0.1µA, 35Mbps, 8-Channel Level Translators

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY
APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV. F | 1/1