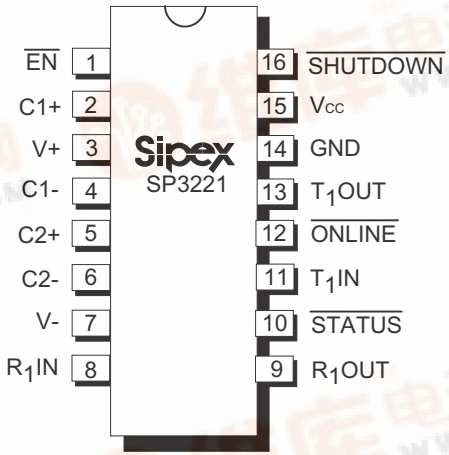
SP3221E

Intelligent +3.0V to +5.5V RS-232 Transceiver

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Operates with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
- ***Auto-Online***™ circuitry allows 1µA supply current when in shutdown
- 240kbps data rate under load
- 6V/µs minimum slew rate
- The SP3221 is the industries smallest single-supply RS-232 transceiver package
- Enhanced ESD Specifications:
  ±15KV Human Body Model
  ±15KV IEC1000-4-2 Air Discharge
  ±8KV IEC1000-4-2 Contact Discharge



Now Available in Lead Free Packaging

DESCRIPTION

The **SP3221E** is a RS-232 transceiver solution intended for portable or hand-held applications such as notebook and palmtop computers. The **SP3221E** has a high-efficiency, charge-pump power supply that requires only 0.1µF capacitors in 3.3V operation. This charge pump and low dropout transmitters allow the **SP3221E** device to deliver true RS-232 performance from a single power supply ranging from +3.3V to +5.0V. The ***Auto-Online*** feature allows the device to automatically "wake-up" during a shutdown state when an RS-232 cable is connected . Otherwise, the device automatically shuts itself down drawing less than 1µA.

SELECTION TABLE

Device	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	Auto-Online Circuitry	TTL 3-State	No. of Pins
SP3221E	+3.0V to +5.5V	1	1	4 (0.1µF) capacitors	YES	YES	16
SP3220E	+3.0V to +5.5V	1	1	4 (0.1µF) capacitors	NO	YES	16

Applicable U.S. Patents - 5,306,954; and other patents pending.

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}.....-0.3V to +6.0V
V+ (NOTE 1).....-0.3V to +7.0V
V- (NOTE 1).....+0.3V to -7.0V
V+ + |V-| (NOTE 1).....+13V
I_{CC} (DC V_{CC} or GND current).....±100mA

Input Voltages

TxIN, $\overline{\text{ONLINE}}$, $\overline{\text{SHUTDOWN}}$, $\overline{\text{EN}}$ .....-0.3V to +6.0V
RxIN.....±15V

Output Voltages

TxOUT.....±15V
RxOUT, $\overline{\text{STATUS}}$.....-0.3V to (V_{CC} + 0.3V)

Short-Circuit Duration

TxOUT.....Continuous
Storage Temperature.....-65°C to +150°C

Power Dissipation per package

16-pin PDIP (derate 14.3mW/°C above+70°C).....1150mW
16-pin SSOP (derate 9.69mW/°C above +70°C)....775mW

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

SPECIFICATIONS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.5V with T_{AMB} = T_{MIN} to T_{MAX}. Typical values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current, *Auto-Online*		1.0	10	µA	All RxIN open, $\overline{\text{ONLINE}}$ = GND, $\overline{\text{SHUTDOWN}}$ = V_{CC}, V_{CC} = +3.3V, T_{AMB} = +25° C
Supply Current, Shutdown		1.0	10	µA	$\overline{\text{SHUTDOWN}}$ = GND, V_{CC} = +3.3V, T_{AMB} = +25° C
Supply Current, *Auto-Online* Disabled		0.3	1.0	mA	$\overline{\text{ONLINE}}$ = $\overline{\text{SHUTDOWN}}$ = V_{CC}, no load, V_{CC} = +3.3V, T_{AMB} = +25° C
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW HIGH	 2.0		0.8	V	V_{CC} = +3.3V or +5.0V, TxIN, $\overline{\text{EN}}$, $\overline{\text{ONLINE}}$, $\overline{\text{SHUTDOWN}}$
Input Leakage Current		±0.01	±1.0	µA	TxIN, $\overline{\text{EN}}$, $\overline{\text{ONLINE}}$, $\overline{\text{SHUTDOWN}}$, T_{AMB} = +25° C
Output Leakage Current		±0.05	±10	µA	Receivers disabled
Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
Output Voltage HIGH	V_{CC} - 0.6	V_{CC} - 0.1		V	I_{OUT} = -1.0mA

SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.5V with $T_{AMB} = T_{MIN}$ to T_{MAX}. Typical values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER OUTPUTS					
Output Voltage Swing	±5.0	±5.4		V	All driver outputs loaded with 3KΩ to GND, T_{AMB} = +25° C
Output Resistance	300			Ω	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V
Output Short-Circuit Current		±35 ±70	±60 ±100	mA	V_{OUT} = 0V V_{OUT} = ±15V
Output Leakage Current			±25	µA	V_{CC} = 0V or 3.0V to 5.5V, V_{OUT} = ±12V, Drivers disabled
RECEIVER INPUTS					
Input Voltage Range	-15		15	V	
Input Threshold LOW	0.6	1.2		V	V_{CC} = 3.3V
Input Threshold LOW	0.8	1.5		V	V_{CC} = 5.0V
Input Threshold HIGH		1.5	2.4	V	V_{CC} = 3.3V
Input Threshold HIGH		1.8	2.4	V	V_{CC} = 5.0V
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	kΩ	
Auto-Online **CIRCUITRY CHARACTERISTICS ($\overline{\text{ONLINE}}$ = GND, $\overline{\text{SHUTDOWN}}$ = V_{CC})**					
$\overline{\text{STATUS}}$ Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
$\overline{\text{STATUS}}$ Output Voltage HIGH	V_{CC} - 0.6			V	I_{OUT} = -1.0mA
Receiver Threshold to Drivers Enabled (t_{ONLINE})		200		µS	Figure 15
Receiver Positive or Negative Threshold to $\overline{\text{STATUS}}$ HIGH (t_{STSH})		0.5		µS	Figure 15
Receiver Positive or Negative Threshold to $\overline{\text{STATUS}}$ LOW (t_{STSL})		20		µS	Figure 15

SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.5V with T_{AMB} = T_{MIN} to T_{MAX}. Typical values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TIMING CHARACTERISTICS					
Maximum Data Rate	120	240		kbps	R_L = 3KΩ, C_L = 1000pF, one driver active
Receiver Propagation Delay t_{PHL} t_{PLH}		 0.3 0.3		µs	Receiver input to Receiver output, C_L = 150pF
Receiver Output Enable Time		200		ns	Normal operation
Receiver Output Disable Time		200		ns	Normal operation
Driver Skew		100	500	ns	$\lvert t_{PHL} - t_{PLH} \rvert$, T_{AMB} = 25°C
Receiver Skew		200	1000	ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Transition-Region Slew Rate			30	V/µs	V_{CC}= 3.3V, R_L = 3KΩ, T_{AMB} = 25°C, measurements taken from -3.0V to +3.0V or +3.0V to -3.0V

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 235Kbps data rate, all drivers loaded with 3KΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

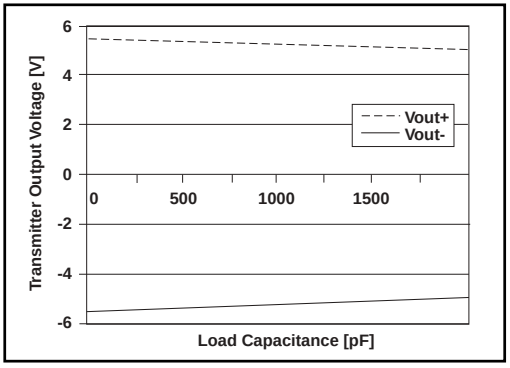


Figure 1. Transmitter Output Voltage VS. Load Capacitance

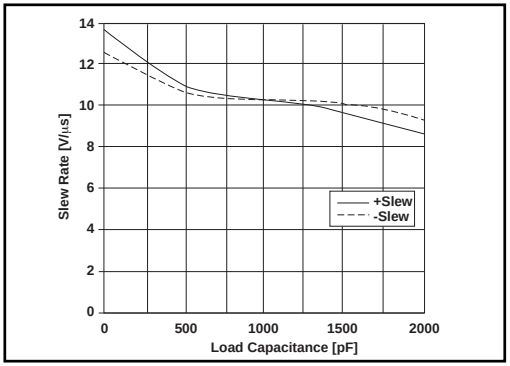


Figure 2. Slew Rate VS. Load Capacitance

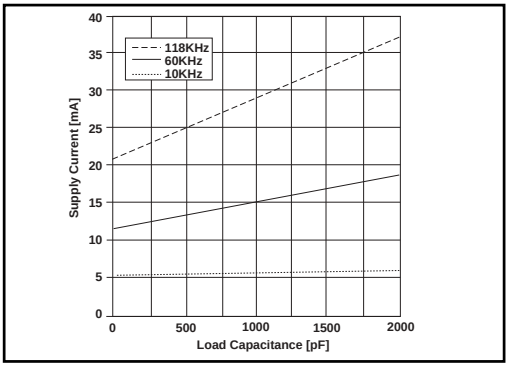


Figure 3. Supply Current VS. Load Capacitance when Transmitting Data

NAME	FUNCTION	PIN NO.
$\overline{EN}$	Receiver Enable. Apply logic HIGH for normal operation. Apply logic LOW to disable the receiver outputs (high-Z state).	1
C1+	Positive terminal of the voltage doubler charge-pump capacitor.	2
V+	Regulated +5.5V output generated by the charge pump.	3
C1-	Negative terminal of the voltage doubler charge-pump capacitor.	4
C2+	Positive terminal of the inverting charge-pump capacitor.	5
C2-	Negative terminal of the inverting charge-pump capacitor.	6
V-	Regulated -5.5V output generated by the charge pump.	7
R_1IN	RS-232 receiver input.	8
R_1OUT	TTL/CMOS receiver output.	9
$\overline{STATUS}$	TTL/CMOS Output indicating ONLINE and SHUTDOWN status.	10
T_1IN	TTL/CMOS driver input.	11
$\overline{ONLINE}$	Apply logic HIGH to override ***Auto-Online*** circuitry keeping drivers active (SHUTDOWN must also be logic HIGH, refer to *Table 2*).	12
T_1OUT	RS-232 driver output.	13
GND	Ground.	14
V_{CC}	+3.0V to +5.5V supply voltage.	15
$\overline{SHUTDOWN}$	Apply logic LOW to shut down drivers and charge pump. This overrides all ***Auto-Online*** circuitry and ONLINE (refer to *Table 2*).	16

Table 1. Device Pin Description

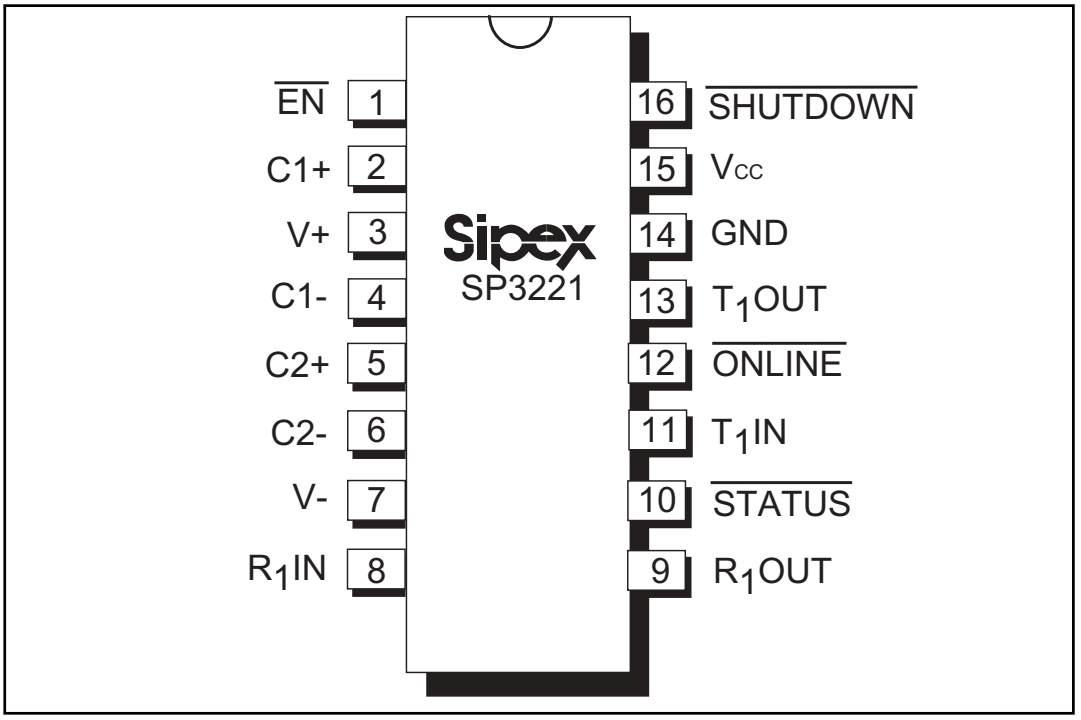


Figure 4. SP32221E Pinout Configuration

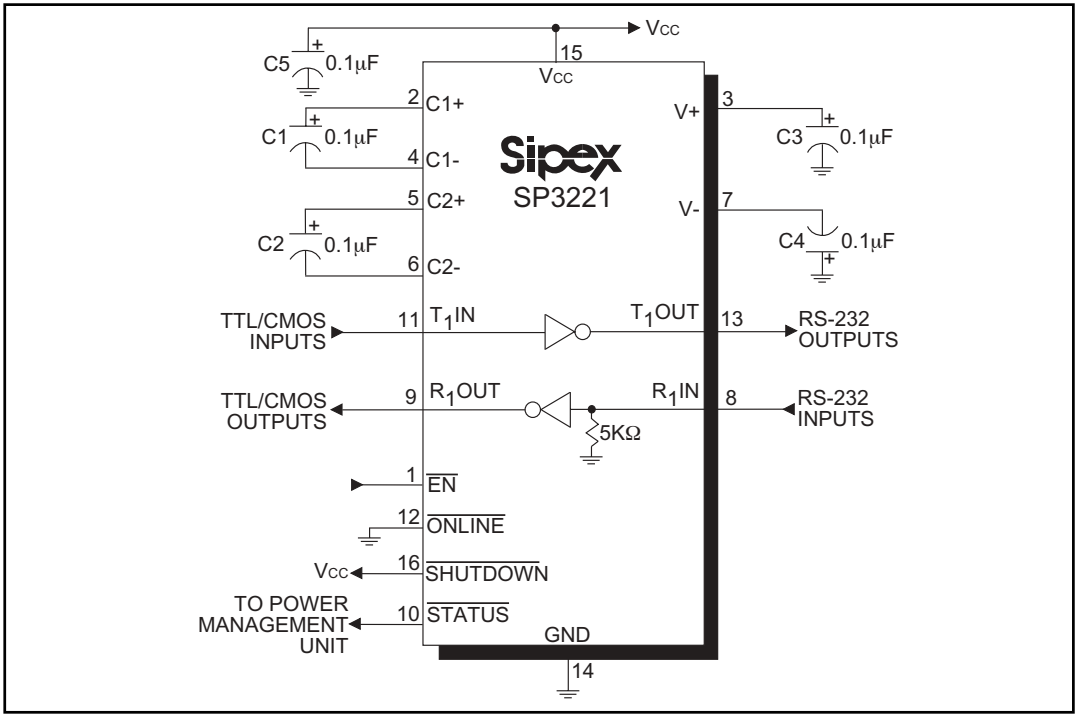


Figure 5. SP3221E Typical Operating Circuit

DESCRIPTION

The **SP3221E** transceiver meets the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or hand held computers. The **SP3221E** device features **Sipex's** proprietary and patented (U.S.-- 5,306,954) on-board charge pump circuitry that generates ±5.5V RS-232 voltage levels from a single +3.0V to +5.5V power supply. The **SP3221E** device can operate at a typical data rate of 240Kbps fully loaded.

The **SP3221E** is a 1-driver/1-receiver device is ideal for portable or hand-held applications and power sensitive designs. The device features ***Auto-Online*** circuitry which reduces the power supply drain to a 1µA supply current. In many portable or hand-held applications, an RS-232 cable can be disconnected when not in use. Under these conditions, the internal charge pump and the driver will be shut down. Otherwise, the device automatically comes online. This feature allows design engineers to address power saving concerns without major design changes.

THEORY OF OPERATION

The **SP3221E** device is made up of four basic circuit blocks: 1. Drivers, 2. Receivers, 3. the Sipex proprietary charge pump, and 4. ***Auto-Online*** circuitry.

Drivers

The driver is inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is ±5.4V with no load and ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. This driver complies with the EIA-TIA-232F and all previous RS-232 versions.

The driver typically can operate at a data rate of 250Kbps. The driver can guarantee a data rate of 250Kbps fully loaded with 3KΩ in parallel with 1000pF, ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver output is internally limited to a maximum of 30V/µs in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

The **SP3221E** driver can maintain high data rates up to 240Kbps fully loaded. *Figure 6* shows a loopback test circuit used to test the RS-232 drivers. *Figure 7* shows the test results of the loopback circuit with the driver active at 250Kbps with typical RS-232 loads in parallel with 1000pF capacitors. *Figure 8* shows the test results where the loaded driver was active at 235Kbps with an RS-232 receiver in parallel with a 1000pF capacitor. A solid RS-232 data transmission rate of 250Kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

DEVICE: SP3221E			
$\overline{SHUTDOWN}$	$\overline{EN}$	T_xOUT	R_xOUT
0	0	High Z	Active
0	1	High Z	High Z
1	0	Active	Active
1	1	Active	High Z

Table 2. $\overline{SHUTDOWN}$ and $\overline{EN}$ Truth Tables
Note: In Auto-Online Mode where $\overline{ONLINE}$ = GND and $\overline{SHUTDOWN}$ = V_{CC}, the device will shut down if there is no activity present at the Receiver inputs.

Receivers

The receiver converts ±5.0V EIA/TIA-232 levels to TTL or CMOS logic output levels. The receiver has an inverting output that can be disabled by using the $\overline{EN}$ pin.

The receiver is active when the ***Auto-Online*** circuitry is enabled or when in shutdown. During the shutdown, the receiver will continue to be active.

Driving $\overline{EN}$ to a logic HIGH forces the output of the receiver into high-impedance.

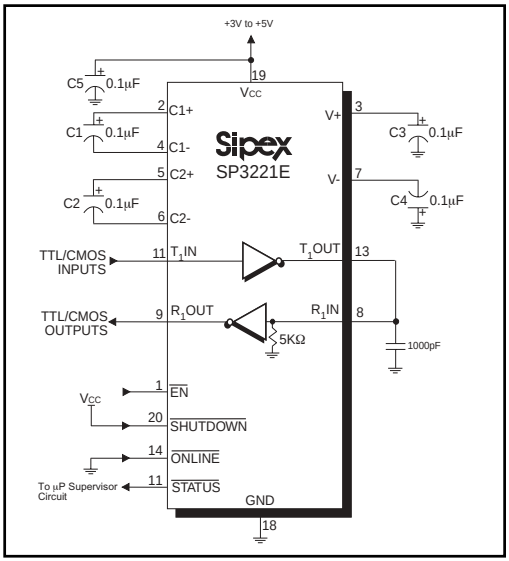


Figure 6. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5KΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

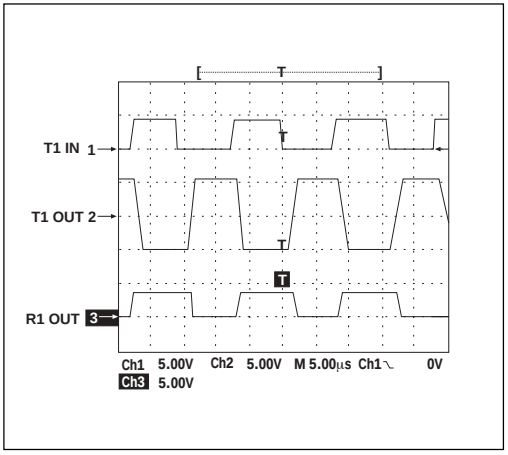


Figure 7. Loopback Test Circuit Result at 250Kbps (Driver Fully Loaded)

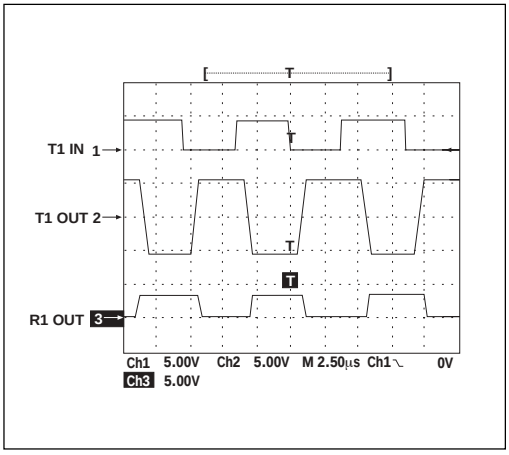


Figure 8. Loopback Test Circuit result at 235Kbps (Driver Fully Loaded)

Charge Pump

The charge pump is a **Sipex**–patented design (U.S. 5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC}. C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now 2 times V_{CC}.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at V_{CC}, the voltage potential across C_2 is 2 times V_{CC}.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC}, in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 250kHz. The external capacitors can be as low as 0.1µF with a 16V breakdown voltage rating.

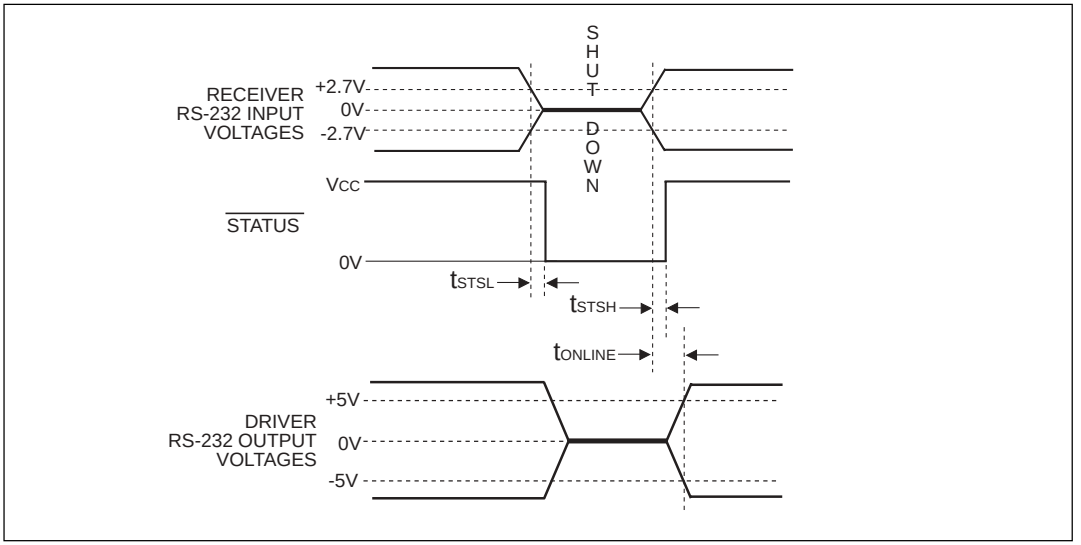


Figure 9. Auto-Online Timing Waveforms

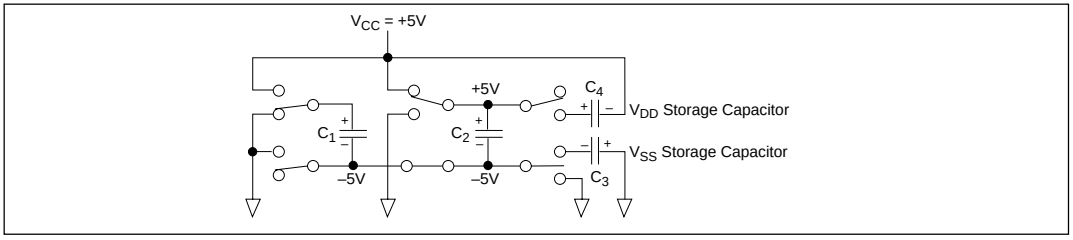


Figure 10. Charge Pump — Phase 1

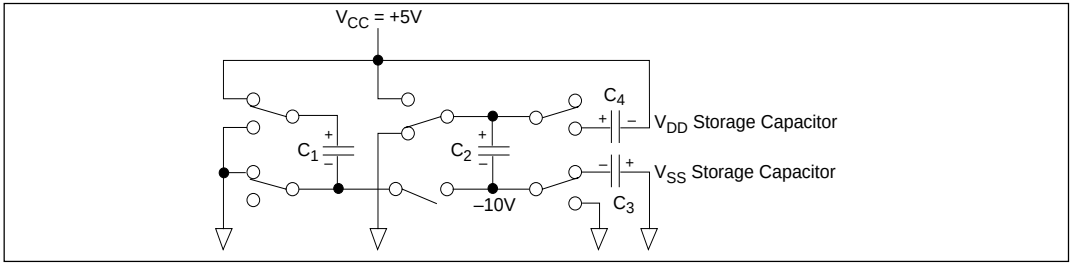


Figure 11. Charge Pump — Phase 2

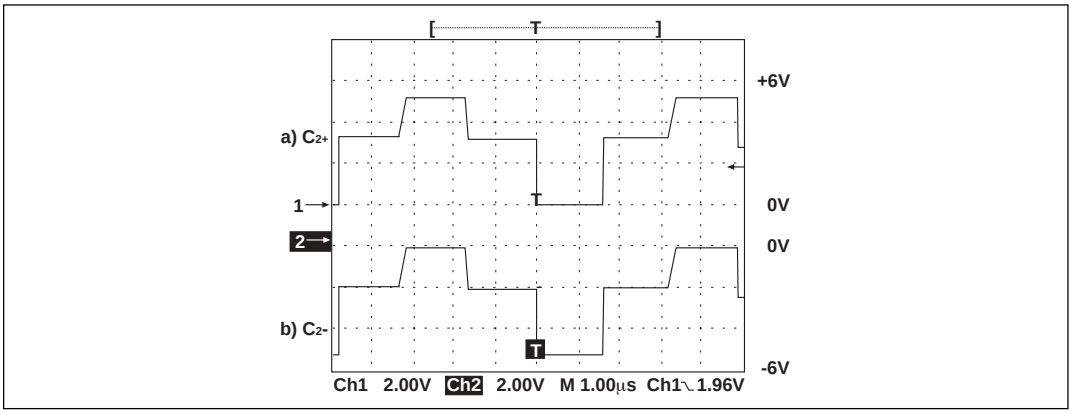


Figure 12. Charge Pump Waveforms

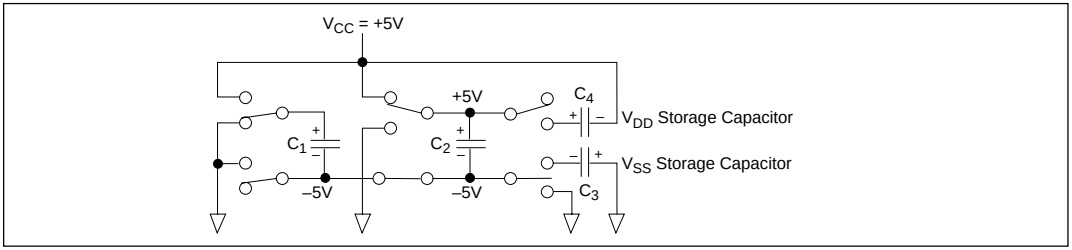


Figure 13. Charge Pump — Phase 3

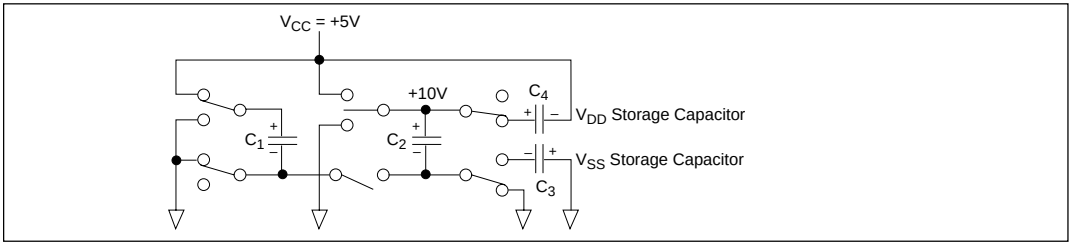


Figure 14. Charge Pump — Phase 4

RS-232 Cable Connected?	$\overline{\text{SHUTDOWN}}$ INPUT	$\overline{\text{ONLINE}}$ INPUT	$\overline{\text{STATUS}}$ OUTPUT	TRANSCEIVER STATUS	TxOUT
YES	HIGH	-	HIGH	Normal Operation	Active
NO	HIGH	HIGH	LOW	Normal Operation	Active
NO	HIGH	LOW	LOW	Shutdown (***Auto-Online***)	HiZ
YES	LOW	-	HIGH	Shutdown	HiZ
NO	LOW	-	LOW	Shutdown	HiZ

Table 3. Auto-Online Logic NOTE: For proper $\overline{\text{ONLINE}}$ function the SP3221E and cable must be connected to another RS232 Transceiver (3kΩ to 7kΩ load).

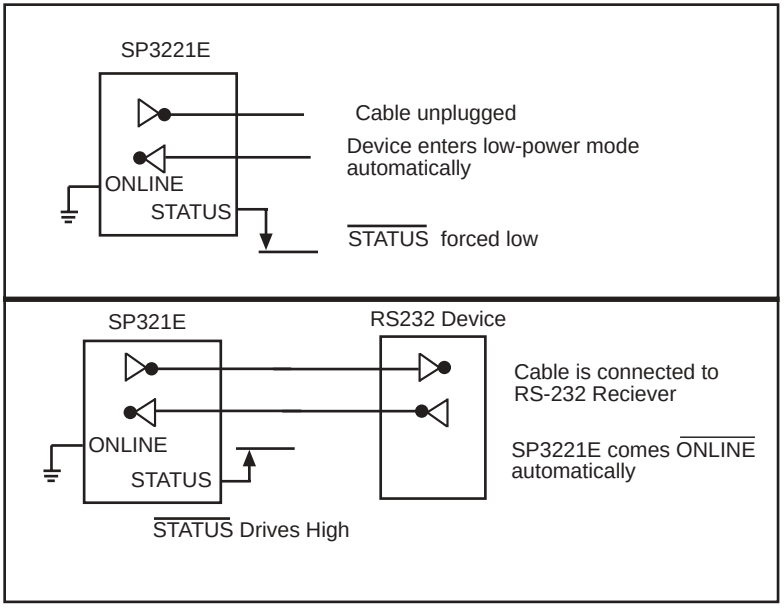


Figure 15. SP3221E AutoOnline Operation

Auto-Online Circuitry

The **SP3221E** device has an ***Auto-Online*** circuitry on board that saves power in the system the device is designed into without changes to the existing BIOS or operating system.

The **SP3221E** device incorporates an ***Auto-Online*** circuit that automatically enables itself when the cable is connected to another RS232 device. Conversely, the ***Auto-Online*** circuit also disables most of the internal circuitry when the cable is disconnected and goes into a standby mode where the device typically draws 1µA. This function is controlled by the $\overline{\text{ONLINE}}$ pin. When this pin is tied to a logic LOW, the ***Auto-Online*** function is active. When the cable is disconnected, the receiver inputs will be pulled down by its internal 5kΩ resistors to ground. When $\overline{\text{ONLINE}}$ is HIGH, the ***Auto-Online*** mode is disabled.

When the **SP3221E** driver or internal charge pump are disabled, the supply current is reduced to 1µA.

The ***Auto-Online*** mode can be overridden by the $\overline{\text{SHUTDOWN}}$ pin. If this pin is a logic LOW, the ***Auto-Online*** function will not operate regardless of the logic state of the $\overline{\text{ONLINE}}$ pin. *Table 3* summarizes the logic of the ***Auto-Online*** operating modes. The truth table logic of the driver and receiver outputs can be found in *Table 2*.

The $\overline{\text{STATUS}}$ pin outputs a logic LOW signal if the device is shutdown. This pin goes to a logic HIGH when the external cable is connected to another RS232 device.

When the **SP3221E** device is shutdown, the charge pump is turned off. V+ charge pump output decays to V_{CC}, the V- output decays to GND. The decay time will depend on the size of capacitors used for the charge pump. Once in shutdown, the time required to exit the shut down state and have valid V+ and V- levels is typically 200µs.

Tying $\overline{\text{ONLINE}}$ and $\overline{\text{SHUTDOWN}}$ together will bypass the ***Auto-Online*** circuitry so this connection acts like a shutdown input pin.

ESD TOLERANCE

The **SP3221E** device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electrostatic discharges and associated transients. The improved ESD tolerance is at least ±15kV without damage nor latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) IEC1000-4-2 Air-Discharge
c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electrostatic energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 17*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown on *Figure 18*. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

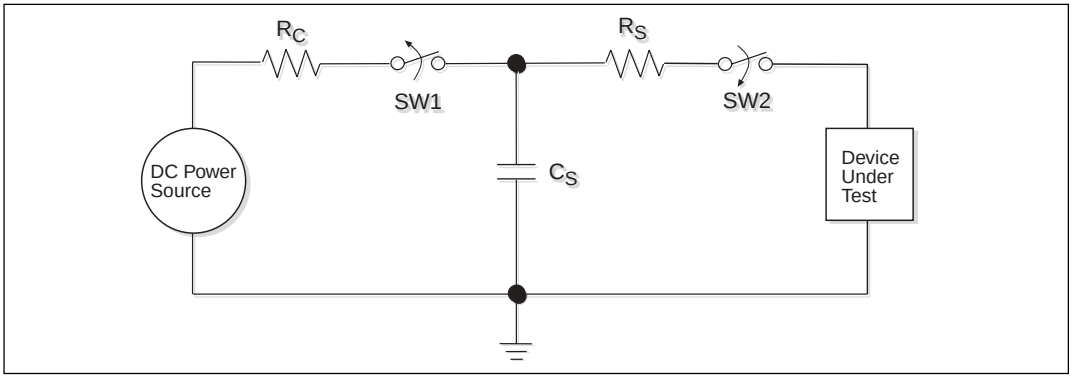


Figure 17. ESD Test Circuit for Human Body Model

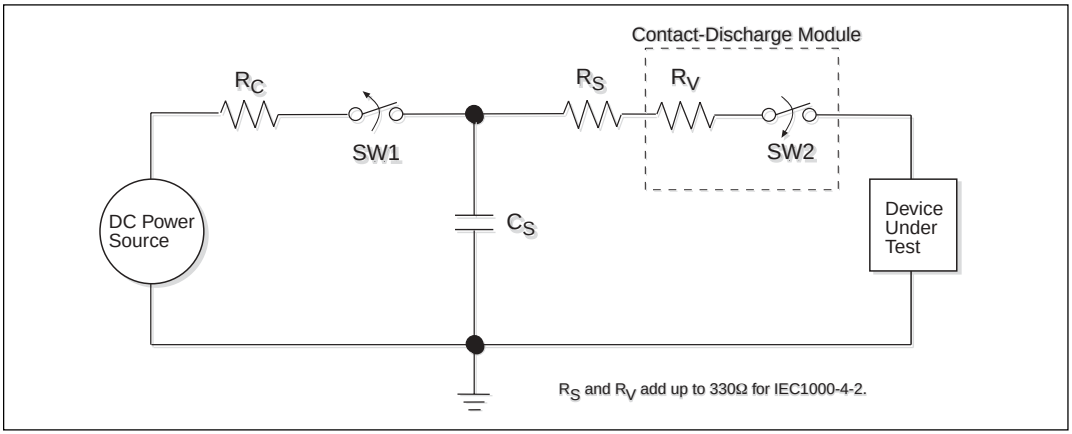


Figure 18. ESD Test Circuit for IEC1000-4-2

The circuit model in *Figures 17* and *18* represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ an 100pF, respectively. For IEC-1000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω an 150pF, respectively.

The higher C_S value and lower R_S value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

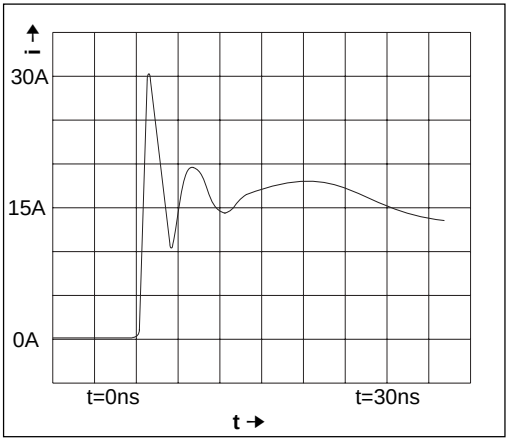
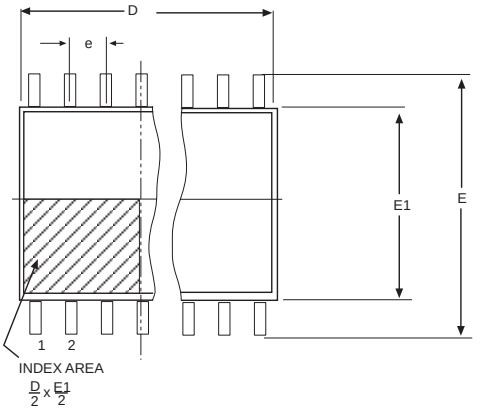


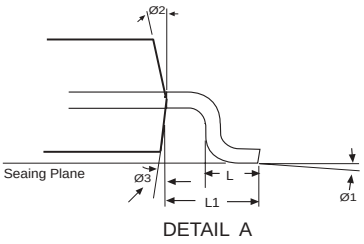
Figure 19. ESD Test Waveform for IEC1000-4-2

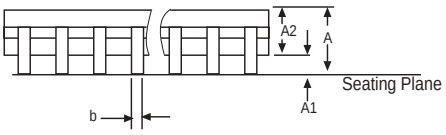
DEVICE PIN TESTED	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

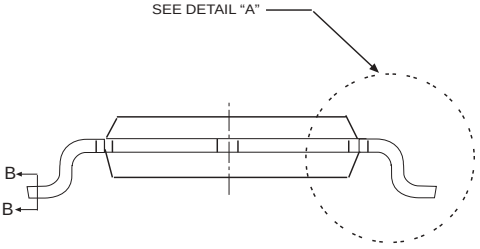
Table 4. Transceiver ESD Tolerance Levels

PACKAGE: 16 PIN TSSOP

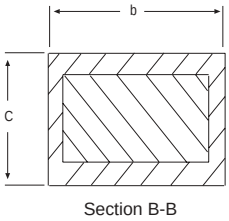








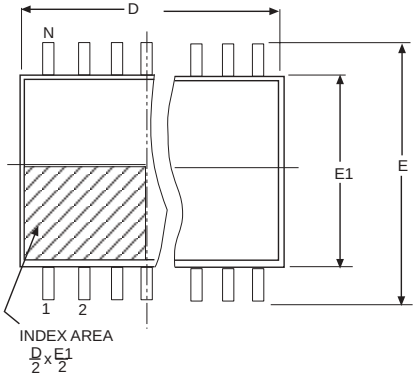
16 PIN TSSOP JEDEC MO-153 (AB) Variation	Dimensions in (mm)		
	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	5.00	5.10
E	6.40 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
Ø1	0º	4º	8º
Ø2	12º REF		
Ø3	12º REF		
L	0.45	0.60	0.75
L1	1.00 REF		

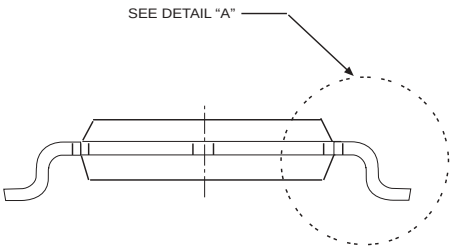


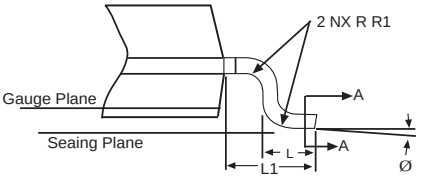
Section B-B

16 PIN TSSOP

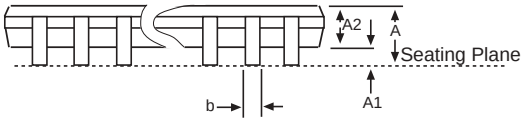
PACKAGE: 16 PIN SSOP

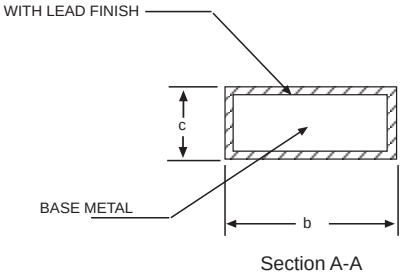






DETAIL A





Section A-A

16 PIN SSOP JEDEC MO-150 (AC) Variation	Dimensions in (mm)		
	MIN	NOM	MAX
A	-	-	2.0
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	5.90	6.20	6.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
L	0.55	0.75	0.95
L1	1.25 REF		
Ø	0º	4º	8º

16 PIN SSOP

ORDERING INFORMATION

Part Number	Operating Temperature Range	Package Type
SP3221ECY	0°C to +70°C	16-pin TSSOP
SP3221ECY/TR	0°C to +70°C	16-pin TSSOP
SP3221ECA	0°C to +70°C	16-pin SSOP
SP3221ECA/TR	0°C to +70°C	16-pin SSOP
SP3221EEY	-40°C to +85°C	16-pin TSSOP
SP3221EEY/TR	-40°C to +85°C	16-pin TSSOP
SP3221EEA	-40°C to +85°C	16-pin SSOP
SP3221EEA/TR	-40°C to +85°C	16-pin SSOP

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP3221ECA/TR = standard; SP3221ECA-L/TR = lead free

/TR = Tape and Reel

Pack quantity is 1,500 for TSSOP and 2,500 for SSOP.

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