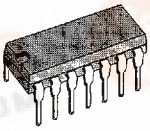
SGS-THOMSON MICROELECTRONICS

EFG7189
EFG71891

DTMF GENERATOR FOR BINARY CODED HEXADECIMAL DATA

- GENERATES 16 STANDARD DTMF TONE PAIRS
- USES LOW COST 3.579 MHz CRYSTAL
- DIRECT MICROPROCESSOR INTERFACE
- ACCEPTS 4 BIT DATA IN SERIAL OR PARALLEL FORMAT
- DATA IS STORED DURING TRANSMISSION PERIOD
- LOW HARMONIC DISTORTION
- HIGH GROUP PRE EMPHASIS
- LOW POWER CONSUMPTION IN STANDBY MODE
- PULL-UP TO V^+ ON ALL LOGIC INPUTS

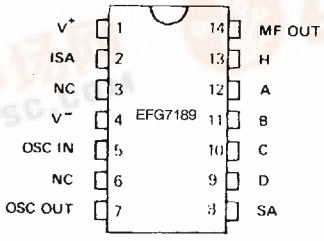
Minidip



DIP14

ORDERING NUMBERS : EFG71891PD (Minidip)
EFG7189PD (DIP14)

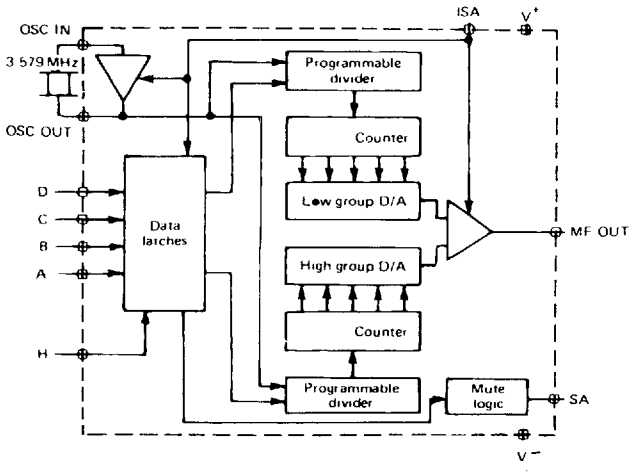
PIN CONNECTIONS (Top view)



DESCRIPTION

This CMOS circuit is designed specifically to provide, with a minimum number of external components, a low cost DTMF dialer for microprocessor controlled telephone sets operating in accordance with existing standards. The 4 bits identifying the frequency pair to be generated may be supplied via either 5 connections between the EFG7189 and the microprocessor in parallel format or in serial format through 3 connections linking the EFG7189 to the microprocessor. This feature eliminates the necessity to simulate keyboard type inputs normally required by standard DTMF generators. Input data is stored on trailing edge of ISA signal. The tone pair selected by this code is generated while ISA remains low. With ISA high, the oscillator is inhibited and the device is in standby mode. SA pin is connected to V^- while device is outputting any tone pair.

BLOCK DIAGRAM



PIN DESCRIPTION

N°	Name	Function	Description
1 4	V^+ V^-	Supply Voltage Supply Voltage	Positive Supply 0V
11 10 9	B C D	Logic Input Logic Input Logic Input	Parallel input for hexadecimal code allowing the selection of 2 frequencies constituting the DTMF signal (see attached table).
12	A	Logic Input	Serial or Parallel Input for Hexadecimal Code
13	H	Serial Input Clock	Clock Input for Hexadecimal Code Serial Input Register on Pin A Furthermore, it allows for the selection of the serial or parallel operating mode of this code. When ISA input goes low, the validated code is : • the parallel input code if input H is high. • the serial input code if input H is low.
2	ISA	Logic Input	This pin allows for the inhibition of the analog output MF OUT : • when ISA is high, output MF OUT is idle and connected to V^-. • when ISA is low, the hexadecimal code is validated and MF OUT output is activated.
8	SA	Logic Output	This pin indicates the state of the analog output : • if ISA is low, SA is a low impedance output at V^-. • if ISA is high, SA is a high impedance output.
14	MF OUT	Analog Output	This pin is the DTMF signal output.
5	OSC IN	Oscillator Input	This pin corresponds to the input of the inverter of the oscillator. The nominal frequency of the oscillator is 3.579 MHz.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V^+	Supply Voltage	– 0.3 to + 5.5	V
V_{in}	Digital Input Range	– 0.3 to V^+ + 0.3	V
T_{stg}	Storage Temperature Range	– 55 to + 125	°C

ELECTRICAL OPERATING CHARACTERISTICS

All voltages referenced to V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V^+	Positive Supply Voltage	3	–	5.25	V
T_{oper}	Operating Temperature Range	– 25	–	70	°C
f_c	Crystal Frequency	–	3.579545	–	MHz

DC ELECTRICAL CHARACTERISTICS

T_{amb} = – 25 °C to 70 °C, V^+ = – 3 to 5.25 V, f_c = 3.579 MHz (all voltages are referenced to V^-)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{DD}	Operating Current in Transmission Mode (V^+ = 4 V, output not loaded)	–	0.6	1	mA
ISB	Standby Current (ISA, H, A, B, C, D open circuit or connected to V^+)	–	–	10	µA
V_{IL}	Input Low Voltage (ISA, H, A, B, C, D)	0	–	0.3 V^+	V
V_{IH}	Input High Voltage (ISA, H, A, B, C, D)	0.7 V^+	–	V^+	V
R_T	Pull up Resistor on Logic Inputs ISA, H, A, B, C, D	100	–	–	kΩ
I_{OLSA}	SA Output Current (V_{OLSA} = 0.5 V)	500	–	–	µA
I_{FSA}	SA Leakage Current, Open Current (V_{OHSA} = 5 V)	–	–	2	µA

A.C. ELECTRICAL CHARACTERISTICS

T_{amb} = – 25 °C to 70 °C, V^+ – 3 V to 5.25 V, f_c = 3.579 MHz

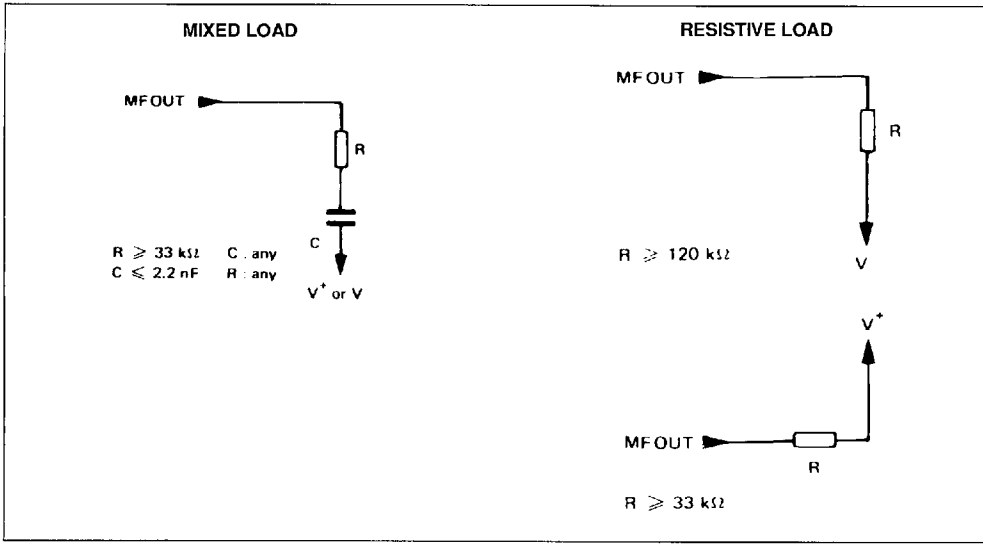
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_r t_f	Rise/Fall Time on Input Signals	–	–	50	ns
$TISA_{ON}$	Transmission Delay	–	–	5	ms
$TISA_{OFF}$	Blocking Delay	–	–	5	ms
T_H	Clock Period	10	–	–	µs
T_{HH}	High Level Clock Width	5	–	–	µs
T_{HL}	Low Level Clock Width	5	–	–	µs
T_{PH}	Set-up Time of A Related to Clock	1	–	–	µs
T_{MH}	Hold Time of A Related to Clock	7	–	–	µs
T_{PISA}	Set-up Time of the Code or Clock Related to ISA	1	–	–	µs
T_{MISA}	Hold Time of Code Related to ISA	2	–	–	µs

TRANSMISSION CHARACTERISTICS T_{amb} = – 25 °C to 70 °C, V^+ 3 V to 5.25 V, f_c = 3.579

Symbol	Parameter	Min.	Typ.	Max.	Unit
DFH DFB	High and Low Frequency Precision	–	–	1	%
AFB	Low Frequency Transmission Level (V^+ = 4 V) - Note 1	– 8	– 7	– 6	dBm
GBH	High Band Pre-emphasis	2.3	2.7	3.5	dB
D	Output Distortion	–	–	– 20	dB

Note : 1. 0 dBm = 0.775 V_{rms}
These specifications are related to the following loads.

Figure 1.



FUNCTIONAL DESCRIPTION

With ISA input at logic level "1", the device is in low power mode. The oscillator is inhibited and analog output MF OUT is at ground level. DTMF input data is detected on trailing edge of ISA. This transition enables both the oscillator and the analog output then the data is stored and corresponding DTMF pair is generated during the low state interval of the ISA signal. Any modification to H, A, B, C and D signals during this period will not have any further effect on DTMF pair generated.

The device accepts input data in two different formats :

- Parallel format : this requires 4 connections (A, B, C, D) between the microprocessor and the circuit.
- Serial format : in this case data is supplied to the circuit by the microprocessor via 2 connections A and H (see typical application diagram).

Pre-emphasis is applied to high group tone and both tones of DTMF pair are supplied through analog output pin.

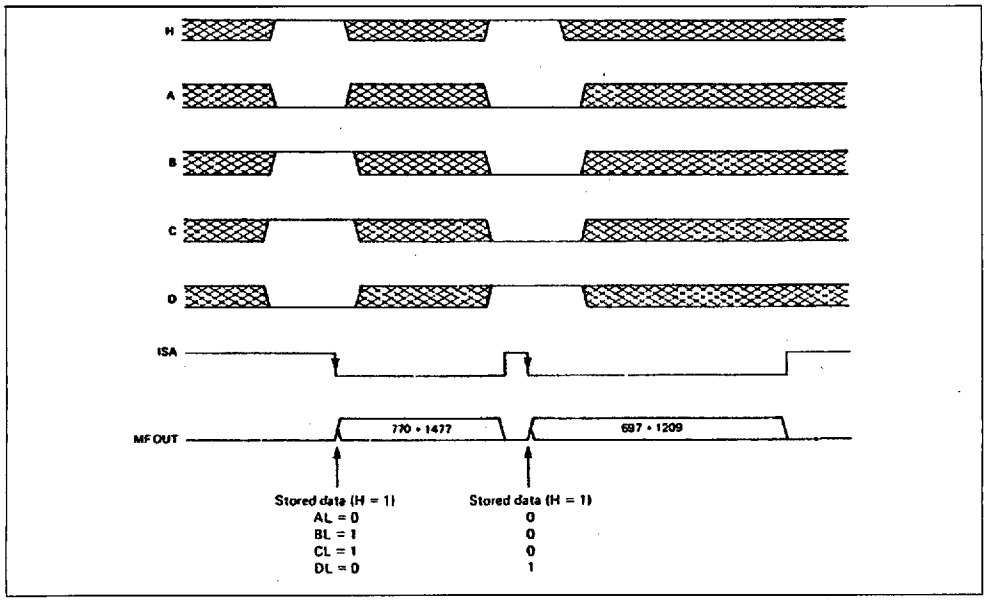
DATA ACQUISITION LOGIC

This section includes : A 4-bit shift register, an 8-line to 4-line multiplexer and a 4-bit storage register.

- The 4-bit shift register has its input connected to pin A and is enabled by the signal applied to pin H. Its outputs are AS, BS, CS and DS signals.
- The multiplexer is enabled by signal H and operates according to the following law : AI = H.AP + $\overline{H}$.AS.
- The 4-bit storage register operates on trailing edge of ISA signal. AI, BI, CI, DI and AL, BL, CL, DL are its inputs and outputs respectively.

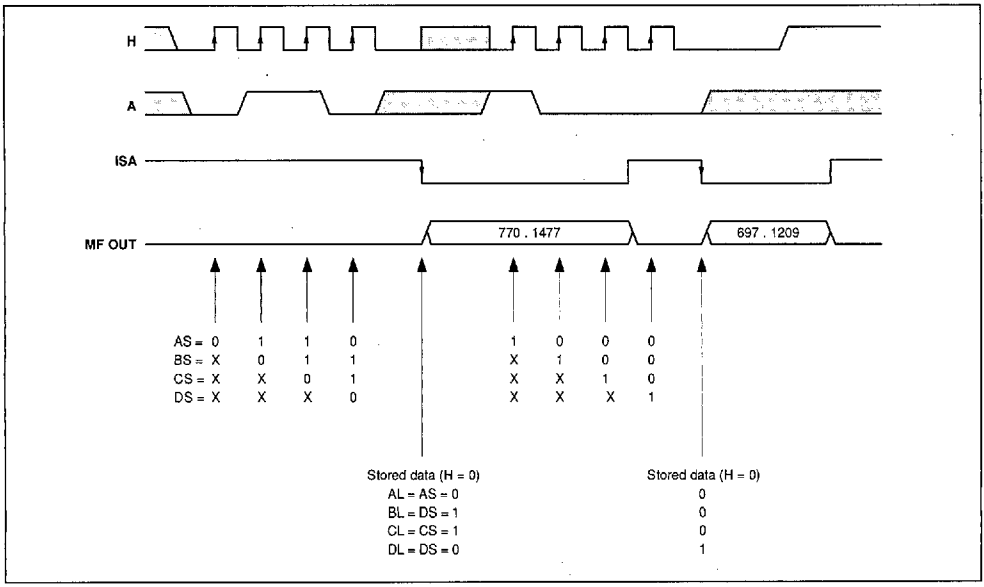
During the low state period of ISA input, AL, BL, CL and DL signals determine the DTMF pair to be generated.

Figure 2 : Example of Parallel Operating Mode.



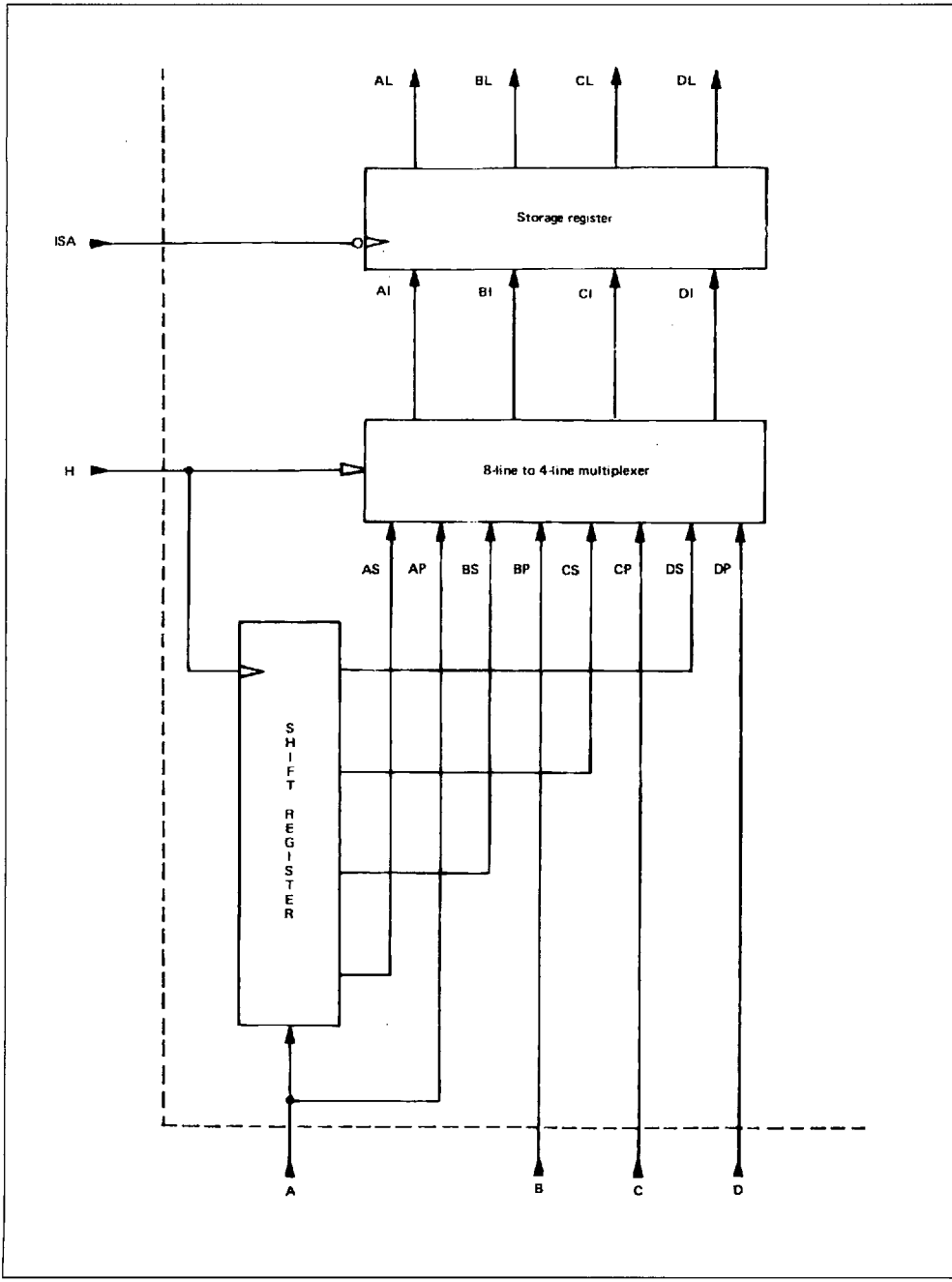
Note : If the circuit operates permanently in parallel mode, then the H input may be left floating (internally pulled-up to V+) or tied to logic 1. With ISA at logic 0, H,A,B,C, and D inputs cannot modify the generated DTMF pair.

Figure 3 : Example of Serial-Operating Mode.



Notes : 1. With ISA at logic 0, H, A, B, C and D signals cannot modify the generated DTMF pair. As a result, in serial operating mode, it is possible to enter AS, BS, CS and DS data while another DTMF pair is being generated.
2. First data to be entered is DS.

Figure 4 : Data Acquisition Logic.



TIMING DIAGRAM

Figure 5 : Rise/Fall Time on Input Signals.

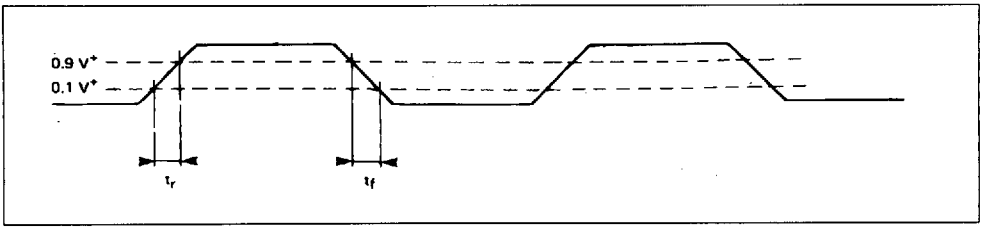


Figure 6 : Parallel Operating Mode (H = "1").

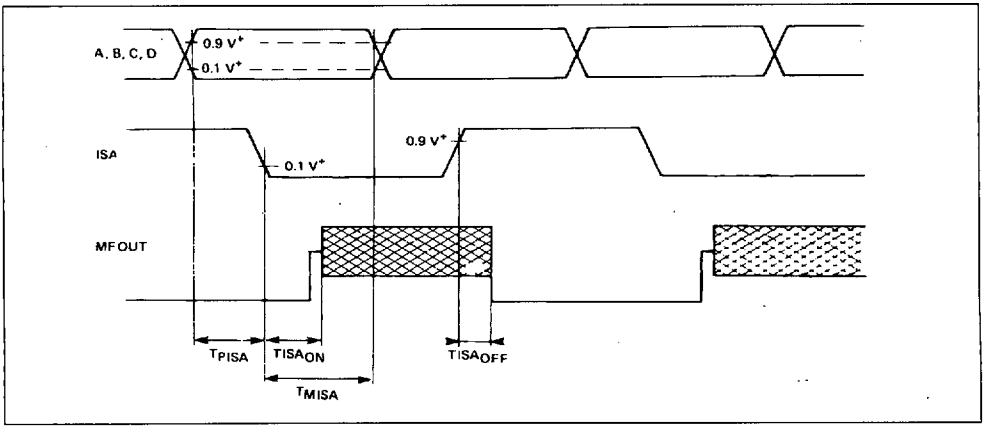


Figure 7 : Serial Operating Mode.

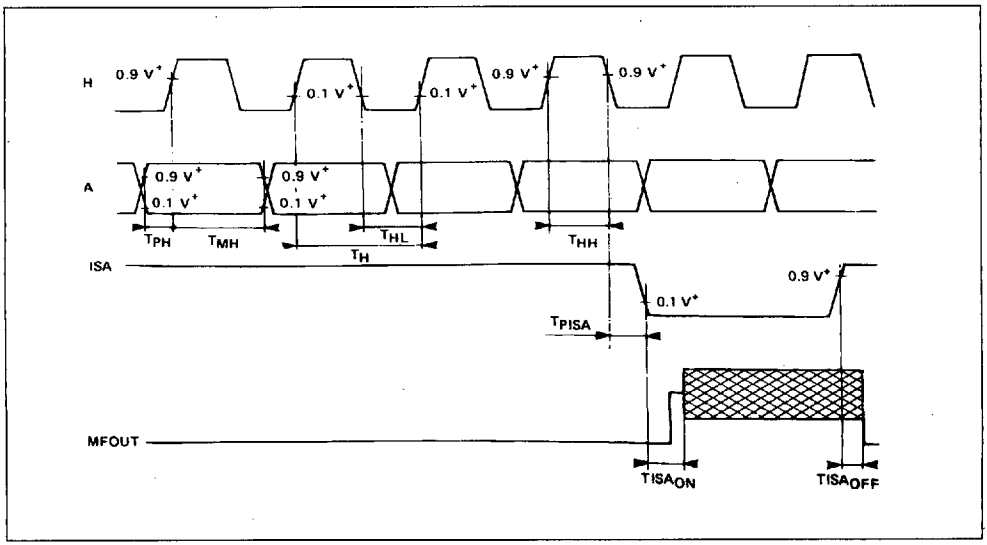


Table 1

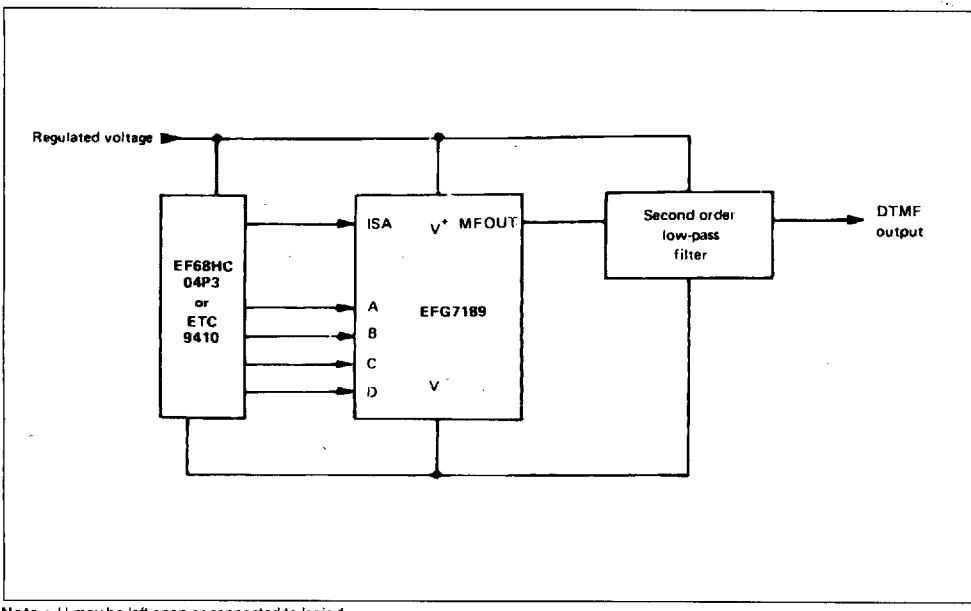
	DTMF Specification (Hz)	Frequencies Derived from a 3.579 MHz Quartz (Hz)	Division Rank	% Deviation from Standard
f1	697	701.3	5104	0.62
f2	770	771.4	4640	0.19
f3	852	857.2	4176	0.61
f4	941	935.1	3828	– 0.63
f5	1209	1215.9	2944	0.57
f6	1336	1331.7	2688	– 0.32
f7	1477	1471.9	2432	– 0.35
f8	1633	1645	2176	0.74

Table 2

Keyboard Code	Hexadecimal Code				ISA	Generated Frequencies	
	A	B	C	D		f(Hz)	f(Hz)
X	X	X	X	X	1		
1	0	0	0	1	↓	697	1209
2	0	0	1	0	↓	697	1336
3	0	0	1	1	↓	697	1477
4	0	1	0	0	↓	770	1209
5	0	1	0	1	↓	770	1336
6	0	1	1	0	↓	770	1477
7	0	1	1	1	↓	852	1209
8	1	0	0	0	↓	852	1336
9	1	0	0	1	↓	852	1477
0	1	0	1	0	↓	941	1336
•	1	0	1	1	↓	941	1209
≠	1	1	0	0	↓	941	1477
A	1	1	0	1	↓	697	1633
B	1	1	1	0	↓	770	1633
C	1	1	1	1	↓	852	1633
D	0	0	0	0	↓	941	1633

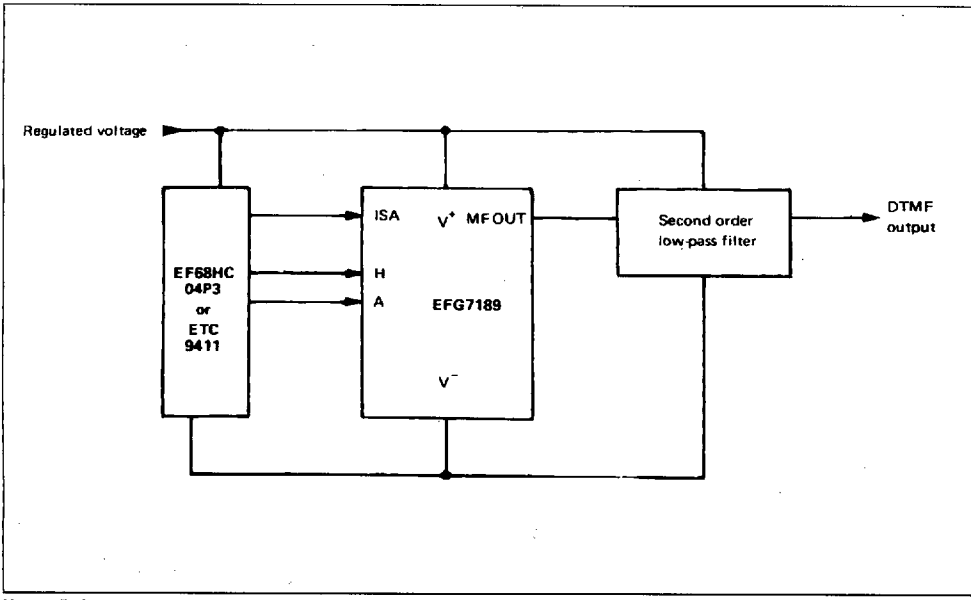
TYPICAL APPLICATION (european standards)

Figure 8 : Parallel Connection.



Note : H may be left open or connected to logic 1.

Figure 9 : Serial Connection.



Note : B, C and D may be left floating or connected to logic 1.

SECOND ORDER LOW-PASS FILTERS

Figure 10 : With Transistor (gain = 1).

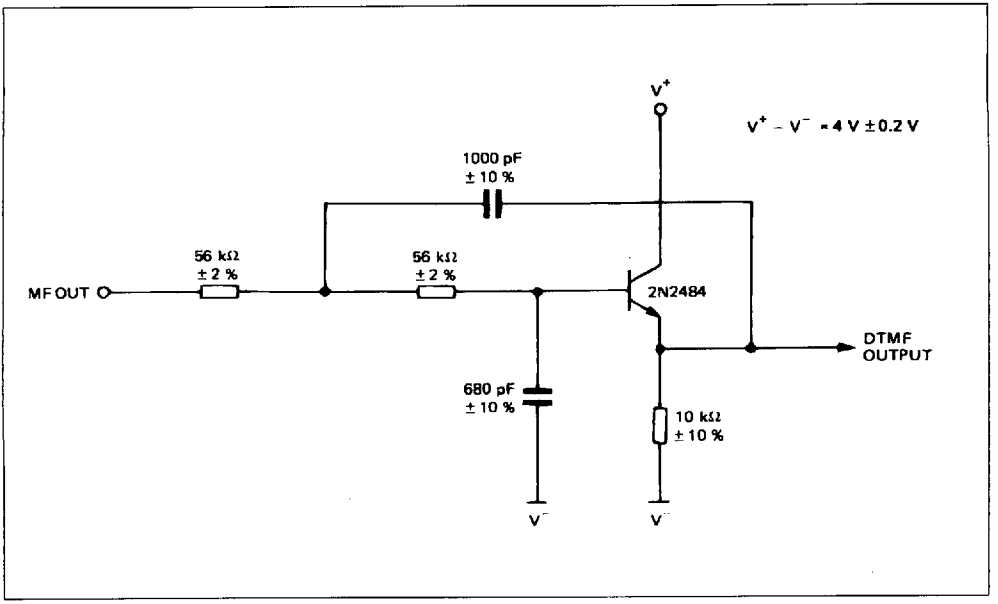


Figure 11 : With Op. Amp. (gain = 1).