

**SN55500E, SN65500E, SN75500E  
AC PLASMA DISPLAY DRIVERS**

SLDS013B - D2471, DECEMBER 1985 - REVISED MAY 1993

- Controls 32 Electrodes
- 100-V Totem-Pole Outputs
- Low Standby Power Consumption
- All Outputs Contain Sink and Source Clamp Diodes
- 15-mA Steady-State Output Current
- Rugged DMOS Outputs
- CMOS Inputs
- Direct Replacement for SN55500D and SN75500A

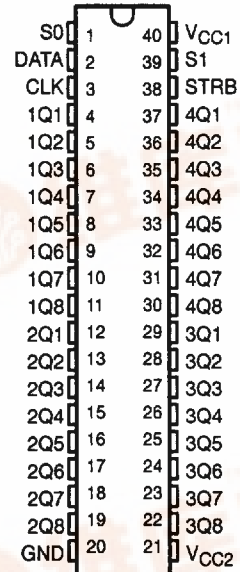
**description**

The SN55500E, SN65500E, and SN75500E are monolithic BIFET<sup>†</sup> integrated circuits designed to perform the line-select operation of a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

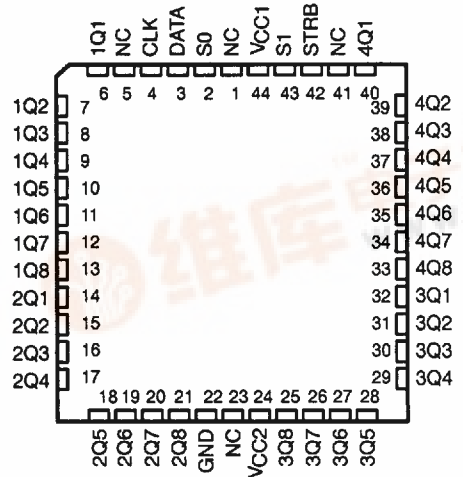
The outputs of these drivers are normally low and can be selectively switched high when the strobe input is low. Selection of the outputs is achieved through the data S0 and S1 inputs. The 8-bit data stored internally in the serial register is inverted and sent to one of four output sections by the 2-line to 4-line decoder. All other outputs remain low. Internal circuits provide a high-current pulse to the level-shifting circuit during positive output transitions. When the output transition is complete, the low steady-state current reduces the circuit's standby power consumption. All outputs contain clamp diodes to the V<sub>CC2</sub> and GND supply inputs.

The SN55500E is characterized for operation over the full military temperature range of -55°C to 125°C. The SN65500E is characterized for operation from -40°C to 85°C. The SN75500E is characterized for operation from 0°C to 70°C.

**SN55500E . . . J PACKAGE  
SN65500E, SN75500E . . . N PACKAGE  
(TOP VIEW)**



**SN55500E . . . FD OR FJ PACKAGE  
SN65500E, SN75500E . . . FN PACKAGE  
(TOP VIEW)**



NC - No internal connection



找BIFET - Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

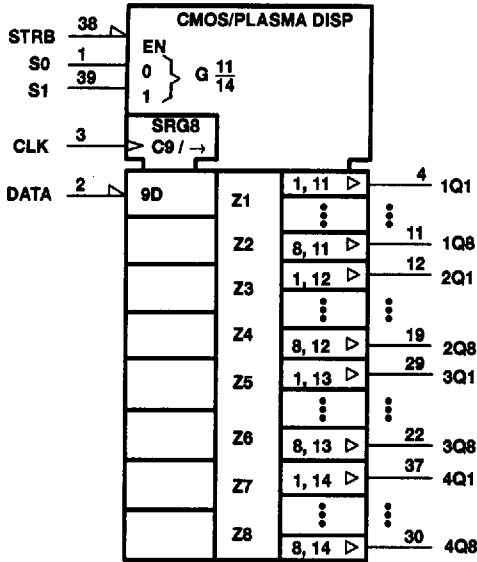
PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



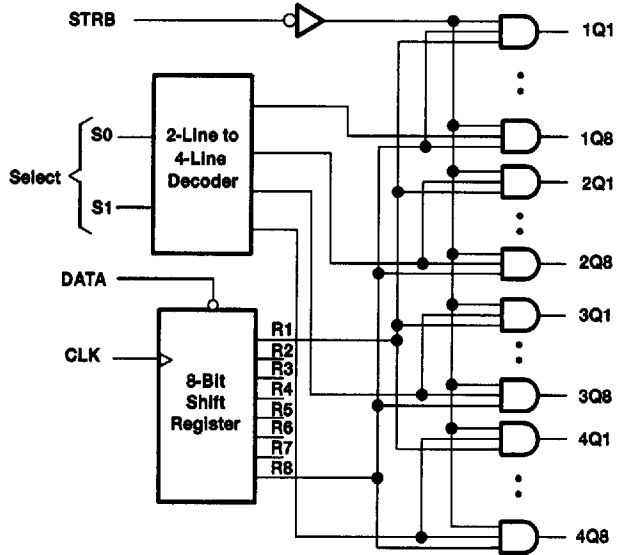
# SN5550E, SN6550E, SN7550E AC PLASMA DISPLAY DRIVERS

SLDS013B - D2471, DECEMBER 1985 - REVISED MAY 1993

## logic symbol†



## functional block diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the J and N packages.

FUNCTION TABLE

FUNCTION	INPUTS				OUTPUTS							
	DATA	CLK	SELECT S1 S0		STRB	SHIFT REGISTER R1 R2 R3 ... R8				1Q1 ... 1Q8	2Q1 ... 2Q8	3Q1 ... 3Q8
Load	H	↑	X	X	H	L	R <sub>1n</sub>	R <sub>2n</sub> ... R <sub>7n</sub>	L ... L	L ... L	L ... L	L ... L
	L	↑	X	X	H	H	R <sub>1n</sub>	R <sub>2n</sub> ... R <sub>7n</sub>	L ... L	L ... L	L ... L	L ... L
Strobe	X	X	X	X	H	R <sub>1n</sub>	R <sub>2n</sub>	R <sub>3n</sub> ... R <sub>8n</sub>	L ... L	L ... L	L ... L	L ... L
	X	H	L	L	L	R <sub>1n</sub>	R <sub>2n</sub>	R <sub>3n</sub> ... R <sub>8n</sub>	R <sub>1</sub> ... R <sub>8</sub>	L ... L	L ... L	L ... L
	X	H	H	L	L	R <sub>1n</sub>	R <sub>2n</sub>	R <sub>3n</sub> ... R <sub>8n</sub>	L ... L	R <sub>1</sub> ... R <sub>8</sub>	L ... L	L ... L
	X	H	H	H	L	R <sub>1n</sub>	R <sub>2n</sub>	R <sub>3n</sub> ... R <sub>8n</sub>	L ... L	L ... L	L ... L	R <sub>1</sub> ... R <sub>8</sub>

H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.

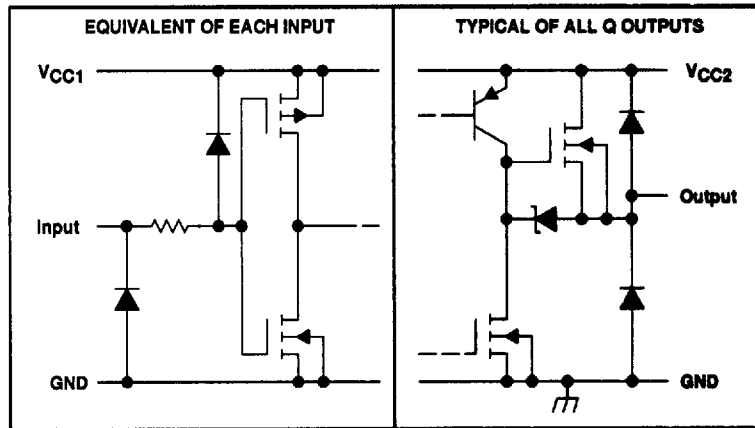
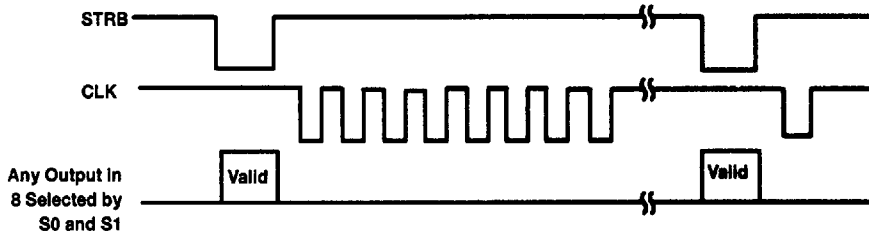
R<sub>1</sub> ... R<sub>8</sub> = levels currently at internal outputs of shift registers one through eight, respectively.

R<sub>1n</sub> ... R<sub>8n</sub> = levels at shift-register outputs R<sub>1</sub> through R<sub>8</sub>, respectively, before the most recent ↑ transition of the clock.

# SN55500E, SN65500E, SN75500E AC PLASMA DISPLAY DRIVERS

SLDS013B - D2471, DECEMBER 1985 - REVISED MAY 1993

## typical operating sequence



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC1}$ (see Note 1):	SN55500E .....	13.8 V
	SN65500E, SN75500E .....	15 V
Supply voltage, $V_{CC2}$ .....		100 V
Input voltage .....		$V_{CC1} + 0.3$ V
Continuous total power dissipation .....		See Dissipation Rating Table
Operating free-air temperature range:	SN55500E .....	-55°C to 125°C
	SN65500E .....	-40°C to 85°C
	SN75500E .....	0°C to 70°C
Storage temperature range .....		-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package .....		300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package .....		260°C
Case temperature for 60 seconds: FD or FJ package .....		260°C
Case temperature for 10 seconds: FN package .....		260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FD or FJ	1825 mW	14.6 mW/°C	1168 mW	949 mW	365 mW
FN	1775 mW	14.2 mW/°C	1136 mW	923 mW	—
J	3050 mW	24.4 mW/°C	1952 mW	1586 mW	610 mW
N	1275 mW	10.2 mW/°C	816 mW	663 mW	—

# SN55500E, SN65500E, SN75500E AC PLASMA DISPLAY DRIVERS

SLDS013B - D2471, DECEMBER 1985 - REVISED MAY 1993

## recommended operating conditions

	SN55500E			SN65500E			SN75500E			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, $V_{CC1}$	10.8	12	13.2	10.8	12	13.2	10.8	12	13.2	V	
Supply voltage, $V_{CC2}$	0		100	0		100	0		100	V	
High-level input voltage as a percentage of $V_{CC1}$ , $V_{IH}$	75%			75%			75%				
Low-level input voltage as a percentage of $V_{CC1}$ , $V_{IL}$				25%			25%				
High-level output clamp current				20			20			mA	
Low-level output clamp current				-20			-20			mA	
Clock frequency, $f_{clock}$ (see Figure 2)	0		8	0		8	0		8	MHz	
Duration of high or low clock pulse, $t_w$	62			62			62			ns	
Setup time, $t_{SU}$	Data inputs before CLK $\uparrow$	20		20		20				ns	
	Select inputs before STRB $\downarrow$	50		50		50					
Hold time, $t_H$	Data inputs after CLK $\uparrow$ (see Note 2)	50		50		50				ns	
	Strobe input high after CLK $\uparrow$	50		50		50					
	Select inputs after STRB $\uparrow$	50		50		50					
Operating free-air temperature, $T_A$	-55			-40			85			70	$^{\circ}C$
Operating case temperature, $T_C$				125							$^{\circ}C$

NOTE 2: For operation above 25 $^{\circ}C$  junction temperature, refer to Figure 2.

## electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS	SN55500E		SN65500E		SN75500E		UNIT			
		MIN	TYP†	MAX	MIN	TYP†	MAX		MIN	TYP†	MAX
$V_{IK}$ Input clamp voltage	$V_{CC1} = 12 V$ , $I_I = -12 mA$	-1		-1.5	-1		-1.5	-1		-1.5	V
$V_{OH}$ High-level output voltage	$V_{CC1} = 13.2 V$ , $V_{CC2} = 100 V$	$I_{OH} = -1 mA$	94	97.5	94	97.5	95	97.5			V
		$I_{OH} = -10 mA$	92	94.5	92	94.5	93	94.5			
		$I_{OH} = -15 mA$	90	93.5	90	93.5	91	93.5			
$V_{OL}$ Low-level output voltage	$V_{CC1} = 13.2 V$ , $V_{CC2} = 100 V$	$I_{OL} = 1 mA$	0.85	2	0.85	2	0.85	2			V
		$I_{OL} = 10 mA$	2	4	2	4	2	4			
		$I_{OL} = 15 mA$	2.75	5	2.75	5	2.75	5			
$V_{OK}$ Output clamp voltage	$V_{CC2} = 0$	$I_O = 20 mA$	1	2.5	1	2.5	1	2.5			V
		$I_O = -20 mA$	-1.2	-2.5	-1.2	-2.5	-1.2	-2.5			
$I_{IH}$ High-level input current	$V_{CC1} = 13.2 V$ , $V_I = V_{IH} \text{ min}$			1			1			1	$\mu A$
$I_{IL}$ Low-level input current	$V_{CC1} = 13.2 V$ , $V_I = V_{IL} \text{ max}$			-1			-1			-1	$\mu A$
$I_{CC1}$ Supply current	$V_{CC1} = 13.2 V$ , $V_{CC2} = 100 V$	0.05		1	0.05		1	0.05		1	mA
$I_{CC2}$ Supply current	$V_{CC2} = 100 V$		1	5		1	5		1	3	mA

† All typical values are at  $V_{CC1} = 12 V$ ,  $T_A = 25^{\circ}C$ .

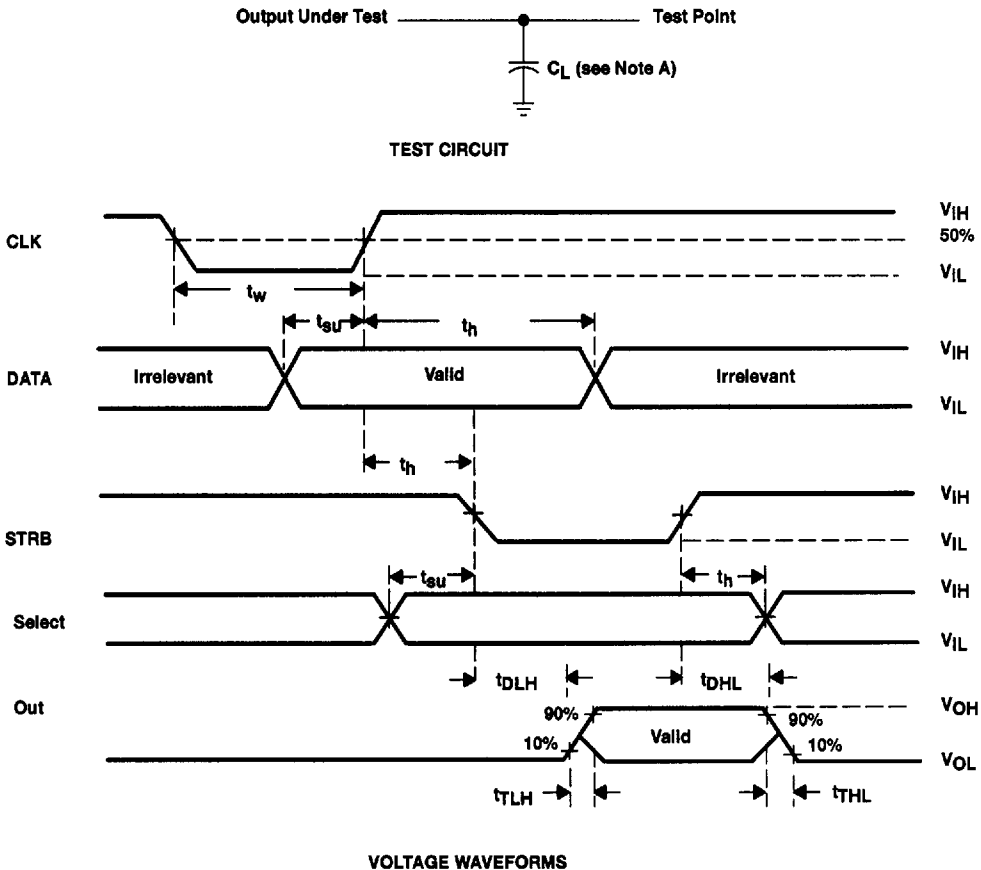
## switching characteristics, $V_{CC1} = 12 V$ , $V_{CC2} = 100 V$ , $T_A = 25^{\circ}C$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$t_{DHL}$ Delay time, high-to-low-level output from strobe input	$C_L = 30 pF$ , See Figure 1		250	ns
$t_{DLH}$ Delay time, low-to-high-level output from strobe input			450	ns
$t_{THL}$ Transition time, high-to-low-level output			200	ns
$t_{TLH}$ Transition time, low-to-high-level output			300	ns

**SN55500E, SN65500E, SN75500E  
AC PLASMA DISPLAY DRIVERS**

SLDS013B – D2471, DECEMBER 1985 – REVISED MAY 1993

**PARAMETER MEASUREMENT INFORMATION**



NOTE A.  $C_L$  includes probe and jig capacitance.

**Figure 1. Load Test Circuit and Voltage Waveforms**

# SN55500E, SN65500E, SN75500E AC PLASMA DISPLAY DRIVERS

SLDS013B - D2471, DECEMBER 1985 - REVISED MAY 1993

## TYPICAL CHARACTERISTICS

MAXIMUM CLOCK FREQUENCY  
vs  
VIRTUAL JUNCTION TEMPERATURE†

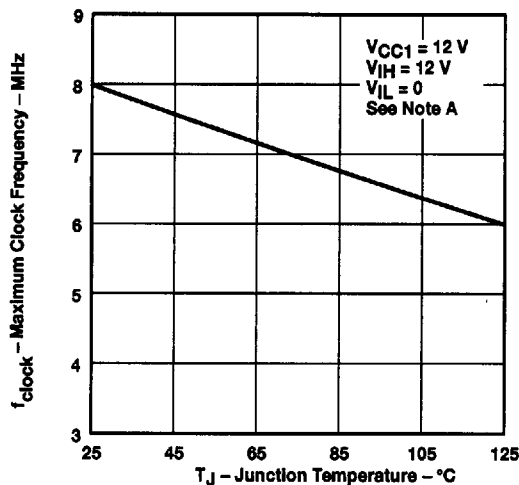


Figure 2

† Only the 25°C to 70°C portion of the curve applies to the SN75500E.  
NOTE A: This curve assumes a symmetrical clock pulse.

## THERMAL INFORMATION

### Junction temperature formula

$$T_J = T_A + P_D R_{\theta JA}$$

$$T_J = T_C + P_D R_{\theta JC}$$

where

T<sub>J</sub> = virtual junction temperature

T<sub>A</sub> = free-air temperature

P<sub>D</sub> = average device power dissipation

R<sub>θ</sub> = thermal resistance (junction-to-air, R<sub>θJA</sub>, or junction-to-case, R<sub>θJC</sub>)

PACKAGE TYPE	R <sub>θJA</sub>	R <sub>θJC</sub>
FD 44-pin ceramic	68°C/W	20°C/W
FN 44-pin plastic	70°C/W	22°C/W
J 40-pin ceramic	45°C/W	12°C/W
N 40-pin plastic	97°C/W	27°C/W