RELIABILITY REPORT

FOR

MAX3863EGJ

PLASTIC ENCAPSULATED DEVICES

July 20, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX3863 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3863 is designed for direct modulation of laser diodes at data rates up to 2.7Gbps. An automatic power-control (APC) loop is incorporated to maintain a constant average optical power. Modulation compensation is available to increase the modulation current in proportion to the bias current. The optical extinction ratio is then maintained over temperature and lifetime.

The laser driver can modulate laser diodes at amplitudes up to 80mA. Typical (20% to 80%) edge speeds are 50ps. The MAX3863 can supply a bias current up to 100mA. External resistors can set the laser output levels.

The MAX3863 includes adjustable pulse-width control to minimize laser pulse-width distortion. The device offers a failure monitor output to indicate when the APC loop is unable to maintain the average optical power.

The MAX3863 accepts differential CML clock and data input signals with on-chip 50Ω termination resistors. If a clock signal is available, an input data-retiming latch can be used to reject input pattern-dependent jitter. The laser driver is fabricated with Maxim's in-house second-generation SiGe process.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage, VCC	-0.5V to +7.0V
DATA+, DATA- and CLK+, CLK-	(VCC - 1.5V) to (VCC + 0.5V)
RTEN , EN , BIAS, MK+, MK-, PWC+, PWC-MODMON, BIASMON, MDMON, MODCOMP,APCFILT1, APCFILT2, BIASMAX, MODSET,APCSET Voltage	-0.5V to VCC + 0.5V
MOD, MODN Voltage	0 to VCC + 1.5V
MOD, MODN Current	-20mA to +150mA
BIAS Current	-20mA to +150mA
MD Current	-5mA to +5mA
Operating Junction Temperature Range	-55°C to +150°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation (TA = +85°C)	
32-Pin TQFP	1.3W
Derates above +85°C	
32-Pin TQFP	21.1mW/°C

II. Manufacturing Information

A. Description/Function:	2.7Gbps Laser Driver with Modulation Compensation
B. Process:	F60
C. Number of Device Transistors:	1786
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea
F. Date of Initial Production:	January, 2002

III. Packaging Information

A. Package Type:	**32-Pin TQFP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-7001-0506
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	81 x 81 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Poly / Au
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1: 1.2; Metal2: 1.2; Metal3: 1.2; Metal4: 5.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1: 1.6; Metal2: 1.6; Metal3: 1.6; Metal4: 4.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliability Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 44 \times 2}$$

(Chi square value for MTTF upper limit)

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 11.03 \times 10^{-9}$ $\lambda = 11.03$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HF87 die type has been found to have all pins able to withstand a transient pulse of ±400V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±200mA.

Table 1
Reliability Evaluation Test Results

MAX3863EGJ

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality		44	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TQFP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process Data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

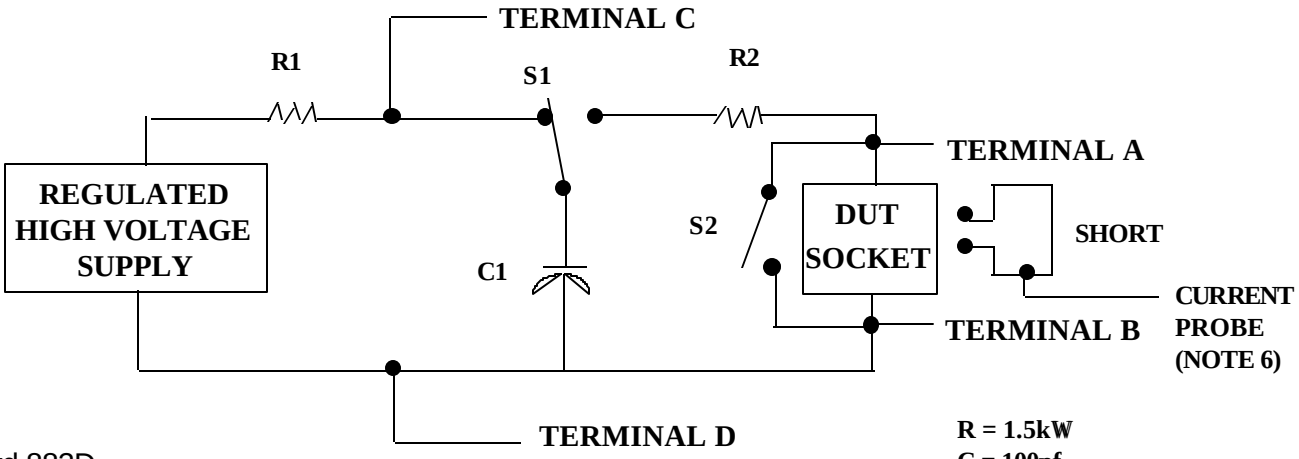
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

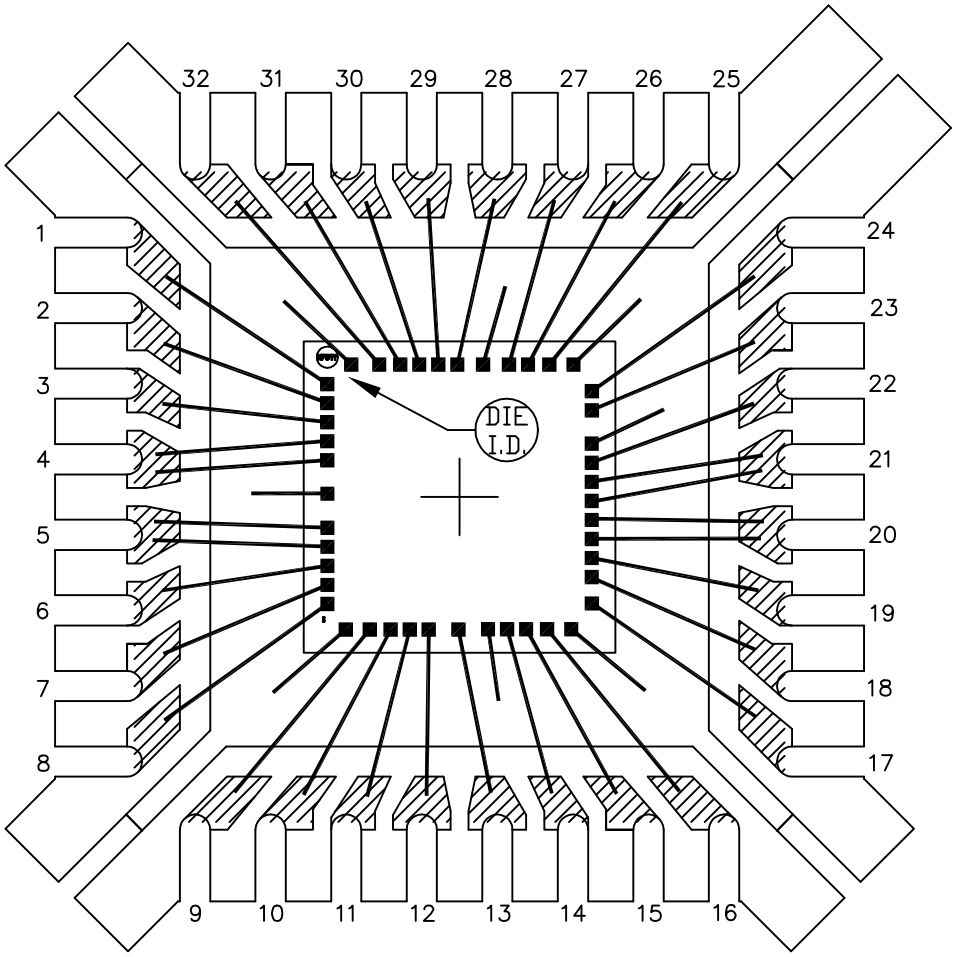
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



EXPOSED PAD PKG.



BONDABLE AREA

PKG. BODY SIZE: 5x5 mm

PKG. CODE: G3255-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 130x130	PKG.			BOND DIAGRAM #: 05-7001-0506	REV: B
	DESIGN				