



1:10 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

General Description

The MAX9311/MAX9313 are low-skew, 1-to-10 differential drivers designed for clock and data distribution. These devices allow selection between two inputs. The selected input is reproduced at 10 differential outputs. The differential inputs can be adapted to accept single-ended inputs by connecting the on-chip V_{BB} supply to one input as a reference voltage.

The MAX9311/MAX9313 feature low part-to-part skew (30ps) and output-to-output skew (12ps), making them ideal for clock and data distribution across a backplane or a board. For interfacing to differential HSTL and LVPECL signals, these devices operate over a +2.25V to +3.8V supply range, allowing high-performance clock or data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, these devices operate from a -2.25V to -3.8V supply.

The MAX9311 features an on-chip V_{BB} reference output of 1.425V below the positive supply voltage. The MAX9313 offers an on-chip V_{BB} reference output of 1.32V below the positive supply voltage.

Both devices are offered in space-saving, 32-pin 5mm x 5mm TQFP, 5mm x 5mm QFN, and industry-standard 32-pin 7mm x 7mm LQFP packages.

Applications

Precision Clock Distribution

Low-Jitter Data Repeater

Features

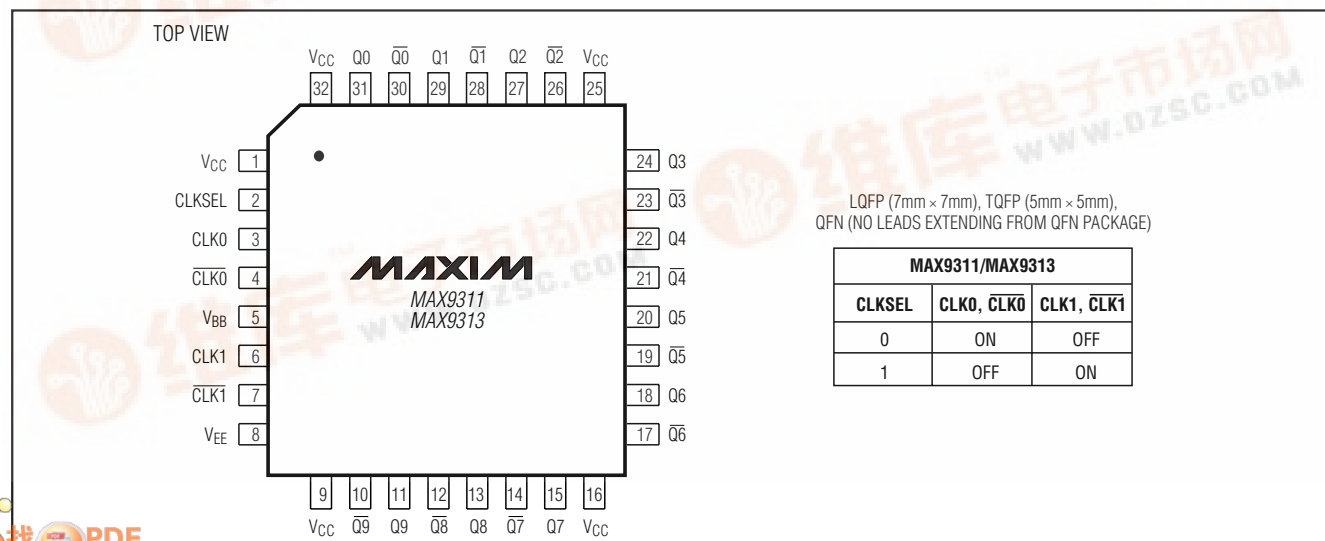
- ◆ +2.25V to +3.8V Differential HSTL/LVPECL Operation
- ◆ -2.25V to -3.8V LVECL Operation
- ◆ 30ps (typ) Part-to-Part Skew
- ◆ 12ps (typ) Output-to-Output Skew
- ◆ 312ps (typ) Propagation Delay
- ◆ $\geq 300\text{mV}$ Differential Output at 3GHz
- ◆ On-Chip Reference for Single-Ended Inputs
- ◆ Output Low with Open Input
- ◆ Pin Compatible with MC100LVEP111 (MAX9311) and MC100EP111 (MAX9313)
- ◆ Offered in Tiny QFN* Package (70% Smaller Footprint than LQFP)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX9311ECJ	-40°C to +85°C	32 LQFP (7mm x 7mm)
MAX9311EGJ*	-40°C to +85°C	32 QFN (5mm x 5mm)
MAX9311EHJ*	-40°C to +85°C	32 TQFP (5mm x 5mm)
MAX9313ECJ	-40°C to +85°C	32 LQFP (7mm x 7mm)
MAX9313EGJ*	-40°C to +85°C	32 QFN (5mm x 5mm)
MAX9313EHJ*	-40°C to +85°C	32 TQFP (5mm x 5mm)

*Future product—contact factory for availability.

Pin Configuration



MAX9311/MAX9313

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ABSOLUTE MAXIMUM RATINGS

$V_{CC} - V_{EE}$ 4.1V
 Inputs (CLK₊, CLK₋, CLKSEL) $V_{EE} - 0.3V$ to $V_{CC} + 0.3V$
 CLK₊ to CLK₋ $\pm 3.0V$
 Continuous Output Current 50mA
 Surge Output Current 100mA
 V_{BB} Sink/Source Current $\pm 0.65mA$
 Junction-to-Ambient Thermal Resistance in Still Air
 7mm x 7mm LQFP +90°C/W
 Junction-to-Ambient Thermal Resistance with
 500 LFPM Airflow
 7mm x 7mm LQFP +60°C/W

Junction-to-Case Thermal Resistance
 7mm x 7mm LQFP +12°C/W
 Operating Temperature Range -40°C to +85°C
 Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 ESD Protection
 Human Body Model (CLKSEL, CLK₊, CLK₋,
 Q₊, Q₋, V_{BB}) 2kV
 Soldering Temperature (10s) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} - V_{EE} = +2.25V$ to $+3.8V$, outputs loaded with $50\Omega \pm 1\%$ to $V_{CC} - 2V$, CLKSEL = high or low, unless otherwise noted.) (Notes 1–4)

PARAMETER	SYMBOL	CONDITIONS		-40°C		+25°C		+85°C		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
SINGLE-ENDED INPUT (CLKSEL)										
Input High Voltage	V _{IH}	Internal V _{BB} threshold	MAX9311	V _{CC} - 1.23	V _{CC}	V _{CC} - 1.23	V _{CC}	V _{CC} - 1.23	V _{CC}	V
			MAX9313	V _{CC} - 1.165	V _{CC}	V _{CC} - 1.165	V _{CC}	V _{CC} - 1.165	V _{CC}	
Input Low Voltage	V _{IL}	Internal V _{BB} threshold	MAX9311	V _{EE}	V _{CC} - 1.62	V _{EE}	V _{CC} - 1.62	V _{EE}	V _{CC} - 1.62	V
			MAX9313	V _{EE}	V _{CC} - 1.475	V _{EE}	V _{CC} - 1.475	V _{EE}	V _{CC} - 1.475	
Input High Current	I _{IH}			150		150		150		μA
Input Low Current	I _{IL}			-10 +10		-10 +10		-10 +10		μA
DIFFERENTIAL INPUTS (CLK ₊ , CLK ₋)										
Single-Ended Input High Voltage	V _{IH}	V _{BB} connected to CLK ₋ (V _{IL} for V _{BB} connected to CLK ₊), Figure 1	MAX9311	V _{CC} - 1.23	V _{CC}	V _{CC} - 1.23	V _{CC}	V _{CC} - 1.23	V _{CC}	V
			MAX9313	V _{CC} - 1.165	V _{CC}	V _{CC} - 1.165	V _{CC}	V _{CC} - 1.165	V _{CC}	

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} - V_{EE} = +2.25V$ to $+3.8V$, outputs loaded with $50\Omega \pm 1\%$ to $V_{CC} - 2V$, CLKSEL = high or low, unless otherwise noted.) (Notes 1–4)

PARAMETER	SYMBOL	CONDITIONS		-40°C		+25°C		+85°C		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
Single-Ended Input Low Voltage	V _{IL}	V _{BB} connected to CLK ₋ (V _{IH} for V _{BB} connected to CLK ₋), Figure 1	MAX9311	V _{EE}	V _{CC} - 1.62	V _{EE}	V _{CC} - 1.62	V _{EE}	V _{CC} -1.62	V
			MAX9313	V _{EE}	V _{CC} - 1.475	V _{EE}	V _{CC} - 1.475	V _{EE}	V _{CC} -1.475	
High Voltage of Differential Input	V _{IHD}			V _{EE} +1.2	V _{CC}	V _{EE} + 1.2	V _{CC}	V _{EE} +1.2	V _{CC}	V
Low Voltage of Differential Input	V _{ILD}			V _{EE}	V _{CC} - 0.095	V _{EE}	V _{CC} - 0.095	V _{EE}	V _{CC} - 0.095	V
Differential Input Voltage	V _{IHD} - V _{ILD}	For V _{CC} - V _{EE} < 3.0V		0.095	V _{CC} - V _{EE}	0.095	V _{CC} - V _{EE}	0.095	V _{CC} - V _{EE}	V
		For V _{CC} - V _{EE} ≥ 3.0V		0.095	3.0	0.095	3.0	0.095	3.0	
Input High Current	I _{IH}				150		150		150	μA
CLK ₋ Input Low Current	I _{ILCLK}			-10	+10	-10	+10	-10	+10	μA
CLK ₋ Input Low Current	I _{ILCLK}			-150		-150		-150		μA
OUTPUTS (Q ₊ , Q ₋)										
Single-Ended Output High Voltage	V _{OH}	Figure 1		V _{CC} - 1.025	V _{CC} - 0.900	V _{CC} - 1.025	V _{CC} - 0.900	V _{CC} - 1.025	V _{CC} - 0.900	V
Single-Ended Output Low Voltage	V _{OL}	Figure 1		V _{CC} - 1.93	V _{CC} - 1.695	V _{CC} - 1.93	V _{CC} - 1.695	V _{CC} - 1.93	V _{CC} - 1.695	V
Differential Output Voltage	V _{OH} - V _{OL}	Figure 1		670	950	670	950	670	950	mV
REFERENCE (V _{BB})										
Reference Voltage Output (Note 5)	V _{BB}	I _{BB} = ±0.5mA	MAX9311	V _{CC} - 1.525	V _{CC} - 1.325	V _{CC} - 1.525	V _{CC} - 1.325	V _{CC} - 1.525	V _{CC} - 1.325	V
			MAX9313	V _{CC} - 1.38	V _{CC} - 1.26	V _{CC} - 1.38	V _{CC} - 1.26	V _{CC} - 1.38	V _{CC} - 1.26	
POWER SUPPLY										
Supply Current (Note 6)	I _{EE}				75		82		95	mA

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AC ELECTRICAL CHARACTERISTICS

($V_{CC} - V_{EE} = 2.25V$ to $3.8V$, outputs loaded with $50\Omega \pm 1\%$ to $V_{CC} - 2V$, input frequency = $1.5GHz$, input transition time = $125ps$ (20% to 80%), CLKSEL = high or low, $V_{IHD} = V_{EE} + 1.2V$ to V_{CC} , $V_{ILD} = V_{EE}$ to $V_{CC} - 0.15V$, $V_{IHD} - V_{ILD} = 0.15V$ to the smaller of $3V$ or $V_{CC} - V_{EE}$, unless otherwise noted. Typical values are at $V_{CC} - V_{EE} = 3.3V$, $V_{IHD} = V_{CC} - 1V$, $V_{ILD} = V_{CC} - 1.5V$.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MA	MIN	TYP	MAX	
Differential Input-to-Output Delay	t_{PLHD} , t_{PHLD}	Figure 2	220	321	380	220	312	410	260	322	400	ps
Output-to-Output Skew (Note 8)	t_{SKOO}			12	46		12	46		10	35	ps
Part-to-Part Skew (Note 9)	t_{SKPP}			30	160		30	190		30	140	ps
Added Random Jitter (Note 10)	t_{RJ}	$f_{IN} = 1.5GHz$, Clock pattern		1.2	2.5		1.2	2.5		1.2	2.5	ps (RMS)
		$f_{IN} = 3.0GHz$, Clock pattern		1.2	2.6		1.2	2.6		1.2	2.6	
Added Deterministic Jitter (Note 10)	t_{DJ}	3Gbps, $2^{23} - 1$ PRBS pattern		80	95		80	95		80	95	ps (p-p)
Switching Frequency	f_{MAX}	$V_{OH} - V_{OL} \geq 350mV$, Clock pattern, Figure 2	2.0			2.0	3.0		2.0			GHz
		$V_{OH} - V_{OL} \geq 500mV$, Clock pattern, Figure 2	1.5			1.5			1.5			
Output Rise/Fall Time (20% to 80%)	t_R , t_F	Figure 2	100	112	140	100	116	140	100	121	140	ps

Note 1: Measurements are made with the device in thermal equilibrium.

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.

Note 3: Single-ended input operation using V_{BB} is limited to $V_{CC} - V_{EE} = 3.0V$ to $3.8V$ for the MAX9311 and $V_{CC} - V_{EE} = 2.7V$ to $3.8V$ for the MAX9313.

Note 4: DC parameters production tested at $T_A = +25^\circ C$. Guaranteed by design and characterization over the full operating temperature range.

Note 5: Use V_{BB} only for inputs that are on the same device as the V_{BB} reference.

Note 6: All pins open except V_{CC} and V_{EE} .

Note 7: Guaranteed by design and characterization. Limits are set at ± 6 sigma.

Note 8: Measured between outputs of the same part at the signal crossing points for a same-edge transition.

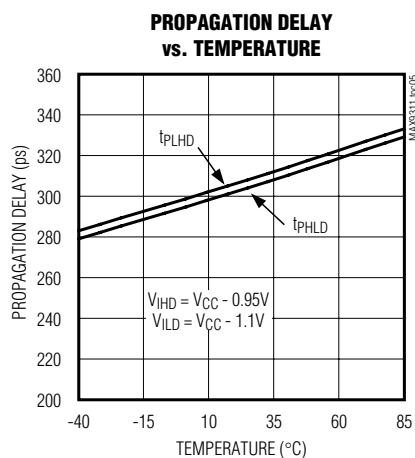
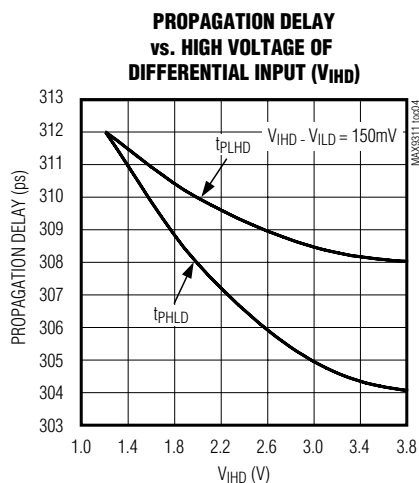
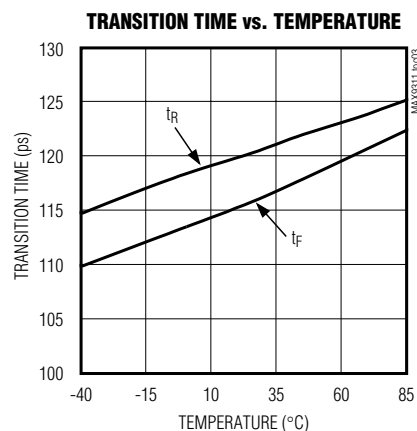
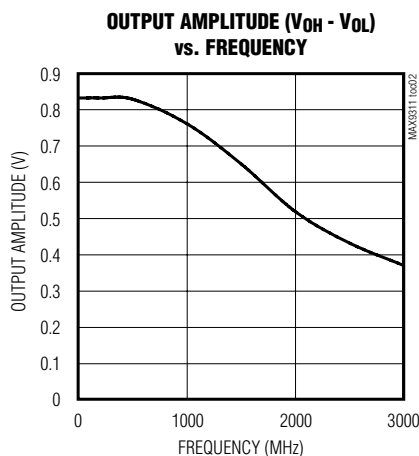
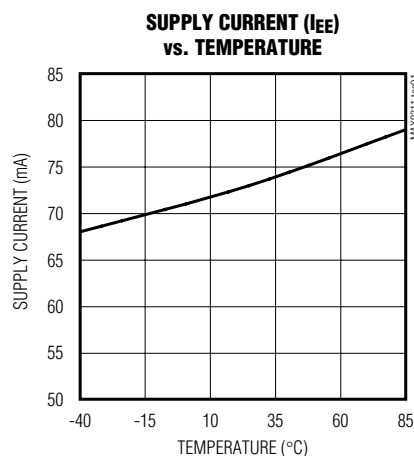
Note 9: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.

Note 10: Device jitter added to the input signal.

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Typical Operating Characteristics

($V_{CC} = +3.3V$, $V_{EE} = 0$, $V_{IHD} = V_{CC} - 0.95V$, $V_{ILD} = V_{CC} - 1.25V$, input transition time = 125ps (20% to 80%), $f_{IN} = 1.5GHz$, outputs loaded with 50Ω to $V_{CC} - 2V$, $T_A = +25^\circ C$, unless otherwise noted.)



MAX9311/MAX9313

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Pin Description

PIN	NAME	FUNCTION
1, 9, 16, 25, 32	V _{CC}	Positive Supply Voltage. Bypass from V _{CC} to V _{EE} with 0.1μF and 0.01μF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	CLKSEL	Clock Select Input (Single-Ended). Drive low to select the CLK0, $\overline{\text{CLK0}}$ input. Drive high to select the CLK1, $\overline{\text{CLK1}}$ input. The CLKSEL threshold is V _{BB} . If CLKSEL is not driven by a logic signal, use a 1kΩ pulldown to V _{EE} to select CLK0, $\overline{\text{CLK0}}$, or a 1kΩ pullup to V _{CC} to select CLK1, $\overline{\text{CLK1}}$.
3	CLK0	Noninverting Differential Clock Input 0. Internal 75kΩ pulldown resistor.
4	$\overline{\text{CLK0}}$	Inverting Differential Clock Input 0. Internal 75kΩ pullup and pulldown resistors.
5	V _{BB}	Reference Output Voltage. Connect to the inverting or noninverting clock input to provide a reference for single-ended operation. When used, bypass with a 0.01μF ceramic capacitor to V _{CC} ; otherwise, leave open.
6	CLK1	Noninverting Differential Clock Input 1. Internal 75kΩ pulldown resistor.
7	$\overline{\text{CLK1}}$	Inverting Differential Clock Input 1. Internal 75kΩ pullup and pulldown resistors.
8	V _{EE}	Negative Supply Voltage
10	$\overline{\text{Q9}}$	Inverting Q9 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
11	Q9	Noninverting Q9 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
12	$\overline{\text{Q8}}$	Inverting Q8 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
13	Q8	Noninverting Q8 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
14	$\overline{\text{Q7}}$	Inverting Q7 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
15	Q7	Noninverting Q7 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
17	$\overline{\text{Q6}}$	Inverting Q6 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
18	Q6	Noninverting Q6 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
19	$\overline{\text{Q5}}$	Inverting Q5 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
20	Q5	Noninverting Q5 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
21	$\overline{\text{Q4}}$	Inverting Q4 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
22	Q4	Noninverting Q4 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
23	$\overline{\text{Q3}}$	Inverting Q3 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
24	Q3	Noninverting Q3 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
26	$\overline{\text{Q2}}$	Inverting Q2 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
27	Q2	Noninverting Q2 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
28	$\overline{\text{Q1}}$	Inverting Q1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
29	Q1	Noninverting Q1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
30	$\overline{\text{Q0}}$	Inverting Q0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.
31	Q0	Noninverting Q0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V.

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Detailed Description

The MAX9311/MAX9313 are low skew, 1-to-10 differential drivers designed for clock and data distribution.

A 2:1 mux selects between the two differential inputs, CLK0, $\overline{\text{CLK0}}$ and CLK1, $\overline{\text{CLK1}}$. The 2:1 mux is switched by the single-ended CLKSEL input. A logic low selects the CLK0, $\overline{\text{CLK0}}$ input. A logic high selects the CLK1, $\overline{\text{CLK1}}$ input. The logic threshold for CLKSEL is set by an internal V_{BB} voltage reference. The CLKSEL input can be driven to V_{CC} and V_{EE} or by a single-ended LVPECL/LVECL signal. The selected input is reproduced at 10 differential outputs.

For interfacing to differential HSTL and LVPECL signals, these devices operate over a +2.25V to +3.8V supply range, allowing high-performance clock or data distribution in systems with a nominal +2.5V or +3.3V supply. For differential LVECL operation, these devices operate from a -2.25V to -3.8V supply.

The differential inputs can be configured to accept single-ended inputs when operating at approximately $V_{CC} - V_{EE} = +3.0V$ to +3.8V for the MAX9311 or $V_{CC} - V_{EE} = +2.7V$ to +3.8V for the MAX9313. This is accomplished by connecting the on-chip reference voltage, V_{BB} , to an input as a reference. For example, the differential CLK0, $\overline{\text{CLK0}}$ input is converted to a noninverting, single-ended input by connecting V_{BB} to $\overline{\text{CLK0}}$ and connecting the single-ended input to CLK0. Similarly, an inverting input is obtained by connecting V_{BB} to CLK0 and connecting the single-ended input to $\overline{\text{CLK0}}$. With a differential input configured as single-ended (using V_{BB}), the single-ended input can be driven to V_{CC} and V_{EE} or with a single-ended LVPECL/LVECL signal.

When a differential input is configured as a single-ended input (using V_{BB}), the approximate supply range is $V_{CC} - V_{EE} = +3.0V$ to +3.8V for the MAX9311 and $V_{CC} - V_{EE} = +2.7V$ to +3.8V for the MAX9313. This is because one of the inputs must be $V_{EE} + 1.2V$ or higher for proper operation of the input stage. V_{BB} must be at least $V_{EE} + 1.2V$ because it becomes the high-level input when the other (single-ended) input swings below it. Therefore, minimum $V_{BB} = V_{EE} + 1.2V$.

The minimum V_{BB} output for the MAX9311 is $V_{CC} - 1.525V$ and the minimum V_{BB} output for the MAX9313 is $V_{CC} - 1.38V$. Substituting the minimum V_{BB} output for each device into $V_{BB} = V_{EE} + 1.2V$ results in a minimum supply of 2.725V for the MAX9311 and 2.58V for the MAX9313. Rounding up to standard supplies gives the single-ended operating supply ranges of $V_{CC} - V_{EE} = 3.0V$ to 3.8V for the MAX9311 and $V_{CC} - V_{EE} = 2.7V$ to 3.8V for the MAX9313.

When using the V_{BB} reference output, bypass it with a 0.01 μF ceramic capacitor to V_{CC} . If the V_{BB} reference is not used, it can be left open. The V_{BB} reference can source or sink 0.5mA, which is sufficient to drive two inputs. Use V_{BB} only for inputs that are on the same device as the V_{BB} reference.

The maximum magnitude of the differential input from CLK_ to $\overline{\text{CLK}}$ is 3.0V or $V_{CC} - V_{EE}$, whichever is less. This limit also applies to the difference between any reference voltage input and a single-ended input.

The differential inputs have bias resistors that drive the outputs to a differential low when the inputs are open. The inverting inputs ($\overline{\text{CLK0}}$ and $\overline{\text{CLK1}}$) are biased with a 75k Ω pullup to V_{CC} and a 75k Ω pulldown to V_{EE} . The noninverting inputs (CLK0 and CLK1) are biased with a 75k Ω pulldown to V_{EE} . The single-ended CLKSEL input does not have a bias resistor. If not driven, pull CLKSEL up or down with a 1kHz resistor (see *Pin Description*).

Specifications for the high and low voltages of a differential input (V_{IHD} and V_{ILD}) and the differential input voltage ($V_{IHD} - V_{ILD}$) apply simultaneously (V_{ILD} cannot be higher than V_{IHD}).

Output levels are referenced to V_{CC} and are considered LVPECL or LVECL, depending on the level of the V_{CC} supply. With V_{CC} connected to a positive supply and V_{EE} connected to GND, the outputs are LVPECL. The outputs are LVECL when V_{CC} is connected to GND and V_{EE} is connected to a negative supply.

A single-ended input of at least $V_{BB} \pm 95mV$ or a differential input of at least 95mV switches the outputs to the V_{OH} and V_{OL} levels specified in the *DC Electrical Characteristics* table.

Applications Information

Supply Bypassing

Bypass V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1 μF and 0.01 μF capacitors in parallel as close to the device as possible, with the 0.01 μF value capacitor closest to the device. Use multiple parallel vias for low inductance. When using the V_{BB} reference output, bypass it with a 0.01 μF ceramic capacitor to V_{CC} (if the V_{BB} reference is not used, it can be left open).

Traces

Input and output trace characteristics affect the performance of the MAX9311/MAX9313. Connect each signal of a differential input or output to a 50 Ω characteristic impedance trace. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50 Ω characteristic impedance through connectors and across cables. Reduce skew within a

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differential pair by matching the electrical length of the traces.

Chip Information

TRANSISTOR COUNT: 250

Output Termination

Terminate outputs through 50Ω to $V_{CC} - 2V$ or use an equivalent Thevenin termination. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if Q0 is used as a single-ended output, terminate both Q0 and $\overline{Q0}$.

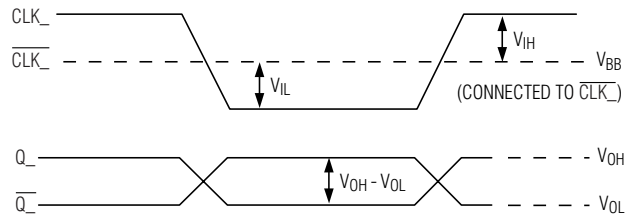


Figure 1. Switching with Single-Ended Input

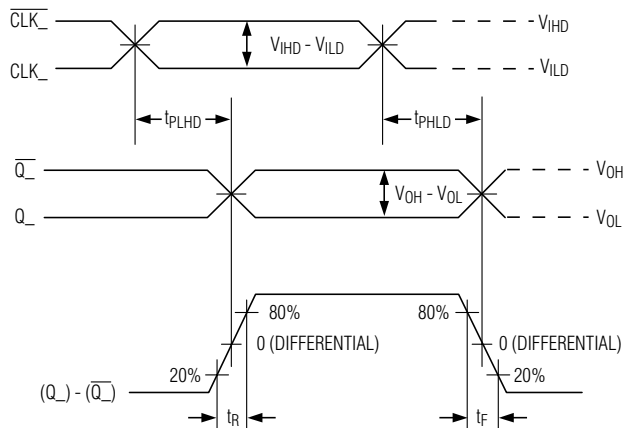


Figure 2. Differential Transition Time and Propagation Delay Timing Diagram

MAX9311/MAX9313

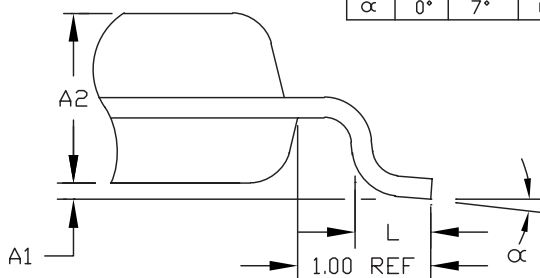
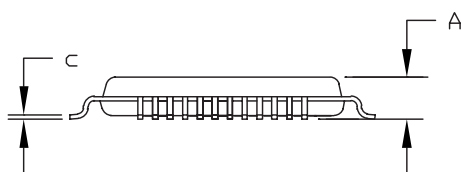
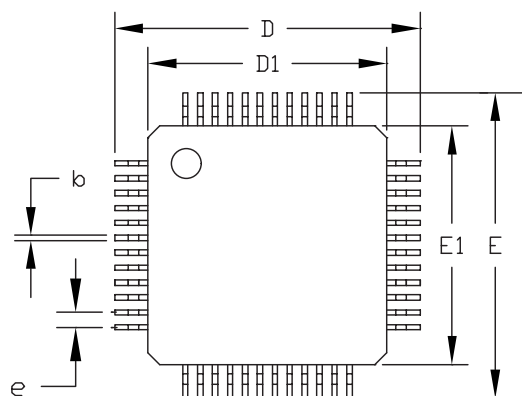
The circuit diagram illustrates a 10-bit counter implemented using three logic components: two 74VHC04 inverters and one 74VHC00 NAND gate.

- Input Section:** Two clock inputs, CLK0 and CLK1, are provided. Each input has a pull-up resistor of 75kΩ connected to V_{CC} and a pull-down resistor of 75kΩ connected to V_{EE}. The active-low complemented versions, $\overline{\text{CLK0}}$ and $\overline{\text{CLK1}}$, are also indicated.
- Inverter Stage:** Two inverters (74VHC04) are used. The first inverter takes CLK0 as input and its output is labeled Q0. The second inverter takes CLK1 as input and its output is labeled Q1. Both inverters have their non-inverting inputs tied to V_{CC} via 75kΩ resistors and their inverting inputs tied to V_{EE} via 75kΩ resistors.
- NAND Gate and Output Drivers:** A NAND gate (74VHC00) receives Q0 and Q1 as inputs. Its output is inverted by another 74VHC04 inverter to produce the final output Q2. This output Q2 is then fed back into the CLKSEL input of the NAND gate. The NAND gate's other input is connected to V_{BB}.
- Output Section:** The outputs of the inverters are Q0, Q1, and Q2. The output of the NAND gate is Q3. The output of the feedback inverter is Q4. The output of the NAND gate is Q5. The output of the feedback inverter is Q6. The output of the NAND gate is Q7. The output of the feedback inverter is Q8. The output of the NAND gate is Q9.

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



JEDEC VARIATION				
	BC		BE	
	32 LEAD		48 LEAD	
	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60
A ₁	0.05	0.15	0.05	0.15
A ₂	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D ₁	7.00	BSC.	7.00	BSC.
E	8.90	9.10	8.90	9.10
E ₁	7.00	BSC.	7.00	BSC.
e	0.8	BSC.	0.5	BSC.
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
c	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MD-136, VARIATIONS BC AND BE.
4. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

MAXIM			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.4 MM TQFP			
APPROVAL	DOCUMENT CONTROL NO.	REV	D
	21-0054		1/1

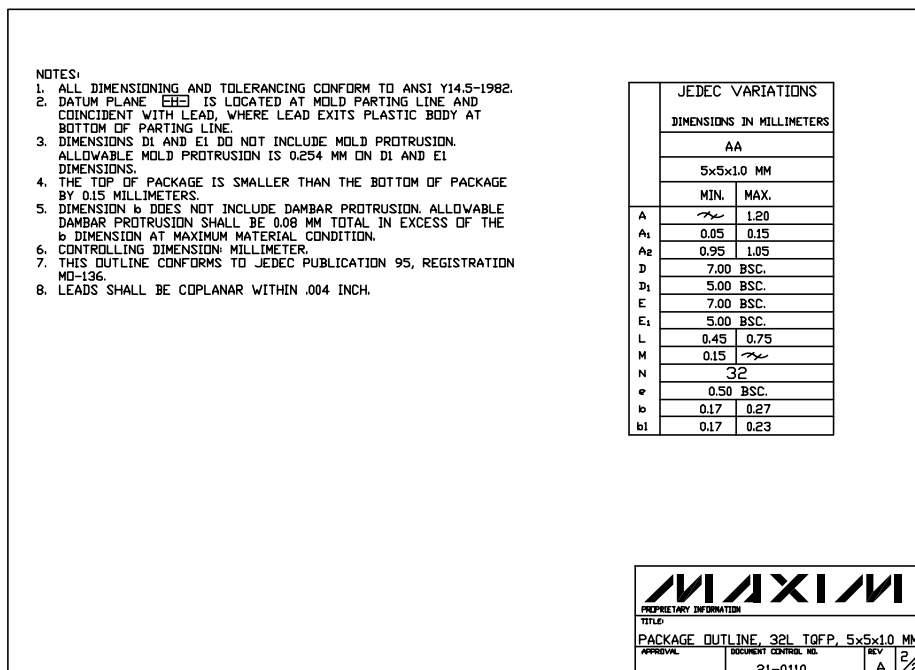
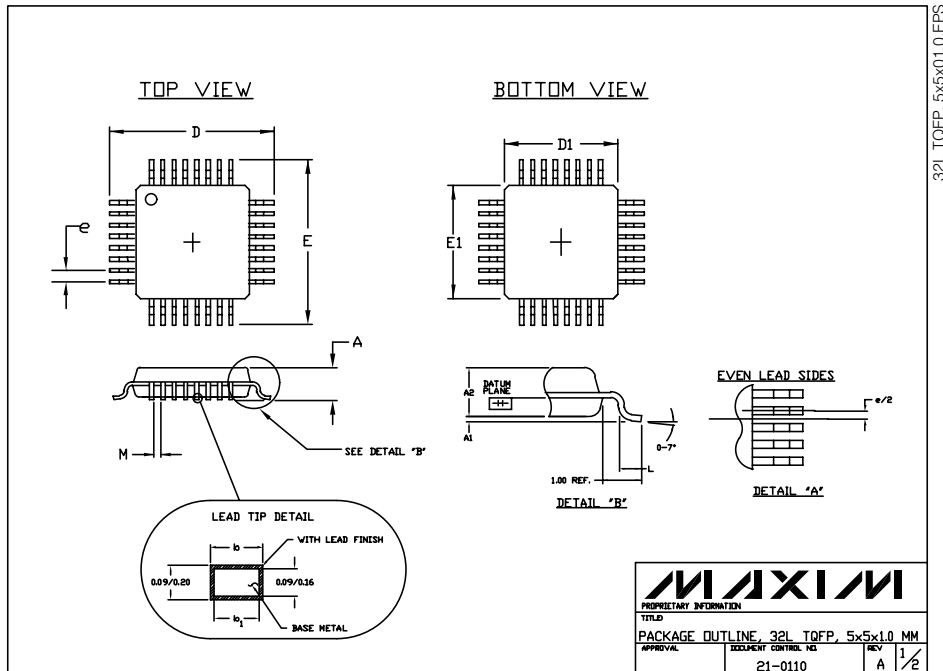
32/48L TQFP EPS

1:10 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

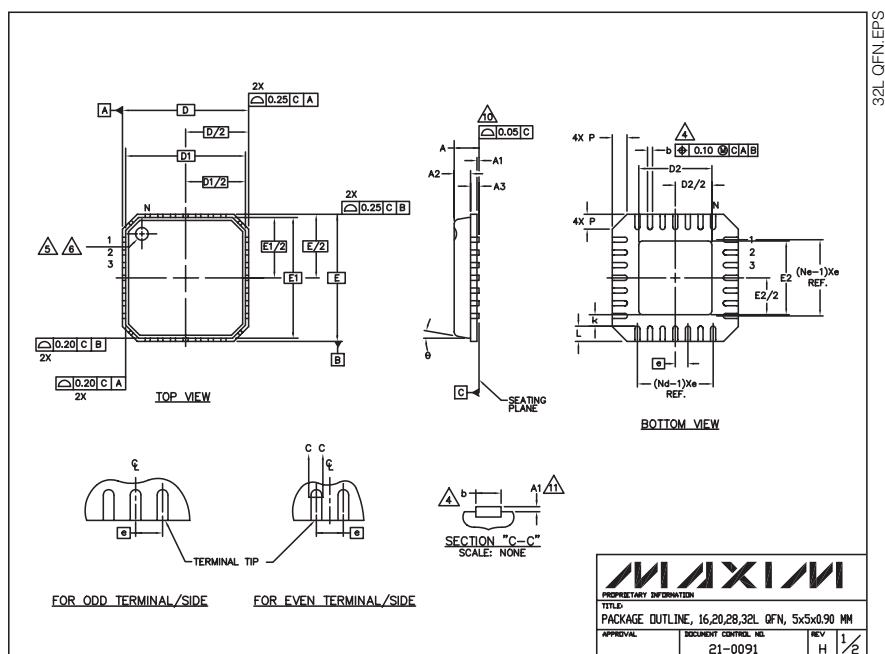
MAX9311/MAX9313



1:10 Differential LVPECL/LVECL/HSTL Clock and Data Drivers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



COMMON DIMENSIONS												
PKG	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00	0.00	0.65	1.00
A3	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.28	0.33	0.40	0.23	0.28	0.35	0.18	0.23	0.30	0.18	0.23	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
D1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E1	4.75 BSC			4.75 BSC			4.75 BSC			4.75 BSC		
e	0.80 BSC			0.65 BSC			0.50 BSC			0.50 BSC		
k	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—
L	0.35	0.55	0.75	0.35	0.55	0.75	0.35	0.55	0.75	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
P	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60	0.00	0.42	0.60
θ	0°			0°			0°			0°		

EXPOSED PAD VARIATIONS						
PKG CODES	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1655-3	2.95	3.10	3.25	2.95	3.10	3.25
G2055-1	2.95	2.70	2.85	2.95	2.70	2.85
G2055-2	2.95	3.10	3.25	2.95	3.10	3.25
G2855-1	2.95	2.70	2.85	2.95	2.70	2.85
G2855-2	2.95	3.10	3.25	2.95	3.10	3.25
G3255-1	2.95	3.10	3.25	2.95	3.10	3.25

NOTES:

- DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
- DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
- N IS THE NUMBER OF TERMINALS.
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
- THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED.
- EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- PACKAGE WARPAGE MAX 0.05mm.
- APPLIED FOR EXPOSED PAD AND TERMINALS.
EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
- MEETS JEDEC MO220.
- THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM

APPROVAL: 21-0091

REVISION: 2/2

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