



2.4GHz 802.11b Zero-IF Transceivers

MAX2820/MAX2821

General Description

The MAX2820/MAX2821 single-chip zero-IF transceivers are designed for the 802.11b (11Mbps) applications operating in the 2.4GHz to 2.5GHz ISM band. The transceivers are nearly identical, except the MAX2821 provides a low-power shutdown mode and an analog voltage reference output feature and the MAX2820 does not. The transceivers include all the circuitry required to implement an 802.11b RF-to-baseband transceiver solution, providing a fully integrated receive path, transmit path, VCO, frequency synthesis, and baseband/control interface. Only a PA, RF switch, RF BPF, and a small number of passive components are needed to form the complete radio front-end solution.

The ICs eliminate the need for external IF and baseband filters by utilizing a direct-conversion radio architecture and monolithic baseband filters for both receiver and transmitter. They are specifically optimized for 802.11b (11Mbps CCK) applications. The baseband filtering and RX and TX signal paths support the CCK modulation scheme for BER = 10⁻⁵ at the required sensitivity levels.

The devices are suitable for the full range of 802.11b data rates (1Mbps, 2Mbps, 5.5Mbps, and 11Mbps) and also the higher-rate 22Mbps PBCC™ standard. The MAX2820/MAX2821 are available in the very small 7mm x 7mm 48-lead QFN package.

Applications

- 802.11b 11Mbps WLAN
- 802.11b+ 22Mbps PBCC High-Data-Rate WLAN
- 802.11a + b Dual-Band WLAN
- 2.4GHz ISM Band Radios

PBCC is a trademark of Texas Instruments, Inc.

Pin Configuration/Functional Diagram and Typical Application Circuit appear at end of data sheet.

Features

- ◆ 2.4GHz to 2.5GHz ISM Band Operation
- ◆ 802.11b (11Mbps CCK and 22Mbps PBCC) PHY Compatible
- ◆ Complete RF-to-Baseband Transceiver
 - Direct-Conversion Upconverters and Downconverters
 - Monolithic Low-Phase-Noise VCO
 - Integrated Baseband Lowpass Filters
 - Integrated PLL with 3-Wire Serial Interface
 - Digital Bias Control for External PA
 - Transmit Power Control (Range > 25dB)
 - Receive Baseband AGC (Range > 65dB)
 - Complete Baseband Interface
 - Digital TX/RX Mode Control
 - Analog Receive Level Detection
- ◆ -97dBm RX Sensitivity at 1Mbps
- ◆ -87dBm RX Sensitivity at 11Mbps
- ◆ +2dBm Transmit Power (11Mbps CCK)
- ◆ Single +2.7V to +3.6V Supply
- ◆ Low-Current Shutdown Mode (MAX2821 only)
- ◆ Very Small 48-Pin QFN Package (s)

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---------------|----------------|------------------|
| MAX2820EGM-TD | -40°C to +85°C | 48 QFN |
| MAX2820ETM+TD | -40°C to +85°C | 48 QFN Lead Free |
| MAX2821EGM-TD | -40°C to +85°C | 48 QFN |
| MAX2821ETM+TD | -40°C to +85°C | 48 QFN Lead Free |



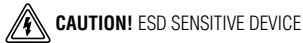
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ABSOLUTE MAXIMUM RATINGS

V_{CC} Pins to GND-0.3V to +4.2V
 RF Inputs: RX_RFP, RX_RFN to GND-0.3V to (V_{CC} + 0.3V)
 RF Outputs: TX_RFP, TX_RFN to GND-0.3V to +4.2V
 Baseband Inputs: TX_BBIP, TX_BBIN, TX_BBQP,
 TX_BBQN to GND-0.3V to (V_{CC} + 0.3V)
 Baseband Outputs: RX_BBIP, RX_BBIN, RX_BBQP,
 RX_BBQN to GND-0.3V to (V_{CC} + 0.3V)
 Analog Inputs: RX_AGC, TX_GC, TUNE, ROSCN,
 ROSCP to GND-0.3V to (V_{CC} + 0.3V)
 Analog Outputs: PA_BIAS, CP_OUT, VREF
 to GND-0.3V to (V_{CC} + 0.3V)

Digital Inputs: RX_ON, TX_ON, SHDNB, CSB, SCLK,
 DIN, RF_GAIN, RX_1K to GND-0.3V to (V_{CC} + 0.3V)
 Bias Voltages: RBIAS, BYP+0.9V to +1.5V
 Short-Circuit Duration Digital Outputs: DOUT, RX_DET 10s
 RF Input Power: RX_RFN, RX_RFP +10dBm
 Continuous Power Dissipation (T_A = +70°C)
 48-Lead QFN (derate 27.0mW/°C above +70°C)2162mW
 Operating Temperature Range-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +160°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



DC ELECTRICAL CHARACTERISTICS

(MAX2820/MAX2821 EV kit: V_{CC} = +2.7V to +3.6V, RF_GAIN = V_{IH}, 0V ≤ V_{TX_GC} ≤ +2.0V, 0V ≤ V_{RX_AGC} ≤ +2.0V, RBIAS = 12kΩ, no input signals at RF and baseband inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open, transmitter baseband inputs biased at +1.2V, registers set to default power-up settings, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.7V, T_A = +25°C, unless otherwise noted.) (Note 1)

| PARAMETERS | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--|-----------------------|------|-----|-------|
| Supply Voltage | | 2.7 | | 3.6 | V |
| Shutdown-Mode Supply Current (MAX2821 Only) | SHDNB = V _{IL} , RX_ON = V _{IL} , TX_ON = V _{IL} T _A = -40°C to +85°C | | 2 | 50 | μA |
| Standby-Mode Supply Current | SHDNB = V _{IH} , RX_ON = V _{IL} , TX_ON = V _{IL} T _A = +25°C | | 25 | 35 | mA |
| | T _A = -40°C to +85°C | | | 40 | |
| Receive-Mode Supply Current | SHDNB = V _{IH} , RX_ON = V _{IH} , TX_ON = V _{IL} T _A = +25°C | | 80 | 100 | mA |
| | T _A = -40°C to +85°C | | | 110 | |
| Transmit-Mode Supply Current | SHDNB = V _{IH} , RX_ON = V _{IL} , TX_ON = V _{IH} T _A = +25°C | | 70 | 85 | mA |
| | T _A = -40°C to +85°C | | | 90 | |
| LOGIC INPUTS: SHDNB, RX_ON, TX_ON, SCLK, DIN, CSB, RF_GAIN | | | | | |
| Digital Input Voltage High (V _{IH}) | | V _{CC} - 0.5 | | | V |
| Digital Input Voltage Low (V _{IL}) | | | | 0.5 | V |
| Digital Input Current High (I _{IH}) | | -5 | | +5 | μA |
| Digital Input Current Low (I _{IL}) | | -5 | | +5 | μA |
| LOGIC OUTPUTS: DOUT, RX_DET | | | | | |
| Digital Output Voltage High (V _{OH}) | Sourcing 100μA | V _{CC} - 0.5 | | | V |
| Digital Output Voltage Low (V _{OL}) | Sinking 100μA | | | 0.5 | V |
| RX BASEBAND I/O | | | | | |
| RX_AGC Input Resistance | 0V ≤ V _{RX_AGC} ≤ +2.0V | | 50 | | kΩ |
| RX I/Q Common-Mode Voltage | | | 1.25 | | V |
| RX I/Q Output DC Offsets | | | | 15 | mV |
| VOLTAGE REFERENCE | | | | | |
| Reference Voltage Output | T _A = -40°C to +85°C, I _{LOAD} = ±2mA | 1.1 | 1.2 | 1.3 | V |
| Output Impedance | | | 25 | | Ω |

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DC ELECTRICAL CHARACTERISTICS (continued)

(MAX2820/MAX2821 EV kit: $V_{CC} = +2.7V$ to $+3.6V$, $RF_GAIN = V_{IH}$, $0V \leq V_{TX_GC} \leq +2.0V$, $0V \leq V_{RX_AGC} \leq +2.0V$, $RBIAS = 12k\Omega$, no input signals at RF and baseband inputs, all RF inputs and outputs terminated into 50Ω , receiver baseband outputs are open, transmitter baseband inputs biased at $+1.2V$, registers set to default power-up settings, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +2.7V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETERS | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|---------------------------------|-----|-----|-----|-----------|
| TX BASEBAND I/O | | | | | |
| TX BB Input Common-Mode Range | | 1.0 | 1.2 | 1.4 | V |
| TX BBI and BBQ Input Bias Current | | | -10 | | μA |
| TX BB Input Impedance | Differential resistance | | 100 | | $k\Omega$ |
| TX_GC Input Bias Current | $0V \leq V_{TX_GC} \leq +2.0V$ | | 10 | | μA |
| TX_GC Input Impedance | Resistance | | 250 | | $k\Omega$ |
| REFERENCE OSCILLATOR INPUT | | | | | |
| Reference Oscillator Input Impedance | | | 20 | | $k\Omega$ |

AC ELECTRICAL CHARACTERISTICS—RECEIVE MODE

(MAX2820/MAX2821 EV kit: $V_{CC} = +2.7V$ to $+3.6V$, f_{RF} and $f_{LO} = 2400MHz$ to $2499MHz$, $f_{OSC} = 22MHz$ or $44MHz$, receive baseband outputs = $500mV_{P-P}$, $SHDNB = RX_ON = V_{IH}$, $TX_ON = V_{IL}$, $CSB = V_{IH}$, $SCLK = DIN = V_{IL}$, $RF_GAIN = V_{IH}$, $0V \leq V_{RX_AGC} \leq +2.0V$, $RBIAS = 12k\Omega$, $I_{CP} = +2mA$, $BW_{PLL} = 45kHz$, differential RF input matched to 50Ω , registers set to default power-up settings, $T_A = +25^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +2.7V$, $f_{LO} = 2437MHz$, $f_{OSC} = 22MHz$, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|--------------------------------------|-----|------|-------|
| RECEIVER CASCADE PERFORMANCE (RF INPUT TO BASEBAND OUTPUT) | | | | | |
| RF Frequency Range | | 2400 | | 2499 | MHz |
| LO Frequency Range | | 2400 | | 2499 | MHz |
| Voltage Gain (Note 2) | RF_GAIN = V_{IH} , V _{RX_AGC} = 0V | $T_A = +25^\circ C$ | 97 | 105 | dB |
| | | $T_A = -40^\circ C$ to $+85^\circ C$ | 95 | | |
| | RF_GAIN = V_{IH} , V _{RX_AGC} = +2.0V | $T_A = +25^\circ C$ | | 33 | |
| | RF_GAIN = V_{IL} , V _{RX_AGC} = 0V | $T_A = +25^\circ C$ | | 75 | |
| | RF_GAIN = V_{IL} , V _{RX_AGC} = +2.0V | $T_A = +25^\circ C$ | | 2 | |
| RF Gain Step | From RF_GAIN = V_{IH} to RF_GAIN = V_{IL} | | 30 | | dB |
| DSB Noise Figure (Notes 3, 11) | RF_GAIN = V_{IH} , RX gain $\geq 80dB$ | | 3.5 | 4.5 | dB |
| | RF_GAIN = V_{IH} , RX gain = 50dB | | 4.5 | | |
| | RF_GAIN = V_{IL} , RX gain = 50dB | | 34 | | |
| Adjacent Channel Rejection | RX gain = 70dB (Note 4) | | 49 | | dB |
| Input Third-Order Intercept Point (Note 5) | RF_GAIN = V_{IH} , RX gain = 80dB | | -14 | | dBm |
| | RF_GAIN = V_{IL} , RX gain = 50dB | | 18 | | |
| Input Second-Order Intercept Point (Note 6) | RF_GAIN = V_{IH} , RX gain = 80dB | | 22 | | dBm |
| | RF_GAIN = V_{IL} , RX gain = 50dB | | 60 | | |

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AC ELECTRICAL CHARACTERISTICS—RECEIVE MODE (continued)

(MAX2820/MAX2821 EV kit: $V_{CC} = +2.7V$ to $+3.6V$, f_{RF} and $f_{LO} = 2400MHz$ to $2499MHz$, $f_{OSC} = 22MHz$ or $44MHz$, receive baseband outputs = $500mV_{P-P}$, SHDNB = RX_ON = V_{IH} , TX_ON = V_{IL} , CSB = V_{IH} , SCLK = DIN = V_{IL} , RF_GAIN = V_{IH} , $0V \leq V_{RX_AGC} \leq +2.0V$, RBIAS = $12k\Omega$, $I_{CP} = +2mA$, $BW_{PLL} = 45kHz$, differential RF input matched to 50Ω , registers set to default power-up settings, $T_A = +25^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +2.7V$, $f_{LO} = 2437MHz$, $f_{OSC} = 22MHz$, unless otherwise noted.) (Note 1)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--|---|-----|-----|-----------|
| LO Leakage | | | -65 | | dBm |
| Input Return Loss | With external match | | 15 | | dB |
| RECEIVER BASEBAND | | | | | |
| BASEBAND FILTER RESPONSE | | | | | |
| -3dB Frequency | Default bandwidth setting BW (2:0) = (010) | | 7 | | MHz |
| Attenuation Relative to Passband | At 12.5MHz | | 40 | | dB |
| | At 16MHz | | 65 | | |
| | At 20MHz | | 70 | | |
| | At 25MHz | | 85 | | |
| BASEBAND OUTPUT CHARACTERISTICS | | | | | |
| RX I/Q Gain Imbalance | | -1 | | +1 | dB |
| RX I/Q Phase Quadrature Imbalance | | -5 | | +5 | Degrees |
| RX I/Q Output 1dB Compression | Differential voltage into $5k\Omega$ | | 1 | | V_{P-P} |
| RX I/Q Output THD | $V_{OUT} = 500mV_{P-P}$ at 5.5MHz, $Z_L = 5k\Omega 5pF$ | | -35 | | dBc |
| BASEBAND AGC AMPLIFIER | | | | | |
| AGC Range | $V_{RX_AGC} = 0$ to $+2.0V$ | | 70 | | dB |
| AGC Slope | Peak gain slope | | 60 | | dB/V |
| AGC Response Time | 20dB gain step, 80dB to 60dB, settling to $\pm 1dB$ | | 2 | | μs |
| BASEBAND RX PEAK LEVEL DETECTION | | | | | |
| RX Detector Trip Point (at RX_RF) | CW signal | RF_GAIN = V_{IH} , RX_DET = V_{OL} to V_{OH} | | -49 | dBm |
| | | RF_GAIN = V_{IL} , RX_DET = V_{OH} to V_{OL} | | -54 | |
| RX Detector Hysteresis | | | 5 | | dB |
| RX Detector Rise Time | With 3dB overdrive | | 1 | | μs |

AC ELECTRICAL CHARACTERISTICS—TRANSMIT MODE

(MAX2820/MAX2821 EV kit: $V_{CC} = +2.7V$ to $+3.6V$, f_{RF} and $f_{LO} = 2400MHz$ to $2499MHz$, $f_{OSC} = 22MHz$ or $44MHz$, transmit baseband inputs = $400mV_{P-P}$, SHDNB = TX_ON = V_{IH} , RX_ON = V_{IL} , CSB = V_{IH} , $0V \leq V_{TX_GC} \leq +2.0V$, RBIAS = $12k\Omega$, $I_{CP} = +2mA$, $BW_{PLL} = 45kHz$, differential RF output matched to 50Ω through a balun, baseband input biased at $+1.2V$, registers set to default power-up settings, $T_A = +25^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +2.7V$, $f_{LO} = 2437MHz$, $f_{OSC} = 22MHz$, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------|------|-----|------|-------|
| TRANSMIT SIGNAL PATH: BASEBAND INPUT TO RF OUTPUT | | | | | |
| RF Output Frequency Range | | 2400 | | 2499 | MHz |
| LO Output Frequency Range | | 2400 | | 2499 | MHz |

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AC ELECTRICAL CHARACTERISTICS—TRANSMIT MODE (continued)

(MAX2820/MAX2821 EV kit: $V_{CC} = +2.7V$ to $+3.6V$, f_{RF} and $f_{LO} = 2400MHz$ to $2499MHz$, $f_{OSC} = 22MHz$ or $44MHz$, transmit baseband inputs = $400mV_{P-P}$, SHDNB = TX_ON = V_{IH} , RX_ON = V_{IL} , CSB = V_{IH} , $0V \leq V_{TX_GC} \leq +2.0V$, RBIAS = $12k\Omega$, $I_{CP} = +2mA$, $BW_{PLL} = 45kHz$, differential RF output matched to 50Ω through a balun, baseband input biased at $+1.2V$, registers set to default power-up settings, $T_A = +25^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +2.7V$, $f_{LO} = 2437MHz$, $f_{OSC} = 22MHz$, unless otherwise noted.)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|--|--------------------------------------|-----|------|-----|---------|
| TX RF Output Power | $V_{IN} = 400mV_{P-P}$ at 5.5MHz, $V_{TX_GC} = 0V$, I/Q CW signal (Note 7) | $T_A = +25^\circ C$ | -1 | +3 | | dBm |
| | | $T_A = -40^\circ C$ to $+85^\circ C$ | -2 | | | |
| TX RF ACPR (Note 8) | $-22MHz \leq f_{OFFSET} \leq -11MHz$, $11MHz \leq f_{OFFSET} \leq 22MHz$ | | | -37 | | dBc |
| | $-33MHz \leq f_{OFFSET} < -22MHz$, $22MHz < f_{OFFSET} \leq 33MHz$ | | | -59 | | |
| In-Band Spurious Signals Relative to Modulated Carrier | $f_{RF} = 2400MHz$ to 2483MHz | Unwanted sideband | | -40 | | dBc |
| | | LO signal | | -30 | | |
| | | Spurs $> \pm 22MHz$ | | -80 | | |
| TX RF Harmonics | $2 \times f_{LO}$ | | | -40 | | dBm |
| | $3 \times f_{LO}$ | | | -55 | | |
| TX RF Spurious Signal Emissions (Outside 2400MHz to 2483.5MHz) Nonharmonic Signals | $f_{RF} < 2400MHz$ | | | -60 | | dBm |
| | $f_{RF} = 2500MHz$ to $3350MHz$ | | | -43 | | |
| | $f_{RF} > 3350MHz$ | | | -45 | | |
| TX RF Output Noise | $f_{OFFSET} \geq 22MHz$, $0V \leq V_{TX_GC} \leq +2.0V$ | | | -135 | | dBm/Hz |
| TX RF Output Return Loss | With external match | | | 15 | | dB |
| TX BASEBAND FILTER RESPONSE | | | | | | |
| -3dB Frequency | | | | 10 | | MHz |
| Attenuation Relative to Passband | At 22MHz | | | 25 | | dB |
| | At 44MHz | | | 50 | | |
| TX GAIN-CONTROL CHARACTERISTICS | | | | | | |
| Gain-Control Range | $0V \leq V_{TX_GC} \leq +2.0V$ | | | 30 | | dB |
| Gain-Control Slope | Peak gain slope | | | 40 | | dB/V |
| Gain-Control Response Time | $V_{TX_GC} = +2.0V$ to $0V$ step | | | 0.3 | | μs |

AC ELECTRICAL CHARACTERISTICS—PA BIAS

(MAX2820/MAX2821 EV kit: $V_{CC} = +2.7V$ to $+3.6V$, SHDNB = V_{IH} , TX_ON = V_{IH} , CSB = V_{IH} , PA_BIAS enabled, RBIAS = $12k\Omega$, registers set to default power-up settings, $T_A = +25^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +2.7V$, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|--|-----|-----|-----|---------|
| Resolution | | | 4 | | Bits |
| Full-Scale Output Current | | | 300 | | μA |
| LSB Size | | | 20 | | μA |
| Output Voltage Compliance Range | (Note 11) | 1.0 | 1.2 | 1.3 | V |
| Settling Time | Relative to rising edge of CSB, zero to full-scale step 0000 \rightarrow 1111, settle to 1/2 LSB, 2pF load | | 1 | | μs |

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AC ELECTRICAL CHARACTERISTICS—SYNTHESIZER

(MAX2820/MAX2821 EV kit: $V_{CC} = +2.7V$ to $+3.6V$, f_{RF} and $f_{LO} = 2400MHz$ to $2499MHz$, $f_{OSC} = 22MHz$ or $44MHz$, $SHDNB = V_{IH}$, $CSB = V_{IH}$, $RBIAS = 12k\Omega$, $I_{CP} = +2mA$, $BW_{PLL} = 45kHz$, registers set to default power-up settings, $T_A = +25^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +2.7V$, $f_{LO} = 2437MHz$, $f_{OSC} = 22MHz$, unless otherwise noted.) (Note 11)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|--|------|---------|----------------|-------------------|
| FREQUENCY SYNTHESIZER | | | | | |
| LO Frequency Range | | 2400 | | 2499 | MHz |
| Reference Frequency | $R(0) = 0$ | | 22 | | MHz |
| | $R(0) = 1$ | | 44 | | |
| Channel Spacing | | 1 | | | MHz |
| Charge-Pump Output Current | $ICP = 0$ | | ± 2 | | mA |
| | $ICP = 1$ | | ± 1 | | |
| Charge-Pump Compliance Range | | 0.4 | | $V_{CC} - 0.4$ | V |
| Reference Spur Level (Note 10) | $-11MHz \leq f_{OFFSET} \leq 11MHz$ | | -41 | | dBc |
| | $-22MHz \leq f_{OFFSET} < -11MHz$, $11MHz < f_{OFFSET} \leq 22MHz$ | | -75 | | |
| | $f_{OFFSET} < -22MHz$, $f_{OFFSET} > 22MHz$ | | -90 | | |
| Closed-Loop Phase Noise | $f_{OFFSET} = 10kHz$ | | -80 | | dBc/Hz |
| | $f_{OFFSET} = 100kHz$ | | -87 | | |
| Closed-Loop Integrated Phase Noise | Noise integrated from 100Hz to 10MHz, measured at the TX_RF output | | 2.5 | | $^\circ$ RMS |
| Reference Oscillator Input Level | AC-coupled sine wave input | 200 | 300 | 500 | mV _{p-p} |
| VOLTAGE-CONTROLLED OSCILLATOR | | | | | |
| VCO Tuning Voltage Range | | 0.4 | | 2.3 | V |
| VCO Tuning Gain | $f_{LO} = 2400MHz$ | | 170 | | MHz/V |
| | $f_{LO} = 2499MHz$ | | 130 | | |

AC ELECTRICAL CHARACTERISTICS—SYSTEM TIMING

(MAX2820/MAX2821 EV kit: $V_{CC} = +2.7V$ to $+3.6V$, f_{RF} and $f_{LO} = 2400MHz$ to $2499MHz$, $f_{OSC} = 22MHz$ or $44MHz$, $SHDNB = V_{IH}$, $CSB = V_{IH}$, $RBIAS = 12k\Omega$, $I_{CP} = +2mA$, $BW_{LOOP} = 45kHz$, registers set to default power-up settings, $T_A = +25^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +2.7V$, $f_{LO} = 2437MHz$, $f_{OSC} = 22MHz$, unless otherwise noted.) (Note 11)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|--|-----|-----|-----|---------|
| Channel-Switching Time | $f_{LO} = 2400MHz \leftrightarrow 2499MHz$, f_{LO} settles to $\pm 10kHz$ (Note 9) | | 150 | 200 | μs |
| RX/TX Turnaround Time | RX to TX, f_{LO} settles to within $\pm 30kHz$, relative to rising edge of TX_ON | | | 5 | μs |
| | TX to RX, f_{LO} settles to within $\pm 30kHz$, relative to rising edge of RX_ON | | | 10 | |

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AC ELECTRICAL CHARACTERISTICS—SYSTEM TIMING (continued)

(MAX2820/MAX2821 EV kit: $V_{CC} = +2.7V$ to $+3.6V$, f_{RF} and $f_{LO} = 2400MHz$ to $2499MHz$, $f_{OSC} = 22MHz$ or $44MHz$, $SHDNB = V_{IH}$, $CSB = V_{IH}$, $R_{BIAS} = 12k\Omega$, $I_{CP} = +2mA$, $BW_{LOOP} = 45kHz$, registers set to default power-up settings, $T_A = +25^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = +2.7V$, $f_{LO} = 2437MHz$, $f_{OSC} = 22MHz$, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|--|-----|-----|-----|---------|
| Standby-to-Receive Mode | Standby to RX, f_{LO} settles to within $\pm 30kHz$, relative to rising edge of RX_ON | | | 5 | μs |
| Standby-to-Transmit Mode | Standby to TX, f_{LO} settles to within $\pm 30kHz$, relative to rising edge of TX_ON | | | 10 | μs |

AC ELECTRICAL CHARACTERISTICS—SERIAL INTERFACE TIMING

(MAX2820/MAX2821 EV kit: $V_{CC} = +2.7V$ to $+3.6V$, registers set to default power-up settings, $T_A = +25^\circ C$, unless otherwise noted. (Note 11))

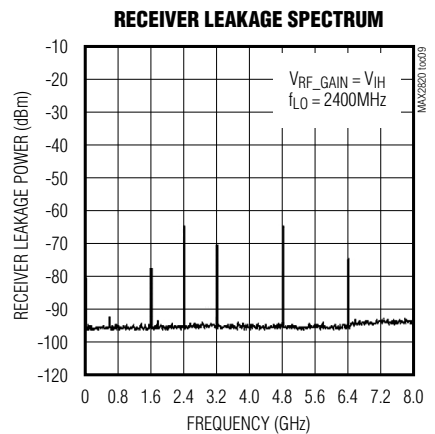
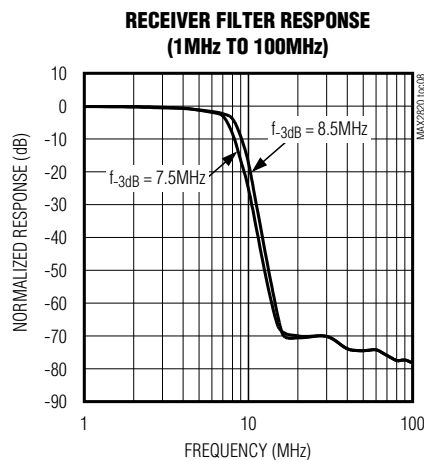
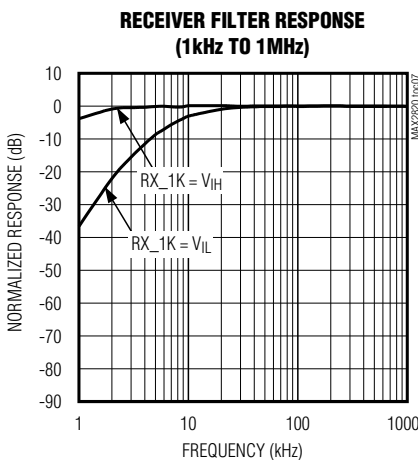
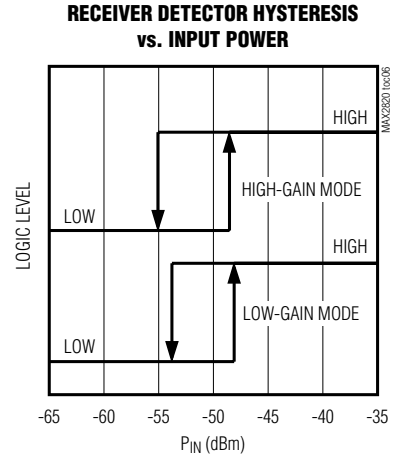
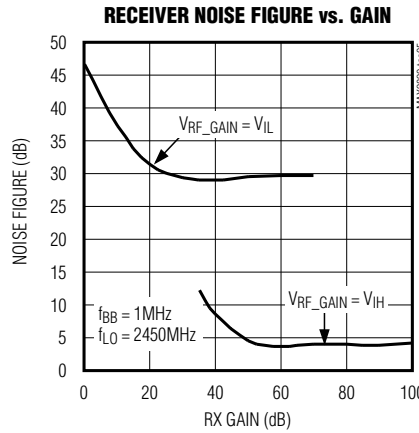
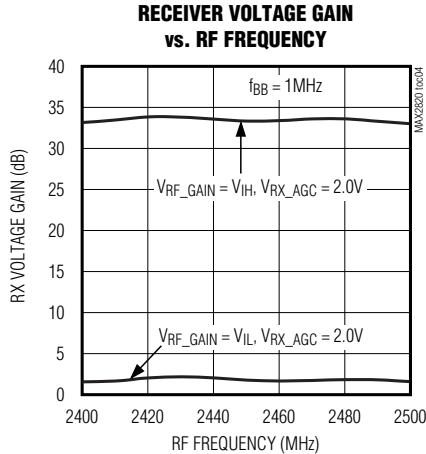
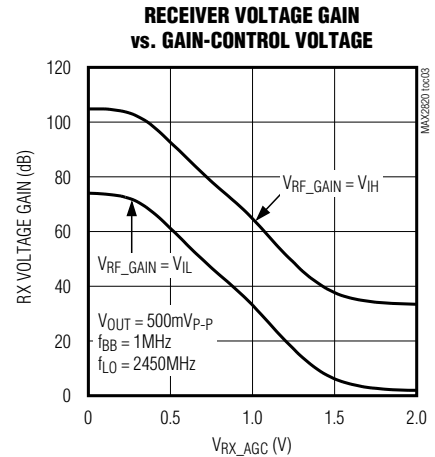
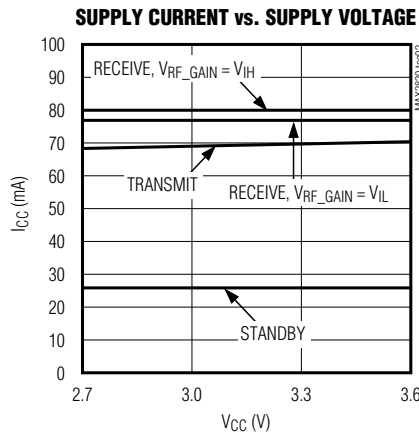
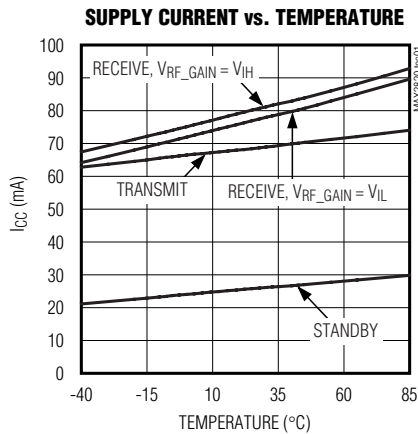
| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--|-----|-----|-----|-------|
| SERIAL INTERFACE TIMING (See Figure 1) | | | | | |
| t_{CSO} | SCLK rising edge to CSB falling edge wait time | 5 | | | ns |
| t_{CSS} | Falling edge of CSB to rising edge of first SCLK time | 5 | | | ns |
| t_{DS} | Data-to-serial clock setup time | 5 | | | ns |
| t_{DH} | Data-to-clock hold time | 10 | | | ns |
| t_{CH} | Serial clock pulse-width high | 10 | | | ns |
| t_{CL} | Clock pulse-width low | 10 | | | ns |
| t_{CSH} | Last SCLK rising edge to rising edge of CSB | 5 | | | ns |
| t_{CSW} | CSB high pulse width | 10 | | | ns |
| t_{CS1} | Time between the rising edge of CSB and the next rising edge of SCLK | 5 | | | ns |
| f_{CLK} | Clock frequency | | | 50 | MHz |

- Note 1:** Parameters are production tested at $+25^\circ C$ only. Min/max limits over temperature are guaranteed by design and characterization.
- Note 2:** Defined as the baseband differential RMS output voltage divided by the RMS input voltage (at the RF balun input).
- Note 3:** Noise-figure specification excludes the loss of the external balun. The external balun loss is typically $\sim 0.5dB$.
- Note 4:** CCK interferer at 25MHz offset. Desired signal equals $-73dBm$. Interferer amplitude increases until baseband output from interferer is 10dB below desired signal. Adjacent channel rejection = $P_{interferer} - P_{desired}$.
- Note 5:** Measured at balun input. Two CW tones at $-43dBm$ with 15MHz and 25MHz spacing from the MAX2820/MAX2821 channel frequency. IP3 is computed from 5MHz IMD3 product measured at the RX I/Q output.
- Note 6:** Two CW interferers at $-38dBm$ with 24.5MHz and 25.5MHz spacing from the MAX2820/MAX2821 channel frequency. IP2 is computed from the 1MHz IMD2 product measured at the RX I/Q output.
- Note 7:** Output power measured after the matching and balun. TX gain is set to maximum.
- Note 8:** Adjacent and alternate channel power relative to the desired signal. TX gain is adjusted until the output power is $-1dBm$. Power measured with 100kHz video BW and 100kHz resolution BW.
- Note 9:** Time required to reprogram the PLL, change the operating channel, and wait for the operating channel center frequency to settle within $\pm 10kHz$ of the nominal (final) channel frequency.
- Note 10:** Relative amplitude of reference spurious products appearing in the TX RF output spectrum relative to a CW tone at 0.5MHz offset from the LO.
- Note 11:** Min/max limits are guaranteed by design and characterization.

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Typical Operating Characteristics

(MAX2820/MAX2821 EV kit, $V_{CC} = +2.7V$, $f_{BB} = 1MHz$, $f_{LO} = 2450MHz$, receive baseband outputs = 500mVp-p, transmit baseband inputs = 400mVp-p, $I_{CP} = +2mA$, $BW_{PLL} = 45kHz$, differential RF input/output matched to 50Ω through a balun, baseband input biased at +1.2V, registers set to default power-up settings, $T_A = +25^\circ C$, unless otherwise noted.)

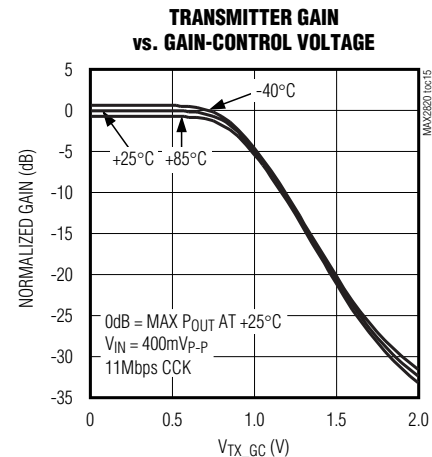
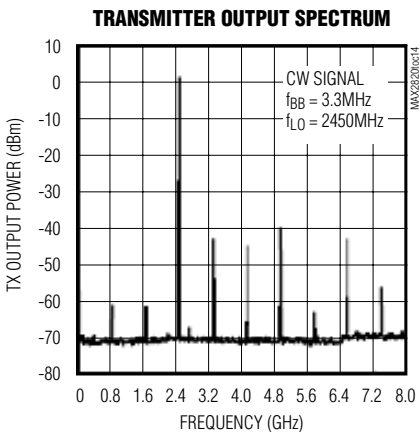
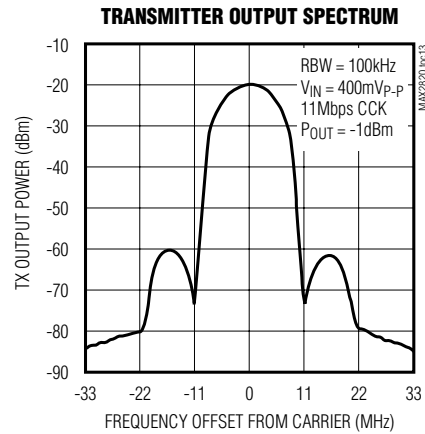
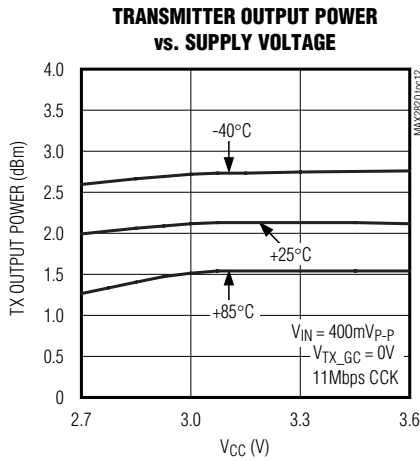
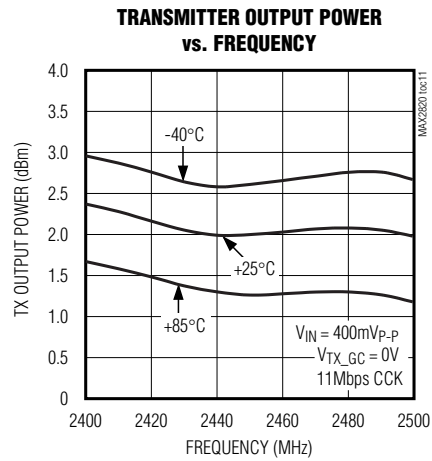
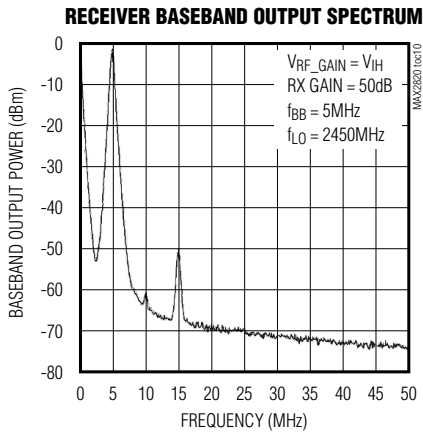


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MAX2820/MAX2821

Typical Operating Characteristics (continued)

(MAX2820/MAX2821 EV kit, $V_{CC} = +2.7V$, $f_{BB} = 1MHz$, $f_{LO} = 2450MHz$, receive baseband outputs = 500mVp-p, transmit baseband inputs = 400mVp-p, $I_{CP} = +2mA$, $BW_{PLL} = 45kHz$, differential RF input/output matched to 50Ω through a balun, baseband input biased at +1.2V, registers set to default power-up settings, $T_A = +25^\circ C$, unless otherwise noted.)

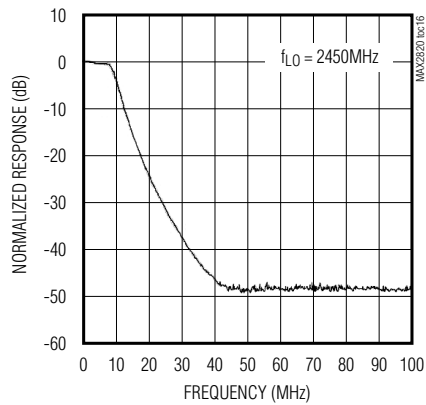


2.4GHz 802.11b Zero-IF Transceivers

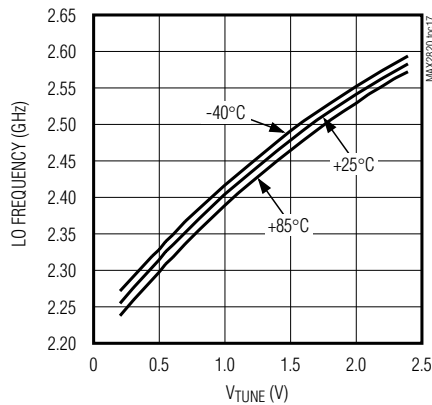
Typical Operating Characteristics (continued)

(MAX2820/MAX2821 EV kit, $V_{CC} = +2.7V$, $f_{BB} = 1MHz$, $f_{LO} = 2450MHz$, receive baseband outputs = $500mV_{P-P}$, transmit baseband inputs = $400mV_{P-P}$, $I_{CP} = +2mA$, $BW_{PLL} = 45kHz$, differential RF input/output matched to 50Ω through a balun, baseband input biased at $+1.2V$, registers set to default power-up settings, $T_A = +25^\circ C$, unless otherwise noted.)

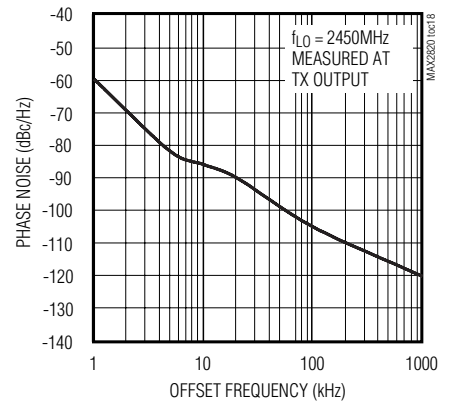
TRANSMITTER BASEBAND FILTER RESPONSE



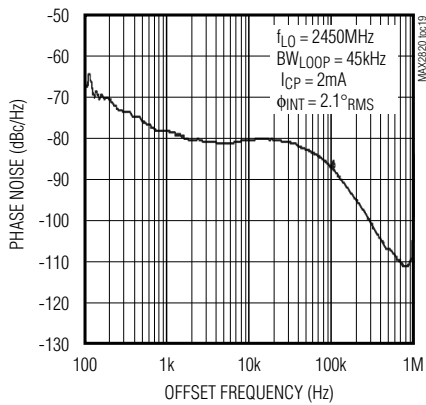
LO FREQUENCY vs. TUNING VOLTAGE



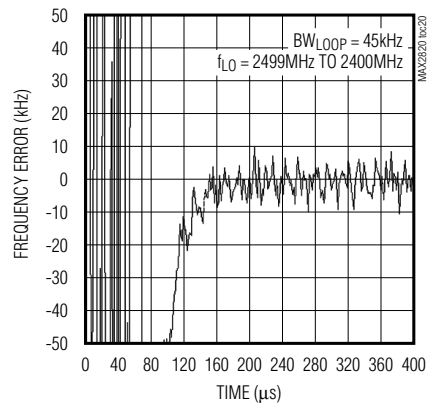
OPEN-LOOP PHASE NOISE vs. OFFSET FREQUENCY



CLOSED-LOOP PHASE NOISE vs. OFFSET FREQUENCY

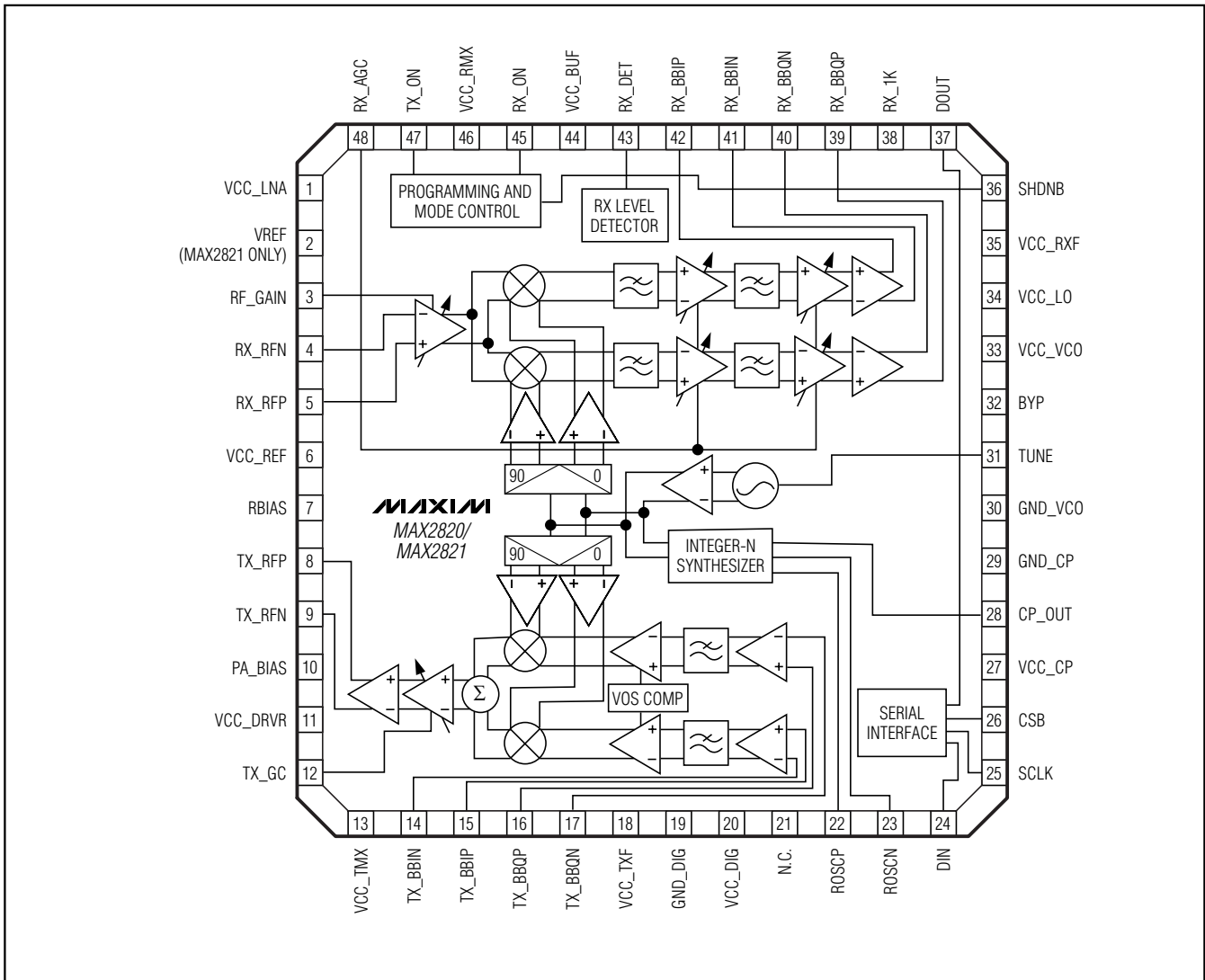


VCO/PLL SETTING TIME



2.4GHz 802.11b Zero-IF Transceivers

Pin Configuration/Functional Diagram



MAX2820/MAX2821

2.4GHz 802.11b Zero-IF Transceivers

Pin Description

| PIN | NAME | DESCRIPTION |
|-----|----------|---|
| 1 | VCC_LNA | Supply Voltage for LNA. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches. |
| 2 | N.C. | No Connection. Not internally connected. (MAX2820 only) |
| | VREF | Voltage Reference Output. (MAX2821 only) |
| 3 | RF_GAIN | LNA Gain Select Logic Input. Logic high for LNA high-gain mode, logic low for LNA low-gain mode. |
| 4 | RX_RFN | Receiver LNA Negative Input. On-chip AC-coupling. Requires off-chip impedance match and connection to 2:1 balun. |
| 5 | RX_RFP | Receiver LNA Positive Input. On-chip AC-coupling. Requires off-chip impedance match and connection to 2:1 balun. |
| 6 | VCC_REF | Supply Voltage for Bias Circuitry and Autotuner. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches. |
| 7 | RBIAS | Precision Bias Resistor Pin. Connect a 12k Ω precision resistor ($\leq 2\%$) to GND. |
| 8 | TX_RFP | Transmit Driver Amplifier Positive Output. On-chip pullup choke to VCC. Requires off-chip impedance match and connection to 4:1 balun. |
| 9 | TX_RFN | Transmit Driver Amplifier Negative Output. On-chip pullup choke to VCC. Requires off-chip impedance match and connection to 4:1 balun. |
| 10 | PA_BIAS | Power-Amplifier Bias-Current Control Signal. Analog output. High-impedance, open-drain current source. Connect directly to bias-current control input on external PA. |
| 11 | VCC_DRVR | Supply Voltage for Transmit Driver. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches. |
| 12 | TX_GC | Transmit Gain-Control Input. Analog high-impedance input. Connect directly to baseband IC DAC output. See the <i>Typical Operating Characteristics</i> for Transmitter Gain vs. Gain-Control Voltage. |
| 13 | VCC_TMX | Supply Voltage for Transmit Mixer and VGA. Bypass with a capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches. |
| 14 | TX_BBIN | Transmit Negative In-Phase Baseband Input. Analog high-impedance differential input. Connect directly to baseband IC DAC voltage output. Requires a 1.2V common-mode voltage. |
| 15 | TX_BBIP | Transmit Positive In-Phase Baseband Input. Analog high-impedance differential input. Connect directly to baseband IC DAC voltage output. Requires a 1.2V common-mode voltage. |
| 16 | TX_BBQP | Transmit Positive Quadrature Baseband Input. Analog high-impedance differential input. Connect directly to baseband IC DAC voltage output. Requires a 1.2V common-mode voltage. |
| 17 | TX_BBQN | Transmit Negative Quadrature Baseband Input. Analog high-impedance differential input. Connect directly to baseband IC DAC voltage output. Requires a 1.2V common-mode voltage. |
| 18 | VCC_TXF | Supply Voltage for Transmit Baseband Filter. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches. |
| 19 | GND_DIG | Digital Ground |

2.4GHz 802.11b Zero-IF Transceivers

Pin Description (continued)

MAX2820/MAX2821

| PIN | NAME | DESCRIPTION |
|-----|---------|--|
| 20 | VCC_DIG | Supply Voltage for Digital Circuitry. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches. |
| 21 | N.C. | No Connection. Not internally connected. |
| 22 | ROSCP | Reference Oscillator Positive Input. Analog, high-impedance differential input. DC-coupled. Requires external AC-coupling. Connect an external reference oscillator to this analog input. |
| 23 | ROSCN | Reference Oscillator Negative Input. Analog, high-impedance differential input. DC-coupled. Requires external AC-coupling. Bypass this analog input to ground with capacitor for single-ended operation. |
| 24 | DIN | 3-Wire Serial Interface Data Input. Digital, high-impedance input. Connect directly to baseband IC serial interface CMOS output. (SPI/QSPI/MICROWIRE compatible) |
| 25 | SCLK | 3-Wire Serial Interface Clock Input. Digital, high-impedance input. Connect this digital input directly to baseband IC serial interface CMOS output. (SPI/QSPI/MICROWIRE compatible). |
| 26 | CSB | 3-Wire Serial Interface Enable Input. Digital, high-impedance input. Connect directly to baseband IC serial interface CMOS output. (SPI/QSPI/MICROWIRE compatible) |
| 27 | VCC_CP | Supply Voltage for PLL Charge Pump. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches. |
| 28 | CP_OUT | PLL Charge-Pump Output. Analog, high-impedance output. Current source. Connect directly to the PLL loop filter input. |
| 29 | GND_CP | PLL Charge-Pump Ground. Connect to PC board ground plane. |
| 30 | GND_VCO | VCO Ground. Connect to PC board ground plane. |
| 31 | TUNE | VCO Frequency Tuning Input. Analog voltage input. High impedance. Connect directly to the PLL loop filter output. |
| 32 | BYP | VCO Bias Bypass Pin. Bypass with a 2000pF capacitor to ground. |
| 33 | VCC_VCO | Supply Voltage for VCO. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches. Important note: Operate off separate regulated supply voltage. |
| 34 | VCC_LO | Supply Voltage for VCO, LO Buffers, and LO Quadrature Circuitry. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches. |
| 35 | VCC_RXF | Supply Voltage for Receiver Baseband Filter. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches. |
| 36 | SHDNB | Active Low Shutdown Input. Digital CMOS input. High impedance. Connect directly to baseband IC mode control CMOS output. Logic low to disable all device functions. Logic high to enable normal chip operation. |
| 37 | DOUT | Serial Interface Data Output. Digital CMOS output. Optional connection. |
| 38 | RX_1K | Receiver 1kHz Highpass Bandwidth Control. Digital CMOS input. Connect directly to baseband IC CMOS output. Controls receiver baseband highpass -3dB corner frequency; logic low for 10kHz, logic high for 1kHz. See the <i>Applications Information</i> section for proper use of this function. |

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2.4GHz 802.11b Zero-IF Transceivers

Pin Description (continued)

| PIN | NAME | DESCRIPTION |
|----------------|---------|--|
| 39 | RX_BBQP | Receive Positive Quadrature Baseband Output. Analog low-impedance differential buffer output. Connect output directly to baseband ADC input. Internally biased to 1.2V common-mode voltage and can drive loads up to 5k Ω 5pF. |
| 40 | RX_BBQN | Receive Negative Quadrature Baseband Output. Analog low-impedance differential buffer output. Connect output directly to baseband ADC input. Internally biased to 1.2V common-mode voltage and can drive loads up to 5k Ω 5pF. |
| 41 | RX_BBIN | Receive Negative In-Phase Baseband Output. Analog low-impedance differential buffer output. Connect output directly to baseband ADC input. Internally biased to 1.2V common-mode voltage and can drive loads up to 5k Ω 5pF. |
| 42 | RX_BBIP | Receive Positive In-Phase Baseband Output. Analog low-impedance differential buffer output. Connect output directly to baseband ADC input. Internally biased to 1.2V and can drive loads up to 5k Ω 5pF. |
| 43 | RX_DET | Receive Level Detection Output. Digital CMOS output. Connect output directly to baseband IC input. Used to indicate RF input level. Logic high for input levels above -49dBm (typ). Logic low for levels below -54dBm (typ). |
| 44 | VCC_BUF | Supply Voltage for Receiver Baseband Buffer. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches. |
| 45 | RX_ON | Receiver-On Control Input. Digital CMOS input. Connect to baseband IC mode control CMOS output. |
| 46 | VCC_RMX | Supply Voltage for Receiver Downconverter. Bypass with capacitor as close to the pin as possible. Do not share the bypass capacitor ground vias with other branches. |
| 47 | TX_ON | Transmitter-On Control Input. Digital CMOS input. Connect directly to baseband IC mode control CMOS output. |
| 48 | RX_AGC | Receive AGC Control. Analog high-impedance input. Connect directly to baseband IC DAC voltage output. See the <i>Typical Operating Characteristics</i> for Gain vs. V _{RX_AGC} . |
| Exposed Paddle | GND | DC and AC Ground Return for IC. Connect to PC board ground plane using multiple vias. |

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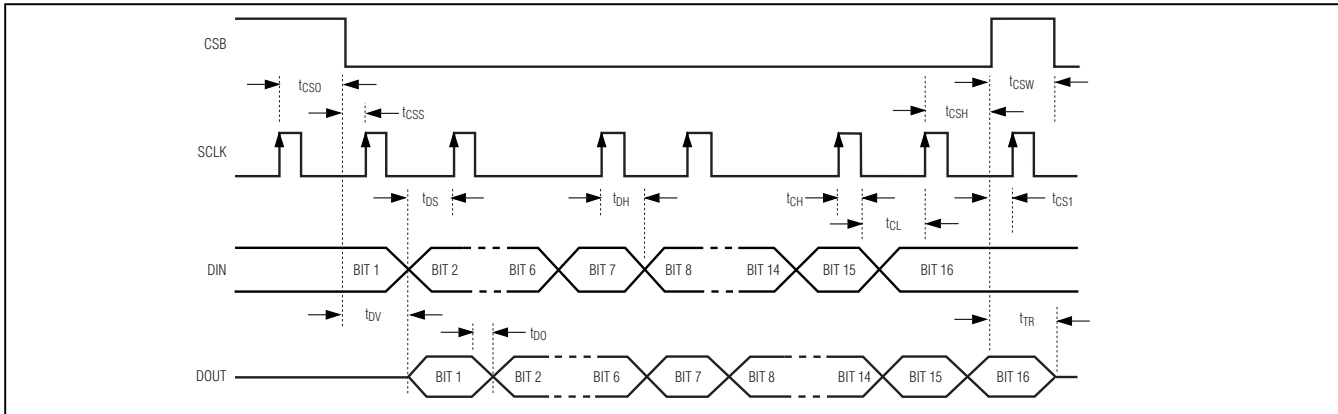


Figure 1. MAX2820/MAX2821 Serial Interface Timing Diagram

Table 1. Operating Mode Truth Table

| OPERATING MODE | MODE CONTROL INPUTS | | | CIRCUIT BLOCK STATES | | |
|----------------|---------------------|-------|-------|----------------------|---------|-----------------|
| | SHDNB | TX_ON | RX_ON | RX_PATH | TX_PATH | PLL/VCO/LO GEN. |
| Shutdown | 0 | X | X | OFF | OFF | OFF |
| Standby | 1 | 0 | 0 | OFF | OFF | ON |
| Receive | 1 | 0 | 1 | ON | OFF | ON |
| Transmit | 1 | 1 | 0 | OFF | ON | ON |

Operating Modes

The MAX2820/MAX2821 have four primary modes of operation: shutdown, standby, receive active, and transmit active. The modes are controlled by the digital inputs SHDNB, TX_ON, and RX_ON. Table 1 shows the operating mode vs. the digital mode control input.

Shutdown Mode

Shutdown mode is achieved by driving SHDNB low. In shutdown mode, all circuit blocks are powered down, except for the serial interface circuitry. While the device is in shutdown, the serial interface registers can still be loaded by applying V_{CC} to the digital supply voltage (V_{CC_DIG}). All previously programmed register values are preserved during the shutdown mode, as long as V_{CC_DIG} is applied.

Standby Mode

Standby mode is achieved by driving SHDNB high, RX_ON, and TX_ON low. In standby mode, the PLL, VCO, LO generator, LO buffer, LO quadrature, and filter autotuner are powered on by default. The standby mode is intended to provide time for the slower-settling circuitry (PLL and autotuner) to turn on and settle to the correct frequency before making RX or TX active. The 3-wire serial interface is active and can load register

values at any time. Refer to serial interface specification for details.

Receive Mode

Receive mode is enabled by driving the digital inputs SHDNB high, RX_ON high, and TX_ON low. In receive mode, all receive circuit blocks are powered on and all VCO, PLL, and autotuner circuits are powered on. None of the transmit path blocks are active in this mode. Although the receiver blocks turn on quickly, the DC offset nulling requires ~10μs to settle. The receiver signal path is ready ~10μs after a low-to-high transition on RX_ON.

Transmit Mode

Transmit mode is achieved by driving the digital inputs SHDNB high, RX_ON low, and TX_ON high. In transmit mode, all transmit circuit blocks are powered on and all VCO, PLL, and autotuner circuits are powered on. None of the receive path blocks is active in this mode. Although the transmitter blocks turn on quickly, the baseband DC offset calibration requires ~2.2μs to complete. In addition, the TX driver amplifier is ramped from the low-gain state (minimum RF output) to high-gain state (peak RF output) over the next 1μs to 2μs. The transmit signal path is ready ~4μs after a low-to-high transition on TX_ON.

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Table 2. Programming Register Definition Summary (Address and Data)

| REGISTER NAME | 4 ADDRESS BITS | | | | 12 DATA BITS | | | | | | | | | | | |
|---------------|----------------|----|----|----|--------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| | A3 | A2 | A1 | A0 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | MSB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | LSB |
| ENABLE | 0 | 0 | 0 | 1 | E11 | E10 | E9 | E8 | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| SYNTH | 0 | 0 | 1 | 0 | X | X | X | X | PD | ICP | R5 | R4 | R3 | R2 | R1 | R0 |
| CHANNEL | 0 | 0 | 1 | 1 | X | X | X | X | X | CF6 | CF5 | CF4 | CF3 | CF2 | CF1 | CF0 |
| RECEIVE | 0 | 1 | 0 | 0 | 2C2 | 2C1 | 2C0 | 1C2 | 1C1 | 1C0 | DL1 | DL0 | SF | BW2 | BW1 | BW0 |
| TRANSMIT | 0 | 1 | 0 | 1 | X | X | X | X | X | X | X | X | PA3 | PA2 | PA1 | PA0 |

X = Don't care.

Programmable Registers

The MAX2820/MAX2821 contain programmable registers to control various modes of operation for the major circuit blocks. The registers can be programmed through the 3-wire SPI/QSPI/MICROWIRE-compatible serial port. The MAX2820/MAX2821 include five programmable registers:

- 1) Block-enable register
- 2) Synthesizer register
- 3) Channel frequency register
- 4) Receiver settings register
- 5) Transmitter settings register

Each register consists of 16 bits. The four most significant bits (MSBs) are the register's address. The twelve least significant bits (LSBs) are used for register data. Table 2 summarizes the register configuration. A detailed description of each register is provided in Tables 3–6.

Data is shifted in the MSB first. The data sent to the MAX2820/MAX2821, in 16-bit words, is framed by CSB. When CSB is low, the clock is active and data is shifted with the rising edge of the clock. When CSB transitions to high, the shift register is latched into the register selected by the contents of the address bits. Only the last 16 bits shifted into the MAX2820/MAX2821 are retained in the shift register. No check is made on the number of clock pulses. Figure 1 documents the serial interface timing for the MAX2820/MAX2821.

Power-Up Default States

The MAX2820/MAX2821 provide power-up loading of default states for each of the registers. The states are loaded on a VCC_DIG supply voltage transition from 0V to VCC. The default values are retained until reprogrammed through the serial interface or the power supply voltage is taken to 0V. The default state of each

register is described in Table 3. **Note:** Putting the IC in shutdown mode does not change the contents of the programming registers.

Block-Enable Register

The block-enable register permits individual control of the enable state for each major circuit block in the MAX2820/MAX2821. The actual enable condition of the circuit block is a logical function of the block-enable bit setting and other control input states. Table 4 documents the logical definition of state for each major circuit block.

Synthesizer Register

The synthesizer register (SYNTH) controls the reference frequency divider and charge-pump current of the PLL. See Table 5 for a description of the bit settings.

Channel Frequency Register

The channel frequency register (CHANNEL) sets the RF carrier frequency for the MAX2820/MAX2821. The channel is programmed as a number from 0 to 99. The actual frequency is 2400 + channel in MHz. The default setting is 37 for 2437MHz. See Table 6 for a description of the bit settings.

Receiver Settings Register

The receive settings register (RECEIVE) controls the receive filter -3dB corner frequency, RX level detector midpoint, and VGA DC offset nulling parameters. The defaults are intended to provide proper operation. However, the filter frequency and detector can be modified if desired. Do not reprogram VGA DC offset nulling parameters. These settings were optimized during development. See Table 7 for a description of the bit settings.

Transmitter Settings Register

The transmitter settings register (TRANSMIT) controls the 4-bit PA bias DAC. The 4 bits correspond to a PA bias current between 0 and full scale (~300µA). See Table 8 for the bit settings.

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Table 3. Register Power-Up Default States

| REGISTER | ADDRESS | DEFAULT | FUNCTION |
|----------|---------|--------------|--|
| ENABLE | 0001 | 000000011110 | Block-Enable Control Settings (E) |
| SYNTH | 0010 | 000001000000 | Synthesizer Settings: <ul style="list-style-type: none"> • Reference frequency (R) • Charge-pump current (ICP) • PLL phase detector (PD) |
| CHANNEL | 0011 | 000000100101 | Channel frequency settings (CF) |
| RECEIVE | 0100 | 111111010010 | Receiver Settings: <ul style="list-style-type: none"> • VGA DC offset nulling parameter 1 (1C) • VGA DC offset nulling parameter 2 (2C) • -3dB lowpass filter bandwidth (BW) • Detector midpoint level (DL) • Special function bit (SF) |
| TRANSMIT | 0101 | 000000000000 | Transmit Settings: <ul style="list-style-type: none"> • PA bias (PA) |

Table 4. Block-Enable Register (ENABLE)

| ADDRESS | DATA BIT | CONTENT | DEFAULT | DESCRIPTION AND LOGICAL DEFINITION |
|---------|----------|---------|---------|--|
| 0001 | D11 | E(11) | 0 | Reserved |
| | D10 | E(10) | 0 | PA Bias-Control Enable (PAB_EN) • PAB_EN = SHDNB • E(10) + TX_ON |
| | D9 | E(9) | 0 | Transmit Baseband Filters Enable (TXFLT_EN) • TXFLT_EN = SHDNB • E(9) + TX_ON |
| | D8 | E(8) | 0 | TX Upconverter + VGA + Driver Amp Enable (TXUVD_EN) • TXUVD_EN = SHDNB • E(8) + TX_ON |
| | D7 | E(7) | 0 | Receive Detector Enable (DET_EN) • DET_EN = SHDNB • E(7) + RX_ON |
| | D6 | E(6) | 0 | RX Downconverter + Filters + AGC Amps Enable (RXDFA_EN) • RXDFA_EN = SHDNB • E(6) + RX_ON |
| | D5 | E(5) | 0 | Receive LNA Enable (RXLNA_EN) • RXLNA_EN = SHDNB • E(5) + RX_ON |
| | D4 | E(4) | 1 | Autotuner Enable (AT_EN) • AT_EN = SHDNB • E(4) + RX_ON + TX_ON |
| | D3 | E(3) | 1 | PLL Charge-Pump Enable (CP_EN) • CP_EN = SHDNB • E(3) |
| | D2 | E(2) | 1 | PLL Enable (PLL_EN) • PLL_EN = SHDNB • E(2) |
| | D1 | E(1) | 1 | VCO Enable (VCO_EN) • VCO_EN = SHDNB • E(1) |
| | D0 | E(0) | 0 | Reserved |

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Table 5. Synthesizer Register (SYNTH)

| ADDRESS | DATA BIT | CONTENT | DEFAULT | DESCRIPTION |
|---------|----------|---------|---------|--|
| 0010 | D11:D8 | X | 0000 | Reserved |
| | D7 | PD | 0 | Phase-Detector Polarity Select <ul style="list-style-type: none"> 0 = No phase inversion 1 = Not permitted |
| | D6 | ICP | 1 | Charge-Pump Current Select <ul style="list-style-type: none"> 0 = ± 1mA charge-pump current 1 = ± 2mA charge-pump current |
| | D5:D0 | R(5:0) | 000000 | Reference Frequency Divider <ul style="list-style-type: none"> 000000 = 22MHz 000001 = 44MHz |

Table 6. Channel Frequency Block Register (CHANNEL)

| ADDRESS | DATA BIT | CONTENT | DEFAULT | DESCRIPTION |
|---------|----------|---------|---------|--|
| 0011 | D11:D7 | X | 00000 | Reserved |
| | D6:D0 | CF(6:0) | 0100101 | Channel Frequency Select: $f_{LO} = (2400 + CF(6:0))$ MHz <ul style="list-style-type: none"> 0000000 = 2400MHz 0000001 = 2401MHz 1100010 = 2498MHz 1100011 = 2499MHz |

Applications Information

Receive Path

LNA

The MAX2820/MAX2821 RX_RF inputs are high-impedance RF differential inputs AC-coupled on-chip to the LNA. The LNA inputs require external impedance matching and differential to single-ended conversion. The balanced to single-ended conversion and interface to 50Ω is achieved through the use of an off-chip 2:1 balun transformer, such as the small surface-mount baluns offered by Murata and Toko. In the case of the 2:1 balun, the RX RF input must be impedance-matched to a differential/balanced impedance of 100Ω . A simple LC network is sufficient to impedance-match the LNA to the balun. The *Typical Application Circuit* shows the balun, inductors, and capacitors that constitute the matching network. Refer to the MAX2820/MAX2821 EV kit schematic for component values of the matching network.

The line lengths and parasitics have a noticeable impact on the matching element values in the board-level circuit. Some empirical adjustment of LC component values is likely. Balanced line layout on the differential input traces is essential to maintaining good IP2 performance and RF common-mode noise rejection.

The MAX2820/MAX2821 have two LNA gain modes that are digitally controlled by the logic signal applied to RF_GAIN. RF_GAIN high enables the high-gain mode, and RF_GAIN low enables the low-gain mode. The LNA gain step is nominally 30dB. In most applications, RF_GAIN is connected directly to a CMOS output of the baseband IC, and the baseband IC controls the state of the LNA gain based on the detected signal amplitude.

Receiver Baseband Lowpass Filtering

The MAX2820/MAX2821 on-chip receive lowpass filters provide the steep filtering necessary to attenuate the out-of-band (> 11 MHz) interfering signals to sufficiently low levels to preserve receiver sensitivity. The filter frequency response is precisely controlled on-chip and does not require user adjustment. However, a provision is made to permit the -3dB corner frequency and entire response to be slightly shifted up or down in frequency. This is intended to offer some flexibility in trading off adjacent channel rejection vs. passband distortion. The filter -3dB frequency is programmed through the serial interface. The specific bit setting vs. -3dB frequency is shown in Table 7. The typical receive baseband filter gain vs. frequency profile is shown in the *Typical Operating Characteristics*.

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Table 7. Receive Settings Register (RECEIVE)

| ADDRESS | DATA BIT | CONTENT | DEFAULT | DESCRIPTION |
|---------|----------|---------|---------|---|
| 0100 | D11:D9 | 2C(2:0) | 111 | VGA DC Offset Nulling Parameter 2 |
| | D8:D6 | 1C(2:0) | 111 | VGA DC Offset Nulling Parameter 1 |
| | D5:D4 | DL(1:0) | 01 | RX Level Detector Midpoint Select <ul style="list-style-type: none"> • 11 = 01 = 50.2mVp • 10 = 70.9mVp • 00 = 35.5mVp |
| | D3 | SF(0) | 0 | Special Function Select (not presently used) <ul style="list-style-type: none"> • 0 = OFF • 1 = ON |
| | D2:D0 | BW(2:0) | 010 | Receive Filter -3dB Frequency Select (frequencies are approximate) <ul style="list-style-type: none"> • 000 = 8.5MHz • 001 = 8.0MHz • 010 = 7.5MHz • 011 = 7.0MHz • 100 = 6.5MHz • 101 = 6.0MHz |

Table 8. Transmit Settings Register (TRANSMIT)

| ADDRESS | DATA BIT | CONTENT | DEFAULT | DESCRIPTION |
|---------|----------|---------|---------|--|
| 0101 | D11:D4 | X | X | Reserved |
| | D3:D0 | PA(3:0) | 0000 | PA Bias Select: <ul style="list-style-type: none"> • 1111 = Highest PA bias • • 0000 = Lowest PA bias |

Receive Gain Control and DC Offset Nulling

The MAX2820/MAX2821 receive path gain is varied through an external voltage applied to the pin RX_AGC. Maximum gain is at $V_{RX_AGC} = 0V$ and minimum gain is at $V_{RX_AGC} = 2V$. The RX_AGC input is a high-impedance analog input designed for direct connection to the RX_AGC DAC output of the baseband IC. The gain-control range, which is continuously variable, is typically 70dB. The gain-control characteristic is shown in the *Typical Operating Characteristics* section graph Receiver Voltage Gain vs. Gain-Control Voltage.

Some local noise filtering through a simple RC network at the input is permissible. However, the time constant of this network should be kept sufficiently low in order not to limit the desired response time of the RX gain-control function.

Receiver Baseband Amplifier Outputs

The MAX2820/MAX2821 receiver baseband outputs (RX_BBIP, RX_BBIN, RX_BBQP, and RX_BBQN) are differential low-impedance buffer outputs. The outputs

are designed to be directly connected (DC-coupled) to the in-phase (I) and quadrature-phase (Q) ADC inputs of the baseband IC. The RX I/Q outputs are internally biased to +1.2V common-mode voltage. The outputs are capable of driving loads up to $5k\Omega \parallel 5pF$ with the full bandwidth baseband signals at a differential amplitude of 500mVp-p.

Proper board layout is essential to maintain good balance between I/Q traces. This provides good quadrature phase accuracy.

Receiver Power Detector

The MAX2820/MAX2821 receiver level detector is a digital output from an internal threshold detector that is used to determine when to change the LNA gain state. In most applications, it is connected directly to a comparator input of the baseband IC. The threshold level can be programmed through the MAX2820/MAX2821 control software.

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Transmit Path

Transmitter Baseband Inputs

The MAX2820/MAX2821 transmitter baseband inputs (TX_BBIP, TX_BBIN, TX_BBQP, and TX_BBQN) are high-impedance differential analog inputs. The inputs are designed to be directly connected (DC-coupled) to the in-phase (I) and quadrature-phase (Q) DAC outputs of the baseband IC. The inputs must be externally biased to +1.2V common-mode voltage. Typically, the DAC outputs are current outputs with external resistor loads to ground. I and Q are nominally driven by a 400mV_{P-P} differential baseband signal.

Proper board layout is essential to maintain good balance between I/Q traces. This provides good quadrature phase accuracy by maintaining equal parasitic capacitance on the lines. In addition, it is important not to expose the TX I/Q circuit board traces going from the digital baseband IC to the MAX2820/MAX2821. The lines should be shielded on an inner layer to prevent coupling of RF to these TX I/Q inputs and possible envelope demodulation of the RF signal.

Transmit Path Baseband Lowpass Filtering

The MAX2820/MAX2821 on-chip transmit lowpass filters provide the filtering necessary to attenuate the unwanted higher-frequency spurious signal content that arises from the DAC clock feedthrough and sampling images. In addition, the filter provides additional attenuation of the second sidelobe of signal spectrum. The filter frequency response is set on-chip. No user adjustment or programming is required. The Typical Gain vs. Frequency profile is shown in the *Typical Operating Characteristics*.

Transmitter DC Offset Calibration

In a zero-IF system, in order to achieve low LO leakage at the RF output, the DC offset of the TX baseband signal path must be reduced to as near zero as possible. Given that the amplifier stages, baseband filters, and TX DAC possesses some finite DC offset that is too large for the required LO leakage specification, it is necessary to “null” the DC offset. The MAX2820/MAX2821 accomplish this through an on-chip calibration sequence. During this sequence, the net TX baseband signal path offsets are sampled and cancelled in the baseband amplifiers. This calibration occurs in the first ~2.2μs after TX_ON is taken high. During this time, it is essential that the TX DAC output is in the 0V differential state. The calibration corrects for any DAC offset. However, if the DAC is set to a value other than the 0V state, then an offset is erroneously sampled by the MAX2820/MAX2821 TX offset calibration. The TX DAC output must be put into the 0V differential state at or before the time TX_ON is taken high.

Power Amplifier Driver Output

The MAX2820/MAX2821 TX_RF outputs are high-impedance RF differential outputs directly connected to the driver amplifier. The outputs are essentially open-collector outputs with an on-chip inductor choke connected to VCC_DRVR. The power amplifier driver outputs require external impedance matching and differential to single-ended conversion. The balanced to single-ended conversion and interface to 50Ω is achieved through the use of an off-chip 4:1 balun transformer, such as one from Murata or Toko. In this case, the TX RF output must be impedance-matched to a differential/balanced impedance of 200Ω. The *Typical Application Circuit* shows the balun, inductors, and capacitors that constitute the matching network of the power amplifier driver outputs. The output match should be adjusted until the return loss at the balun output is > 10dB.

Transmit Gain Control

The transmit gain-control input provides a direct analog control over the transmit path gain. The transmit gain of the MAX2820/MAX2821 is controlled by an external voltage at pin TX_GC. The typical gain-control characteristic is provided in the *Typical Operating Characteristics* graph Transmitter Gain Control vs. Gain-Control Voltage. The input is a high-impedance analog input designed to directly connect to the DAC output of the baseband IC. Some local noise filtering through a simple RC network at the input is permissible. However, the time constant of this network should be kept sufficiently low so the desired response time of the TX gain-control function is not limited.

During the TX turn-on sequence, internally the gain is set at the minimum while the TX baseband offset calibration is taking place. The RF output is effectively “blanked” for the first 2.2μs after TX_ON is taken high. After 2.2μs, the “blanking” is released, and the gain-control amplifier ramps to the gain set by the external voltage applied to the TX_GC input.

PA Bias DAC Output

The MAX2820/MAX2821 provide a programmable analog current source output for use in biasing the RF power amplifier, such as the MAX2242. The output is essentially an open-drain output of a current source DAC. The output is designed to directly connect to the bias current pin on the power amplifier. The value of the current is determined by the 4 bits programmed into the internal register on the MAX2820/MAX2821. This programmability permits optimizing of the power amplifier idle current based on the output power level of the PA. Care must be taken in the layout of this line. Avoid running the line in parallel with the RF line. RF might couple

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onto the line, given the high impedance of the output. This might result in rectified RF, altering the value of the bias current and causing erratic PA operation.

Synthesizer

Channel Frequency and Reference Frequency

The synthesizer/PLL channel frequency and reference settings establish the divider/counter settings in the integer-N synthesizer of the MAX2820/MAX2821. Both the channel frequency and reference oscillator frequency are programmable through the serial interface. The channel frequency is programmed as a channel number 0 to 99 to set the carrier frequency to 2400MHz to 2499MHz (LO frequency = channel + 2400). The reference frequency is programmable to 22MHz or 44MHz. These settings are intended to cover only the required 802.11b channel spacing and the two possible crystal oscillator options used in the radios.

Reference Oscillator Input

The reference oscillator inputs ROSCP and ROSCN are high-impedance analog inputs. They are designed to be connected to the reference oscillator output through a coupling capacitor. The input amplitude can range from 200mV_{p-p} to 500mV_{p-p}; therefore, in the case of a reference oscillator with a CMOS output, the signal must be attenuated before being applied to the ROSC inputs. The signal can be attenuated with a resistor- or capacitor-divider network.

Reference Voltage Output

A voltage reference output is provided from pin 2, VREF, for use with certain baseband ICs. The nominal output voltage is 1.2V. The reference voltage is first-order compensated over temperature to provide a reasonably low drift output, 1.1V to 1.3V over temperature, under load conditions. The output stage is designed to drive 2mA loads with up to 20pF of load capacitance. The VREF output is designed to directly connect to the baseband reference input.

Loop Filter

The PLL uses a classical charge pump into an external loop filter (C-RC) in which the filter output connects to the voltage tuning input of the VCO. This simple third-order lowpass loop filter closes the loop around the synthesizer. The Typical Application Circuit shows the loop filter elements around the MAX2820/MAX2821. The capacitor and resistor values are set to provide the loop bandwidth required to achieve the desired lock time while also maintaining loop stability. Refer to the MAX2820/MAX2821 EV kit schematic for component values. A 45kHz loop bandwidth is recommended to ensure that the loop settles quickly enough to achieve 5μs TX turnaround time and 10μs RX turnaround time. This is the loop filter on the EV kit. Narrowing the loop bandwidth increases the settling time and results in unacceptable TX-RX turnaround time performance.

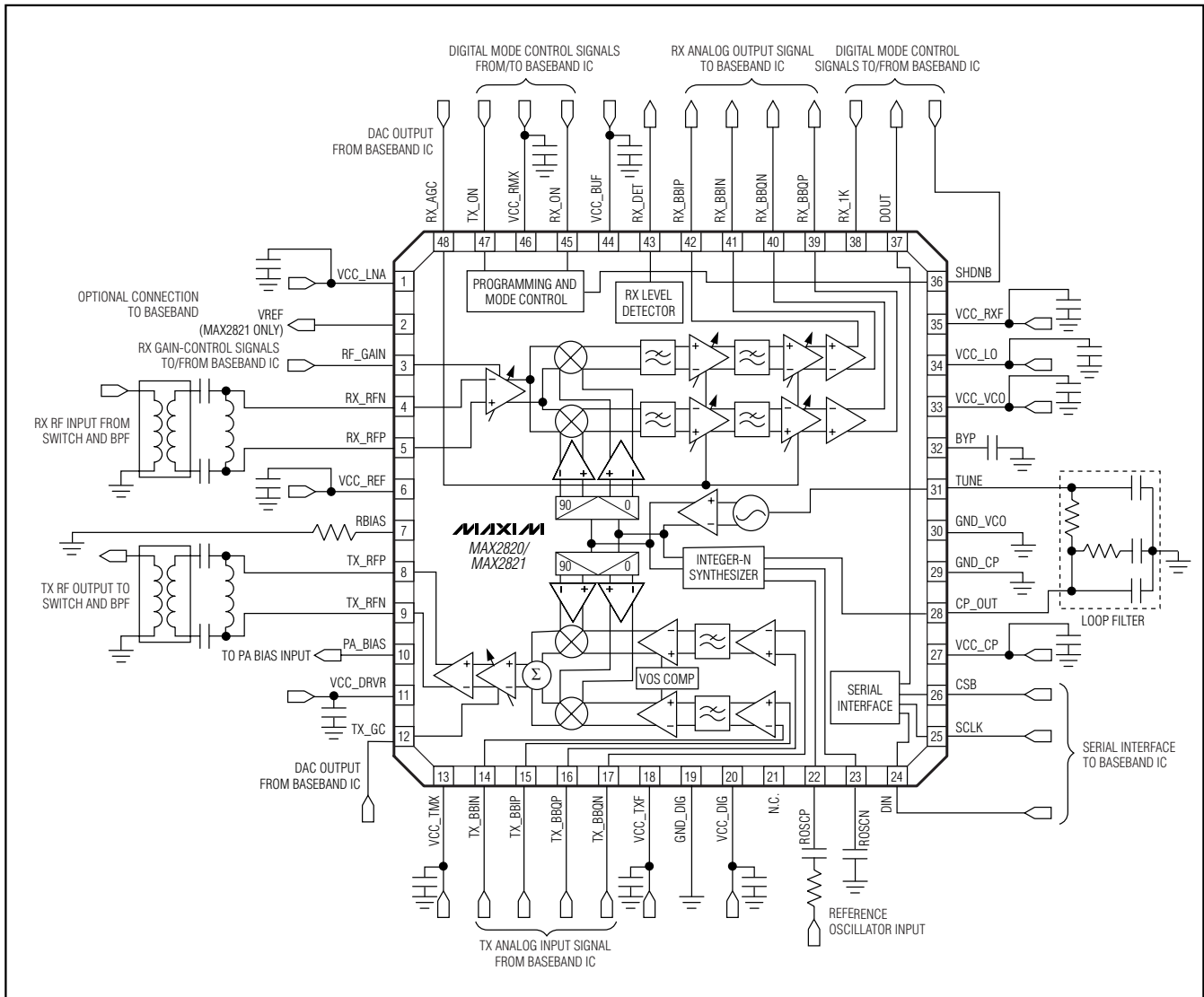
Chip Information

TRANSISTOR COUNT: 13,607

MAX2820/MAX2821

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Typical Application Circuit

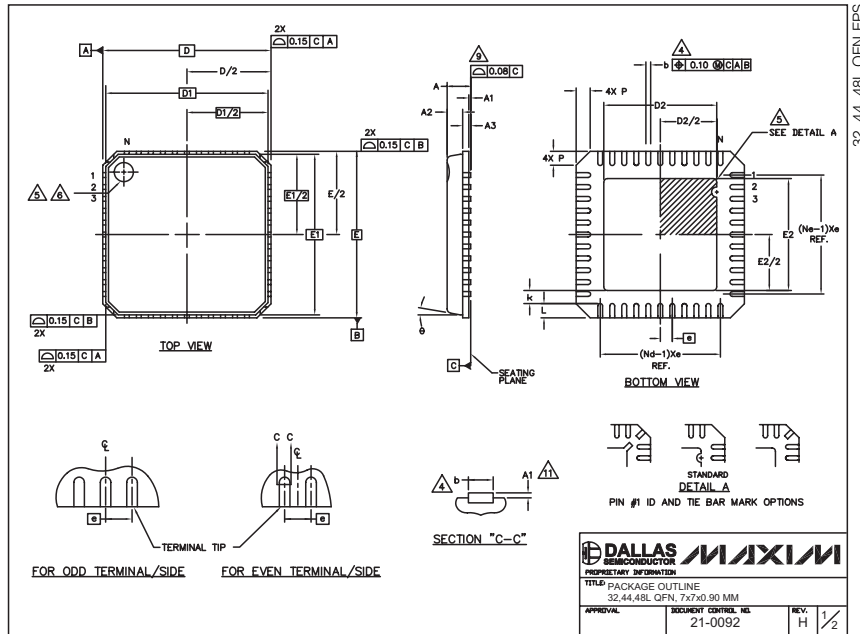


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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX2820/MAX2821



| COMMON DIMENSIONS | | | | | | | | | |
|-------------------|----------|------|------|----------|------|------|----------|------|------|
| PKG | 32L 7x7 | | | 44L 7x7 | | | 48L 7x7 | | |
| | MIN. | NDM. | MAX. | MIN. | NDM. | MAX. | MIN. | NDM. | MAX. |
| A | 0.80 | 0.90 | 1.00 | 0.80 | 0.90 | 1.00 | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.01 | 0.05 | 0.00 | 0.01 | 0.05 | 0.00 | 0.01 | 0.05 |
| A2 | 0.00 | 0.65 | 1.00 | 0.00 | 0.65 | 1.00 | 0.00 | 0.65 | 1.00 |
| A3 | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | |
| b | 0.23 | 0.28 | 0.35 | 0.18 | 0.23 | 0.30 | 0.18 | 0.23 | 0.30 |
| D | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 |
| D1 | 6.75 BSC | | | 6.75 BSC | | | 6.75 BSC | | |
| E | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 | 6.90 | 7.00 | 7.10 |
| E1 | 6.75 BSC | | | 6.75 BSC | | | 6.75 BSC | | |
| e | 0.65 BSC | | | 0.50 BSC | | | 0.50 BSC | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - |
| L | 0.35 | 0.55 | 0.75 | 0.35 | 0.55 | 0.75 | 0.30 | 0.40 | 0.50 |
| N | 32 | | | 44 | | | 48 | | |
| Nd | 8 | | | 11 | | | 12 | | |
| Ne | 8 | | | 11 | | | 12 | | |
| P | 0.00 | 0.42 | 0.60 | 0.00 | 0.42 | 0.60 | 0.00 | 0.42 | 0.60 |
| U | 0" | | | 12" | | | 0" | | |

| PKG. CODES | D2 | | | E2 | | |
|------------|------|------|------|------|------|------|
| | MIN. | NDM. | MAX. | MIN. | NDM. | MAX. |
| G3277-2 | 4.55 | 4.70 | 4.85 | 4.55 | 4.70 | 4.85 |
| G4477-1 | 3.65 | 3.80 | 3.95 | 3.65 | 3.80 | 3.95 |
| G4477-2 | 4.55 | 4.70 | 4.85 | 4.55 | 4.70 | 4.85 |
| G4477-3 | 3.15 | 3.30 | 3.45 | 3.15 | 3.30 | 3.45 |
| G4877-1 | 4.95 | 5.10 | 5.25 | 4.95 | 5.10 | 5.25 |
| G4877-2 | 5.45 | 5.60 | 5.75 | 5.45 | 5.60 | 5.75 |

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M, - 1994.
3. N IS THE NUMBER OF TERMINALS.
4. Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
5. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
7. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
8. ALL DIMENSIONS ARE IN MILLIMETERS.
9. PACKAGE WARPAGE MAX 0.08mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
11. MEETS JEDEC MO220 EXCEPT DIMENSION "b" MINIMUM.
12. APPLY ONLY FOR TERMINAL.
13. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION(STEPPED SIDES).

DALLAS SEMICONDUCTOR
MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
32,44,48L QFN, 7x7x0.90 MM
APPROVAL: _____ DOCUMENT CONTROL: 21-0092 REV: H 1/2

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