

Freescale Semiconductor

Technical Data

MC100ES6039
Rev 2, 06/2005

3.3 V ECL/PECL/HSTL/LVDS $\div 2/4$, $\div 4/6$ Clock Generation Chip

The MC100ES6039 is a low skew $\div 2/4$, $\div 4/6$ clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, LVPECL input signals. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device.

The common enable (EN) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple ES6039s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one ES6039, the MR pin need not be exercised as the internal divider design ensures synchronization between the $\div 2/4$ and the $\div 4/6$ outputs of a single device. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation.

The 100ES Series contains temperature compensation.

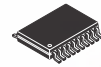
Features

- Maximum Frequency >1.0 GHz Typical
- 50 ps Output-to-Output Skew
- PECL Mode Operating Range: $V_{CC} = 3.135$ V to 3.8 V with $V_{EE} = 0$ V
- ECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -3.135$ V to -3.8 V
- Open Input Default State
- Synchronous Enable/Disable
- Master Reset for Synchronization of Multiple Chips
- V_{BB} Output
- LVDS and HSTL Input Compatible
- 20-Lead Pb-Free Package Available

MC100ES6039



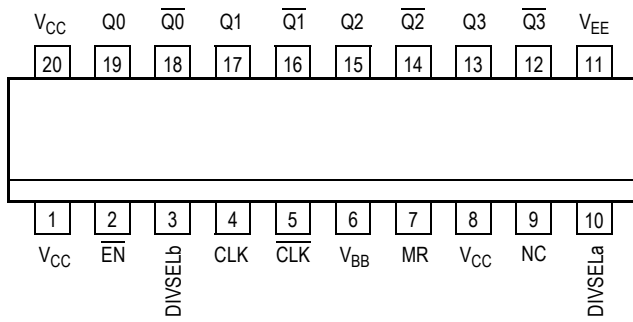
DW SUFFIX
20-LEAD SOIC PACKAGE
CASE 751D-07



EG SUFFIX
20-LEAD TSSOP PACKAGE
Pb-FREE PACKAGE
CASE 751D-07

ORDERING INFORMATION

| Device | Package |
|-----------------|-----------------|
| MC100ES6039DW | SO-20 |
| MC100ES6039DWR2 | SO-20 |
| MC100ES6039EG | SO-20 (Pb-Free) |
| MC100ES6039EGR2 | SO-20 (Pb-Free) |



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View)

Table 1. Pin Description

| Pin | Function |
|--|-----------------------------------|
| $CLK^{(1)}$, $\overline{CLK}^{(1)}$ | ECL Diff Clock Inputs |
| $\overline{EN}^{(1)}$ | ECL Sync Enable |
| $MR^{(1)}$ | ECL Master Reset |
| V_{BB} | ECL Reference Output |
| $Q0, Q1, \overline{Q0}, \overline{Q1}$ | ECL Diff $\div 2/4$ Outputs |
| $Q2, Q3, \overline{Q2}, \overline{Q3}$ | ECL Diff $\div 4/6$ Outputs |
| $DIVSELa^{(1)}$ | ECL Freq. Select Input $\div 2/4$ |
| $DIVSELb^{(1)}$ | ECL Freq. Select Input $\div 4/6$ |
| V_{CC} | ECL Positive Supply |
| V_{EE} | ECL Negative Supply |
| NC | No Connect |

1. Pins will default low when left open.

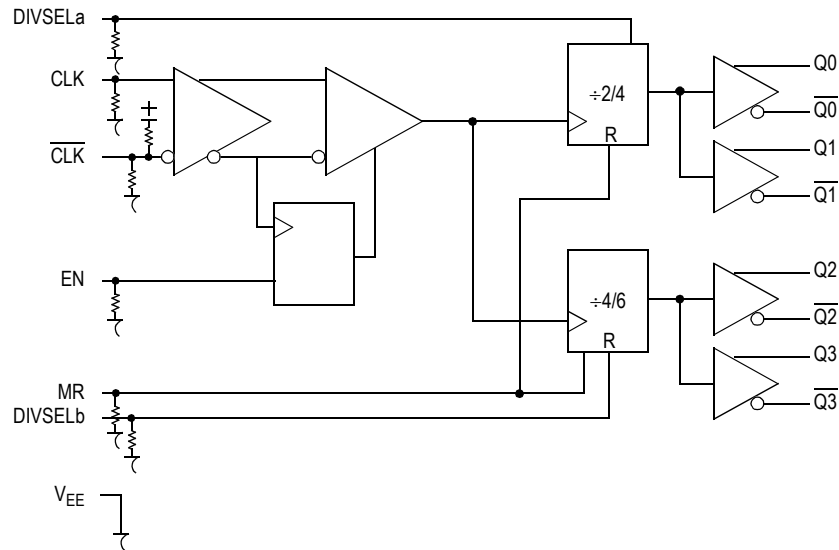


Figure 2. Logic Diagram

Table 2. Function Tables

| CLK | EN | MR | Function |
|-----|----|----|------------|
| Z | L | L | Divide |
| ZZ | H | L | Hold Q0:3 |
| X | X | H | Reset Q0:3 |

X = Don't Care

Z = Low-to-High Transition

ZZ = High-to-Low Transition

| DIVSELa | Q0:1 Outputs |
|---------|--------------|
| L | Divide by 2 |
| H | Divide by 4 |
| DIVSELb | Q2:3 Outputs |
| L | Divide by 4 |
| H | Divide by 6 |

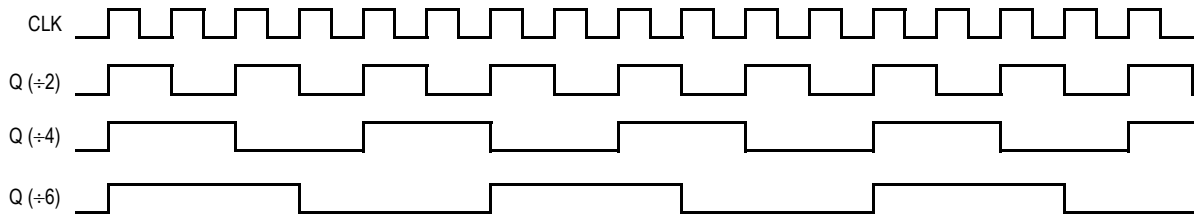


Figure 3. Timing Diagram

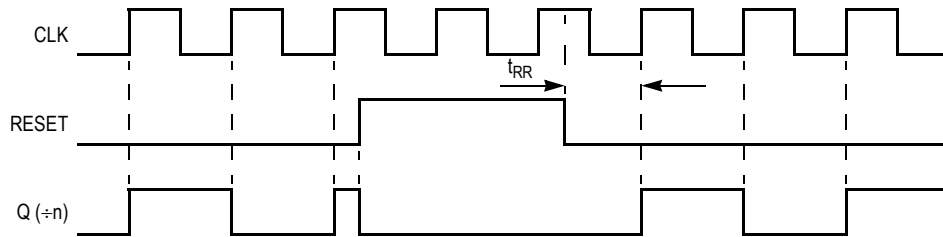


Figure 4. Timing Diagram

Table 3. Attributes

| Characteristics | | Value |
|----------------------------------|----------------------|---------------|
| Internal Input Pulldown Resistor | | 75 k Ω |
| Internal Input Pullup Resistor | | 75 k Ω |
| ESD Protection | Human Body Model | > 4 kV |
| | Machine Model | > 200 V |
| | Charged Device Model | > 2 kV |

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Maximum Ratings⁽¹⁾

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|---------------|---|--|--|-------------|--------------|
| V_{CC} | PECL Mode Power Supply | $V_{EE} = 0\text{ V}$ | | 3.9 | V |
| V_{EE} | ECL Mode Power Supply | $V_{CC} = 0\text{ V}$ | | -3.9 | V |
| V_I | PECL Mode Input Voltage ECL Mode Input Voltage | $V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$ | $V_I \leq V_{CC}$ $V_I \geq V_{EE}$ | 3.9 -3.9 | V V |
| I_{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| I_{BB} | V_{BB} Sink/Source | | | ± 0.5 | mA |
| T_A | Operating Temperature Range | | | -40 to +85 | °C |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 LFPM 500 LFPM | 20 SOIC 20 SOIC | TBD TBD | °C/W °C/W |

1. Maximum Ratings are those values beyond which device damage may occur.

Table 5. DC Characteristics ($V_{CC} = 0\text{ V}$, $V_{EE} = -3.8\text{ V}$ to -3.135 V or $V_{CC} = 3.135\text{ V}$ to 3.8 V , $V_{EE} = 0\text{ V}$)⁽¹⁾

| Symbol | Characteristic | -40°C | | | 0°C to 85°C | | | Unit |
|-----------|---|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 35 | 60 | | 35 | 60 | mA |
| V_{OH} | Output HIGH Voltage ⁽²⁾ | $V_{CC} - 1150$ | $V_{CC} - 1020$ | $V_{CC} - 800$ | $V_{CC} - 1200$ | $V_{CC} - 970$ | $V_{CC} - 750$ | mV |
| V_{OL} | Output LOW Voltage ⁽²⁾ | $V_{CC} - 1950$ | $V_{CC} - 1620$ | $V_{CC} - 1250$ | $V_{CC} - 2000$ | $V_{CC} - 1680$ | $V_{CC} - 1300$ | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | $V_{CC} - 1165$ | | $V_{CC} - 880$ | $V_{CC} - 1165$ | | $V_{CC} - 880$ | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | $V_{CC} - 1810$ | | $V_{CC} - 1475$ | $V_{CC} - 1810$ | | $V_{CC} - 1475$ | mV |
| V_{BB} | Output Reference Voltage | $V_{CC} - 1400$ | | $V_{CC} - 1200$ | $V_{CC} - 1400$ | | $V_{CC} - 1200$ | mV |
| V_{PP} | Differential Input Voltage ⁽³⁾ | 0.12 | | 1.4 | 0.12 | | 1.4 | V |
| V_{CMR} | Differential Cross Point Voltage ⁽⁴⁾ | $V_{EE} + 0.2$ | | $V_{CC} - 0.7$ | $V_{EE} + 0.2$ | | $V_{CC} - 0.7$ | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | μA |

- MC100ES6139 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.
- All loading with $50\ \Omega$ to $V_{CC} - 2.0$ volts.
- V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
- V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC Characteristics ($V_{CC} = 0\text{ V}$, $V_{EE} = -3.8\text{ V}$ to -3.135 V or $V_{CC} = 3.135\text{ V}$ to 3.8 V , $V_{EE} = 0\text{ V}$)⁽¹⁾

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------|---|--------------|-----|--------------|--------------|-----|--------------|--------------|-----|--------------|----------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{\max} | Maximum Frequency | | > 1 | | | > 1 | | | > 1 | | GHz |
| t_{PLH} , t_{PHL} | Propagation Delay CLK, Q (Diff) MR, Q | 575 500 | | 875 850 | 575 500 | | 875 850 | 575 500 | | 875 850 | ps ps |
| t_{RR} | Reset Recovery | 200 | 100 | | 200 | 100 | | 200 | 100 | | ps |
| t_s | Setup Time \overline{EN} , CLK DIVSEL, CLK | 200 | 120 | | 200 | 120 | | 200 | 120 | | ps |
| | | 400 | 180 | | 400 | 180 | | 400 | 180 | | ps |
| t_h | Hold Time CLK, \overline{EN} CLK, DIVSEL | 100 | 50 | | 100 | 50 | | 100 | 50 | | ps |
| | | 200 | 140 | | 200 | 140 | | 200 | 140 | | ps |
| t_{PW} | Minimum Pulse Width MR | 550 | 450 | | 550 | 450 | | 550 | 450 | | ps |
| t_{SKEW} | Within Device Skew Q, \overline{Q} Q, \overline{Q} @ Same Frequency Device-to-Device Skew ⁽²⁾ | | | 80 | | | 80 | | | 80 | ps |
| | | | | 50 | | | 50 | | | 50 | ps |
| | | | | 300 | | | 300 | | | 300 | ps |
| t_{JITTER} | Cycle-to-Cycle Jitter (RMS 1σ) | | | 1 | | | 1 | | | 1 | ps |
| V_{PP} | Input Voltage Swing (Differential) | 150 | | 1400 | 150 | | 1400 | 150 | | 1400 | mV |
| V_{CMR} | Differential Cross Point Voltage | $V_{EE}+0.2$ | | $V_{CC}-1.1$ | $V_{EE}+0.2$ | | $V_{CC}-1.1$ | $V_{EE}+0.2$ | | $V_{CC}-1.1$ | V |
| t_r , t_f | Output Rise/Fall Times (20% – 80%) Q, \overline{Q} | 50 | | 300 | 50 | | 300 | 50 | | 300 | ps |

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

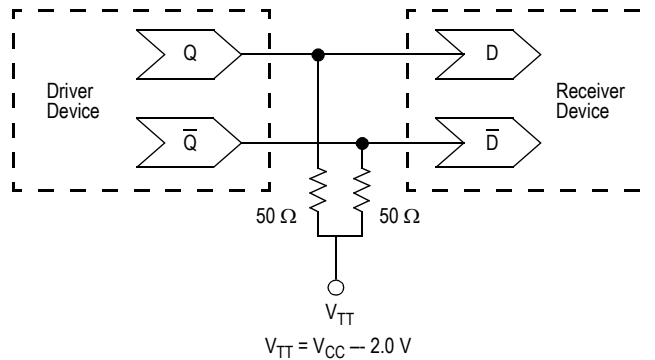
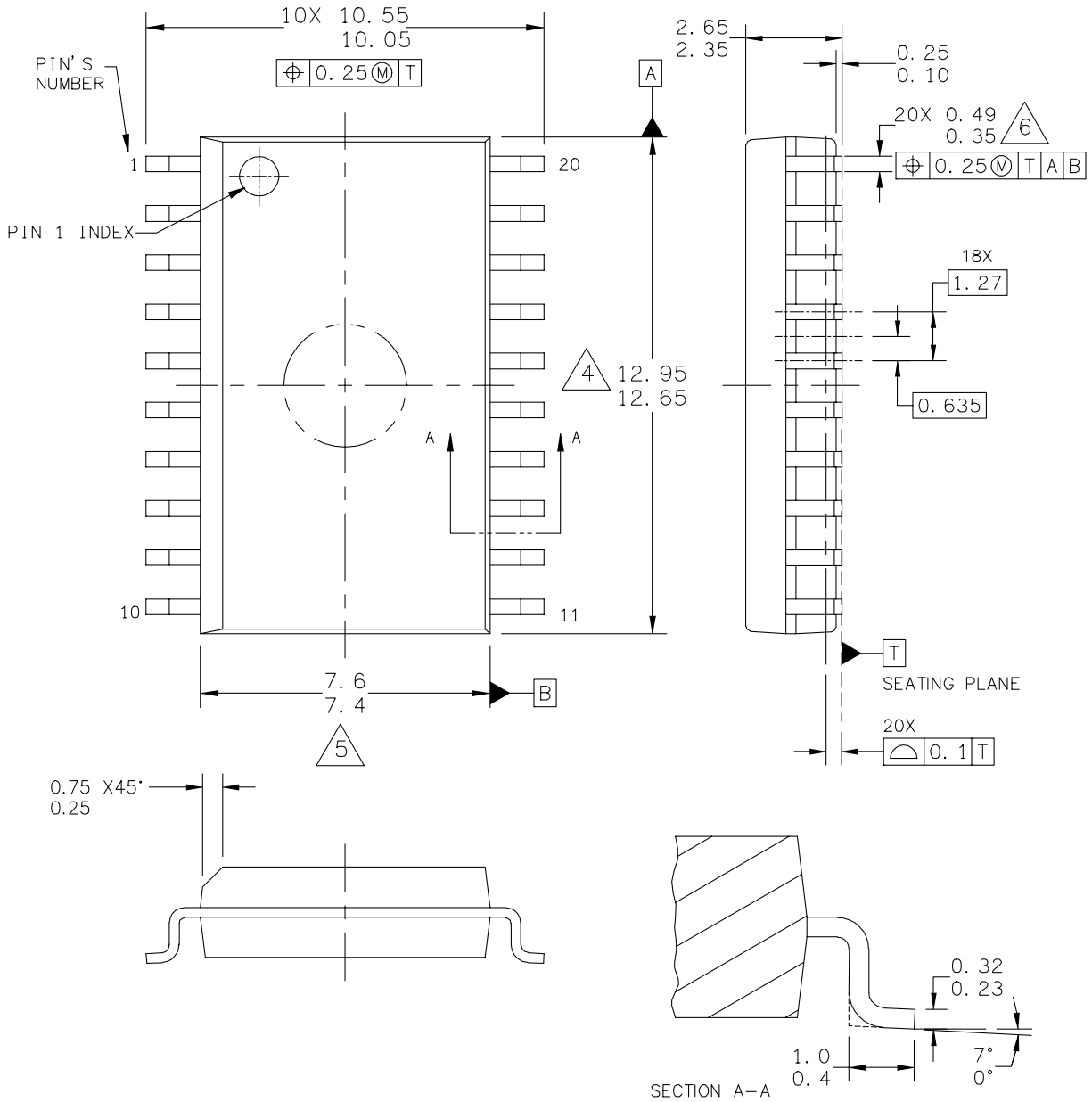


Figure 5. Typical Termination for Output Driver and Device Evaluation

PACKAGE DIMENSIONS



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| | CASE NUMBER: 751D-07 | 23 MAR 2005 |
| | STANDARD: JEDEC MS-013AC | |

**CASE 751D-07
ISSUE J
20-LEAD SOIC PACKAGE**

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

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PAGE 2 OF 2

CASE 751D-07
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20-LEAD SOIC PACKAGE

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