

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS
M37733EHBXXXFP
M37733EHBFS

PROM VERSION OF M37733MHBXXXFP

DESCRIPTION

The M37733EHBXXXFP is a single-chip microcomputer using the 7700 Family core. This single-chip microcomputer has a CPU and a bus interface unit. The CPU is a 16-bit parallel processor that can be an 8-bit parallel processor, and the bus interface unit enhances the memory access efficiency to execute instructions fast. This microcomputer also includes a 32 kHz oscillation circuit, in addition to the PROM, RAM, multiple-function timers, serial I/O, A-D converter, and so on.

The M37733EHBXXXFP has the same function as the M37733MHBXXXFP except that the built-in ROM is PROM. (Refer to the basic function blocks description.) For program development, the M37733EHBFS with erasable ROM that is housed in a windowed ceramic LCC is also provided.

FEATURES

- Number of basic instructions 103
- Memory size PROM 124 Kbytes
RAM 3968 bytes
- Instruction execution time
The fastest instruction at 25 MHz frequency 160 ns

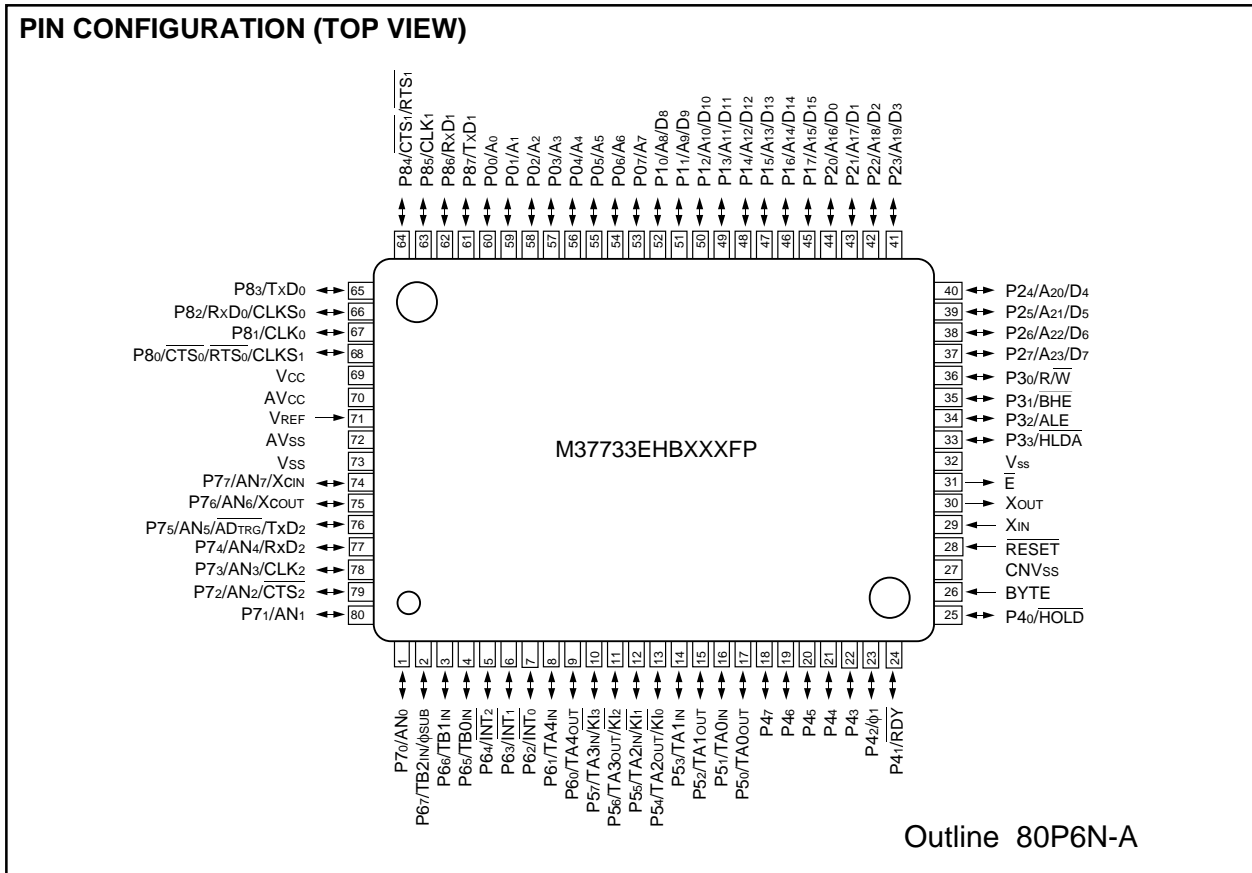
- Single power supply 5 V ± 10%
- Low power dissipation (at 25 MHz frequency) 47.5 mW (Typ.)
- Interrupts 19 types, 7 levels
- Multiple-function 16-bit timer 5 + 3
- Serial I/O (UART or clock synchronous) 3
- 10-bit A-D converter 8-channel inputs
- Watchdog timer
- Programmable input/output (ports P0, P1, P2, P3, P4, P5, P6, P7, P8) 68
- Clock generating circuit 2 circuits built-in

APPLICATION

Control devices for general commercial equipment such as office automation, office equipment, and so on.

Control devices for general industrial equipment such as communication equipment, and so on.

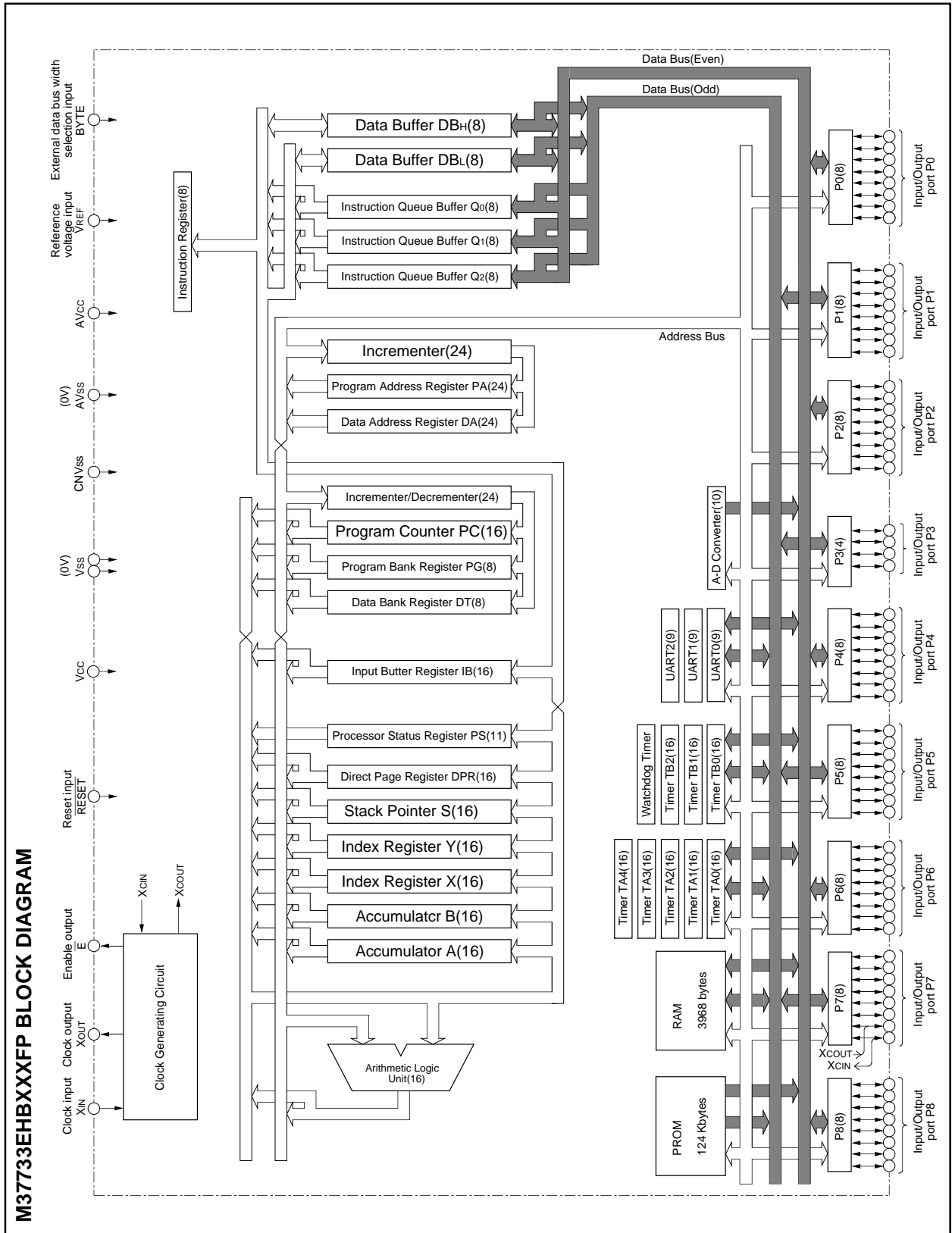
Note. Do not use the windowed EPROM version for mass production, because it is a tool for program development (for evaluation).



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FUNCTIONS OF M37733EHBXXXFP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		160 ns (the fastest instruction at external clock 25 MHz frequency)
Memory size	PROM	124 Kbytes
	RAM	3968 bytes
Input/Output ports	P0 – P2, P4 – P8	8-bit X 8
	P3	4-bit X 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit X 5
	TB0, TB1, TB2	16-bit X 3
Serial I/O		(UART or clock synchronous serial I/O) X 3
A-D converter		10-bit X 1 (8 channels)
Watchdog timer		12-bit X 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		5 V ± 10%
Power dissipation		47.5 mW (at external clock 25 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 16 Mbytes
Operating temperature range		–20 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package	M37733EHBXXXFP	80-pin plastic molded QFP (80P6N-A)
	M37733EHBFS	80-pin ceramic LCC (with a window) (80D0)

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PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 5 V \pm 10% to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.
RESET	Reset input	Input	When "L" level is applied to this pin, the microcomputer enters the reset state.
XIN	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between XIN and XOUT. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
E	Enable output	Output	This pin functions as the enable signal output pin which indicates the access status in the internal bus. When output level of E signal is "L", data/instruction read or data write is performed.
BYTE	External data bus width selection input	Input	In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
VREF	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
P00 – P07	I/O port P0	I/O	In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset. In the memory expansion mode or the microprocessor mode, these pins output address (A0 – A7).
P10 – P17	I/O port P1	I/O	In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data (D8 – D15) is input/output or an address (A8 – A15) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address (A8 – A15) is output.
P20 – P27	I/O port P2	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data (D0 – D7) is input/output or an address (A0 – A7) is output.
P30 – P33	I/O port P3	I/O	In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, R/W, BHE, ALE, and HLDA signals are output.
P40 – P47	I/O port P4	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, P40, P41, and P42 become HOLD and RDY input pins, and a clock ϕ_1 output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, P42 can be selected as an I/O port.
P50 – P57	I/O port P5	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3 and input pins for key input interrupt input (KI0 – KI3).
P60 – P67	I/O port P6	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input (INT0 – INT2) and input pins for timers B0 to B2. P67 also functions as sub-clock ϕ_{SUB} output pin.
P70 – P77	I/O port P7	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. P72 to P75 also function as I/O pins for UART2. Additionally, P76 and P77 have the function as the output pin (XCOUT) and the input pin (XCIN) of the sub-clock (32 kHz) oscillation circuit, respectively. When P76 and P77 are used as the XCOUT and XCIN pins, connect a resonator or an oscillator between the both.
P80 – P87	I/O port P8	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.

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PIN DESCRIPTION (EPROM MODE)

Pin	Name	Input/Output	Functions
VCC, VSS	Power supply		Supply 5V±10% to VCC and 0V to VSS.
CNVSS	VPP input	Input	Connect to VPP when programming or verifying.
BYTE	VPP input	Input	Connect to VPP when programming or verifying.
RESET	Reset input	Input	Connect to VSS.
XIN	Clock input	Input	Connect a ceramic resonator between XIN and XOUT.
XOUT	Clock output	Output	
E	Enable output	Output	Keep open.
AVCC, AVSS	Analog supply input		Connect AVCC to VCC and AVSS to VSS.
VREF	Reference voltage input	Input	Connect to VSS.
P00 – P07	Address input (A0 – A7)	Input	Port P0 functions as the lower 8 bits address input (A0 – A7).
P10 – P17	Address input (A8 – A15)	Input	Port P1 functions as the higher 8 bits address input (A8 – A15).
P20 – P27	Data I/O (D0 – D7)	I/O	Port P2 functions as the 8 bits data input/output (D0 – D7).
P30	Address input (A16)	Input	P30 functions as the most significant bit address input (A16).
P31 – P33	Input port P3	Input	Connect to VSS.
P40 – P47	Input port P4	Input	Connect to VSS.
P50 – P57	Control signal input	Input	P50, P51, and P52 function as PGM, OE, and CE input pins respectively. Connect P53, P54, P55, and P56 to VCC. Connect P57 to VSS.
P60 – P67	Input port P6	Input	Connect to VSS.
P70 – P77	Input port P7	Input	Connect to VSS.
P80 – P87	Input port P8	Input	Connect to VSS.

BASIC FUNCTION BLOCKS

The M37733EHBXXXFP has the same functions as the M37733MHBXXXFP except for the following:

- (1) The built-in ROM is PROM.
- (2) The status of bit 3 of the oscillation circuit control register 1 (address 6F16) at a reset is different.
- (3) The usage condition of bit 3 of the oscillation circuit control register 1 is different.

Accordingly, refer to the basic function blocks description in the M37733MHBXXXFP except for Figure 1 (bit configuration of the oscillation circuit control register 1) and Figure 3 (microcomputer internal status during reset).

In the M37733EHBXXXFP, bit 3 of the oscillation circuit control register 1 must be "1". (Refer to Figure 1.) The status of this bit at a reset is "1".

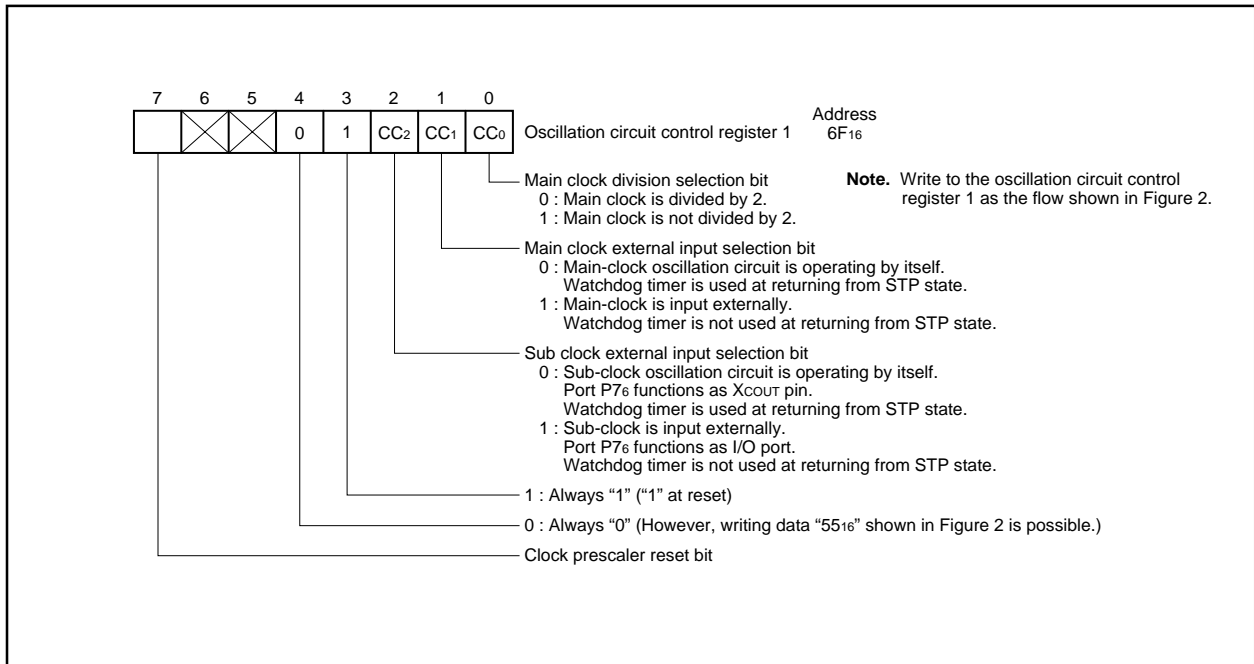


Fig. 1 Bit configuration of oscillation circuit control register 1 (corresponding to Figure 63 in data sheet "M37733MHBXXXFP")

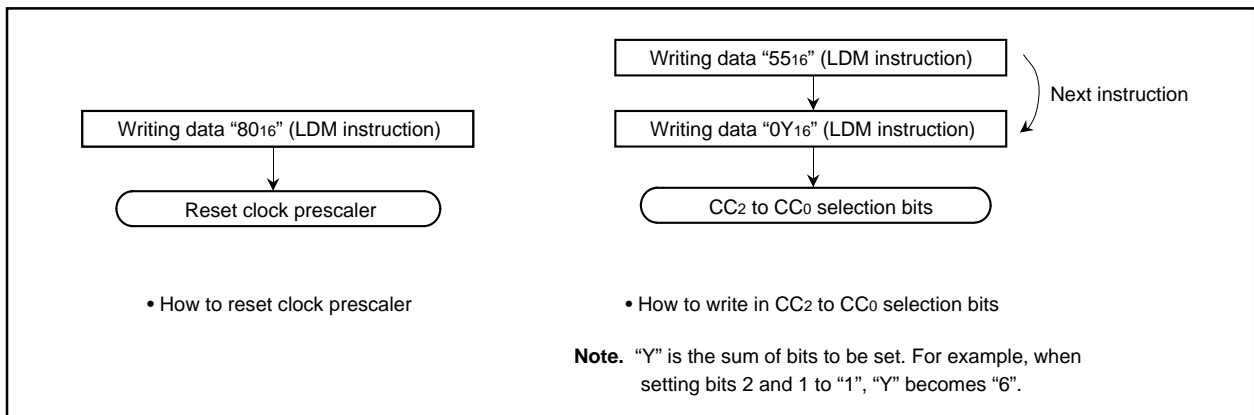


Fig. 2 How to write data in oscillation circuit control register 1 (identical with Figure 64 in data sheet "M37733MHBXXXFP")

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	Address		Address		
Port P0 direction register	(04 ₁₆)	00 ₁₆	Watchdog timer frequency selection flag	(61 ₁₆)	XXXXXXXXXX0
Port P1 direction register	(05 ₁₆)	00 ₁₆	Memory allocation control register	(63 ₁₆)	XXXXXXXX0000
Port P2 direction register	(08 ₁₆)	00 ₁₆	UART2 transmit/receive mode register	(64 ₁₆)	X0000000
Port P3 direction register	(09 ₁₆)	XXXXX000	UART2 transmit/receive control register 0	(68 ₁₆)	XXXXX1000
Port P4 direction register	(0C ₁₆)	00 ₁₆	UART2 transmit/receive control register 1	(69 ₁₆)	00000010
Port P5 direction register	(0D ₁₆)	00 ₁₆	Oscillation circuit control register 0	(6C ₁₆)	X00000X1
Port P6 direction register	(10 ₁₆)	00 ₁₆	Port function control register	(6D ₁₆)	00 ₁₆
Port P7 direction register	(11 ₁₆)	00 ₁₆	Serial transmit control register	(6E ₁₆)	XXXX00XXXX
Port P8 direction register	(14 ₁₆)	00 ₁₆	Oscillation circuit control register 1	(6F ₁₆)	0XXXX01000
A-D control register 0	(1E ₁₆)	00000???	A-D/UART2 trans./rece. interrupt control register	(70 ₁₆)	XXXXXX0000
A-D control register 1	(1F ₁₆)	XXXX00011	UART 0 transmission interrupt control register	(71 ₁₆)	XXXXXX0000
UART 0 transmit/receive mode register	(30 ₁₆)	00 ₁₆	UART 0 receive interrupt control register	(72 ₁₆)	XXXXXX0000
UART 1 transmit/receive mode register	(38 ₁₆)	00 ₁₆	UART 1 transmission interrupt control register	(73 ₁₆)	XXXXXX0000
UART 0 transmit/receive control register 0	(34 ₁₆)	00001000	UART 1 receive interrupt control register	(74 ₁₆)	XXXXXX0000
UART 1 transmit/receive control register 0	(3C ₁₆)	00001000	Timer A0 interrupt control register	(75 ₁₆)	XXXXXX0000
UART 0 transmit/receive control register 1	(35 ₁₆)	00000010	Timer A1 interrupt control register	(76 ₁₆)	XXXXXX0000
UART 1 transmit/receive control register 1	(3D ₁₆)	00000010	Timer A2 interrupt control register	(77 ₁₆)	XXXXXX0000
Count start flag	(40 ₁₆)	00 ₁₆	Timer A3 interrupt control register	(78 ₁₆)	XXXXXX0000
One-shot start flag	(42 ₁₆)	XXXX0000	Timer A4 interrupt control register	(79 ₁₆)	XXXXXX0000
Up-down flag	(44 ₁₆)	00 ₁₆	Timer B0 interrupt control register	(7A ₁₆)	XXXXXX0000
Timer A0 mode register	(56 ₁₆)	00 ₁₆	Timer B1 interrupt control register	(7B ₁₆)	XXXXXX0000
Timer A1 mode register	(57 ₁₆)	00 ₁₆	Timer B2 interrupt control register	(7C ₁₆)	XXXXXX0000
Timer A2 mode register	(58 ₁₆)	00 ₁₆	INT ₀ interrupt control register	(7D ₁₆)	XXXX000000
Timer A3 mode register	(59 ₁₆)	00 ₁₆	INT ₁ interrupt control register	(7E ₁₆)	XXXX000000
Timer A4 mode register	(5A ₁₆)	00 ₁₆	INT ₂ /Key input interrupt control register	(7F ₁₆)	XXXX000000
Timer B0 mode register	(5B ₁₆)	00100000	Processor status register (PS)		000??0001??
Timer B1 mode register	(5C ₁₆)	001X0000	Program bank register (PG)		00 ₁₆
Timer B2 mode register	(5D ₁₆)	001X0000	Program counter (PC _H)		Content of FFFF ₁₆
Processor mode register 0	(5E ₁₆)	00 ₁₆	Program counter (PC _L)		Content of FFFE ₁₆
Processor mode register 1	(5F ₁₆)	XXXXXXXXX0	Direct page register (DPR)		0000 ₁₆
Watchdog timer register	(60 ₁₆)	FFF ₁₆	Data bank register (DT)		00 ₁₆

Contents of other registers and RAM are undefined during reset. Initialize them by software.

Fig. 3 Microcomputer internal status during reset

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EPROM MODE

The M37733EHBXXXFP features an EPROM mode in addition to its normal modes. When the RESET signal level is "L", the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 4 shows the pin connections in the EPROM mode.

The EPROM mode is the 1M mode for the EPROM that is equivalent to the M5M27C101K.

When in the EPROM mode, ports P0, P1, P2, P30, P50, P51, P52, CNVss, and BYTE are used for the EPROM (equivalent to the

M5M27C101K).

When in this mode, the built-in PROM can be programmed or read from using these pins in the same way as with the M5M27C101K.

This chip does not have Device Identifier Mode, so that set the corresponding program algorithm. The program area should specify address 0100016 – 1FFFF16.

Connect the clock which is either ceramic resonator or external clock to XIN pin and XOUT pin.

Table 1 Pin function in EPROM mode

	M37733EHBXXXFP	M5M27C101K
Vcc	Vcc	Vcc
Vpp	CNVss, BYTE	Vpp
Vss	Vss	Vss
Address input	Ports P0, P1, P30	A0 – A16
Data I/O	Port P2	D0 – D7
CE	P52	CE
OE	P51	OE
PGM	P50	PGM

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MITSUBISHI MICROCOMPUTERS

M37733EHBXXXFP
M37733EHBFS

PROM VERSION OF M37733MHBXXXFP

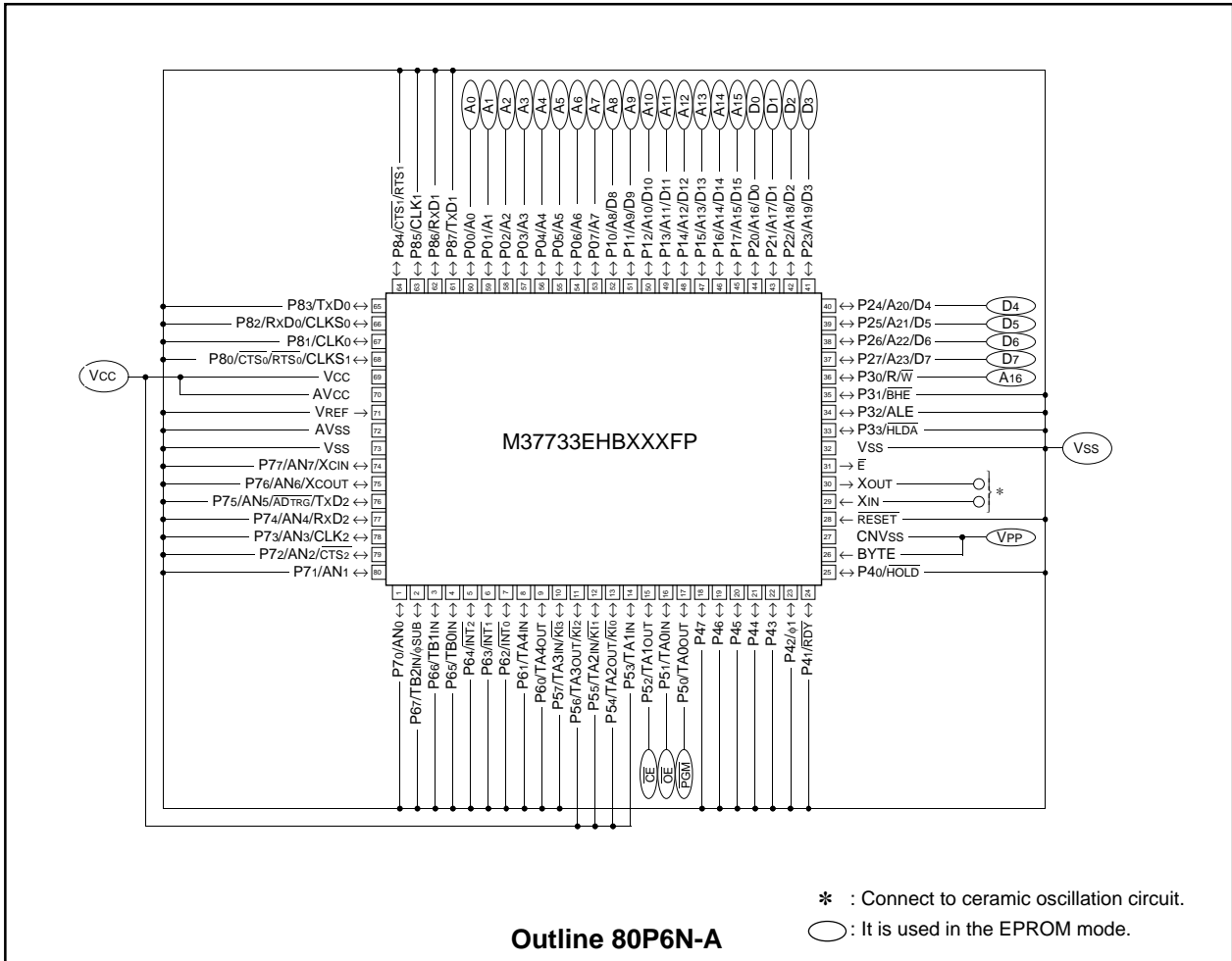


Fig. 4 Pin connection in EPROM mode

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FUNCTION IN EPROM MODE
1M mode (equivalent to the M5M27C101K)

Reading

To read the EPROM, set the \overline{CE} and \overline{OE} pins to a "L" level. Input the address of the data ($A_0 - A_{16}$) to be read, and the data will be output to the I/O pins $D_0 - D_7$. The data I/O pins will be floating when either the \overline{CE} or \overline{OE} pins are in the "H" state.

Programming

Programming must be performed in 8 bits by a byte program. To program to the EPROM, set the \overline{CE} pin to a "L" level and the \overline{OE} pin to a "H" level. The CPU will enter the programming mode when 12.5 V is applied to the V_{PP} pin. The address to be programmed to is selected with pins $A_0 - A_{16}$, and the data to be programmed is input to pins $D_0 - D_7$. Set the \overline{PGM} pin to a "L" level to being programming.

Erasing

To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15 J/cm².

Programming operation

To program the M37733EHBXXXFP, first set $V_{CC} = 6 V$, $V_{PP} = 12.5 V$, and set the address to 0100016. Apply a 0.2 ms programming pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 0.2 ms programming pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further once this number of pulses (0.2 X X ms).

When this series of programming operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.

Finally, when all addresses have been programmed, read with $V_{CC} = V_{PP} = 5 V$ (or $V_{CC} = V_{PP} = 5.5 V$).

Table 2. I/O signal in each mode

Mode	Pin					
	\overline{CE}	\overline{OE}	\overline{PGM}	V_{PP}	V_{CC}	Data I/O
Read-out	V _{IL}	V _{IL}	X	5 V	5 V	Output
Output	V _{IL}	V _{IH}	X	5 V	5 V	Floating
Disable	V _{IH}	X	X	5 V	5 V	Floating
Programming	V _{IL}	V _{IH}	V _{IL}	12.5 V	6 V	Input
Programming Verify	V _{IL}	V _{IL}	V _{IH}	12.5 V	6 V	Output
Program Disable	V _{IH}	V _{IH}	V _{IH}	12.5 V	6 V	Floating

Note 1 : An X indicates either V_{IL} or V_{IH}.

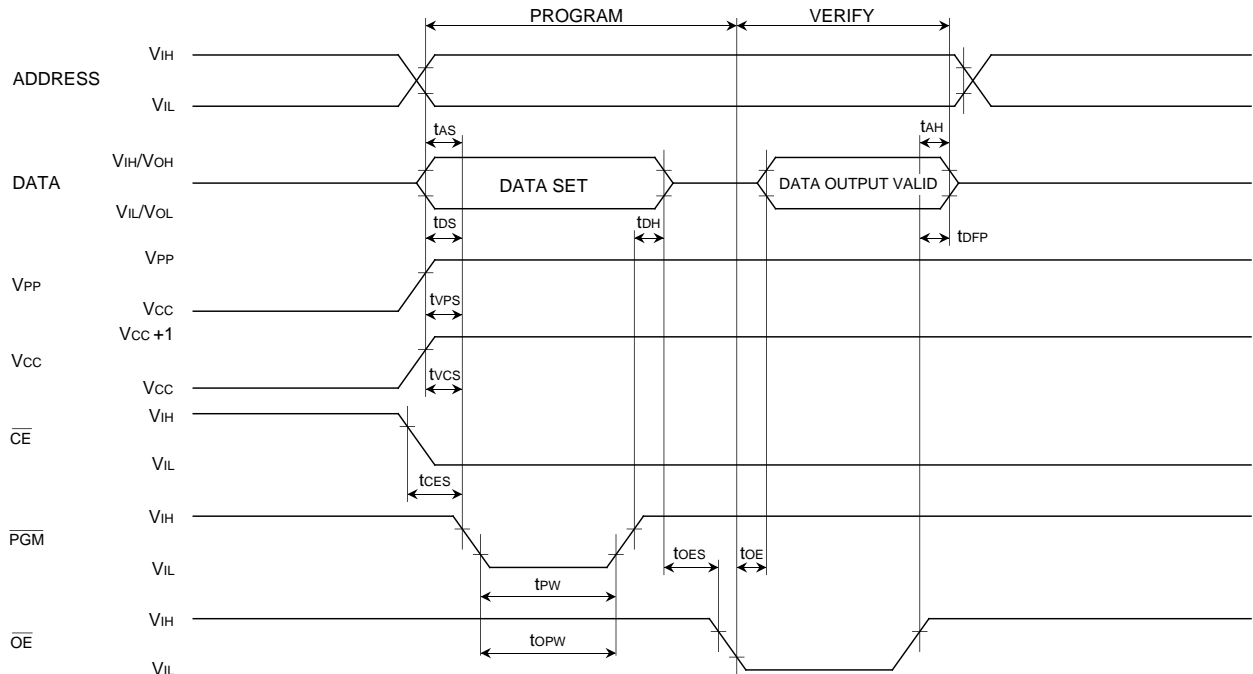
Programming operation (equivalent to the M5M27C101K)

AC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5 \text{ }^\circ\text{C}$, $V_{CC} = 6 V \pm 0.25 V$, $V_{PP} = 12.5 \pm 0.3 V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
tAS	Address setup time		2			μs
tOES	OE setup time		2			μs
tDS	Data setup time		2			μs
tAH	Address hold time		0			μs
tDH	Data hold time		2			μs
tDFP	Output enable to output float delay		0		130	ns
tVCS	VCC setup time		2			μs
tVPS	VPP setup time		2			μs
tPW	PGM pulse width		0.19	0.2	0.21	ms
tOPW	PGM over program pulse width		0.19		5.25	ms
tCES	CE setup time		2			μs
tOE	Data valid from OE				150	ns

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AC waveforms



Test conditions for A.C. characteristics

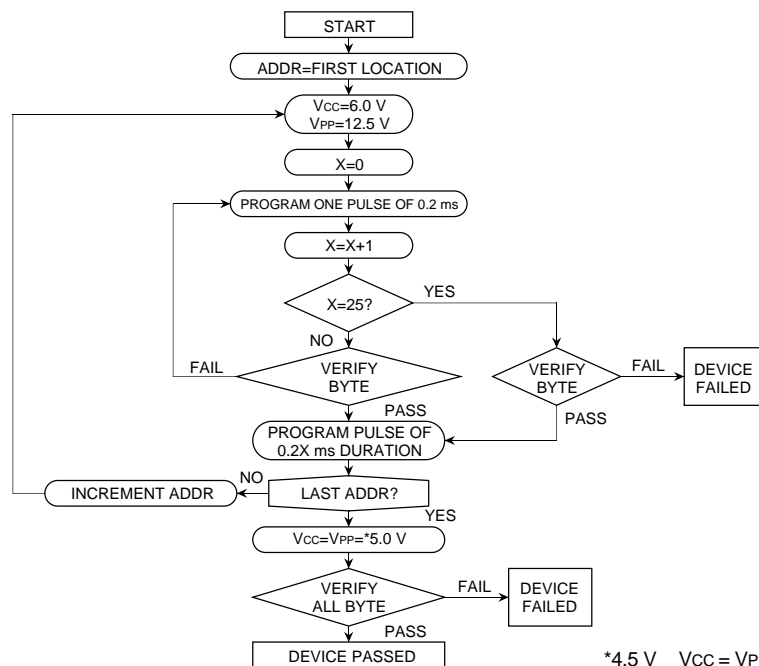
Input voltage : VIL = 0.45 V, VIH = 2.4 V

Input rise and fall times (10% - 90%) : 20 ns

Reference voltage at timing measurement : Input, Output

"L" = 0.8 V, "H" = 2 V

Programming algorithm flow chart



*4.5 V VCC = VPP 5.5 V

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SAFETY INSTRUCTIONS

- (1) Sunlight and fluorescent lamp contain light that can erase written information. When using in read mode, be sure to cover the transparent glass portion with a seal or other materials (ceramic package product).
- (2) Mitsubishi Electric corp. provides the seal for covering the transparent glass. Take care that the seal does not touch the read pins (ceramic package product).
- (3) Clean the transparent glass before erasing. Fingers' fat and paste disturb the passage of ultraviolet rays and may affect badly the erasure capability (ceramic package product).
- (4) A high voltage is used for programming. Take care that over-voltage is not applied. Take care especially at power on.
- (5) The programmable M37733EHBFP that is shipped in blank is also provided. For the M37733EHBFP, Mitsubishi Electric corp. does not perform PROM programming test and screening following the assembly processes. To improve reliability after programming, performing programming and test according to the flow below before use is recommended.

ADDRESSING MODES

The M37733EHBXXXFP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details.

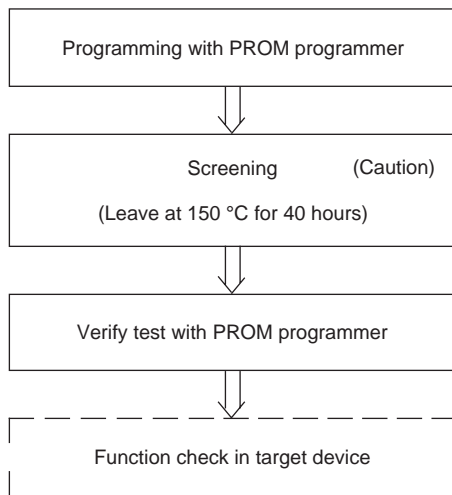
MACHINE INSTRUCTION LIST

The M37733EHBXXXFP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.

DATA REQUIRED FOR PROM ORDERING

Please send the following data for writing to PROM.

- (1) M37733EHBXXXFP writing to PROM order confirmation form
- (2) 80P6N mark specification form
- (3) ROM data (EPROM 3 sets)



Caution : Never expose to 150 °C exceeding 100 hours.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Power source voltage		-0.3 to +7	V
AV _{cc}	Analog power source voltage		-0.3 to +7	V
V _i	Input voltage RESET, CNV _{ss} , BYTE		-0.3 to +12 (Note)	V
V _i	Input voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, V _{REF} , X _{IN}		-0.3 to V _{cc} + 0.3	V
V _o	Output voltage P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X _{OUT} , E		-0.3 to V _{cc} + 0.3	V
P _d	Power dissipation	T _a = 25 °C	300	mW
T _{opr}	Operating temperature		-20 to +85	°C
T _{stg}	Storage temperature		-40 to +150	°C

Note. When the EPROM is programmed, input voltage of pins CNV_{ss} and BYTE is 13 V respectively.

RECOMMENDED OPERATING CONDITIONS (V_{cc} = 5 V ± 10%, T_a = -20 to +85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit	
		Min.	Typ.	Max.		
V _{cc}	Power source voltage	f(X _{IN}) : Operating	4.5	5.0	5.5	V
		f(X _{IN}) : Stopped, f(X _{CIN}) = 32.768 kHz	2.7		5.5	
AV _{cc}	Analog power source voltage		V _{cc}		V	
V _{ss}	Power source voltage		0		V	
AV _{ss}	Analog power source voltage		0		V	
V _{IH}	High-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X _{IN} , RESET, CNV _{ss} , BYTE, X _{CIN} (Note 3)	0.8 V _{cc}		V _{cc}	V	
V _{IH}	High-level input voltage P10 – P17, P20 – P27 (in single-chip mode)	0.8 V _{cc}		V _{cc}	V	
V _{IH}	High-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)	0.5 V _{cc}		V _{cc}	V	
V _{IL}	Low-level input voltage P00 – P07, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, X _{IN} , RESET, CNV _{ss} , BYTE, X _{CIN} (Note 3)	0		0.2V _{cc}	V	
V _{IL}	Low-level input voltage P10 – P17, P20 – P27 (in single-chip mode)	0		0.2V _{cc}	V	
V _{IL}	Low-level input voltage P10 – P17, P20 – P27 (in memory expansion mode and microprocessor mode)	0		0.16V _{cc}	V	
I _{OH(peak)}	High-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87			-10	mA	
I _{OH(avg)}	High-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87			-5	mA	
I _{OL(peak)}	Low-level peak output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87			10	mA	
I _{OL(peak)}	Low-level peak output current P44 – P47, P50 – P53			20	mA	
I _{OL(avg)}	Low-level average output current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87			5	mA	
I _{OL(avg)}	Low-level average output current P44 – P47, P50 – P53			15	mA	
f(X _{IN})	Main-clock oscillation frequency (Note 4)			25	MHz	
f(X _{CIN})	Sub-clock oscillation frequency		32.768	50	kHz	

- Notes**
1. Average output current is the average value of a 100 ms interval.
 2. The sum of I_{OL(peak)} for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OH(peak)} for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I_{OL(peak)} for ports P4, P5, P6, and P7 must be 100 mA or less, and the sum of I_{OH(peak)} for ports P4, P5, P6, and P7 must be 80 mA or less.
 3. Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = "1".
 4. The maximum value of f(X_{IN}) = 12.5 MHz when the main clock division selection bit = "1".

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87	$I_{OH} = -10\text{ mA}$	3			V
V_{OH}	High-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	$I_{OH} = -400\text{ }\mu\text{A}$	4.7			V
V_{OH}	High-level output voltage P30 – P32	$I_{OH} = -10\text{ mA}$	3.1			V
		$I_{CH} = -400\text{ }\mu\text{A}$	4.8			
V_{OH}	High-level output voltage \bar{E}	$I_{OH} = -10\text{ mA}$	3.4			V
		$I_{OH} = -400\text{ }\mu\text{A}$	4.8			
V_{OL}	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87	$I_{OL} = 10\text{ mA}$			2	V
V_{OL}	Low-level output voltage P44 – P47, P50 – P53	$I_{OL} = 20\text{ mA}$			2	V
V_{OL}	Low-level output voltage P00 – P07, P10 – P17, P20 – P27, P33	$I_{OL} = 2\text{ mA}$			0.45	V
V_{OL}	Low-level output voltage P30 – P32	$I_{OL} = 10\text{ mA}$			1.9	V
		$I_{OL} = 2\text{ mA}$			0.43	
V_{OL}	Low-level output voltage \bar{E}	$I_{OL} = 10\text{ mA}$			1.6	V
		$I_{OL} = 2\text{ mA}$			0.4	
$V_{T+} - V_{T-}$	Hysteresis HOLD, RDY, TA0IN – TA4IN, TB0IN – TB2IN, INT0 – INT2, ADTRG, CTS0, CTS1, CTS2, CLK0, CLK1, CLK2, Kl0 – Kl3		0.4		1	V
$V_{T+} - V_{T-}$	Hysteresis RESET		0.2		0.5	V
$V_{T+} - V_{T-}$	Hysteresis XIN		0.1		0.4	V
$V_{T+} - V_{T-}$	Hysteresis XCIN (When external clock is input)		0.1		0.4	V
I_{IH}	High-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, XIN, RESET, CNVss, BYTE	$V_I = 5\text{ V}$			5	μA
I_{IL}	Low-level input current P00 – P07, P10 – P17, P20 – P27, P30 – P33, P40 – P47, P50 – P53, P60, P61, P65 – P67, P70 – P77, P80 – P87, XIN, RESET, CNVss, BYTE	$V_I = 0\text{ V}$			-5	μA
I_{IL}	Low-level input current P54 – P57, P62 – P64	$V_I = 0\text{ V}$, without a pull-up transistor			-5	μA
		$V_I = 0\text{ V}$, with a pull-up transistor	-0.25	-0.5	-1.0	mA
V _{RAM}	RAM hold voltage	When clock is stopped.	2			V

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit		
			Min.	Typ.	Max.			
I _{CC}	Power source current	In single-chip mode, output pins are open, and other pins are V _{SS} .	V _{CC} = 5 V, f(X _{IN}) = 25 MHz (square waveform), (f ₂) = 12.5 MHz, f(X _{CIN}) = 32.768 kHz, in operating (Note 1)		9.5	19	mA	
			V _{CC} = 5 V, f(X _{IN}) = 25 MHz (square waveform), (f ₂) = 1.5625 MHz, f(X _{CIN}) = Stopped, in operating (Note 1)		1.3	2.6	mA	
			V _{CC} = 5V, f(X _{IN}) = 25 MHz (square waveform), f(X _{CIN}) = 32.768 kHz, when a WIT instruction is executed (Note 2)		10	20	μA	
			V _{CC} = 5 V, f(X _{IN}) : Stopped, f(X _{CIN}) : 32.768 kHz, in operating (Note 3)		50	100	μA	
			V _{CC} = 5 V, f(X _{IN}) : Stopped, f(X _{CIN}) : 32.768 kHz, when a WIT instruction is executed (Note 4)		5	10	μA	
			T _a = 25 °C, when clock is stopped				1	μA
			T _a = 85 °C, when clock is stopped				20	μA

- Notes**
1. This applies when the main clock external input selection bit = "1", the main clock division selection bit = "0", and the signal output stop bit = "1".
 2. This applies when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1".
 3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.
 4. This applies when the X_{cout} drivability selection bit = "0" and the system clock stop bit at wait state = "1".

A-D CONVERTER CHARACTERISTICS

($V_{CC} = AV_{CC} = 5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$ (Note), unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V _{REF} = V _{CC}			10	Bits
—	Absolute accuracy	V _{REF} = V _{CC}			± 3	LSB
RLADDER	Ladder resistance	V _{REF} = V _{CC}	10		25	kΩ
t _{CONV}	Conversion time		9.44			μs
V _{REF}	Reference voltage		2		V _{CC}	V
V _{IA}	Analog input voltage		0		V _{REF}	V

Note. This applies when the main clock division selection bit = "0" and f₂ = 12.5 MHz.

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

TIMING REQUIREMENTS ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$, unless otherwise noted (Note))

Notes 1. This applies when the main clock division selection bit = "0" and $f(f_2) = 12.5\text{ MHz}$.

2. Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time (Note 1)	40		ns
$t_{w(H)}$	External clock input high-level pulse width (Note 2)	15		ns
$t_{w(L)}$	External clock input low-level pulse width (Note 2)	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns

Notes 1. When the main clock division selection bit = "1", the minimum value of $t_c = 80\text{ ns}$.

2. When the main clock division selection bit = "1", values of $t_{w(H)} / t_c$ and $t_{w(L)} / t_c$ must be set to values from 0.45 through 0.55.

Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(P0D-E)}$	Port P0 input setup time	60		ns
$t_{su(P1D-E)}$	Port P1 input setup time	60		ns
$t_{su(P2D-E)}$	Port P2 input setup time	60		ns
$t_{su(P3D-E)}$	Port P3 input setup time	60		ns
$t_{su(P4D-E)}$	Port P4 input setup time	60		ns
$t_{su(P5D-E)}$	Port P5 input setup time	60		ns
$t_{su(P6D-E)}$	Port P6 input setup time	60		ns
$t_{su(P7D-E)}$	Port P7 input setup time	60		ns
$t_{su(P8D-E)}$	Port P8 input setup time	60		ns
$t_{h(E-P0D)}$	Port P0 input hold time	0		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		ns
$t_{h(E-P3D)}$	Port P3 input hold time	0		ns
$t_{h(E-P4D)}$	Port P4 input hold time	0		ns
$t_{h(E-P5D)}$	Port P5 input hold time	0		ns
$t_{h(E-P6D)}$	Port P6 input hold time	0		ns
$t_{h(E-P7D)}$	Port P7 input hold time	0		ns
$t_{h(E-P8D)}$	Port P8 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(D-E)}$	Data input setup time	32		ns
$t_{su(RDY-\phi_1)}$	RDY input setup time	55		ns
$t_{su(HOLD-\phi_1)}$	HOLD input setup time	55		ns
$t_{h(E-D)}$	Data input hold time	0		ns
$t_{h(\phi_1-RDY)}$	RDY input hold time	0		ns
$t_{h(\phi_1-HOLD)}$	HOLD input hold time	0		ns

Timer A input (Count input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TAiIN input cycle time	80		ns
t _w (TAH)	TAiIN input high-level pulse width	40		ns
t _w (TAL)	TAiIN input low-level pulse width	40		ns

Timer A input (Gating input in timer mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TAiIN input cycle time (Note)	320		ns
t _w (TAH)	TAiIN input high-level pulse width (Note)	160		ns
t _w (TAL)	TAiIN input low-level pulse width (Note)	160		ns

Note. Limits change depending on f(X_{IN}). Refer to "DATA FORMULAS" on page 19.

Timer A input (External trigger input in one-shot pulse mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TAiIN input cycle time (Note)	320		ns
t _w (TAH)	TAiIN input high-level pulse width	80		ns
t _w (TAL)	TAiIN input low-level pulse width	80		ns

Note. Limits change depending on f(X_{IN}). Refer to "DATA FORMULAS" on page 19.

Timer A input (External trigger input in pulse width modulation mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _w (TAH)	TAiIN input high-level pulse width	80		ns
t _w (TAL)	TAiIN input low-level pulse width	80		ns

Timer A input (Up-down input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (UP)	TAiOUT input cycle time	2000		ns
t _w (UPH)	TAiOUT input high-level pulse width	1000		ns
t _w (UPL)	TAiOUT input low-level pulse width	1000		ns
t _{su} (UP-T _{IN})	TAiOUT input setup time	400		ns
t _h (T _{IN} -UP)	TAiOUT input hold time	400		ns

Timer A input (Two-phase pulse input in event counter mode)

Symbol	parameter	Limits		Unit
		Min.	Max.	
t _c (TA)	TAjIN input cycle time	800		ns
t _{su} (TAjIN-TAjOUT)	TAjIN input setup time	200		ns
t _{su} (TAjOUT-TAjIN)	TAjOUT input setup time	200		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _c (TB)	TBiIN input cycle time (one edge count)	80		ns
t _w (TBH)	TBiIN input high-level pulse width (one edge count)	40		ns
t _w (TBL)	TBiIN input low-level pulse width (one edge count)	40		ns
t _c (TB)	TBiIN input cycle time (both edges count)	160		ns
t _w (TBH)	TBiIN input high-level pulse width (both edges count)	80		ns
t _w (TBL)	TBiIN input low-level pulse width (both edges count)	80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _c (TB)	TBiIN input cycle time (Note)	320		ns
t _w (TBH)	TBiIN input high-level pulse width (Note)	160		ns
t _w (TBL)	TBiIN input low-level pulse width (Note)	160		ns

Note. Limits change depending on f(X_{IN}). Refer to "DATA FORMULAS" on page 19.

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _c (TB)	TBiIN input cycle time (Note)	320		ns
t _w (TBH)	TBiIN input high-level pulse width (Note)	160		ns
t _w (TBL)	TBiIN input low-level pulse width (Note)	160		ns

Note. Limits change depending on f(X_{IN}). Refer to "DATA FORMULAS" on page 19.

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _c (AD)	ADTRG input cycle time (minimum allowable trigger)	1000		ns
t _w (ADL)	ADTRG input low-level pulse width	125		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _c (CK)	CLK _i input cycle time	200		ns
t _w (CKH)	CLK _i input high-level pulse width	100		ns
t _w (CKL)	CLK _i input low-level pulse width	100		ns
t _d (C-Q)	TxD _i output delay time		80	ns
t _h (C-Q)	TxD _i hold time	0		ns
t _{su} (D-C)	RxD _i input setup time	30		ns
t _h (C-D)	RxD _i input hold time	90		ns

External interrupt INT_i input, key input interrupt KI_i input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _w (INH)	INT _i input high-level pulse width	250		ns
t _w (INL)	INT _i input low-level pulse width	250		ns
t _w (KIL)	KI _i input low-level pulse width	250		ns

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

DATA FORMULAS

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{c(TA)}	TAiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
t _{w(TAH)}	TAiIn input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
t _{w(TAL)}	TAiIn input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{c(TA)}	TAiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer B input (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{c(TB)}	TBiIn input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
t _{w(TBH)}	TBiIn input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
t _{w(TBL)}	TBiIn input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Note. f(f₂) represents the clock f₂ frequency.

For the relation to the main clock and sub clock, refer to Table 9 in data sheet "M37733MHBXXXFP".

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85^\circ\text{C}$, $f(X_{IN}) = 25\text{ MHz}$ (Note), unless otherwise noted)
Single-chip mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(E-P0Q)}$	Port P0 data output delay time	Fig. 5		80	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time			80	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			80	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time			80	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time			80	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time			80	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time			80	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time			80	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time			80	ns

Note. This applies when the main clock division selection bit = "0" and $f(f_2) = 12.5\text{ MHz}$.

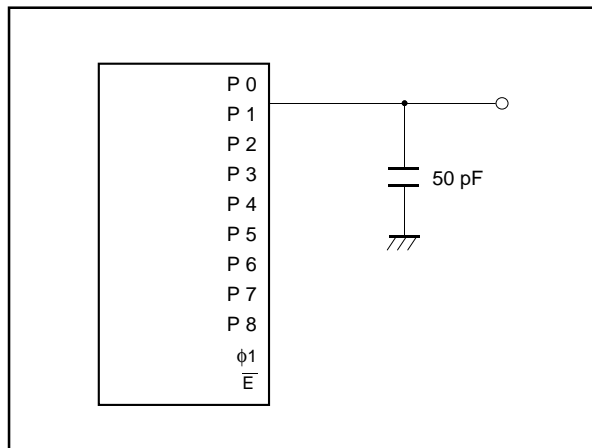


Fig. 5 Measuring circuit for ports P0 – P8 and $\phi 1$

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode

(V_{CC} = 5 V ± 10%, V_{SS} = 0 V, T_a = 25 °C, f(X_{IN}) = 25 MHz (Note 1), unless otherwise noted)

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits		Unit
				Min.	Max.	
td(A _n -E)	Address output delay time	No wait	Fig. 5	12		ns
		Wait 1				
		Wait 0		87		ns
td(A-E)	Address output delay time	No wait		12		ns
		Wait 1				
		Wait 0		75		ns
th(E-A _n)	Address hold time			18		ns
tw(ALE)	ALE pulse width	No wait		22		ns
		Wait 1				
		Wait 0		57		ns
tsu(A-ALE)	Address output setup time	No wait		5		ns
		Wait 1				
		Wait 0		45		ns
th(ALE-A)	Address hold time	No wait		9		ns
		Wait 1				
		Wait 0		15		ns
td(ALE-E)	ALE output delay time	No wait		4		ns
		Wait 1				
		Wait 0		10		ns
td(E-DQ)	Data output delay time				45	ns
th(E-DQ)	Data hold time		18		ns	
tw(EL)	E pulse width	No wait	50		ns	
		Wait 1				
		Wait 0	130		ns	
tpxz(E-DZ)	Floating start delay time			5	ns	
tpzx(E-DZ)	Floating release delay time		20		ns	
td(BHE-E)	BHE output delay time	No wait	12		ns	
		Wait 1				
		Wait 0	87		ns	
td(R/W-E)	R/W output delay time	No wait	12		ns	
		Wait 1				
		Wait 0	87		ns	
th(E-BHE)	BHE hold time		18		ns	
th(E-R/W)	R/W hold time		18		ns	
td(E-φ ₁)	φ ₁ output delay time		0	18	ns	
td(φ ₁ -HLDA)	HLDA output delay time			50	ns	

Notes 1. This applies when the main clock division selection bit = "0" and f(f₂) = 12.5 MHz.

2. No wait : Wait bit = "1".

Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

Memory expansion mode and microprocessor mode

Bus timing data formulas ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(XIN) = 25\text{ MHz}$ (Max., Note 1), unless otherwise noted)

Symbol	Parameter	Wait mode	Limits		Unit
			Min.	Max.	
td(An-E)	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 1	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
td(A-E)	Address output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 45$		ns
th(E-An)	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
tw(ALE)	ALE pulse width	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 18$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 23$		ns
tsu(A-ALE)	Address output setup time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
th(ALE-A)	Address hold time	No wait	9		ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 25$		ns
td(ALE-E)	ALE output delay time	No wait	4		ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
td(E-DQ)	Data output delay time			45	ns
th(E-DQ)	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
tw(EL)	\bar{E} pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
		Wait 1	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
tpxz(E-DZ)	Floating start delay time			5	ns
tpzx(E-DZ)	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 20$		ns
td(BHE-E)	$\overline{\text{BHE}}$ output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
td(R/W-E)	$\overline{\text{R/W}}$ output delay time	No wait	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 28$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 33$		ns
th(E-BHE)	$\overline{\text{BHE}}$ hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
th(E-R/W)	$\overline{\text{R/W}}$ hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 22$		ns
td(E-φ1)	φ1 output delay time		0	18	ns

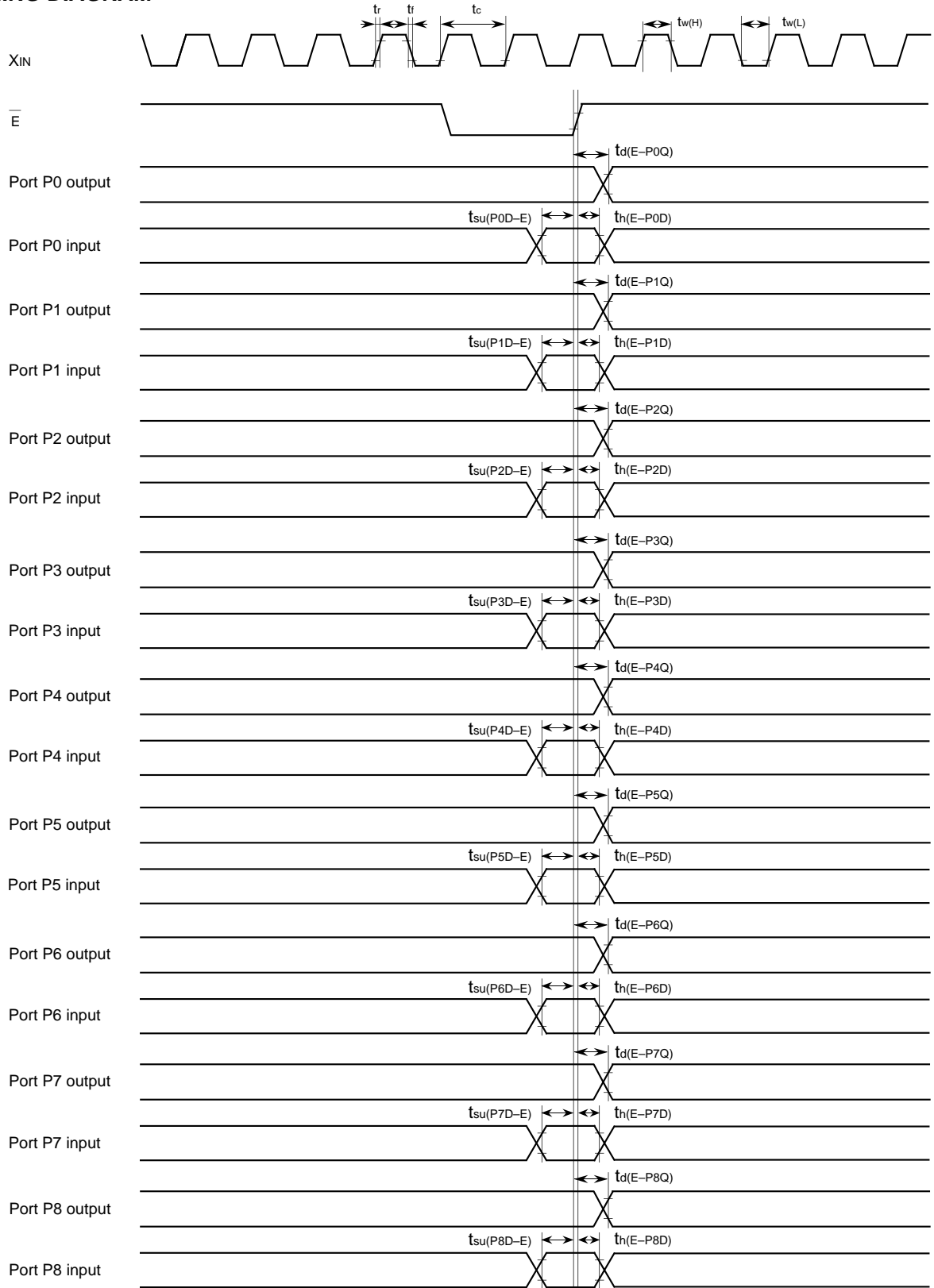
Notes 1. This applies when the main-clock division selection bit = "0".

2. f(f2) represents the clock f2 frequency.

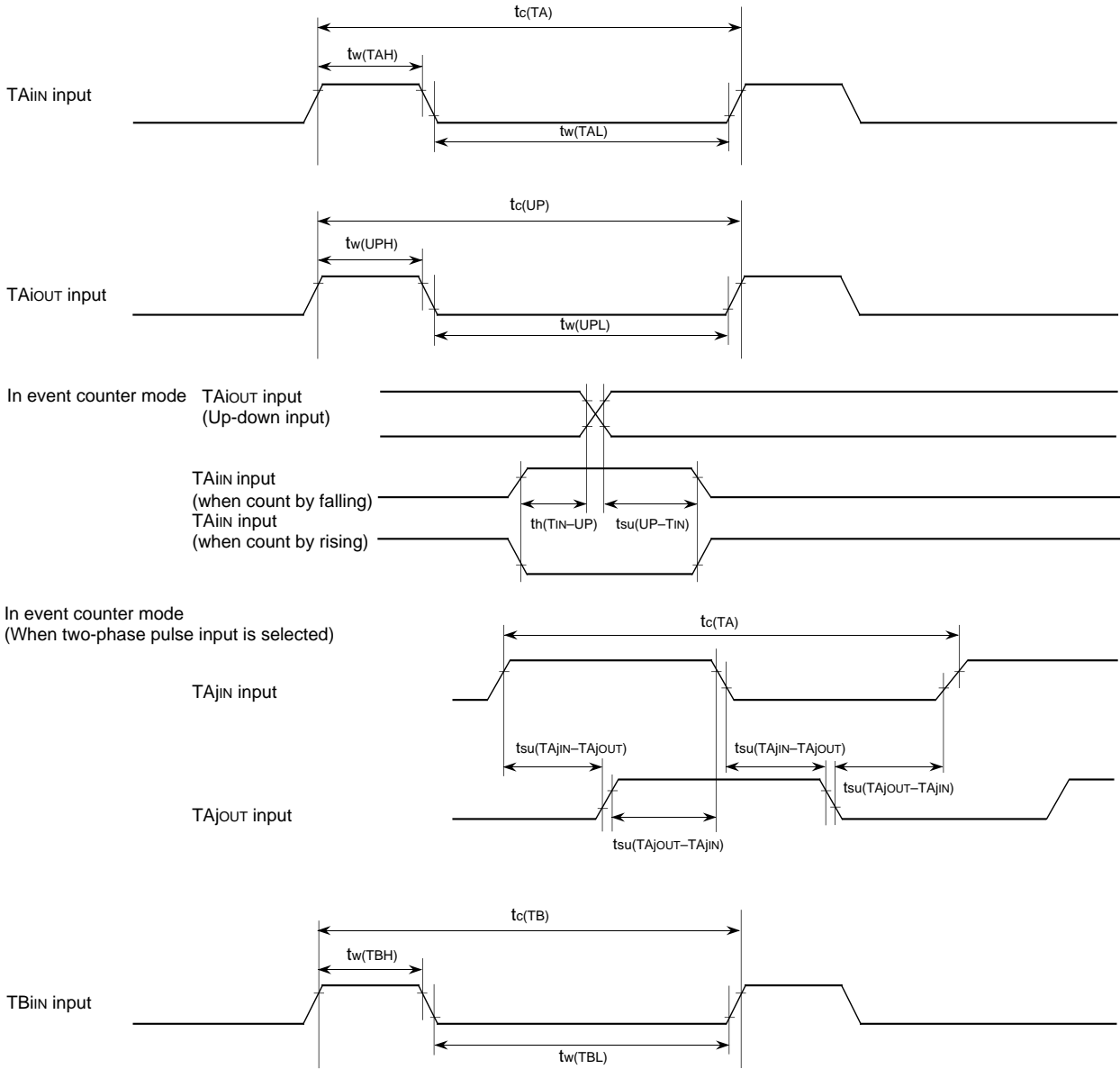
For the relation to the main clock and sub clock, refer to Table 9 in data sheet "M37733MHBXXXFP".

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

TIMING DIAGRAM



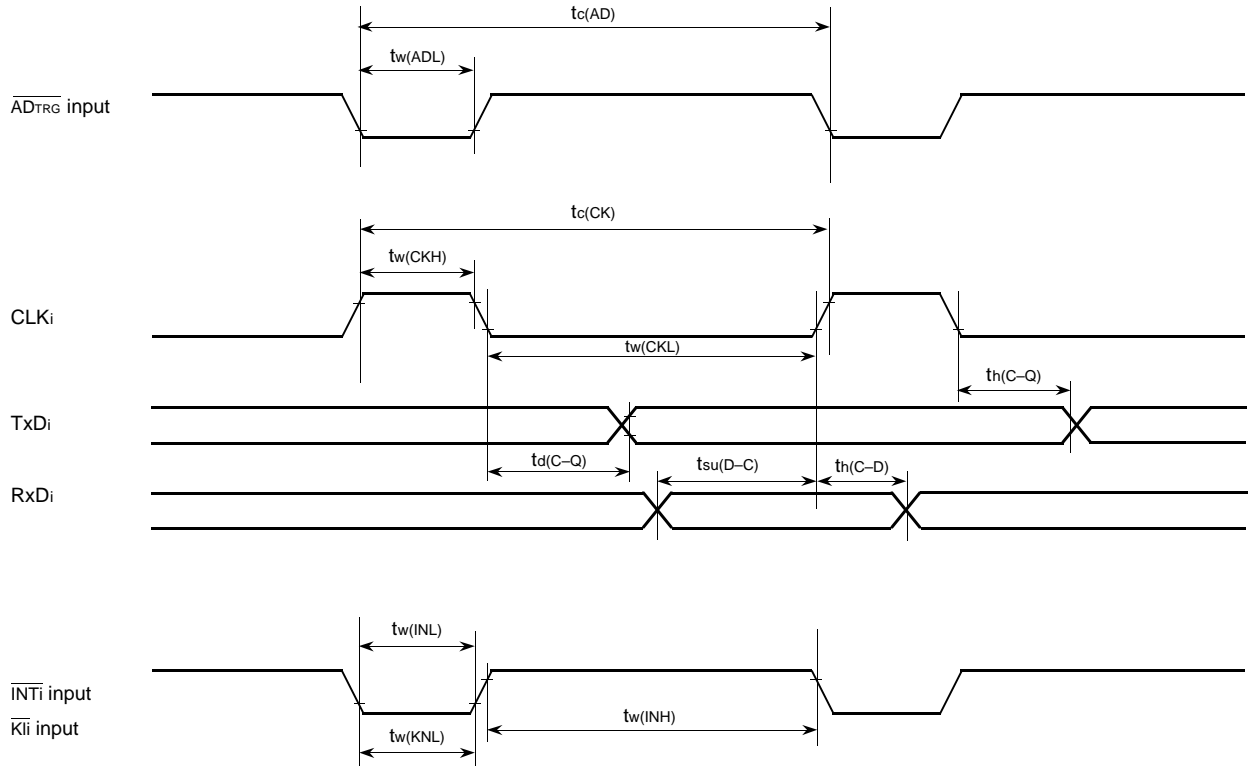
PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.



PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

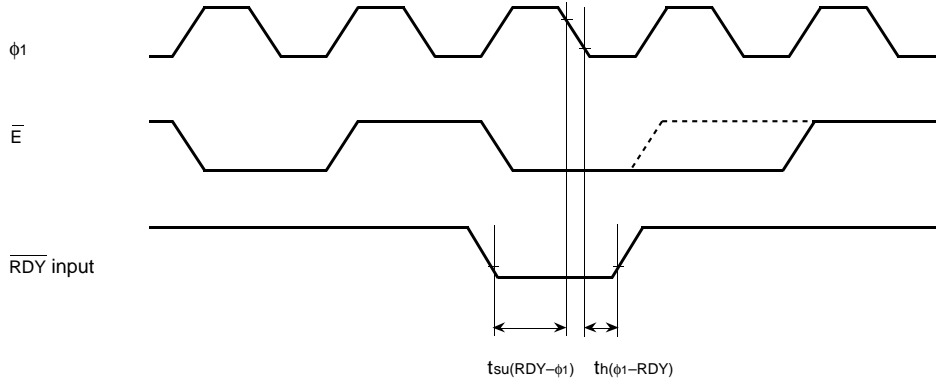
M37733EHBXXXFP
M37733EHBFS

PROM VERSION OF M37733MHBXXXFP

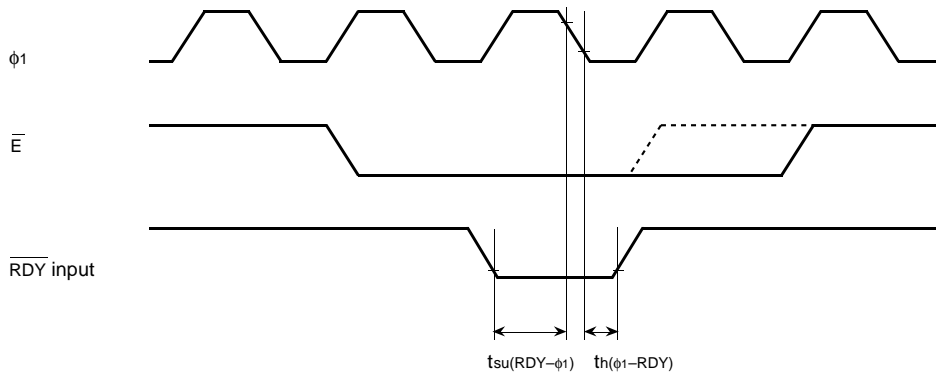


PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

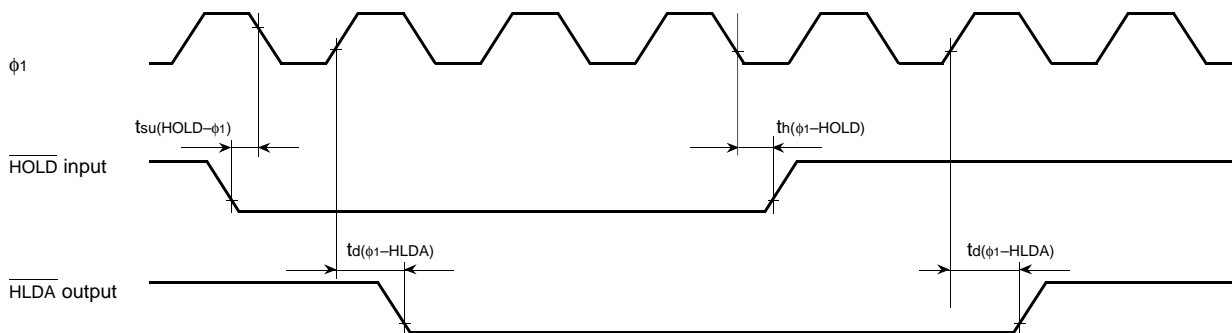
Memory expansion mode and microprocessor mode
 (When wait bit = "1")



(When wait bit = "0")



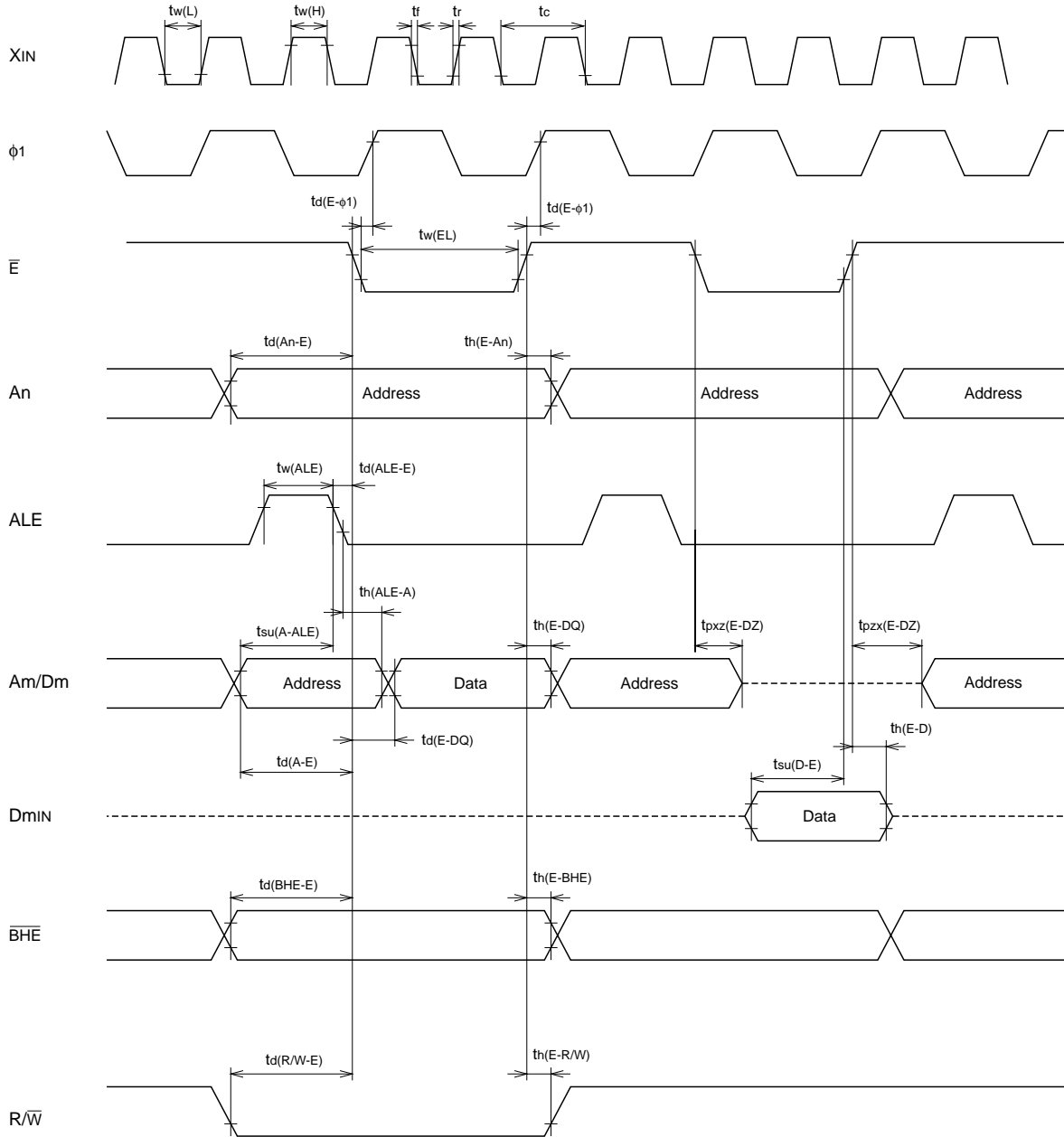
(When wait bit = "1" or "0" in common)



- Test conditions
- $V_{CC} = 5\text{ V} \pm 10\%$
 - Input timing voltage : $V_{IL} = 1.0\text{ V}$, $V_{IH} = 4.0\text{ V}$
 - Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode
 (No wait : When wait bit = "1")

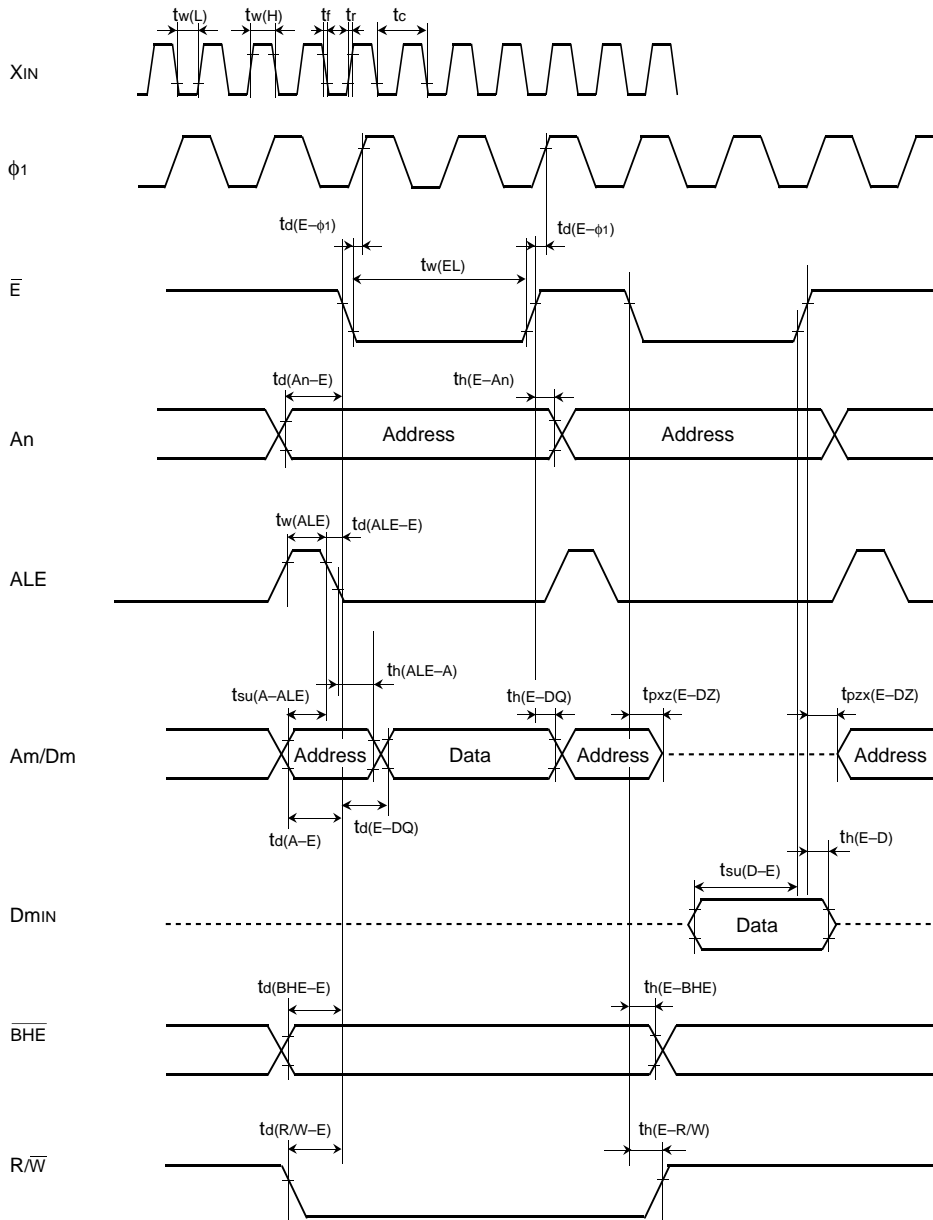


Test conditions

- $V_{CC} = 5 V \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8 V, V_{OH} = 2.0 V$
- Data input D_{min} : $V_{IL} = 0.8 V, V_{IH} = 2.5 V$

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode
 (Wait 1 : The external memory area is accessed when wait bit = "0" and wait selection bit = "1".)

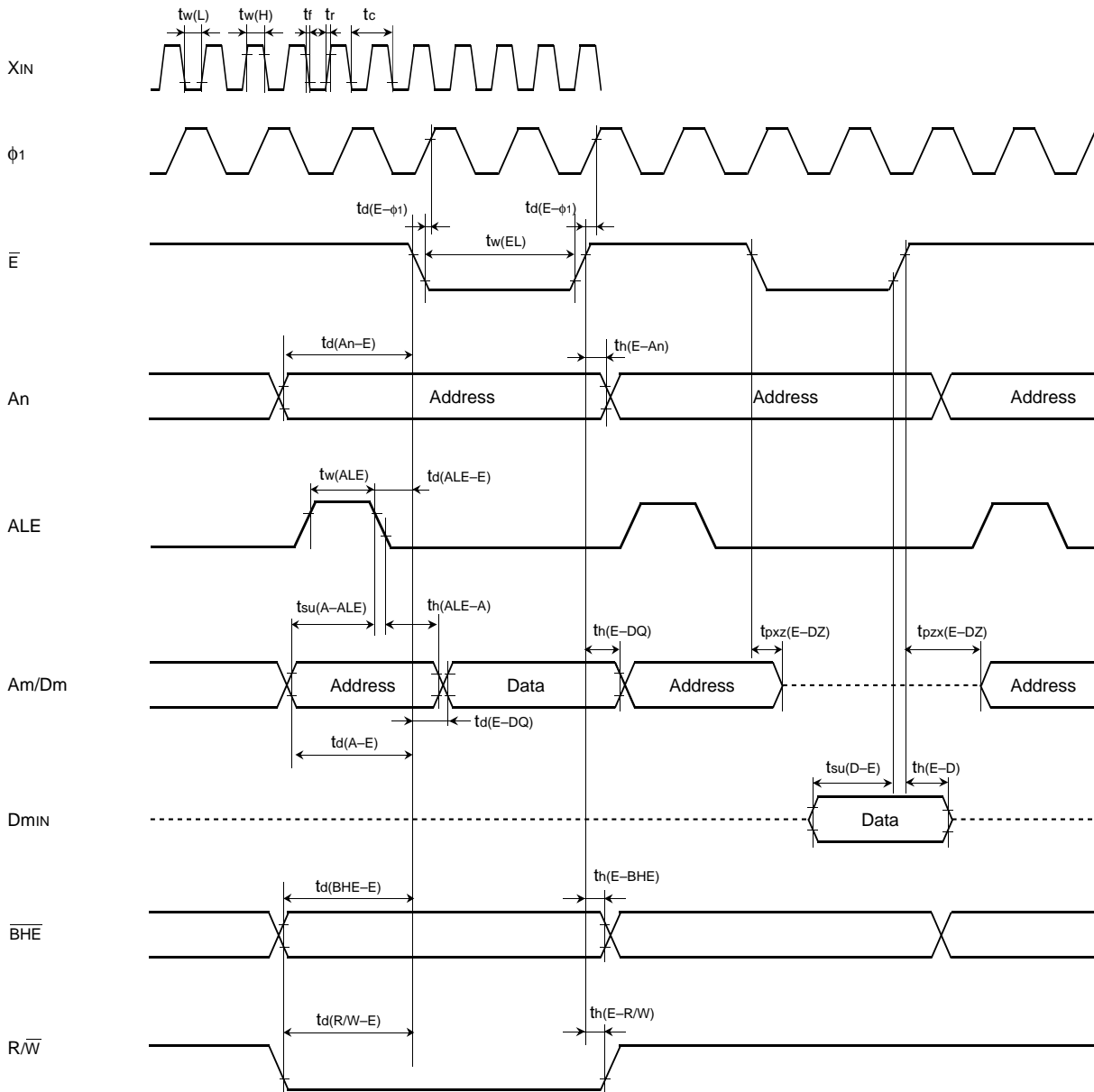


Test conditions

- $V_{cc} = 5\text{ V} \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
- Data input D_{min} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode
 (Wait 0 : The external memory area is accessed when wait bit = "0" and wait selection bit = "0".)



- Test conditions
- $V_{cc} = 5\text{ V} \pm 10\%$
 - Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$
 - Data input D_{min} : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

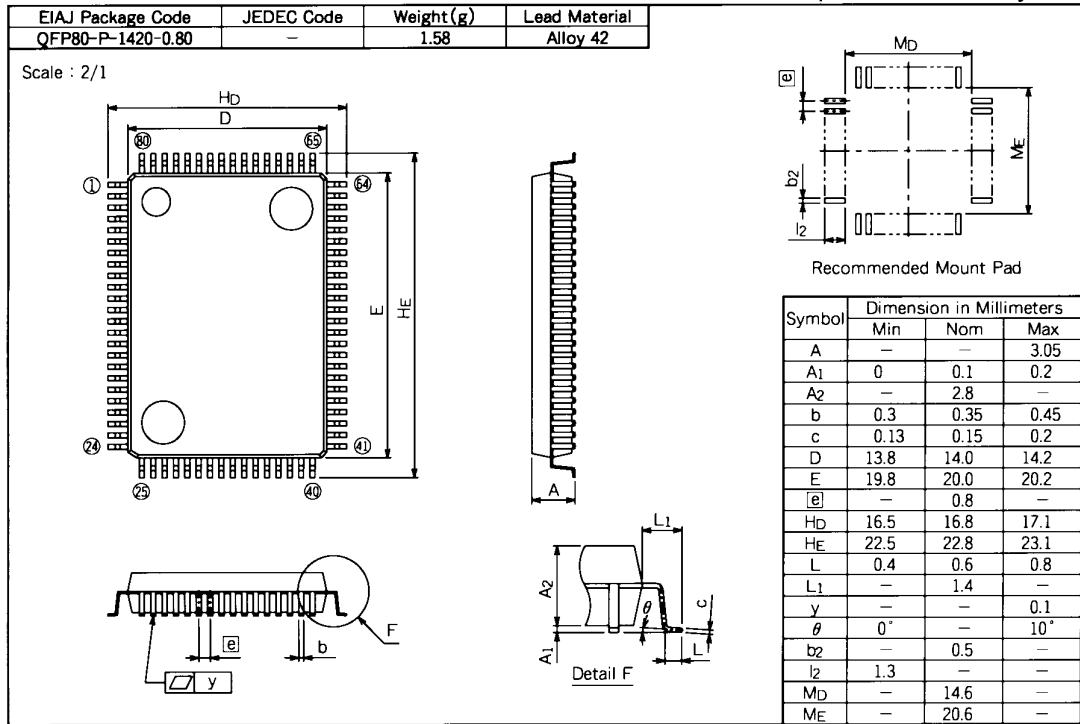
M37733EHBXXXFP
M37733EHBFS

PROM VERSION OF M37733MHBXXXFP

PACKAGE OUTLINE

80P6N-A

Plastic 80pin 14x20mm body QFP



**7700 FAMILY WRITING TO PROM ORDER CONFIRMATION FORM
SINGLE-CHIP 16-BIT MICROCOMPUTER
M37733EHBXXXFP
MITSUBISHI ELECTRIC**

ROM number	
------------	--

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ※

※	Customer	Company name	TEL ()	Issuance signatures	Responsible officer	Supervisor
		Date issued	Date:			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three sets of EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain the identical data, we will produce writing to PROM based on this data. We shall assume the responsibility for errors only if the written PROM data on the products we produce differ from this data.

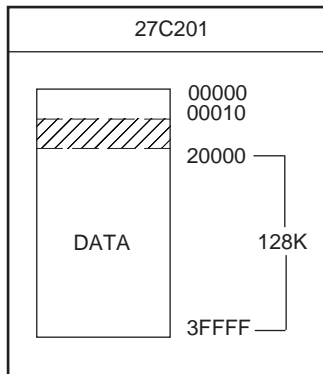
Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas

--	--	--	--

 (hexadecimal notation)

EPROM Type :



Note : Make sure that address 01FFFF₁₆ of the microcomputer's internal ROM corresponds to address 3FFFF₁₆ of EPROM.

(1) Set "FF₁₆" in the shaded area.

(2) Address 0₁₆ to 0F₁₆ are the area for storing the data on model designation. This area must be written with the data shown below.

Address and data are written in hexadecimal notation.

Address	Address		
4D	0	42	8
33	1	FF	9
37	2	FF	A
37	3	FF	B
33	4	FF	C
33	5	FF	D
45	6	FF	E
48	7	FF	F

※2. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered fill out the appropriate 80P6N Mark Specification Form (for M37733EHBXXXFP) and attach to the Writing to PROM Order Confirmation Form.

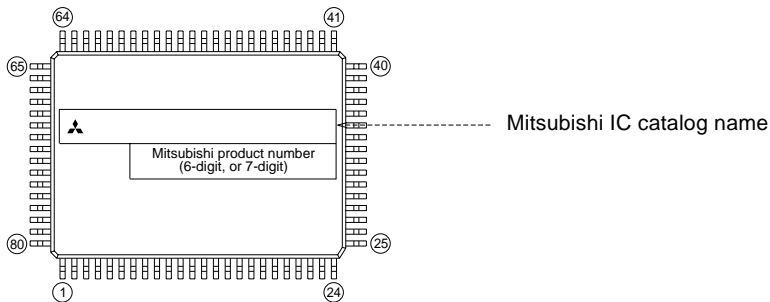
※3. Comments

80P6N (80-PIN QFP) MARK SPECIFICATION FORM

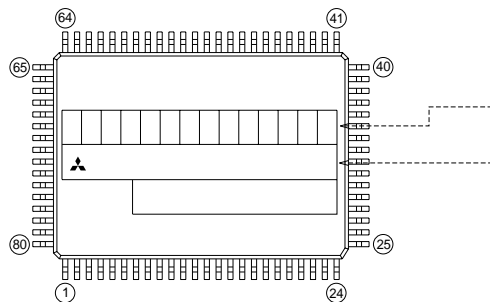
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi IC Catalog Name



Customer's Parts Number

Note : The fonts and size of characters are standard Mitsubishi type.

Mitsubishi IC catalog name

Notes 1 : The mark field should be written right aligned.

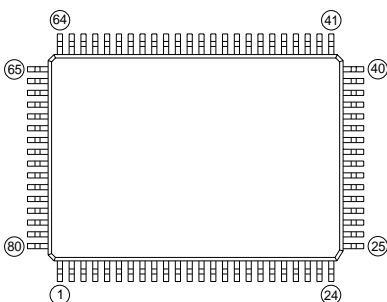
2 : The fonts and size of characters are standard Mitsubishi type.

3 : Customer's parts number can be up to 14 alphanumeric characters for capital letters, hyphens, commas, periods and so on.

4 : If the Mitsubishi logo is not required, check the box below.

▲ Mitsubishi logo is not required

C. Special Mark Required



Notes1 : If special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated technically as close as possible.

Mitsubishi product number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked for sorting the products.

2 : If special character fonts (e.g., customer's trade mark logo) must be used in Special Mark, check the box below.

For the new special character fonts, a clean font original (ideally logo drawing) must be submitted.

Special character fonts required

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

M37733EHBXXXFP
M37733EHBFS

PROM VERSION OF M37733MHBXXXFP

Keep safety first in your circuit designs!

- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

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REVISION DESCRIPTION LIST

M37733EBXXXXFP, M37733EBBFS Datasheet

Rev. No.	Revision Description		Rev. date
1.00	First Edition		970604
1.01	The following are added: <ul style="list-style-type: none"> • PROM ORDER CONFIRMATION FORM • MARK SPECIFICATION FORM 		980526
2.00	The following are revised:		980731
	Page	Previous Version	
	P12 Right Column Line 2	The M37733EBXXXXFP has 28 powerful addressing modes. Refer to the <u>MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS</u> for the details of each addressing mode. MACHINE INSTRUCTION LIST The M37733EBXXXXFP has 103 machine instructions. Refer to the <u>MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS</u> for details.	The M37733EBXXXXFP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details. MACHINE INSTRUCTION LIST The M37733EBXXXXFP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.