élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL1056AC/EL1056C

Monolithic High-Speed Pin Driver

Features

- Wide ±12V output levels
- 250 ps dispersion
- 3 ns delay times
- 1V/ns slew rate—adjustable
- Low overshoot and aberrations in 50Ω systems
- 3-state output
- Power-down mode reduces output leakage to nanoamperes
- Overcurrent sense flag available to protect internal output devices
- Buffered analog inputs
- Differential logic inputs are compatible with ECL, TTL, and CMOS

Applications

- Memory testers
- ASIC testers
- Functional board testers
- Analog/digital incoming component verifiers
- Logic emulators

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL1056CM	0°C to +75°C	24-Lead Thermal SOL	MDP0027
EL1056ACM	0°C to +75°C	24-Lead Thermal SOL	MDP0027

General Description

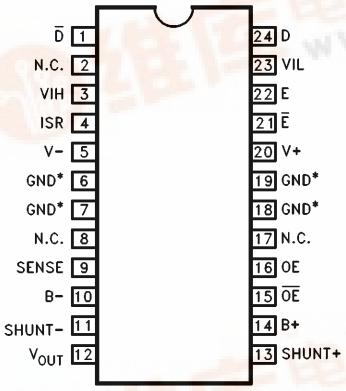
The EL1056 is designed to drive high-quality test signals into close or terminated loads. It has a dispersion of 250 ps or less — whether due to signal size or direction of edge. It can output a very wide 24V output span, encompassing all logic families as well as analog levels. The EL1056 is fabricated in Elantec's oxide isolated process, which eliminates the possibility of latch-up and provides a very durable circuit.

The output can be turned off in two ways; the OE pins allow the output to be put in a high-impedance state which makes the output look like a large resistance in parallel with 3 pF, even for back-driven signals with as much as 2.5V/μs slew rate. The E pins put the output in an even higher impedance state, guaranteed to 150 nA leakage in the EL1056A. This allows accurate measurements on the bus without disconnecting the EL1056 with a relay.

The EL1056 incorporates an output current sense which can warn the system controller that excessive output current is flowing. The trip point is set by two external resistors.

Connection Diagram

24-Lead Thermal SOL Package



*and Heat-spreader

1056–1

Top View

March 1993 Rev A

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	+33V
V−	Supply Voltage	−18V
B+	Supply Voltage	V_{INH} to V+
B−	Supply Voltage	V− to V_{INL}
I_{SR}	Input Current	0 mA to 3 mA
V_{SR}	Input Voltage, Power-Down Mode	−0.3V to +6V
Shunt+	Input Voltage	(B+) −5V to B+
Shunt−	Input Voltage	B− to (B−) +5V
Data, $\overline{Data}$	Input Voltages	V− to V+ or ±6V Differential
OE, $\overline{OE}$	Input Voltages	V− to V+ or ±6V Differential
E, $\overline{E}$	Input Voltages	V− to V+ or ±6V Differential
Sense	Output Voltage	V− to V+
V_{INH}	Input Voltage	V_{INL} −0.3V to B+
V_{INL}	Input Voltage	B− to V_{INH} +0.3V
I_{OUT}	Output Current	−60 mA to +60 mA
T_J	Junction Temperature	150°C
T_A	Operating Ambient Temperature Range	−0°C to +75°C
T_{ST}	Storage Temperature	−65°C to +150°C
P_D	Power Dissipation (T_A = 25°C) (See Curves)	3.1W

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

T_A = 25°C, V+ = B+ =15V, V− = B− = −10V, R_{SHUNT+} = R_{SHUNT-} = 6.5Ω, no load. Data, E, and OE from −1.6V to −0.8V. I_{SR} = 800 μA. V_{INH} = 5V, V_{INL} = −1.6V

Parameter	Description	Min	Typ	Max	Test Level	Units
I_S	(V+) + (B+), (V−) + (B−) Supply Currents		52	60	I	mA
I_S, dis	(V+) + (B+), (V−) + (B−) Supply Currents, Disabled		17	25	I	mA
I_{VINH}		−20	−3	20	I	μA
I_{VINL}		−20	2	20	I	μA
I_{DATA}		−30	−15	30	I	μA
I_{OE}	OE Input Current	−30	−14	30	I	μA
I_E	E Input Current	−20	7	20	I	μA
V_{SR}	Voltage at I_{SR} Pin	0	20	40	I	mV
I_{SHUNT+}, I_{SHUNT-}			4	7	I	mA
V_{SHUNT+}, V_{SHUNT-}	Sense Threshold at Shunts	160	200	250	I	mV
I_{SENSE}	Sense Output Currents	1	1.5	2	I	mA
V_{OS}	Output Offset, Data High, V_{INH} = 0V, V_{INL} = −1.6V	−50		50	I	mV
	Data Low, V_{INL} = 0V, V_{INH} = 5V	−100		100	I	mV

TD is 2.7in

DC Electrical Characteristics — Contd.

T_A = 25°C, V+ = B+ = 15V, V− = B− = −10V, R_{SHUNT+} = R_{SHUNT-} = 6.5Ω, no load. Data, E, and OE from −1.6V to −0.8V. I_{SR} = 800 μA. V_{INH} = 5V, V_{INL} = −1.6V

Parameter	Description	Min	Typ	Max	Test Level	Units
Eg	Gain Error Data High, V_{INH} from 0V to 5V, V_{INL} = −1.6V, No Load	−1.5	−0.6	0	I	%
	Data Low, V_{INH} = 5V, V_{INL} from −5V to 0V, No Load	−1.5	−0.6	0	I	%
NL	Gain Nonlinearity Data High, V_{INH} from 0V to 10V, V_{INL} = −1.6V, No Load		0.04		V	%
	Data Low, V_{INH} = 5V, V_{INL} from −10V to 0V, No Load		0.06		V	%
PSRR	Power Supply Rejection Ratio of V_{OUT} with Respect to B+, B−, Shunt+, or Shunt− Potential		2.2		V	mV/V
R_o, en	Output Resistance, Enabled, Il = ±20 mA	4.5	6	7.5	I	Ω
R_o, dis	Output Resistance, Output Disabled, V_O = −1.6V to −5V, EL1056C	20K	100K		I	Ω
	EL1056AC	100K	200K			
I_o, dis	Output Current, Output, Disabled, V_O = 0V	−20	5	20	I	μA
I_o, off	Output Leakage, E Low, (Shut-Down), V_O = 0V, EL1056C	−20		20	I	μA
	EL1056AC	−150		150	I	nA

AC Electrical Characteristics

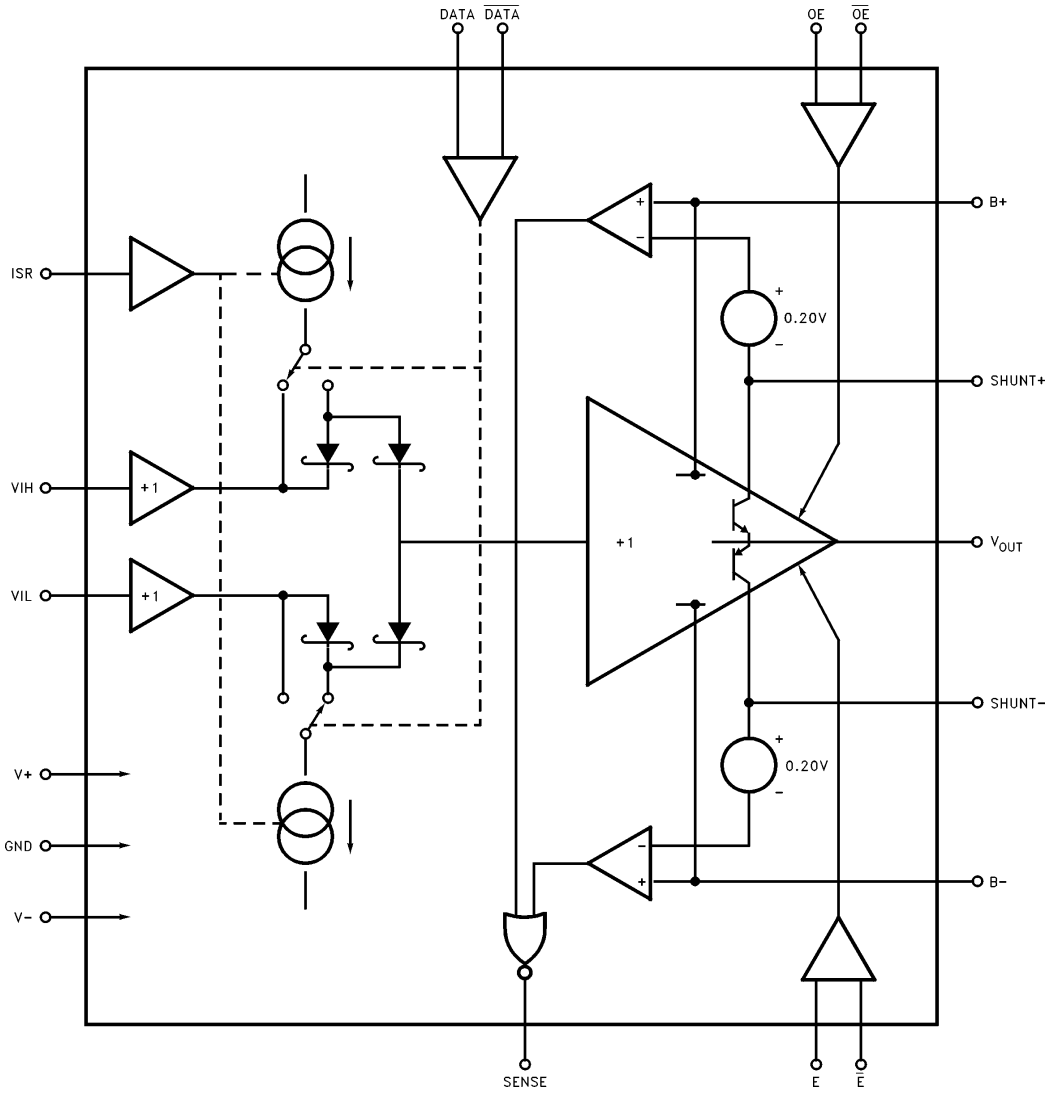
T_A = 25°C, V+ = B+ = +15V, V− = B− = −10V, R_{SHUNT+} = R_{SHUNT-} = 6.5Ω. R_L = 500Ω. 50Ω + 22 pF snubber included at output. Data E, and OE from −1.6V to −0.8V. I_{SR} = 800 μA. ECL swing is defined by V_{INH} = −0.8V and V_{INL} = −1.6V, CMOS swing defined by V_{INH} = 5V and V_{INL} = 0V. Propagation delay is measured at 0.4V movement of output.

Parameter	Description	Min	Typ	Max	Test Level	Units
T_{PD}	Propagation Delay, CMOS Swing	1.0	3.0	4.5	I	ns
Dis	Propagation Delay Dispersion					
	Due to Output Edge Direction		250	450	I	ps
	From ECL to CMOS Swings		250	450	I	ps
	Due to Repetition Rate		80		V	ps
SR	Output Slew Rate, CMOS Swing, 20%–80%	0.8	1	1.2	I	V/ns
SR_{sym}	Slew Rate Symmetry		3	10	I	%
TR	Output Rise Time, ECL Swing, 20%–80%		2.2		V	ns
OS	Output Overshoot					
	CMOS Swing		190	500	I	mV
	ECL Swing (I_{SR} = 350 μA)		65		V	mV
T_{dis}	Output Disable Delay Time		4.7	6.5	I	ns
T_{en}	Output Enable Delay Time		6.0	8.5	I	ns
C_o, dis	Output Capacitance in Disable		3		V	pF
T_{off}	Power-Down Delay Time		0.5		V	μs
T_{on}	Power-On Delay Time		90		V	ns
C_o, off	Output Capacitance in Power-Down		50		V	pF
T_{sense}	Comparator Delay Time — Switching ON		1.5		V	μs
	Switching Off		0.4		V	μs

TD is 2.3in

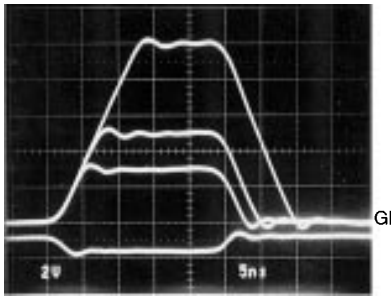
TD is 3.6in

Block Diagram



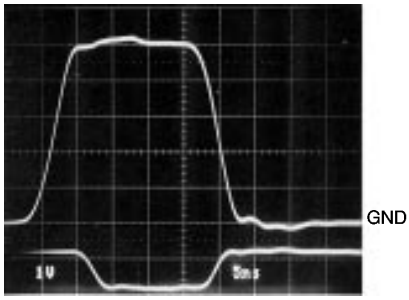
Typical Performance Curves

10V, CMOS, TTL, and ECL Outputs into 550Ω Load



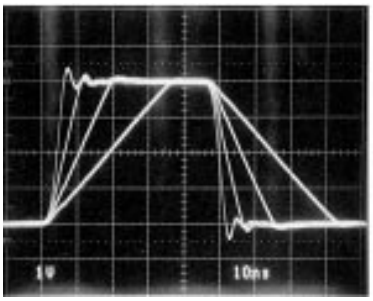
1056-6

CMOS and ECL Outputs As Seen at the End of an Unterminated Cable, Backmatched at Driver



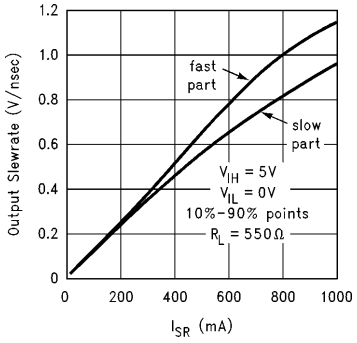
1056-7

CMOS Output at I_{SR} = 100 μA, 200 μA, 400 μA, and 1000 μA



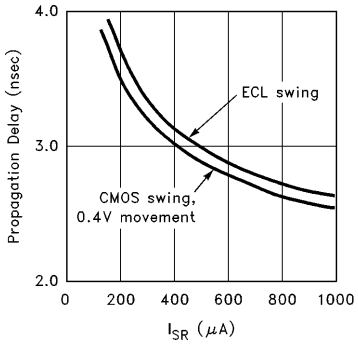
1056-8

Output Slewrate vs I_{SR} (Two Samples)



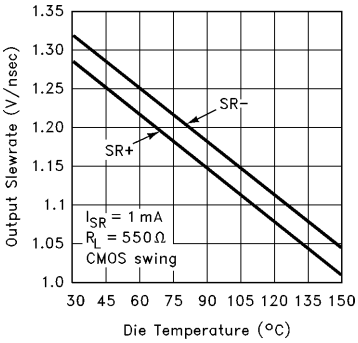
1056-9

Propagation Delay vs I_{SR}



1056-10

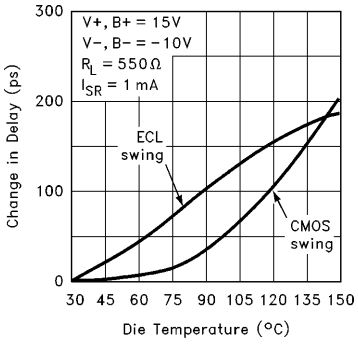
Output Slewrate vs Die Temperature



1056-11

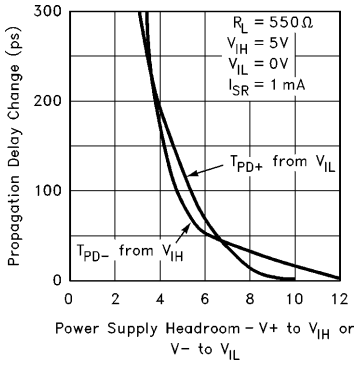
Typical Performance Curves — Contd.

Propagation Delay Change with Die Temperature



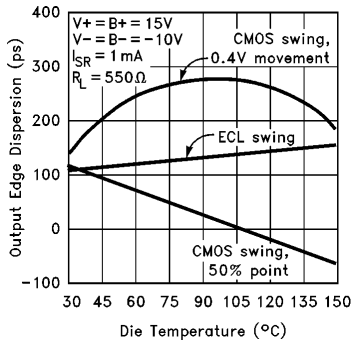
1056-12

Change in Propagation Delay with Power Supply Headroom



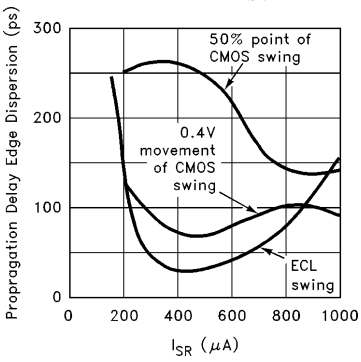
1056-13

Output Edge Dispersion vs Temperature



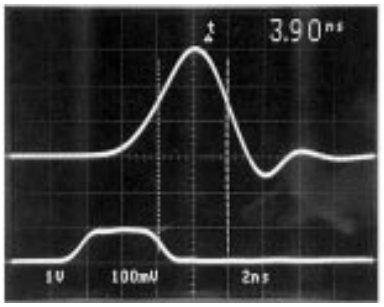
1056-14

Edge Dispersion vs I_{SR}



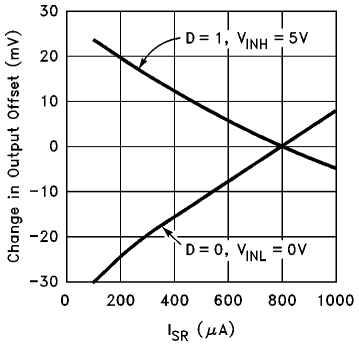
1056-15

Minimum Output Pulse Width



1056-16

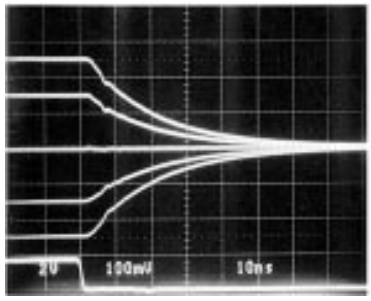
Output Offset vs I_{SR}



1056-17

Typical Performance Curves — Contd.

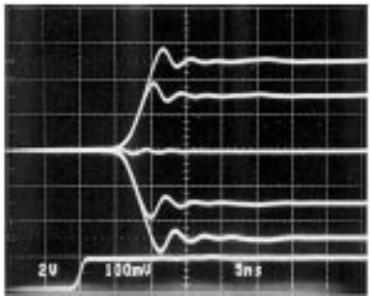
Tristate Turn-off Waveforms



V_{OUT}
GND
V_{OE}

1056-18

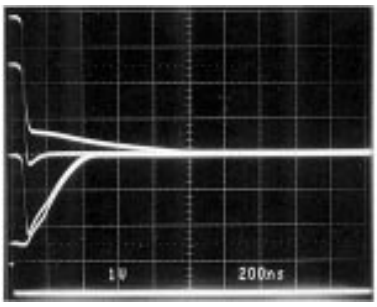
Tristate Turn-on Waveforms



V_{OUT}
GND
V_{OE}

1056-19

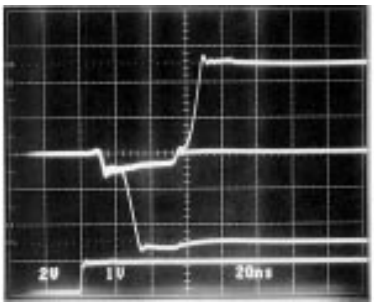
Power-Down Disable Waveforms



V_{OUT}
GND
V_E

1056-20

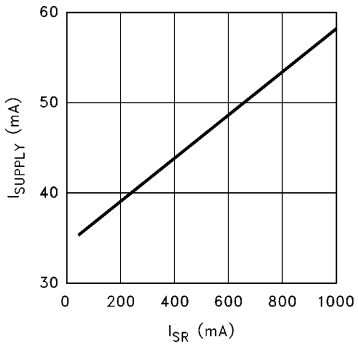
Power-Down Enable Waveforms



V_{OUT}
GND
V_E

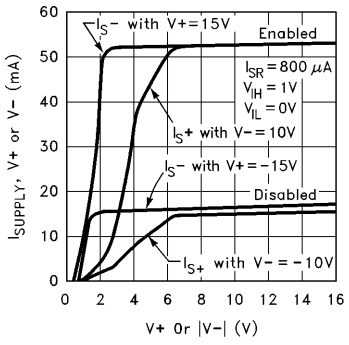
1056-21

Supply Current vs I_{SR}



1056-22

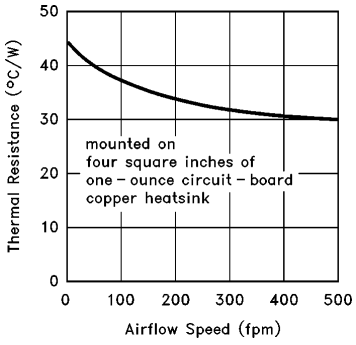
Total Supply Current vs Supply Voltage



1056-23

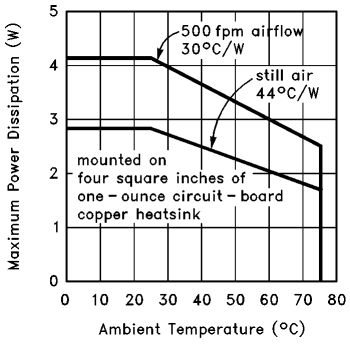
Typical Performance Curves — Contd.

Mounted Thermal Resistance of Package vs Airflow Speed



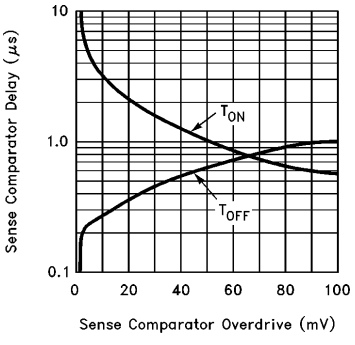
1056-24

Package Power Dissipation vs Ambient Temperature



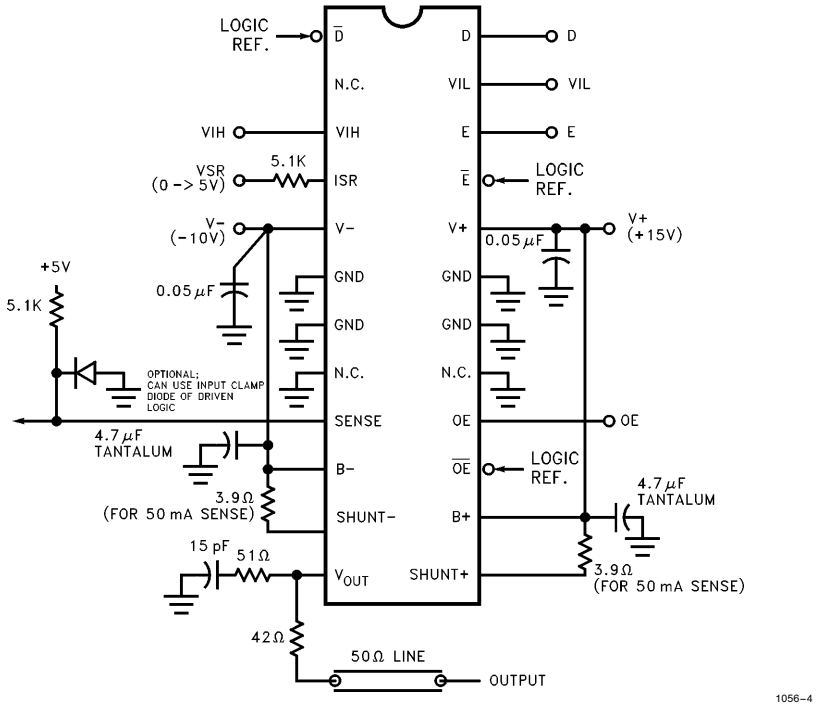
1056-25

Sense Comparator Delay vs Overdrive



1056-26

EL1056 Used in CMOS and TTL Systems



1056-4

Applications Information

Functional Description

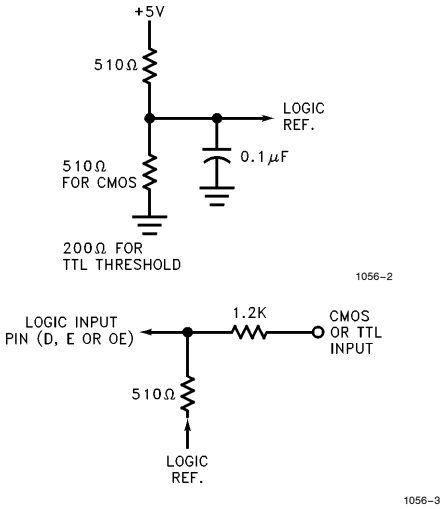
The EL1056 is a fully integrated pin driver for automatic test systems. Pin drivers are essentially pulse generators whose high and low levels can be externally programmed and accurately switched in time, as well as incorporating an output switch to disconnect the driver from a measurement bus. Additionally, the EL1056 has programmable slewrate.

Control Voltage Inputs

The analog level inputs are named V_{INH} and V_{INL}, and the output replicates them as controlled by logic inputs. The analog inputs are buffered and have bandwidths of 35 MHz and slewrates of 25V/μs. For full slewrate, 4V of headroom should be given to the inputs, that is V_{INH} should be 4V less than V+ or B+, and V_{INL} should be 4V more positive than V− or B−. At lower slewrates (I_{SR} = 500 μA or less), 3V of headroom will suffice. Insufficient headroom causes distorted output waveforms or delay errors in output transitions. V_{INH} may be lower in voltage than V_{INL}, but the output will not follow the control logic correctly. Furthermore, V_{INH} should be 200 mV more positive than V_{INL} (the minimum output amplitude) for accurate switching.

Logic Inputs

The logic inputs are all differential types, with both NPN and PNP transistors connected to each terminal. They are optimized for differential ECL drive, which optimizes + to − edge delay time matching. Larger logic levels can introduce feedthrough glitches into the output waveform. For CMOS input logic levels, an ECL output waveform will show feedthrough when the input risetime is shorter than 8 ns, differential or single-ended. CMOS output swings show less aberration, and the EL1056 can tolerate a 4 ns single-ended risetime or 2 ns risetime for differential inputs. Attenuating CMOS or TTL inputs to 1 Vp-p will eliminate all logic feedthrough as shown in Figure 1.



Alternate Logic Interface
Figure 1

Slewrate Control

The slewrate is controlled by the I_{SR} input. This is a current input and scales the output slewrate by a nominal 1.25V/ns/mA. The slewrate maintains calibration and symmetry to at least as slow as 0.2V/ns. The practical upper end of I_{SR} is 1 mA, and supply current increases with increasing I_{SR}.

The I_{SR} control can be used to adjust individual pin drivers to a system standard, by adjusting the value of its series resistor. Slewrate can also be slowed to reduce output ringing and crosstalk.

With ECL output swings, there is not enough voltage excursion to incur slewrate delays to 50% logic threshold. The risetime, delays, and dispersions do not degrade with reasonably reduced I_{SR}, and overshoot will reduce markedly. An I_{SR} of 350 μA produces a very good ECL output, and driver dissipation is also reduced.

Applications Information — Contd.

The I_{SR} pin is connected to the emitter of a PNP transistor whose base is biased a diode below ground (see Figure 2). Thus, the I_{SR} input looks like a low impedance for positive input currents, and is biased close to ground. A protection diode absorbs negative currents, and the input PNP will not conduct. In power-down mode, the PNP releases its current sink and the external circuit must not present more than 6V to the disabled I_{SR} input, or emitter-base damage to the NPN will occur within the driver. A signal diode or zener can be used to clamp the I_{SR} input for positive input voltages if the voltage on the I_{SR} resistor is potentially greater than 6V when the driver is in power-down mode.

Output Stage–Tristate Mode

In tristate mode (OE low) the output transistors have their emitter-base junctions reverse-biased by a diode voltage. This turn-off voltage is in fact provided by an internal buffer whose input is connected to the output pin (see Figure 3). Transistors Q1–Q4 form the output buffer in normal mode. The tristate mode buffer Q5–Q8 replicates externally impressed voltages from the output pin onto the internal schottky switch node. They also turn off Q1–Q4 by a reverse diode voltage between bases and emitters, effectively bootstrapping the internal voltages, so that no transistor's base-emitter junction is reverse-biased by a damaging potential. Another benefit is that the capacitance seen at the output in tristate mode is reduced.

Because the tristate buffer's input is connected to the output terminal, the output is quite "alive" during tristate. For instance, the input bias current of the buffer is seen as the tristate "leakage", and its variation with applied voltage becomes tristate input impedance.

The tristate input current is like a current source, and it can drag an output to unpredictable voltages. It is not a danger to connect a tristated output that has drifted to, say, −6V to a logic pin of a device to be tested. The tristate output current will simply comply with whatever voltage the connected part normally establishes.

The tristate input impedance is also quite active over frequency. The output can oscillate when presented with resonant or inductive impedances. To prevent this, a snubber should be connected from output to ground, consisting of a resistor in series with a small capacitor. The snubber can also reduce the reflections of the coaxial line when driven from the far end, since the line appears to have an open termination during tristate. Typical values for the resistor are 50Ω to 75Ω, and 12 pF to 22 pF for the series capacitor. The effect of the snubber is to "de-Q" resonances at the output.

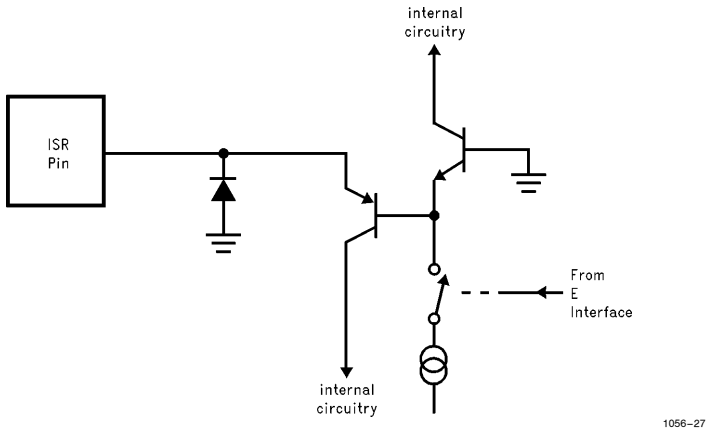


Figure 2. I_{SR} Pin Circuitry

Applications Information — Contd.

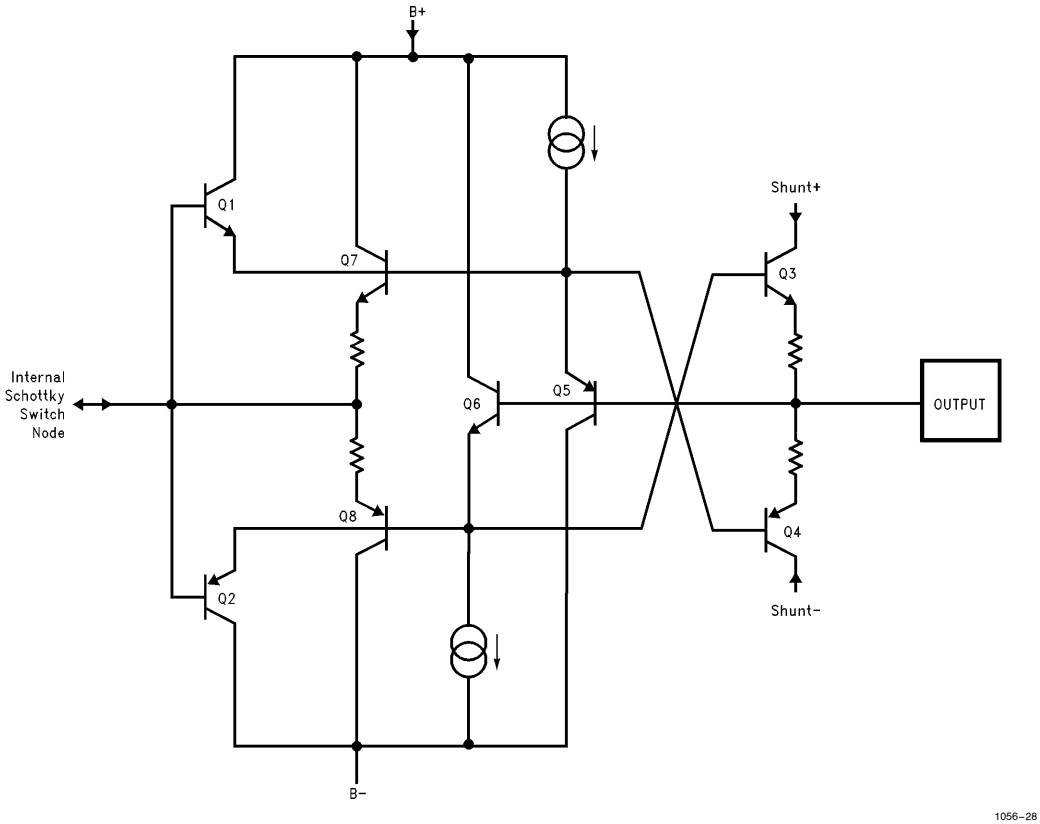


Figure 3. Output Stage Circuit in Tristate Mode

Output Stage–Normal Mode

Capacitive loads can cause the output stage to ring. Little ringing occurs for loads less than 25 pF, but substantial ringing for more than 40 pF. Terminated transmission lines cause no ringing, and actually suppress it as a snubber does. A terminated line draws heavy DC current, however, and greatly raises dissipation.

Driving a back-terminated line also causes little ringing and does not cause DC dissipation. The series matching resistor between the EL1056 output and a back-terminated line also serves to isolate the driver from capacitive loads and short-circuits. The slewrate of the driver slows by about 10% when driving a 50Ω back-matched line, as seen at the end of the line. The snubber can be on either side of the back-match resistor. When placed on the line side it creates a high-frequency termination for the line when the driver is tristated, but it slows the output small-signal risetime by about 10% (although not slew-rate). When placed on the driver side of the back-match resistor, no speed reduction occurs in normal mode but the cable is more poorly terminated in tristate.

The transient currents that occur when driving capacitive or back-matched loads can be very high, approaching 100 mA. The driver is capable of outputting a peak of 140 mA, but long-term

Applications Information — Contd.

load currents must be limited to 60 mA. Short-circuits can rapidly destroy the EL1056, although the part will survive for 20 ms periods. If there is the possibility of output load fault the overcurrent sense circuitry should be used to signal alarm to the controlling system, which should ultimately activate the tristate mode to relieve the output stage. Driving large static currents also raises internal dissipation and should be part of the thermal budget.

The collectors of the output transistors are connected to the Shunt terminals, and the output stage drivers' collectors are connected to the B+ and B− terminals (see Figure 4). The Shunt lines can have transient currents as high as 120 mA and are separated from the V+ and V− terminals to keep switching noise out of the control and logic circuitry. A bypass capacitor should be connected to the B+ and B− terminals.

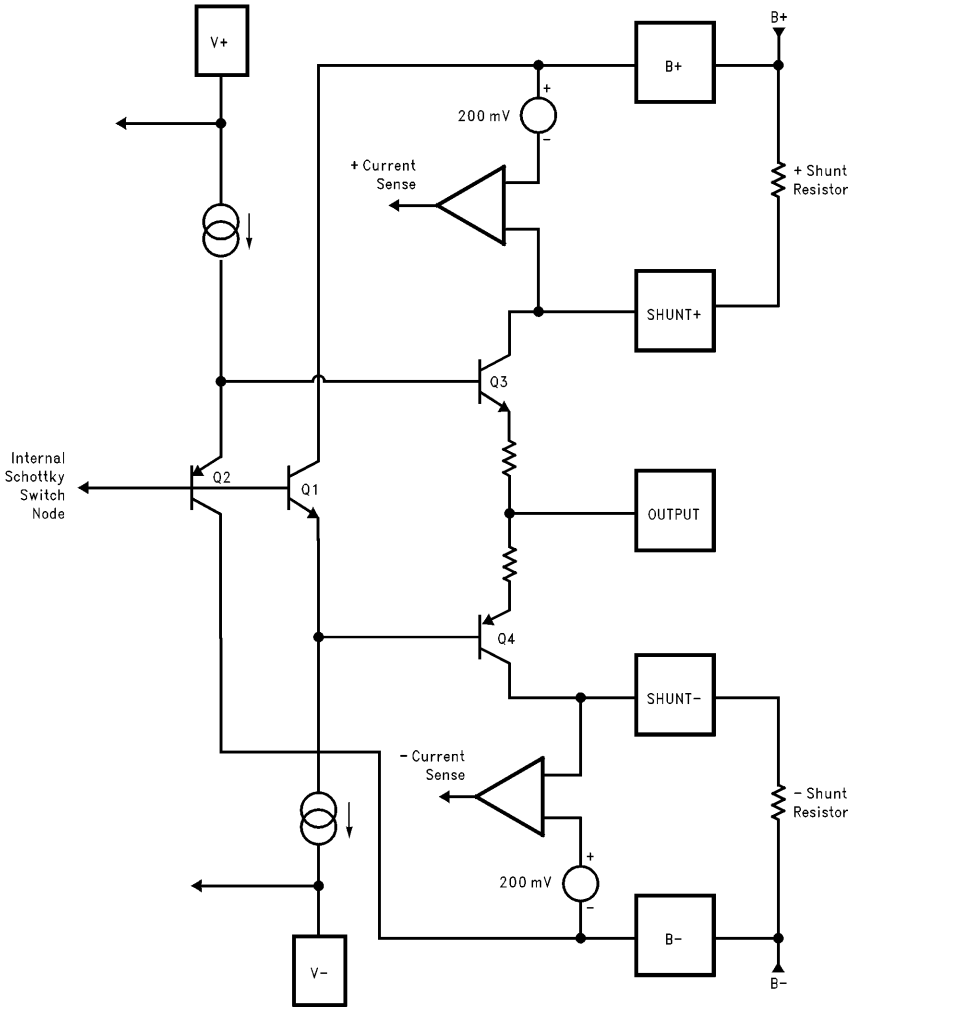


Figure 4. Output Stage in Normal Mode

Applications Information — Contd.

Overcurrent Protection

The sense comparators are available to alert the test system's controller that the driver is outputting excessive current. Shunt resistors are connected from B+ to Shunt+ and B− to Shunt−. When the internal comparators sense more than a nominal 200 mV drop on the shunts, they cause a 1.5 mA current to be sunk from the Sense terminal. The comparators are of "slow attack, fast decay" design, so that transient load currents will not trigger a sense output; only a sustained overcurrent will.

The sense resistors must not be inductive, and the skin resistance of long, narrow connections between Shunt and B+ or B− can cause transient voltages that produce output overshoot (but not ringing).

The Sense output is simply a switched current source connected to V−. It can be used to interface to CMOS, TTL, or ECL inputs. For CMOS and TTL, it can be connected to a pull-up resistor to +5V of 10K value. This establishes a logic high value, and a clamp diode (internal to TTL) establishes a low level of −0.6V. For ECL, a gate should be available to provide a static logic high level. An 820Ω pull-up resistor is wired to that output. The logic low will be more negative than is usual for ECL, but this will cause no problem. In all cases, multiple Sense outputs may be connected together from many drivers to effect a wired-or function.

A further protection scheme is to provide a series resistor from B+ to V+ and B− to V−. The resistor serves to limit the output fault current by allowing B+ and B− voltages to sag under heavy load. This also reduces the dissipation on the output transistors for valid loads. Because B+ and B− are separately bypassed, these voltages will sustain under transient loads and dynamics will not be affected.

Output Accuracy

The accuracy of the output voltage depends on several factors. The first is the gain error from V_{INH} or V_{INL} to the output, unloaded. The gain error is nominally −0.6%, and has a few tenths of a percent variation between parts. The second is supply rejection. If the B+, B−, Shunt+, or Shunt− voltages are different from those used by Elantec to test the part, there will be about 2.2 mV systematic shift in output offset per volt of supply variation. The V+ and V− supplies have much less influence on output error. Finally, there is a random V_{OS} error as specified in the data table.

Of course, the finite output impedance of the EL1056 will cause additional output error when the driver is loaded.

Power-Down

The EL1056 incorporates a power-down feature that drastically reduces power consumption of an unused driver and also drops the output leakage current to nanoamperes ("A" grade only). The output is not a low capacitance in this mode, however, and transients driven from the cable can momentarily turn on the output transistors. Power-down is intended to allow the switching of accurate DC meters onto the bus without having to relay out the driver's leakage current. It takes about 40 μs for the output leakage to sag to nanoamperes, but this is still much faster than relays or voltmeters.

Power-down is controlled by the E and $\overline{E}$ differential inputs. There is no problem with logic amplitude or slewrate, and input resistor networks are not needed.

Power Down — Contd.

Supply and Input Bypassing

The V+, B+, V−, and B− leads should be bypassed very closely with 0.1 μF capacitors, preferably chip type. There should be a wide ground plane between bypasses, and this can be the heatsink copper. It is wise to also have a 4.7 μF tantalum bypass capacitor within a couple of inches to the driver.

The logic inputs are active device bases, and can oscillate if presented with inductive lines. A local resistor of 1000Ω or less to ground will suffice in de-Q'ing any resonance. A 100 pF or larger capacitor can also serve as a bypass.

Thermal Considerations

The package of the EL1056 includes two fused leads on each side which are connected to the internal die mounting metal. Heat generated in the die flows through the mounting pad to the fused leads, and then to the circuit-board copper, achieving a thermal resistance to air around 40°/W. Characterization curves show the thermal resistance versus airflow rate. Consult the EL1056 Demonstration Board literature for a suggested board pattern. Note that thicker layers of copper than we used improves the thermal resistance further, to a limit of 22°C/W for an "infinite heatsink" directly soldered to the fused leads.

As a practical limit, the die temperature should be kept to 125°C rather than the allowable 150°C to retain optimum timing accuracies.

BLANK

EL1056AC/EL1056C
Monolithic High-Speed Pin Driver

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

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