élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2005/EL2005C

High Accuracy Fast Buffer

Features

- Low input current—50 pA
- Low offset and drift—2 mV/25 µV/°C
- High slew rate—1500 V/µs
- Fast rise and fall time—2.5 ns
- High input resistance—1000 GΩ
- Bandwidth—140 MHz
- Pin compatible with ELH0033
- MIL-STD-883 Revision C devices manufactured in U.S.A.

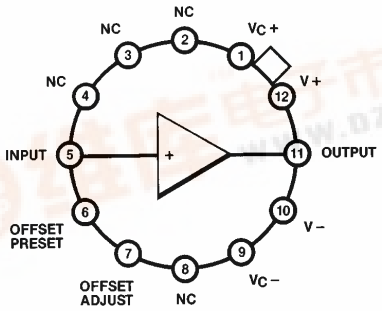
Advantages

- No input loading
- Input current independent of input voltage
- Eliminates offset adjustments
- Drives cables directly

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2005CG	−25°C to +85°C	TO-8	MDP0002
EL2005G	−55°C to +125°C	TO-8	MDP0002
EL2005G/883B	−55°C to +125°C	TO-8	MDP0002

Connection Diagram



2005-1

Top View

Note: Case is electrically isolated.

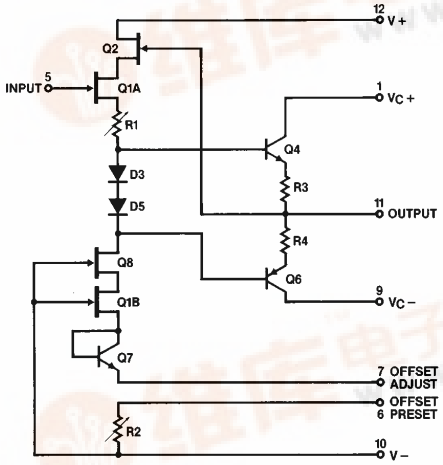
General Description

The EL2005 is a high-speed, FET input buffer similar to ELH0033 and EL2004 but with input specifications significantly improved over the previous types. The input stage employs a cascode configuration to maintain constant input characteristics over the full ±10V input range. The input looks like a 3 pF capacitor to ground in almost all cases since the DC bias current is constant with input voltage. In sample and hold circuits this results in an order of magnitude improvement in hold characteristics. Input offset voltage and offset voltage drift are also improved a factor of two over previous types.

These excellent DC characteristics are complemented by a wide 140 MHz bandwidth while the 1500 V/µs slew rate and excellent phase linearity of the ELH0033 family are preserved allowing direct plug-in replacement for upgraded performance. (For even faster operation see EL2004.)

Elantec facilities comply with MIL-I-45208A and are MIL-STD-1772 certified. Elantec's Military devices comply with MIL-STD-883B Revision C and are manufactured in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance Policy and procedures request brochure QRA-1.

Simplified Schematic



2005-2

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ − V−)	40V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	40V		EL2005	−55°C to +125°C
P_D	Power Dissipation (See curves)	1.5W		EL2005C	−25°C to +85°C
I_{OC}	Continuous Output Current	±100 mA	T_J	Operating Junction Temperature	175°C
I_{OP}	Peak Output Current	±250 mA	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature (Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, V_{IN} = 0V, $T_{MIN} \le T_A \le T_{MAX}$

Parameter	Description	Test Conditions	EL2005				EL2005C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Output Offset Voltage	$R_S \le 100$ kΩ, T_J = 25°C (Note 1)		2	5	I		3	10	I	mV
		$R_S \le 100$ kΩ			10	I			15	III	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Offset Voltage	R_S = 100Ω		25		V		25		V	µV/°C
PSRR	Supply Rejection	±10V ≤ V_S ≤ ±20V	65	75		I	60	75		II	dB
I_B	Input Bias Current	T_J = 25°C (Notes 1 and 3)		2	50	I		5	100	I	pA
		T_A = 25°C (Notes 2 and 3)		50	500	IV		100	1000	IV	pA
		$T_J = T_A = T_{MAX}$		2	5	I		0.5	5	III	nA
A_V	Voltage Gain	R_S = 100Ω, R_L = 1 kΩ, V_{IN} = ±10V	0.97	0.98	1.0	I	0.96	0.98	1.0	II	V/V
		R_S = 100Ω, R_L = 100Ω, v_{IN} = ±10V	0.88	0.95	0.98	I	0.88	0.95	0.99	II	V/V
R_{IN}	Input Impedance	R_L = 1 kΩ, −10V ≤ V_{IN} ≤ ±10V	2×10^9	10^{12}		I	2×10^9	10^{12}		IV	Ω
		T_J = 25°C (Note 1), R_L = 1 kΩ	10^{10}	10^{12}		I	10^{10}	10^{12}		I	Ω
R_O	Output Impedance	R_L = 1 kΩ, V_{IN} = ±1V		4	8	I		4	9	II	Ω

TD is 3.8in

DC Electrical Characteristics $V_S = \pm 15V$, $V_{IN} = 0V$, $T_{MIN} \leq T_A \leq T_{MAX}$ — Contd.

Parameter	Description	Test Conditions	EL2005				EL2005C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_O	Output Voltage Swing	$V_{IN} = \pm 14V$, $R_L = 1\ k\Omega$		± 12.5		V		± 12.5		V	V
		$V_{IN} = \pm 10.5V$, $R_L = 100\Omega$, $T_A = 25°C$	± 9	± 9.8		I	± 9	± 9.8		I	V
I_S	Supply Current	$V_{IN} = 0$ (Note 1)		19	22	I		19	24	II	mA
PD	Power Consumption	$V_{IN} = 0$		570	660	I		570	720	II	mW

AC Electrical Characteristics $T_C = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 1\ k\Omega$

Parameter	Description	Test Conditions	EL2005				EL2005C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
SR	Slew Rate	$V_{IN} = \pm 10V$, $V_{OUT} = \pm 5V$	1000	1500		III	1000	1500		III	V/μs
BW	Bandwidth	$V_{IN} = 1\ V_{rms}$		140		V		140		V	MHz
ϕ_{NL}	Phase Non-Linearity	BW = 1 MHz to 20 MHz		2		V		2		V	Degree
t_r	Rise Time	$\Delta V_{IN} = 0.5V$		2.5		V		2.5		V	ns
t_P	Propagation Delay	$\Delta V_{IN} = 0.5V$		1.0		V		1.0		V	ns
HD	Harmonic Distortion	f >1 kHz		<0.1		V		<0.1		V	%
A_V	Voltage Gain	$R_S = 100\Omega$, $V_{IN} = 1\ V_{rms}$, f = 1 kHz	0.97	0.99	1.0	I	0.96	0.99	1.0	II	V/V
R_O	Output Impedance	$V_{IN} = 1\ V_{rms}$, f = 1 kHz		4	8	I		4	9	II	Ω

Note 1: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperatures will exceed the value at $T_J = 25°C$. When supply voltages are $\pm 15V$, no-load operating junction temperatures may rise 40°C to 60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs Temperature graph for expected values.

Note 2: Measured in still air seven minutes after application of power.

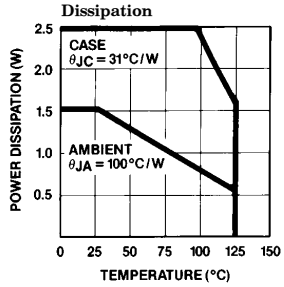
Note 3: Input bias current is guaranteed over the input range of $-10V \leq V_{IN} \leq +10V$.

TD is 1.7in

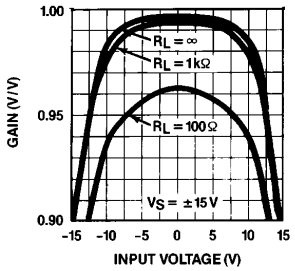
TD is 2.5in

Typical Performance Curves

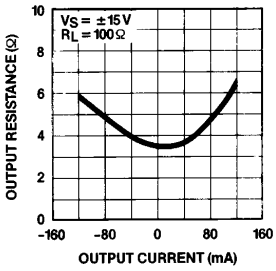
Maximum Power Dissipation



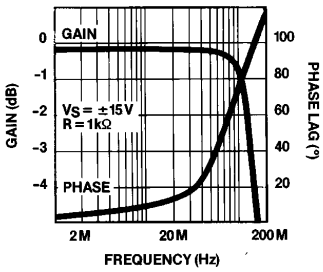
Gain vs Input Voltage



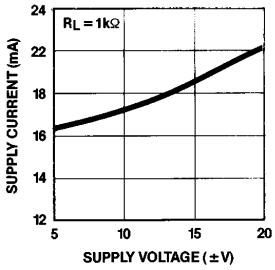
Output Resistance vs Output Current



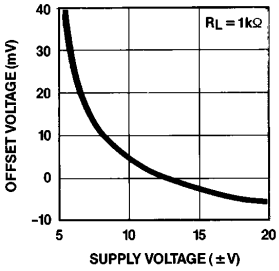
Frequency Response



Supply Current vs Supply Voltage



Offset Voltage vs Supply Voltage



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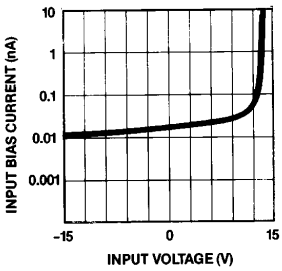
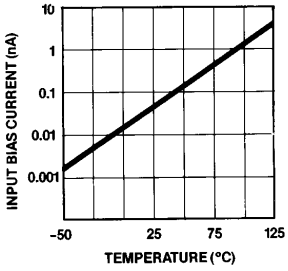
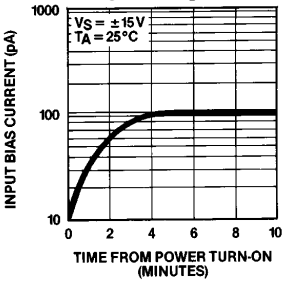
Input Bias Current vs Input Voltage



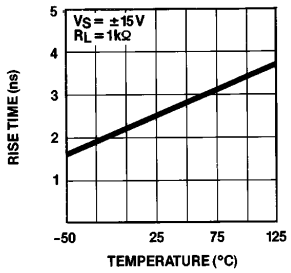
Input Bias Current vs Temperature



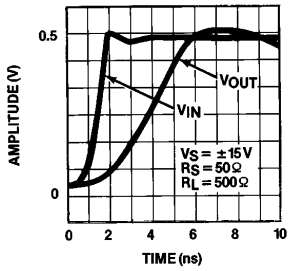
Input Bias Current During Warm-up



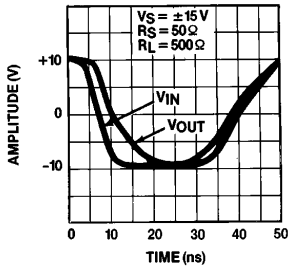
Rise Time vs Temperature



Small Signal Pulse Response



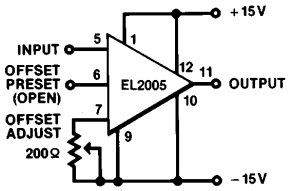
Large Signal Pulse Response



2005–4

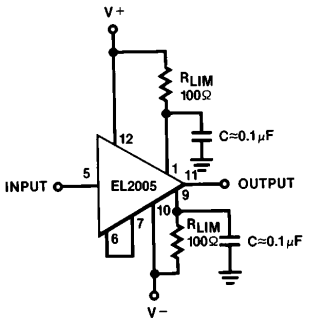
Typical Applications

Offset Zero Adjust



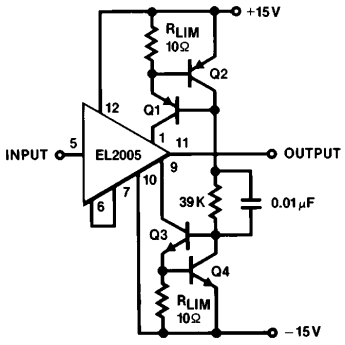
2005–5

Using Resistor Current Limiting



2005–6

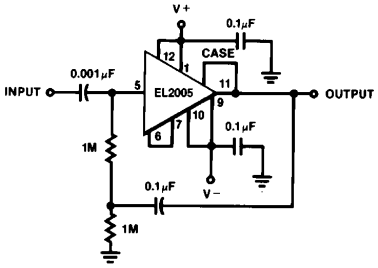
Current Limiting Using Current Sources



2005–7

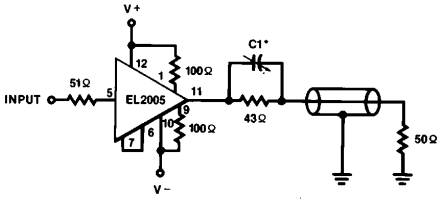
Q1 = Q2 = 2N2905
Q3 = Q4 = 2N2219

High Input Impedance AC Coupled Amplifier



2005–8

Coaxial Cable Driver

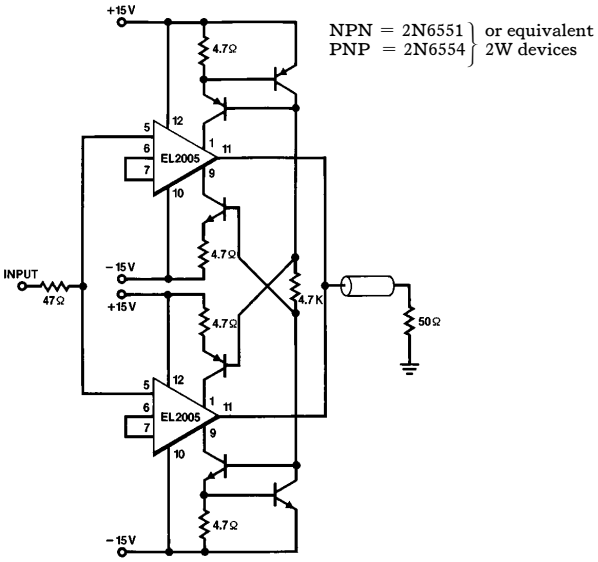


*Select C1 for optimum pulse response

2005–9

Typical Applications — Contd.

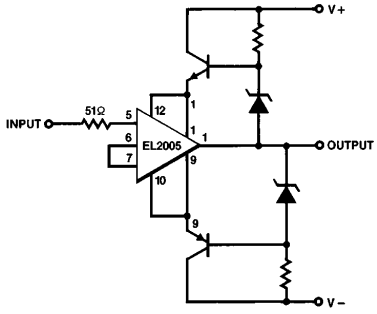
50Ω Cable Driver with Short Circuit Protection



NPN = 2N6551 } or equivalent
PNP = 2N6554 } 2W devices

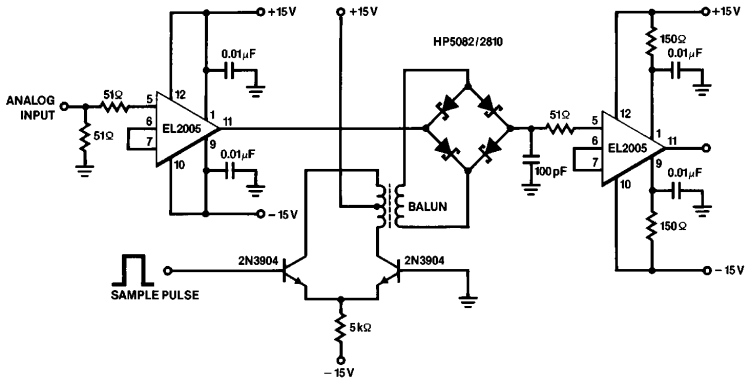
2005–10

Bootstrapped Supplies for High Voltage Applications



2005–11

High-Speed Sample and Hold



2005–12

Applications Information

Recommended Layout Precautions

RF/video printed circuit board layout rules should be followed when using the EL2005 since it will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively, the case should be connected to the output to minimize input capacitance.

Offset Voltage Adjustment

The EL2005's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. The pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 200Ω between the offset adjust pin and V− as illustrated on page 4.

Operation from Single or Asymmetrical Power Supplies

This device type may be readily used in applications where symmetrical supplies are unavailable or not desirable. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V+ - V-)}{2} = 0.005\ (V+ - V-)$$

where: A_V = No load voltage gain, typically 0.99
$V+$ = Positive supply voltage
$V-$ = Negative supply voltage

For example, with $V+ = +5V$ and $V- = -12V$, ΔV_O would be −35 mV. This may be adjusted to zero as described above.

Short Circuit Protection

In order to optimize transient response and output swing, output current limit has been omitted from the EL2005. Short circuit protection may be added by inserting appropriate value resistors between $V+$ and V_C+ pins and $V-$ and V_C- pins as shown on page 4.

Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V+}{I_{SC}} = \frac{V-}{I_{SC}}$$

where: $I_{SC} \leq 100$ mA for EL2005

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C+ and V_C- pins with capacitors to ground will retain full output swing for transient pulses. An alternate active current limit technique that retains full DC output swing is also shown on page 4. In this circuit, the current sources are saturated during normal operation thus applying full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload.

$$R_{LIM} \cong \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{60\ mA} = 10\Omega$$

Capacitive Loading

The EL2005 is designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from ($C \times dV/dt$) should be limited below absolute maximum peak current ratings for the devices.

Thus:

$$\frac{\Delta V_{IN}}{\Delta t} \times C_L \leq I_{OUT} \leq \pm 250\ mA$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below the total package power rating:

$$P_Dpkg \geq P_{DC} + P_{AC}$$

$$P_Dpkg \geq (V+ - V-) \times I_S + P_{AC}$$

$$P_{AC} \cong (V_{P\text{-}P})^2 \times f \times C_L$$

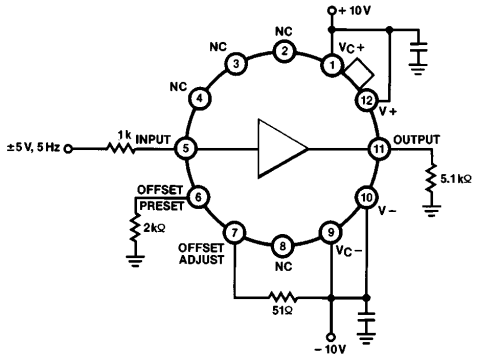
where: $V_{P\text{-}P}$ = Peak-to-peak output voltage swing
f = Frequency
C_L = Load Capacitance

Applications Information — Contd.

Operation within an Op Amp Loop

The EL2005 may be used as a current booster or isolation buffer within a closed loop with op amps such as the ELH0032 and HA2500 and HA2600 series. An isolation resistor of 47Ω should be used between the op amp output and the input of EL2005. The wide bandwidth and high slew rates of the EL2005 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

Burn-In Circuit



2005–13

Hardware

In order to utilize the full drive capabilities of the EL2005, it should be mounted with a heatsink, particularly for extended temperature operation. The case is isolated from the circuit and may be connected to system chassis.

IMPORTANT!

Power supply bypassing is necessary to prevent oscillation with the EL2005 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within ¼″ to ½″ of the device package) to a ground plane. Capacitors should be one or two 0.1 μF in parallel; adding a 4.7 μF solid tantalum capacitor will help in troublesome instances.

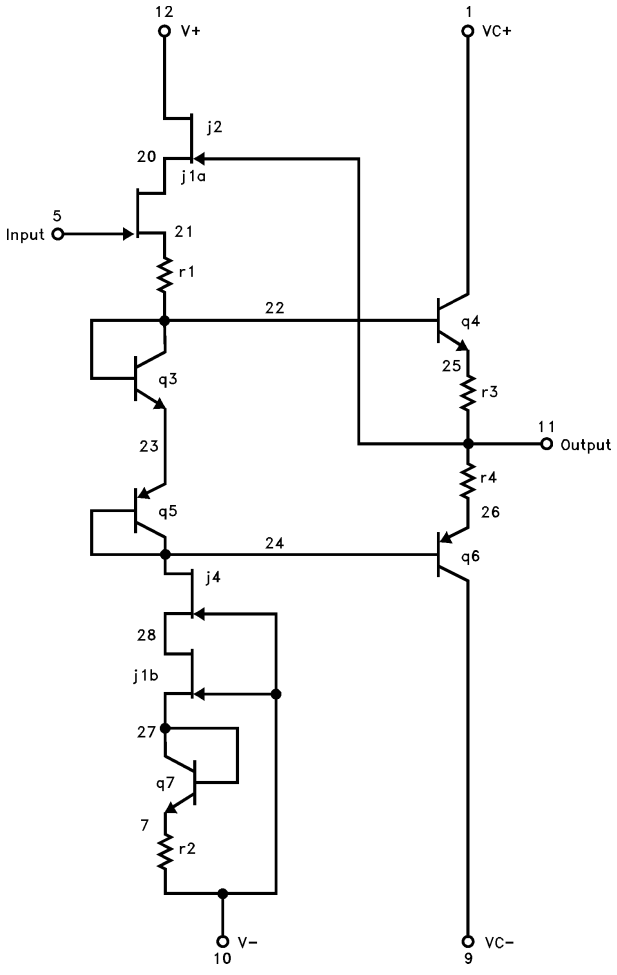
EL2005 Macromodel

```
* Connections:      input
*                   |      V+
*                   |      |      +Vc+
*                   |      |      |      V-
*                   |      |      |      |      Vc-
*                   |      |      |      |      |      output
*                   |      |      |      |      |      |
.subckt M2005       5      12     1      10     9      11
* Models
.model qn npn (is=5e-14 bf=150 vaf=100 rc=1 rb=5 re=1 ikf=200mA
+cje=5pF cjc=5pF mje=.42 mjc=.23 tf=.3nS tr=200nS br=5 vtf=0)
.model qp pnp (is=5e-14 bf=150 vaf=100 rc=.2 rb=3 re=1 ikf=100mA
+cje=5.7pF cjc=4pF tf=.3nS mje=.32 mjc=.43 tr=170nS br=5 vtf=0)
.model qfa njf (vto=-8V beta=2.344e-3 cgd=10pF cgs=7pF lambda=671e-6)
.model qfb njf(vto=-4V beta=1.06e-3 cgd=3pF cgs=3pF)
* Resistors
r1 21 22 30
r2 7 10 30
r3 25 11 3
r4 11 26 3
* Transistors
j1a 20 5 21 qfb
j1b 28 10 27 qfb
j2 12 11 20 qfa
j4 24 10 28 qfa
q3 22 22 23 qn
q4 1 22 25 qn
q5 24 24 23 qp
q6 9 24 26 qp
q7 27 27 7 qn
.ends
```

TAB WIDE

TD is 4.1in

EL2005 Macromodel — Contd.



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EL2005/EL2005C
High Accuracy Fast Buffer

General Disclaimer

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élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

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WARNING — Life Support Policy

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