200MHz Current Feedback Amplifier

élantec

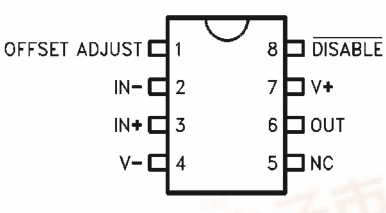
The EL2070 is a wide bandwidth, fast settling monolithic amplifier incorporating a disable/enable feature. Built using an advanced complementary bipolar process, this amplifier uses current-mode feedback to achieve more bandwidth at a given gain than conventional operational amplifiers. Designed for closed-loop gains of ±1 to ±8, the EL2070 has a 200MHz -3dB bandwidth (A_V = +2), and 12ns settling to 0.05% while consuming only 15mA of supply current. Furthermore, the fast disable/enable times of 200ns/100ns allow rapid analog multiplexing.

The EL2070 is an obvious high-performance solution for video distribution and line-driving applications, especially when its disable feature can be used for fast analog multiplexing. Furthermore, the low 15mA supply current, and the very low 5mA of supply current when disabled suggest use in systems where power is critical. With differential gain/phase of 0.02%/0.01°, guaranteed video specifications, and a minimum 50mA output drive, performance in these areas is assured.

The EL2070's settling to 0.05% in 12ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 200MHz bandwidth and extremely linear phase allow unmatched signal fidelity. D/A systems can also benefit from the EL2070, especially if linearity and drive levels are important.

Pinout

EL2070
(8-PIN SO, PDIP)
TOP VIEW



Manufactured under U.S. Patent No. 4,893,091

Features

- 200MHz -3dB bandwidth, A_V = 2
- Disable/enable
- 12ns settling to 0.05%
- V_S = ±5V @ 15mA
- Low distortion: HD2, HD3 @-60dBc at 20MHz
- Differential gain 0.02% at NTSC, PAL
- Differential phase 0.01° at NTSC, PAL
- Overload/short-circuit protected
- ±1 to ±8 closed-loop gain range
- Low cost

Applications

- Video gain block
- Video distribution
- HDTV amplifier
- Analog multiplexing (using disable)
- Power-down mode (using disable)
- High-speed A/D conversion
- D/A I-V conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL2070CN	-40°C to +85°C	8-Pin PDIP	MDP0031
EL2070CS	-40°C to +85°C	8-Pin SO	MDP0027

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S) . . . .±7V
Output Current 70mA
(Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70mA)

Common-Mode Input Voltage . . . . ±V_S
Differential Input Voltage 5V
Disable Input Voltage . . . .+V_S, -1V

Thermal Resistance. . . . .θ_{JA} = 95°C/W PDIP
. . . . θ_{JA} = 175°C/W SO-8
Applied Output Voltage (Disabled). . . . .±V_S
Power Dissipation . . . . See Curves
Operating Temperature . . . . -40C to +85C
Pin Temperature (Soldering, 5 Seconds). . . . . 300°C
Junction Temperature . . . . 175°C
Storage Temperature . . . .-60°C to +150°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Open-Loop DC Electrical Specifications

V_S = ±5V, R_L = 100Ω unless otherwise specified

PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage		25°C		2	5.5	mV
			T_{MIN}			8.2	mV
			T_{MAX}			9.0	mV
d(V_{OS})/dT	Average Offset Voltage Drift	(Note 1)	All		10.0	40.0	µV/°C
+I_{IN}	+Input Current		25°C, T_{MAX}		10	25.0	µA
			T_{MIN}			36.0	µA
d(+I_{IN})/dT	Average +Input Current Drift	(Note 1)	All		50.0	200.0	nA/°C
-I_{IN}	-Input Current		25.0°C		10	30	µA
			T_{MIN}, T_{MAX}			46	µA
d(-I_{IN})/dT	Average -Input Current Drift	(Note 1)	All		50.0	200.0	nA/°C
PSRR	Power Supply Rejection Ratio		All	45.0	50.0		dB
CMRR	Common-Mode Rejection Ratio		All	40.0	50.0		dB
I_S	Supply Current—Quiescent	No Load	All		16.0	20.0	mA
IS_{OFF}	Supply Current—Disabled	(Note 2)	All		4.0	7.0	mA
+R_{IN}	+Input Resistance		25°C, T_{MAX}	100.0	200.0		kΩ
			T_{MIN}	50.0			kΩ
C_{IN}	Input Capacitance		All		0.5	2.0	pF
R_{OUT}	Output Impedance (DC)		All		0.1	0.2	Ω
R_{OUT}D	Output Resistance (DC)	Disabled	All	100.0	200.0		kΩ
C_{OUT}D	Output Capacitance (DC)	Disabled	All		0.5	2.0	pF
CMIR	Common-Mode Input Range	(Note 3)	25°C, T_{MAX}	2.0	2.1		V
			T_{MIN}	1.2			V
I_{OUT}	Output Current		25°C, T_{MAX}	50.0	70.0		mA
			T_{MIN}	35.0			mA
V_{OUT}	Output Voltage Swing	No Load	All	3.3	3.5		V

Open-Loop DC Electrical Specifications

V_S = ±5V, R_L = 100Ω unless otherwise specified **(Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
$V_{OUT}L$	Output Voltage Swing	100Ω	25°C	3.0	3.4		V
-ICMR	Input Current Common Mode Rejection		25°C		8.0	33.0	µA/V
+IPSR	+Input Current Power Supply Rejection		25°C		1.0	3.6	µA/V
-IPSR	-Input Current Power Supply Rejection		25°C		20	24	µA/V
R_{OL}	Transimpedance		25°C	30.0	125.0		V/mA
			T_{MIN}		80.0		V/mA
			T_{MAX}		140.0		V/mA
I_{LOGIC}	Pin 8 Current @ 0V		All		0.8	1.2	mA
V_{DIS}	Maximum Pin 8 V to Disable		All			0.5	V
V_{EN}	Minimum Pin 8 V to Enable		All	3.5			V
I_{DIS}	Minimum Pin 8 I to Disable		All	350.0			µA
I_{EN}	Maximum Pin 8 I to Enable		All			60.0	µA

NOTES:

1. Measured from T_{MIN} to T_{MAX}.
2. Supply current when disabled is measured at the negative supply.
3. Common-mode input range for rated performance.

Closed-Loop AC Electrical Specifications

V_S = ±5V, R_F = 250Ω, A_V = +2, R_L = 100Ω unless otherwise specified

PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
SSBW	-3dB Bandwidth (V_{OUT} < $0.5V_{PP}$)		25°C	150.0	200.0		MHz
			T_{MIN}	150.0			MHz
			T_{MAX}	120.0			MHz
LSBW	-3dB Bandwidth (V_{OUT} < $5.0V_{PP}$)	A_V = +5	All	35.0	50.0		MHz
GAIN FLATNESS							
GFPL	Peaking V_{OUT} < $0.5V_{PP}$	< 40MHz	25°C		0.0	0.3	dB
			T_{MIN}, T_{MAX}			0.4	dB
GFPH	Peaking V_{OUT} < $0.5V_{PP}$	> 40MHz	25°C		0.0	0.5	dB
			T_{MIN}, T_{MAX}			0.7	dB
GFR	Rolloff V_{OUT} < $0.5V_{PP}$	< 75MHz	25°C		0.6	1.0	dB
			T_{MIN}			1.0	dB
			T_{MAX}			1.3	dB
LPD	Linear Phase Deviation V_{OUT} < $0.5V_{PP}$	< 75MHz	25°C, T_{MIN}		0.2	1.0	°
			T_{MAX}			1.2	°

Closed-Loop AC Electrical Specifications

V_S = ±5V, R_F = 250Ω, A_V = +2, R_L = 100Ω unless otherwise specified **(Continued)**

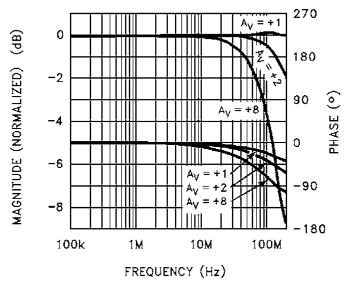
PARAMETER	DESCRIPTION	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNIT
TIME-DOMAIN RESPONSE							
t_{R1}, t_{F1}	Rise Time, Fall Time	0.5V Step	All		1.6	2.4	ns
t_{R2}, t_{F2}	Rise Time, Fall Time	5.0V Step	All		6.5	10.0	ns
t_{S1}	Settling Time to 0.1%	2.0V Step	All		10.0	13.0	ns
t_{S2}	Settling Time to 0.05%	2.0V Step	All		12.0	15.0	ns
OS	Overshoot	0.5V Step	25°C, T_{MAX}		0.0	10.0	%
			T_{MIN}			15.0	%
SR	Slew Rate	A_V = +2	All	430.0	700.0		V/µs
		A_V = - 2	All		1600.0		V/µs
DISTORTION							
HD2	2nd Harmonic Distortion at 20MHz	2V_{PP}	25°C		-60.0	-45.0	dBc
			T_{MIN}			-40.0	dBc
			T_{MAX}			-45.0	dBc
HD3	3rd Harmonic Distortion at 20MHz	2V_{PP}	25°C		-60.0	-50.0	dBc
			T_{MIN}, T_{MAX}			-50.0	dBc
EQUIVALENT INPUT NOISE							
NF	Noise Floor > 100kHz	(Note 1)	25°C		-157.0	-154.0	dBm (1Hz)
			T_{MIN}			-154.0	dBm (1Hz)
			T_{MAX}			-153.0IV	dBm (1Hz)
INV	Integrated Noise 100kHz to 200MHz	(Note 1)	25°C		40.0	57.0	µV
			T_{MIN}			57.0	µV
			T_{MAX}			63.0	µV
DISABLE/ENABLE PERFORMANCE							
T_{OFF}	Disable Time to > 50dB	10MHz	All		1000.0	IV	ns
T_{ON}	Enable Time		All		200.0		ns
OFFIso	Off Isolation	10MHz	All	55.0	59.0		dB
VIDEO PERFORMANCE							
d_G	Differential Gain (Note 2)	NTSC/PAL	25°C		0.02	0.08	% pp
d_P	Differential Phase (Note 2)	NTSC/PAL	25°C		0.01	0.08	° pp
d_G	Differential Gain (Note 2)	30MHz	25°C		0.05	0.18	% pp
d_P	Differential Phase (Note 2)	30MHz	25°C		0.05	0.18	° pp
VBW	-0.1dB Bandwidth (Note 2)		25°C	30.0	60.0		MHz

NOTES:

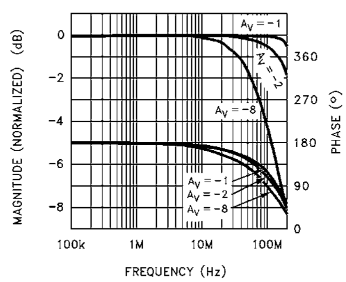
1. Noise Tests are performed from 5MHz to 200MHz.
2. Differential gain/phase tests are with R_L = 100Ω. For other values of R_L, see curves.

Typical Performance Curves

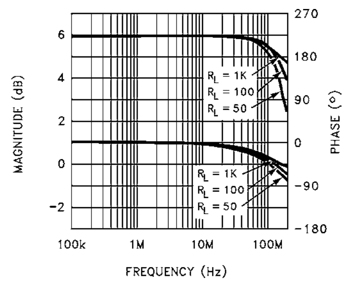
Non-Inverting Frequency Response



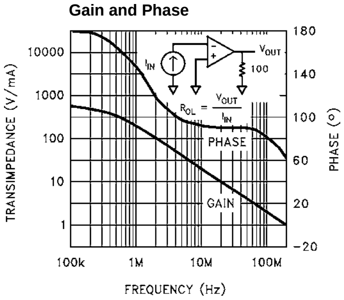
Inverting Frequency Response



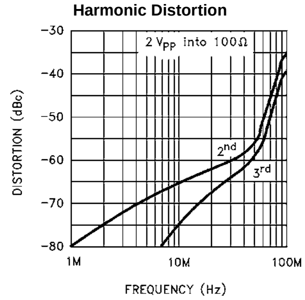
Frequency Response for Various R_Ls



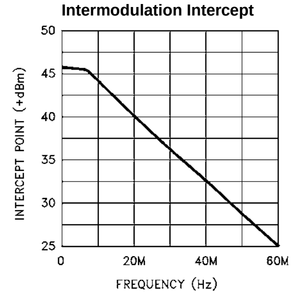
Open-Loop Transimpedance Gain and Phase



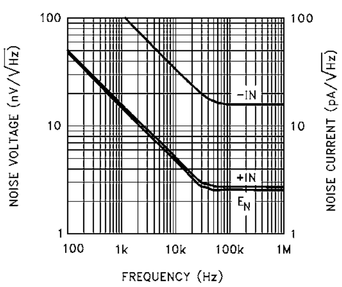
2nd and 3rd Harmonic Distortion



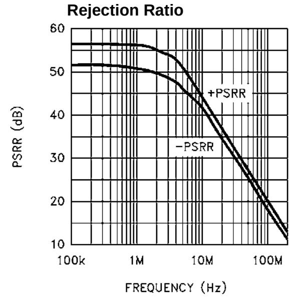
2-Tone 3rd Order Intermodulation Intercept



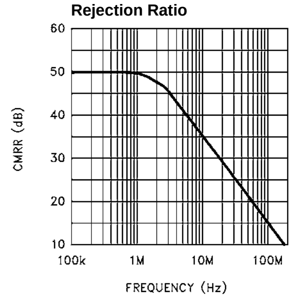
Equivalent Input Noise



Power-Supply Rejection Ratio

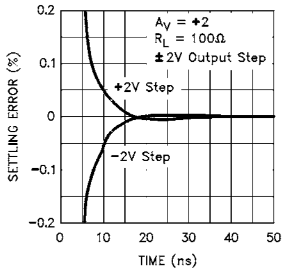


Common-Mode Rejection Ratio

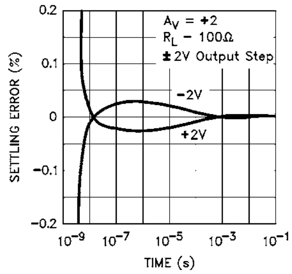


Typical Performance Curves (Continued)

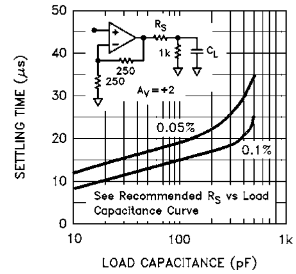
Settling Time



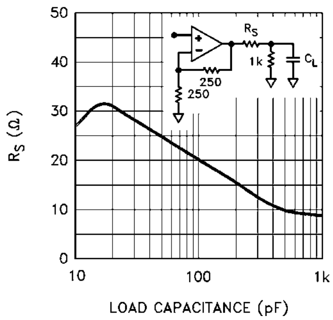
Long-Term Settling Time



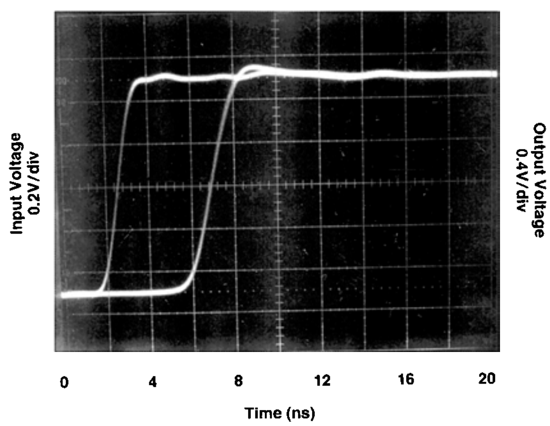
Settling Time vs Load Capacitance



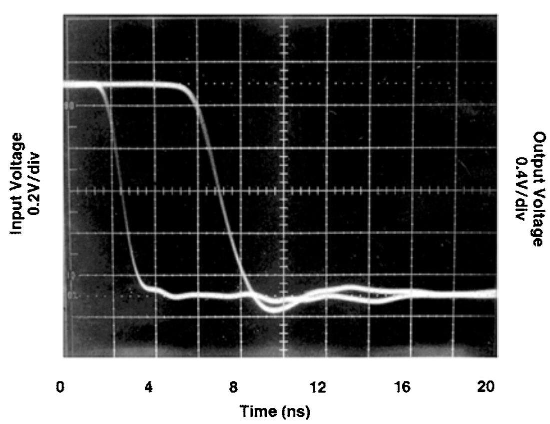
Recommended R_S vs Load Capacitance



Pulse Response A_V = +2

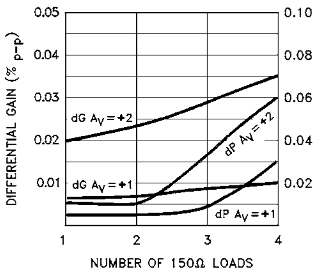


Pulse Response A_V = +2

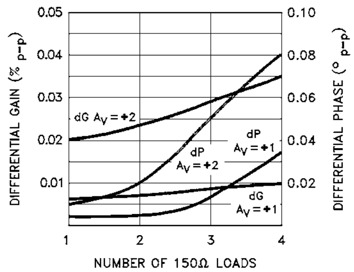


Typical Performance Curves (Continued)

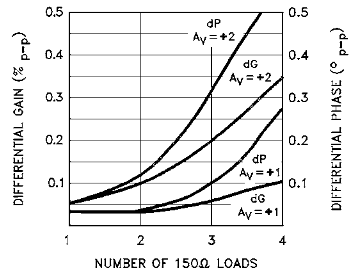
Differential Gain and Phase (3.58MHz)



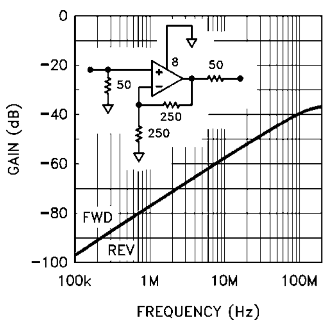
Differential Gain and Phase (4.43MHz)



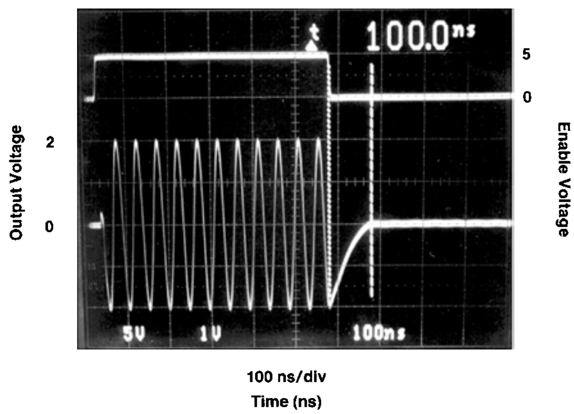
Differential Gain and Phase (30MHz)



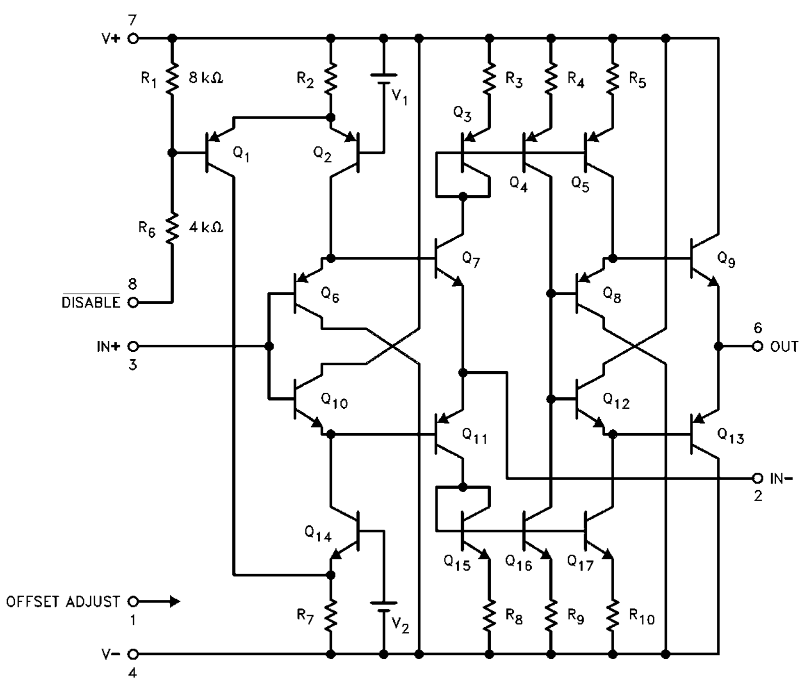
Forward and Reverse Gain during Disable



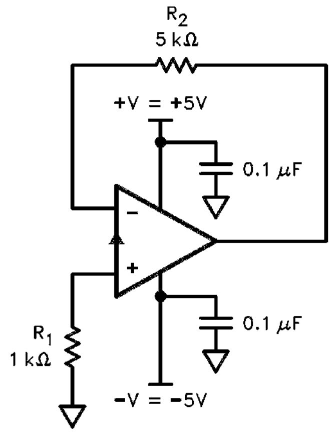
Enable/Disable Response



Equivalent Circuit



Burn-In Circuit



ALL PACKAGES USE THE SAME SCHEMATIC.

Applications Information

Theory of Operation

The EL2070 has a unity gain buffer from the non-inverting input to the inverting input. The error signal of the EL2070 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is called the transimpedance (R_{OL}) of the EL2070 [V_{OUT}=(R_{OL}) * (-I_{IN})]. Since R_{OL} is very large, the current flowing into the inverting input in the steady-state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first-order approximation for circuit analysis, namely that:

1.The voltage across the inputs is approximately 0V.

2.The current into the inputs is approximately 0mA.

Resistor Value Selection and Optimization

The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL2070. The nominal value for the feedback resistor is 250Ω, which is the value used for production testing. This value guarantees stability. For a given closed-loop gain the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth may be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing and eventually oscillations. Increasing the feedback resistor results in a lower -3dB frequency. Attenuation at high frequency is limited by a zero in the closed-loop transfer function which results from stray capacitance between the inverting input and ground. Consequently, it is very important to keep stray capacitance to a minimum at the inverting input.

Differential Gain/Phase

An industry-standard method of measuring the distortion of a video component is to measure the amount of differential gain and phase error it introduces. To measure these, a 40 IRE_{PP} reference signal is applied to the device with 0V DC offset (0 IRE) at 3.58MHz for NTSC, 4.43MHz for PAL, and 30MHz for HDTV. A second measurement is then made with a 0.714V DC offset (100 IRE). Differential Gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential Phase is a measure of the change in phase, and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak values.

In general, a back terminated cable (75Ω in series at the drive end and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double-termination is used, the received signal is reduced by half; therefore a gain of 2 configuration is typically used to compensate for the attenuation. In a gain of 2 configuration, with output swing of $2V_{PP}$, with each back-terminated load at 150Ω. The EL2070 is capable of driving up to 4 back-terminated loads with excellent video performance. Please refer to the typical curves for more information on video performance with respect to frequency, gain, and loading.

Capacitive Feedback

The EL2070 relies on its feedback resistor for proper compensation. A reduction of the impedance of the feedback element results in less stability, eventually resulting in oscillation. Therefore, circuit implementations which have capacitive feedback should not be used because of the capacitor's impedance reduction with frequency. Similarly, oscillations can occur when using the technique of placing a capacitor in parallel with the feedback resistor to compensate for shunt capacitances from the inverting input to ground.

Offset Adjustment Pin

Output offset voltage of the EL2070 can be nulled by tying a 10k potentiometer between $+V_S$ and $-V_S$ with the slider attached to pin 1. A full-range variation of the voltage at pin 1 to ±5V results in an offset voltage adjustment of at least ±10mV. For best settling performance pin 1 should be bypassed to ground with a ceramic capacitor located near to the package, even if the offset voltage adjustment feature is not being used.

Printed Circuit Layout

As with any high frequency device, good PCB layout is necessary for optimum performance. Ground plane construction is a requirement, as is good power-supply and Offset Adjust bypassing close to the package. The inverting input is sensitive to stray capacitance, therefore connections at the inverting input should be minimal, close to the package, and constructed with as little coupling to the ground plane as possible.

Capacitance at the output node will reduce stability, eventually resulting in peaking, and finally oscillation if the capacitance is large enough. The design of the EL2070 allows a larger capacitive load than comparable products, yet there are occasions when a series resistor before the capacitance may be needed. Please refer to the graphs to determine the proper resistor value needed.

Disable/Enable Operation

The EL2070 has a disable/enable control input at pin 8. The device is enabled and operates normally when pin 8 is left open or tied to pin 7. When more than 350µA is pulled from pin 8, the EL2070 is disabled. The output becomes a high impedance, the inverting input is no longer driven to the positive input voltage, and the supply current is reduced by 2/3. To make it easy to use this feature, there is an internal resistor to limit the current to a safe level (0.8mA) if pin 8 is grounded.

To draw current out of pin 8 an open-collector TTL output, a 5V CMOS output, or an NPN transistor can be used.

EL2070 Macromodel

```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:     +input
*                   |    -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2070C      3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 48nH
iinp 3 0 8µA
iinm 2 0 8µA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l3 30 17 0.1µH
c5 17 0 0.1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 150K
cdp 18 0 2.8pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 2
r8 22 6 2

ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
ivos 0 23 5mA
```

EL2070 Macromodel (Continued)

```
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e-15 bf=200 tf=0.05nS)
.model qp pnp (is=5e-15 bf=200 tf=0.05nS)
.model dclamp d(is=1e-30 ibv=0.266 bv=1.3  n=4)
.ends
```