

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2090C

100 MHz DC-Restored Video Amplifier

EL2090C

Features

- Complete video level restoration system
- 0.01% differential gain and 0.02° differential phase accuracy at NTSC
- 100 MHz bandwidth
- 0.1 dB flatness to 20 MHz
- Sample-and-hold has 15 nA typical leakage and 1.5 pC charge injection
- System can acquire DC correction level in 10 μ s, or 5 scan lines of 2 μ s each, to 1/2 IRE
- $V_S = \pm 5V$ to $\pm 15V$
- TTL/CMOS hold signal

Applications

- Input amplifier in video equipment
- Restoration amplifier in video mixers

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2090CN	0°C to +75°C	14-Pin P-DIP	MDP0031
EL2090CM	0°C to +75°C	16-Lead SOL	MDP0027

General Description

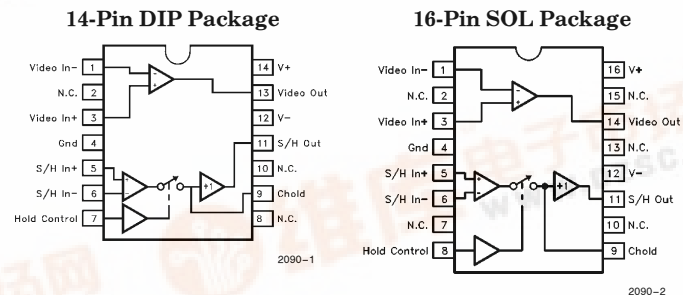
The EL2090C is the first complete DC-restored monolithic video amplifier sub-system. It contains a very high-quality video amplifier and a nulling sample-and-hold amplifier specifically designed to stabilize video performance. When the HOLD logic input is set to a logic 0 during a horizontal sync, the sample-and-hold amplifier may be used as a general-purpose op-amp to null the DC offset of the video amplifier. When the HOLD input goes to a logic 1 the sample-and-hold stores the correction voltage on the hold capacitor to maintain DC correction during the subsequent scan line.

The video amplifier is optimized for video characteristics, and performance at NTSC is nearly perfect. It is a current-feedback amplifier, so that -3 dB bandwidth changes little at various closed-loop gains. The amplifier easily drives video signal levels into 75 Ω loads. With 100 MHz bandwidth, the EL2090 is also useful in HDTV applications.

The sample-and-hold is optimized for fast sync pulse response. The application circuit shown will restore the video DC level in five scan lines, even if the HOLD pulse is only 2 μ s long. The output impedance of the sample-and-hold is low and constant over frequency and load current so that the performance of the video amplifier is not compromised by connections to the DC restore circuitry.

The EL2090C is fabricated in Elantec's proprietary Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL2090C is specified for operation over the 0°C to 75°C temperature range.

Connection Diagrams



January 1996 Rev D

Note: All information contained in this data sheet has been carefully checked and is believed to be accurate as of the date of publication; however, this data sheet cannot be a "controlled document". Current revisions, if any, to these specifications are maintained at the factory and are available upon your request. We recommend checking the revision level before finalization of your design documentation. Patent pending. CMS # 2090DS

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Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Voltage between V^+ and V^-	36V	Current S/H_{OUT}	16 mA
Voltage between V_{IN+} , S/H_{IN+} , S/H_{IN-} , C_{HOLD} , and GND pins	(V^+) + 0.5V to (V^-) - 0.5V	Internal Power Dissipation	See Curves
V_{OUT} Current	60 mA	Operating Ambient Temperature Range	0°C to 75°C
Current into V_{IN-} and HOLD Pins	5 mA	Operating Junction Temperature Plastic DIP or SOL	150°C
		Storage Temperature Range	-65°C to $+150^\circ\text{C}$

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25^\circ\text{C}$ and QA sample tested at $T_A = 25^\circ\text{C}$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25^\circ\text{C}$ for information purposes only.

Open Loop DC Electrical Characteristics

$V_S = \pm 15\text{V}$; $R_L = 150\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
I_S	Total Supply Current	Full		14	17	II	mA

Video Amplifier Section (Not Restored)

V_{OS}	Input Offset Voltage	Full		8	70	II	mV
I_{B+}	+ V_{IN} Input Bias Current	Full		2	15	II	μA
I_{B-}	- V_{IN} Input Bias Current	Full		30	150	II	μA
R_{OL}	Transimpedance	25°C		300		V	V/mA
A_{VOL}	Open-Loop Voltage Gain; $V_{OUT} = \pm 2\text{V}$	Full	56	65		II	dB
V_O	Output Voltage Swing $V_S = \pm 15\text{V}$; $R_L = 2\text{k}\Omega$ $V_S = \pm 5\text{V}$; $R_L = 150\Omega$	Full	± 12	± 13		II	V
		Full	± 3.0	± 3.5		II	V
I_{SC}	Short-Circuit Current; + V_{IN} Set to $\pm 2\text{V}$; - V_{IN} to Ground through $1\text{k}\Omega$	25°C	± 50	± 90	± 160	II	mA

Sample-And-Hold Section

V_{OS}	Input Offset Voltage	Full		2	10	II	mV
I_B	Input Bias Current	Full		0.5	2.5	II	μA
I_{OS}	Input Offset Current	Full		0.05	0.5	II	μA
$R_{IN, DIFF}$	Input Differential Resistance	25°C		200		V	$\text{k}\Omega$
$R_{IN, COMM}$	Input Common-Mode Resistance	25°C		100		V	$\text{M}\Omega$
V_{CM}	Common-Mode Input Range	Full	± 11	± 12.5		II	V

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Open Loop DC Electrical Characteristics

$V_S = \pm 15V$; $R_L = 150\Omega$, $T_A = 25^\circ C$ unless otherwise specified — Contd.

Parameter	Description	Temp.	Min	Typ	Max	Test Level	Units
Sample-And-Hold Section — Contd.							
AVOL	Large Signal Voltage Gain	Full	15k	50k		II	V/V
CMRR	Common-Mode Rejection Ratio $V_{CM} = \pm 11V$	Full	75	95		II	dB
PSRR	Power-Supply Rejection Ratio $V_S = \pm 5V$ to $\pm 15V$	Full	75	95		II	dB
V _{thresh}	HOLD Pin Logic Threshold	Full	0.8	1.4	2.0	II	V
I _{droop}	Hold Mode Droop Current	Full		10	50	II	nA
I _{charge}	Charge Current Available to Chold	Full	± 90	± 135		II	μA
V _O	Output Swing; $R_L = 2k$	Full	± 10	± 13		II	V
I _{SC}	Short-Circuit Current	25°C	± 10	± 17	± 40	II	mA

Closed Loop AC Electrical Characteristics

$V_S = \pm 15V$; $C_L = 15$ pF; $C_{stray} (-V_{IN}) = 2.5$ pF; $R_F = R_G = 300\Omega$; $R_L = 150\Omega$; $C_{hold} = 100$ pF; $T_A = 25^\circ C$

Parameter	Description	Min	Typ	Max	Test Level	Units
Video Amplifier Section						
SR	SlewRate; V_{OUT} from -2 to $+2V$		600		V	V/ μs
BW	Bandwidth; -3 dB ± 1 dB ± 0.1 dB	75	100		III	MHz
		35	60		III	MHz
		10	20		III	MHz
Peaking dG	Differential Gain; V_{IN} from $-0.7V$ to $0.7V$; $F = 3.58$ MHz		0.01		V	%
d θ	Differential Phase; V_{IN} from $-0.7V$ to $0.7V$; $F = 3.58$ MHz		0.02		V	°

Sample-And-Hold Section

BW	Gain-Bandwidth Product		1.3		V	MHz
ΔQ	Sample to Hold Charge Injection (Note 1)		1.5	5	III	pC
ΔT	Sample to Hold or Hold to Sample Delay Time		20		V	ns
T _s	Sample to Hold Settling Time to 2 mV		200		V	ns

Note 1: The logic input is between 0V and 5V, with a 220 Ω resistor in series with the HOLD pin and 39 pF capacitor from HOLD pin to ground.

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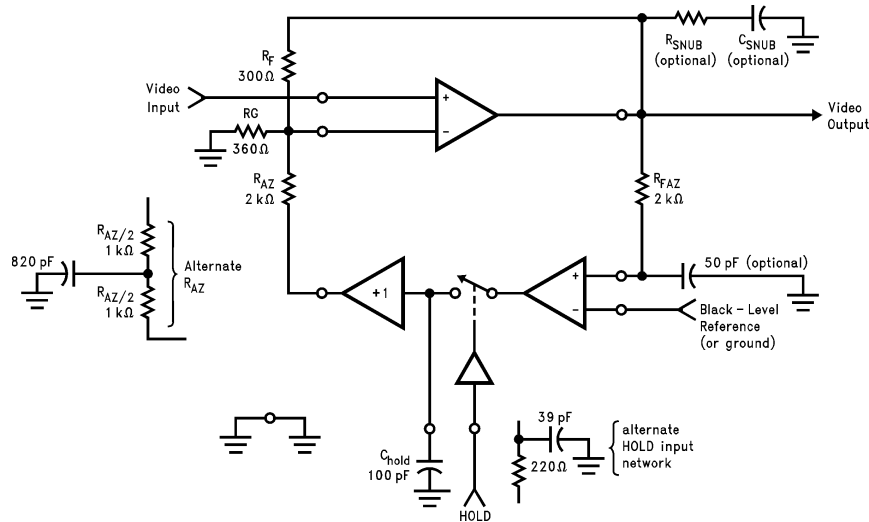
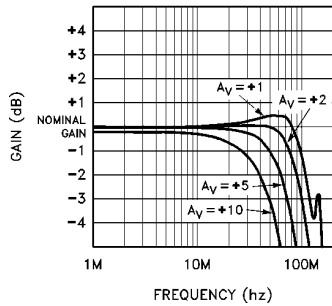


Figure 1. Typical Application ($A_V = +2$)

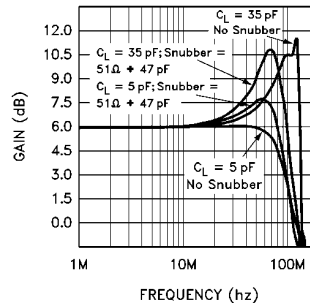
2090-3

Typical Performance Curves

Relative Frequency Response for Various Gains

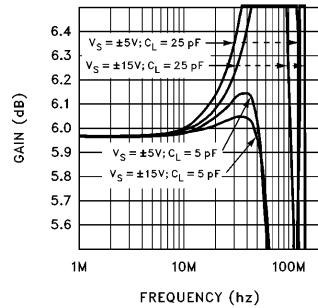


Frequency Response with Different Loads ($A_V = +2$)

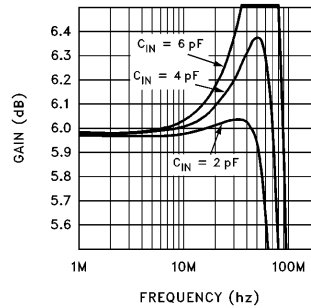


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Frequency Response Flatness for Various Load and Supply Conditions



Frequency Response Flatness vs C_{IN} , $A_V = +2$

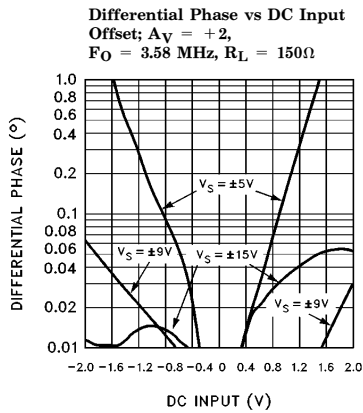
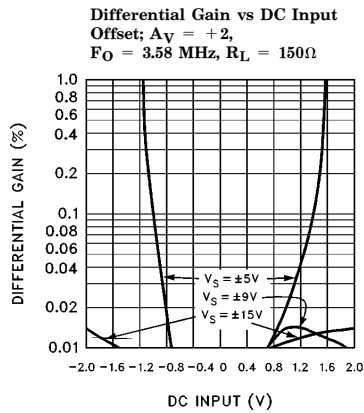
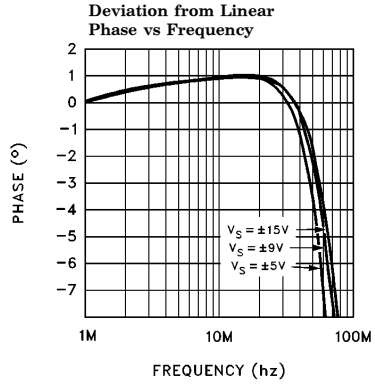
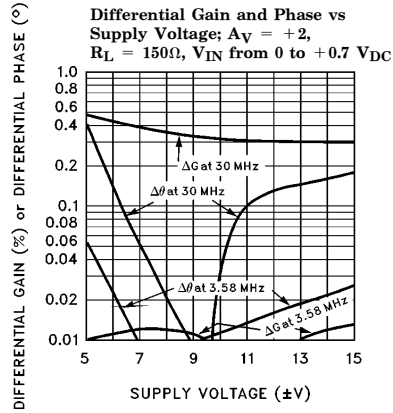


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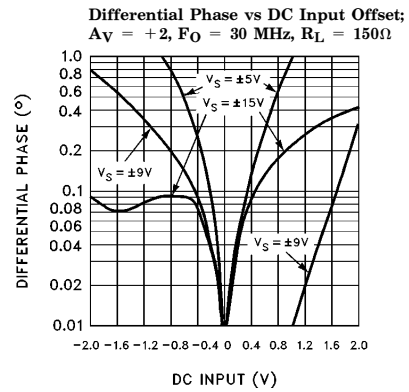
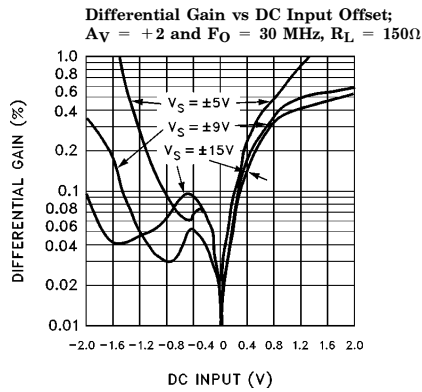
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Typical Performance Curves — Contd.



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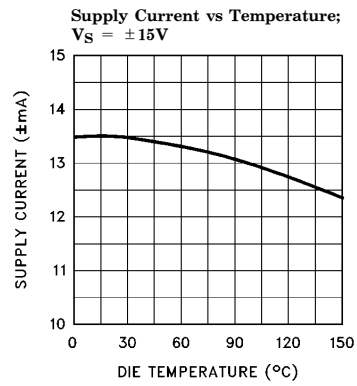
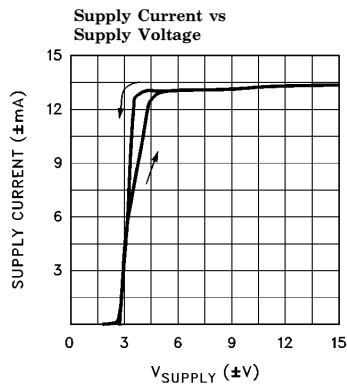
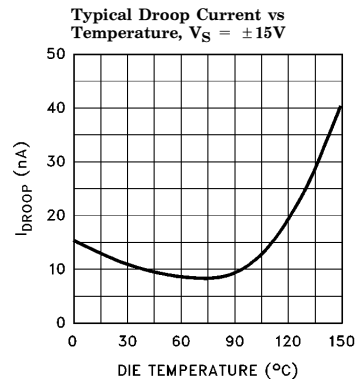
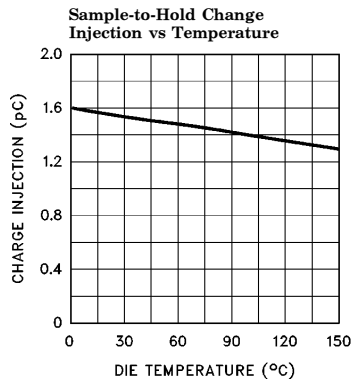
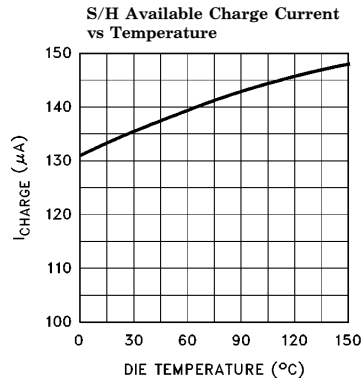


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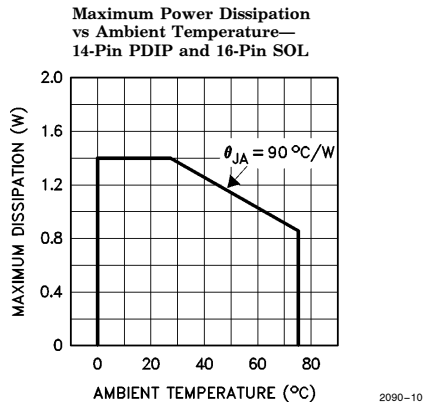
Typical Performance Curves — Contd.



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Typical Performance Curves — Contd.



Applications Information

The EL2090C is a general purpose component and thus the video amplifier and sample-and-hold pins are uncommitted. Therefore much of the ultimate performance as a DC-restored video amplifier will be set by external component values and parasitics. Some application considerations will be offered here.

The DC feedback from the sample-and-hold can be applied to either positive or negative inputs of the video amplifier (with appropriate phasing of the sample-and-hold amplifier inputs). We will consider feedback to the inverting video input. During a sample mode (the HOLD input at a logic low), the sample-and-hold acts as a simple nulling op-amp.

Ideally, the DC feedback resistor R_{az} is a high value so as not to couple a large amount of the AC signal on the video input back to the sample-and-hold amplifier output. The sample-and-hold output is a low impedance at high frequencies, but variations of the DC operating point will change the output impedance somewhat. No more than a few ohms output impedance change will occur, but this can cause gain variations in the 0.01% realm. This DC-dependent gain change is in fact a differential gain effect. Some small differential phase error will also be added. The best approach is to maximize the DC feedback resistor value so as to isolate the sample-and-hold from the video path as much as possible. Values of 1 k Ω or above for R_{az} will cause little to no video degradation.

This suggests that the largest applicable power supply voltages be used so that the output swing of the sample-and-hold can still correct for the variations of DC offset in the video input with large values of R_{az} . The typical application circuit shown will allow correction of $\pm 1\text{V}$ inputs with good isolation of the sample-and-hold output. Good isolation is defined as no video degradation due to the insertion of the sample-and-hold loop. Lower supply voltages will require a smaller value of DC feedback resistor to retain correction of the full input DC variation. The EL2090 differential phase performance is optimum at $\pm 9\text{V}$ supplies, and differential gain only marginally improves above this voltage. Since all video characteristics mildly degrade with increasing die temperature, the $\pm 9\text{V}$ levels are somewhat better than $\pm 15\text{V}$ supplies. However, $\pm 15\text{V}$ supplies are quite usable.

Ultimate video performance, especially in HDTV applications, can also be optimized by setting the black-level reference such that the signal span at the video amplifier's output is set to its optimum range. For instance, setting the span to $\pm 1\text{V}$ of output is preferable to a span of 0V to +2V. The curves of differential gain and phase versus input DC offset will serve as guides.

The DC feedback resistor may be split so that a bypass capacitor is added to reduce the initially small sample-and-hold transients to even smaller levels. The corruption can be reduced to as low as 1 mV peak seen at the video amplifier output. The size of the capacitor should not be so large as to de-stabilize the sample-and-hold feedback loop, nor so small as to reduce the video amplifier's gain flatness. A resistor or some other video isolation network should be inserted between the video amplifier output and the sample-and-hold input to prevent excessive video from bleeding through the autozero section, as well as preventing spurious DC correction due to video signals confusing the sample-and-hold during autozero events. Figure 1 shows convenient component values. A full 3.58 MHz trap is not necessary for suppressing NTSC chroma burst interaction with the sample-and-hold input; the simple R-C network suggested in Figure 1 suffices.

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Applications Information — Contd.

The HOLD input to the sample-and-hold has a 1.4V threshold and is clamped to a diode below ground and 6V above ground. The hold step characteristics are not sensitive to logic high nor low levels (within TTL or CMOS swings), but logic slewrates greater than 1000V/ μ s can couple noise and hold step into the sample-to-hold output waveforms. The logic slewrates should be greater than 50V/ μ s to avoid hold jitter. To avoid artificially high droop in hold mode, the Chold pin and Chold itself should be guarded with circuit board traces connected to the output of the sample-and-hold. Low-leakage hold capacitors should be used, such as mica or mylar, but not ceramic. The excellent properties of more expensive polystyrene, polypropylene, or teflon capacitors are not needed.

The user should be aware of a combination of conditions that may make the EL2090 operate incorrectly upon power-up. The fault condition can be described by noticing that the sample-and-hold output (pin 11) appears locked at a voltage close to V_{CC} . This voltage is maintained regardless of changes at the inputs to the sample-and-hold (pins 5 and 6) or to the HOLD control input (pin 7). Two conditions must occur to bring this about:

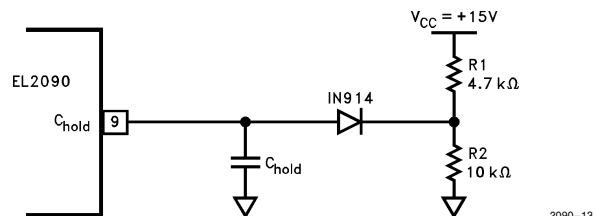
1. A large value of Chold—usually values of 1000 pF or more. This is not an unusual situation. Many users want to reduce the size of the

hold step and increasing Chold is the most direct way to do this. Increasing Chold also reduces the slew rate of the sample and hold section but because of the limited size of the video signal, this is usually not a limitation.

2. A sampling interval (dictated by the HOLD pin) that is too small. By small, we mean less than 2 μ s.

For a sampling interval that is wide enough, there is enough time for the loop to close and for the amplifier to discharge whatever charge was dumped onto Chold it during the initial power spike and to then ramp up (or down) to the voltage that is proper for a balanced loop. When the sampling interval is too small, there is insufficient time for internal devices to recover from their initial saturated state from power-up because the feedback is not closed long enough. Therefore, typical recovery times for the loop are 2 μ s or greater. Summarizing, the two things that could prevent proper saturation recovery are (as mentioned above) too large a capacitor which slows the charge and discharge rate of the stored voltage at Chold and too small a sampling interval in which the entire feedback loop is closed.

The circuit shown below prevents the fault condition from occurring by preventing the node from ever saturating. By clamping the value of Chold to some value lower than the supply voltage less



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Applications Information — Contd.

a saturation voltage, we prevent this node from approaching the positive rail. The maximum voltage is set by the resistive voltage divider (between V+ and GND) R1 and R2 plus a diode. This value can be adjusted if the maximum size of the input signal is known. The diode used is an off-the-shelf 1N914 or 1N916.

As is true of all 100 MHz amplifiers, good bypassing of the supplies to ground is mandatory. 1 μ F tantalums are sufficient, and 0.01 μ F leaded chip capacitors in parallel with medium value electrolytics are also good. Leads longer than $\frac{1}{2}$ can induce a characteristic 150 MHz resonance and ringing.

The V_{IN-} of the video amplifier should have the absolute minimum of parasitic capacitance. Stray capacitance of more than 3 pF will cause peaking and compromise the gain flatness. The bandwidth of the amplifier is fundamentally set by the value of Rf. As demonstrated by the frequen-

cy response versus gain graph, the peaking and bandwidth is a weak function of gain. The EL2090 was designed for Rf = 300 Ω giving optimum gain flatness at Av = +2. Unity-gain response is flattest for Rf = 360 Ω ; gains of +5 can use Rf = 270 Ω . In situations where the peaking is accentuated by load capacitance or -input capacitance the value of Rf will have to be increased, and some bandwidth will be sacrificed.

The V_{IN+} of the video amplifier should not look into an inductive source impedance. If the source is physically remote and a terminated input line is not provided, it may be necessary to connect an input "snubber" to ground. A snubber is a resistor in series with a capacitor which de-Q's the input resonance. Typical values are 100 Ω and 30 pF.

The output of the video amplifier is sensitive to capacitive loads greater than 25 pF, and a snubber to ground or a resistor in series with the output is useful to isolate reactive loads.

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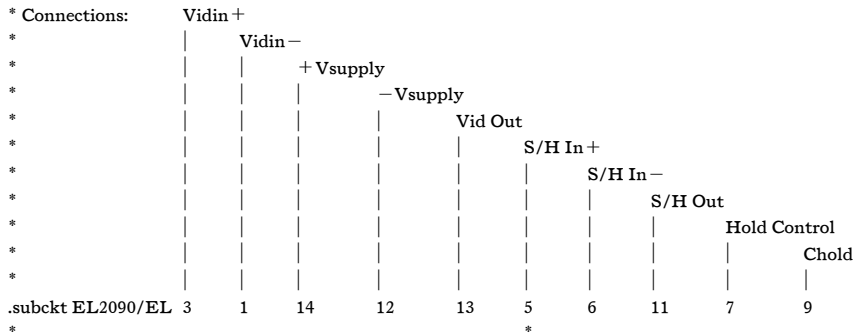
EL2090 Macromodel

* Revision A, October 1992

.param vclamp = {-0.002 * (TEMP-25)}

*

* Connections:



.subckt EL2090/EL 3 1 14 12 13 5 6 11 7 9

*

***** Video Amplifier *****

*

e1 20 0 3 0 1.0
 vis 20 34 0V
 h2 34 38 vxx 1.0
 r10 1 36 25
 l1 36 38 20nH
 iinp 3 0 10μA
 iinm 1 0 5μA
 h1 21 0 vis 600
 r2 21 22 1K
 d1 22 0 dclamp
 d2 0 22 dclamp
 e2 23 0 22 0 0.001666666666
 l5 23 24 0.7μH
 c5 24 0 0.5pF
 r5 24 0 600
 g1 0 25 24 0 1.0
 rol 25 0 400K
 cdp 25 0 7.7pF
 q1 12 25 26 qp
 q2 14 25 27 qn
 q3 14 26 28 qn
 q4 12 27 29 qp
 r7 28 13 4
 r8 29 13 4
 ios1 14 26 2.5mA
 ios2 27 12 2.5mA
 ips 14 12 7.2mA
 ivos 0 33 5mA
 vxx 33 0 0V
 r11 33 0 1K

***** Sample & Hold *****

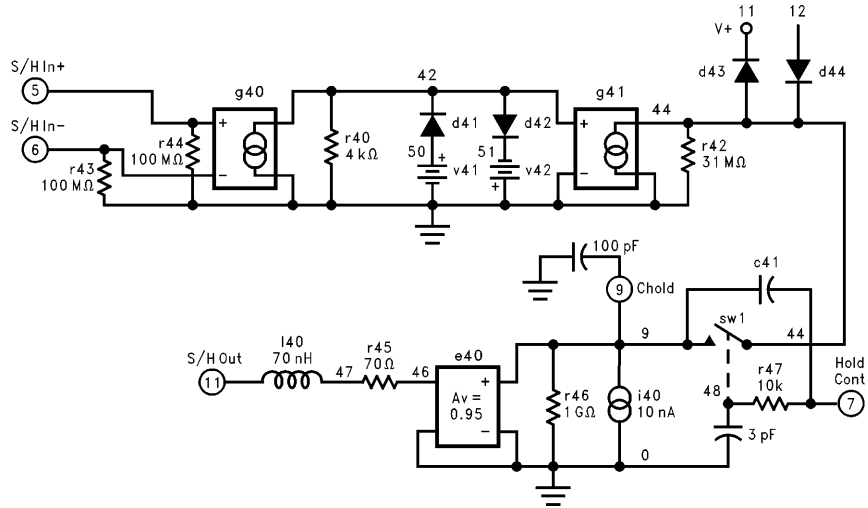
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 vcur 49 42 0v
 r43 6 0 100Meg
 r44 5 0 100Meg
 r40 42 0 4K
 d41 50 42 diode
 d42 42 51 diode
 v41 50 0 {vclamp}
 v42 0 51 {vclamp}
 g41 44 0 42 0 200e-6
 r42 44 0 31Meg
 d45 9 14 diode
 d46 12 9 diode
 s1 44 9 48 0 swa
 e40 46 0 9 0 0.95
 i40 0 9 10nA
 r45 46 47 70
 l40 47 11 70nH
 c40 7 9 0.32pF
 r47 7 48 10K
 c41 48 0 3pF
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 * Models
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 .model diode d
 .model swa vswitch(von=1.2v voff=1.6v roff=1e12 ron=100)
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EL2090 Macromodel — Contd.



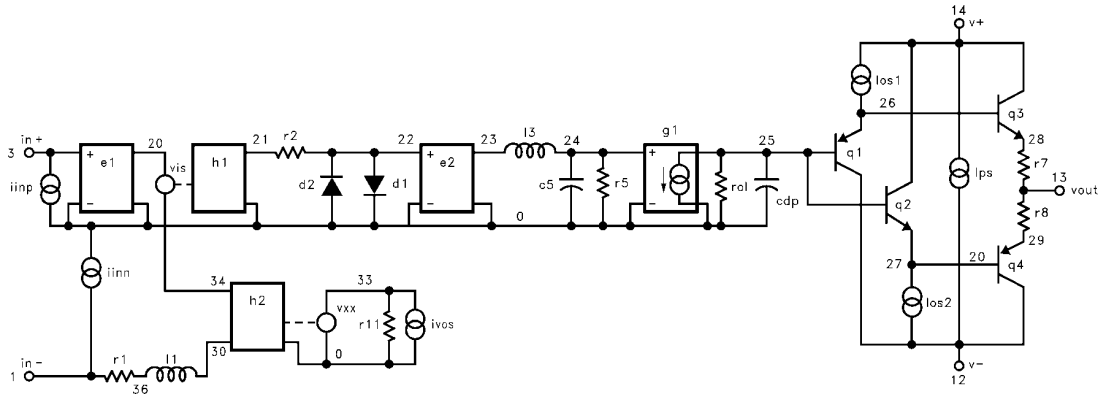
Sample and Hold Amplifier

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100 MHz DC-Restored Video Amplifier

EL2090 Macromodel — Contd.



Video Amplifier

2090-14

General Disclaimer

Specifications contained in this data sheet are in effect as of the publication date shown. Elantec, Inc. reserves the right to make changes in the circuitry or specifications contained herein at any time without notice. Elantec, Inc. assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Elantec, Inc.

1996 Tarob Court

Milpitas, CA 95035

Telephone: (408) 945-1323

(800) 333-6314

Fax: (408) 945-9305

European Office: 44-71-482-4596

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