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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4089C
DC Restored Video Amplifier

Features

- Complete video level restoration system
- 0.02% differential gain and 0.05° differential phase accuracy at NTSC
- 60 MHz bandwidth
- 0.1 dB flatness to 10 MHz
- V_S = ±5V to ±15V
- TTL/CMOS hold signal

Applications

- Input amplifier in video equipment
- Restoration amplifier in video mixers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4089CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL4089CS	0°C to +75°C	8-Lead SO	MDP0027

General Description

The EL4089C is an 8-pin complete DC-restored monolithic video amplifier sub-system. It contains a high quality video amplifier and a nulling, sample-and-hold amplifier specifically designed to stabilize video performance.

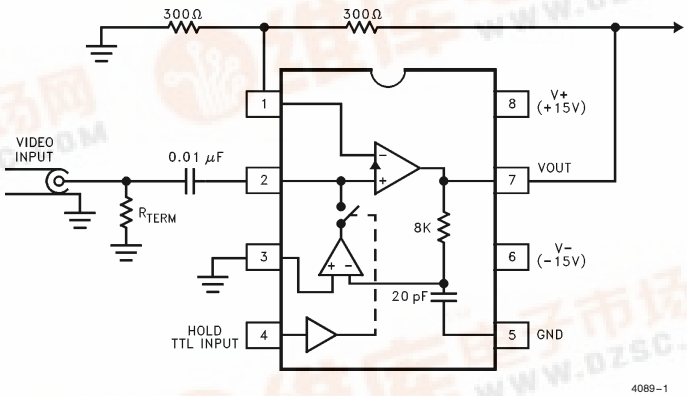
When the HOLD logic input is set to a TTL/CMOS logic 0, the sample- and-hold amplifier can be used to null the DC offset of the video amplifer.

When the HOLD input goes to a TTL/CMOS logic l, the correcting voltage is stored on the video amplifier's input coupling capacitor. The correction voltage can be further corrected as need be, on each video line.

The video amplifier is optimized for video performance and low power. Its current feedback design allows the user to maintain essentially the same bandwidth over a gain range of nearly 10:1. The amplifier drives back-terminated 75Ω lines.

The EL4089C is fabricated in Elantec's proprietary Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL4089C is specified for operation over 0°C to +75°C temperature range.

Connection Diagram



DC restoring amplifier with a gain of 2, restoring to ground.

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	33V	Operating Ambient Temperature Range	0°C to +75°C
Voltage between $V_{IN}+$, $S/H_{IN}+$, and GND pins	(V+) +0.5V to (V−) −0.5V	Operating Junction Temperature Plastic DIP or SOL	150°C
V_{OUT} Current	60 mA	Storage Temperature Range	−65°C to +150°C
Current into $V_{IN}-$ and HOLD Pins	5 mA		
Internal Power Dissipation	See Curves		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

Provisional Supplies at ±15V, Load = 1 kΩ; T_A = +25°C

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Amplifier Section (HOLD = 5V)							
V_{OS}	Input Offset Voltage	+25°C		12	25	II	mV
Ib+	IN+ Input Bias Current	+25°C		1	5	II	µA
Ib−	IN− Input Bias Current	+25°C		18	150	II	µA
R_{OL}	Transimpedance (Note 1)	+25°C	180	800		II	kΩ
$R_{IN}-$	IN− Resistance	+25°C		20		V	Ω
CMRR	Common Mode Rejection Ratio (Note 2)	+25°C	44	60		II	dB
V_O	Output Voltage Swing	+25°C	±12	±13		II	V
I_{SC}	Short Circuit Current (IN+ Only Driven to 0.5V)	+25°C	45	100		II	mA
Restore Section							
V_{OS}, Comp	Composite Input Offset Voltage (Note 3)	+25°C		3	7	II	mV
Ib+,r	Restore In+ Input Bias Current	+25°C		3	12	II	µA
I_{OUT}	Restoring Current Available	+25°C	180	300		II	µA
CMRR	Common Mode Rejection Ratio (Note 2)	+25°C	60	70		II	dB

TD is 3.5in

Open Loop DC Electrical Characteristics — Contd.

Provisional Supplies at ±15V, Load = 1 kΩ; T_A = +25°C

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Restore Section —Contd.							
PSRR	Power Supply Rejection Ratio (Note 4)	+25°C	60	90		II	dB
$V_{THRESHOLD}$	HOLD Logic Threshold	+25°C	0.8		2.0	II	V
I_{IH}, Hold	HOLD Input Current @ Logic High	+25°C		1	5	II	µA
I_{IL}, Hold	HOLD Input Current @ Logic Low	+25°C		5	15	II	µA
Supply Current							
Isy, Hold	Supply Current (HOLD = 5V)	+25°C	4.8	6.0	9.0	II	mA
Isy, Sampling	Supply Current (HOLD = 0V)	+25°C	5.0	6.5	11.0	II	mA

Closed Loop AC Electrical Characteristics

Provisional Supplies at ±15V, Load = 150Ω and 15 pF. R_f and R_g = 300Ω; A_V = 2, T_A = 25°C. (See Note 7 about Test Fixture)

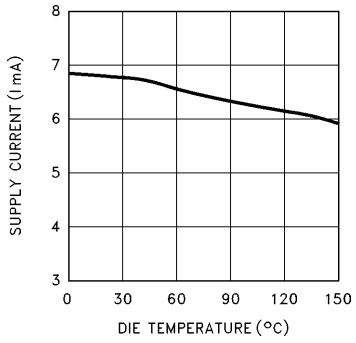
Parameter	Description		Min	Typ	Max	Test Level	Units
Amplifier Section							
SR	Slew Rate (Note 5)			500		V	V/µs
SR	Slew Rate with ±5V Supplies (Note 5)			275		V	V/µs
BW	Bandwidth	−3 dB		60		V	MHz
	±5V Supplies	−3 dB		55		V	MHz
BW	Bandwidth	±0.1 dB		25		V	MHz
	±5V Supplies	±0.1 dB		23		V	MHz
dG	Differential Gain	V_S = ±15V		0.02		V	%
	at 3.58 MHz (Note 6)	V_S = ±5V		0.03		V	%
dPh	Differential Phase	V_S = ±15V		0.05		V	°
	at 3.58 MHz (Note 6)	V_S = ±5V		0.06		V	°
Restore Section							
SR	Restore Amplifier Slew Rate (Test Circuit) 20%–80%			25		V	V/µs
T_{HE}	Time to Enable Hold			25		V	ns
T_{HD}	Time to Disable Hold			40		V	ns

Note 1: For current feedback amplifiers, $A_{VOL} = R_{OL}/R_{IN-}$.
Note 2: V_{CM} = ±10V for V_S = ±15V.
Note 3: Measured from S/H Input to amplifier output, while restoring.
Note 4: V_{OS} is measured at V_S = ±4.5V and V_S = ±16V, both supplies are changed simultaneously.
Note 5: SR measured at 20% to 80% of a 4V pk-pk square wave.
Note 6: DC offset from −0.714V through +0.714V, ac amplitude is 286 mVp-p, equivalent to 40 ire.
Note 7: Test fixture was designed to minimize capacitance at the IN− input. A "good" fixture should have less than 2 pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.

TD is 3.2in

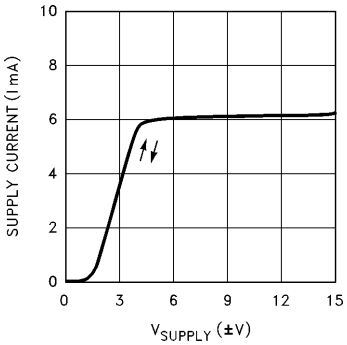
Typical Performance Curves

Supply Current vs Temperature
V_S = ±15V



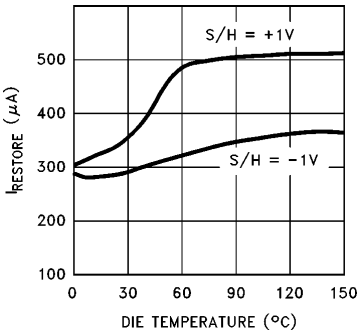
4089-2

Supply Current vs Supply Voltage



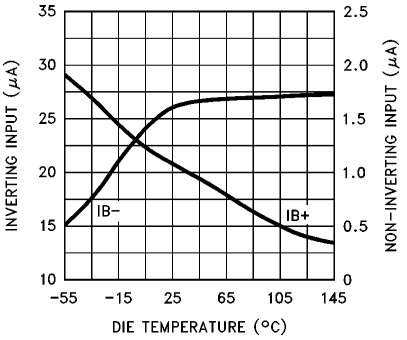
4089-3

Restoring Current vs Temperature



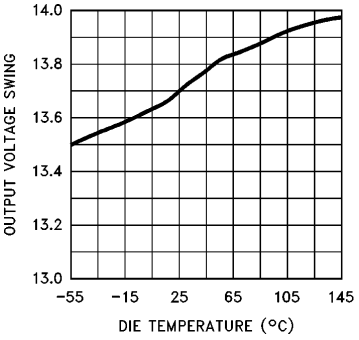
4089-4

Amplifier Input Current vs Die Temperature



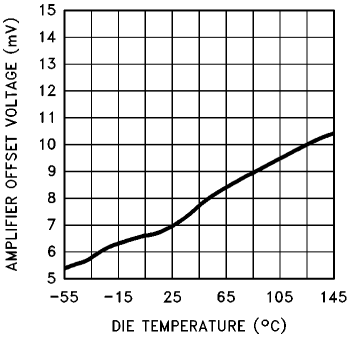
4089-5

Amplifier Output Voltage vs Die Temperature;
V_S = ±15V



4089-6

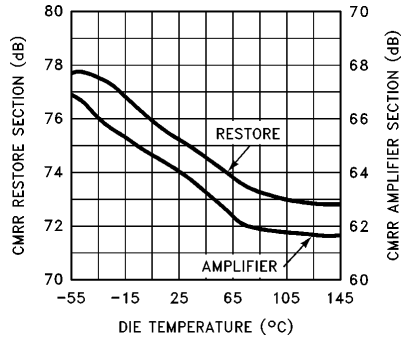
Amplifier Offset Voltage vs Die Temperature



4089-7

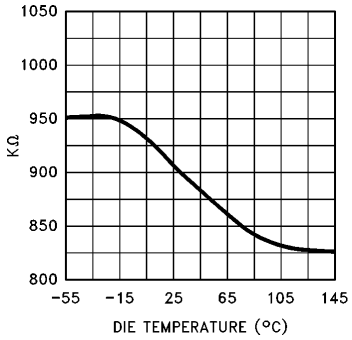
Typical Performance Curves — Contd.

CMRR for Amplifier and Restore Section vs Die Temperature



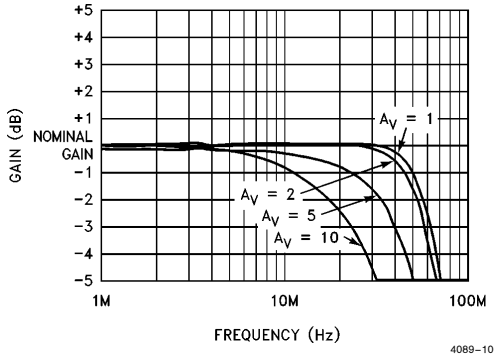
4089-8

Transimpedance (R_{OL}) vs Die Temperature



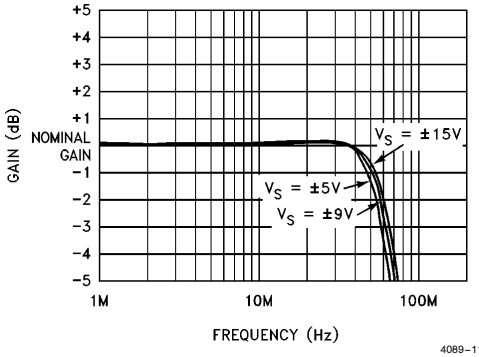
4089-9

Relative Frequency Response for Various Gains, R_F = 300Ω



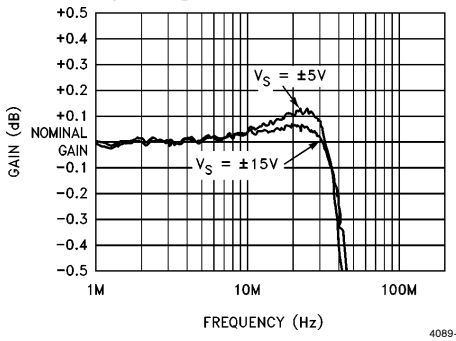
4089-10

Frequency Response vs Supply A_V = 2; R_F = 300



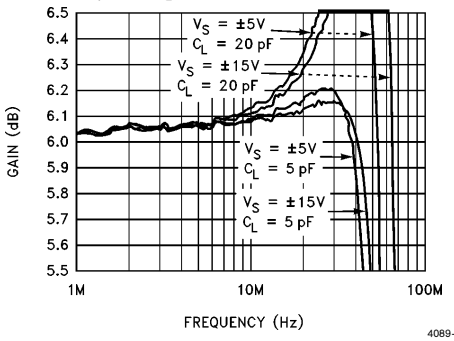
4089-11

Frequency Response Flatness vs Supply A_V = 2; R_F = 300



4089-12

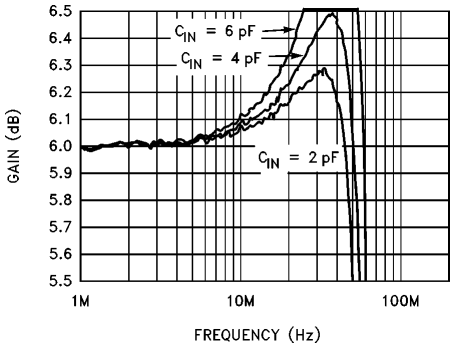
Frequency Response Flatness for Various Load and Supply Conditions A_V = 2; R_F = 300



4089-13

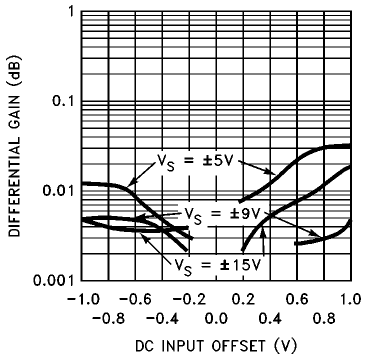
Typical Performance Curves — Contd.

Frequency Response Flatness vs C_{IN-}; A_V = 2; R_F = 300



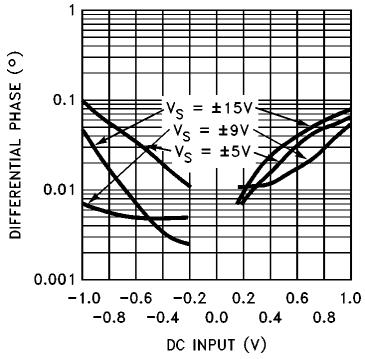
4089-14

Differential Gain vs DC Input Offset; A_V = 2, F_O = 3.58 MHz, R_L = 150Ω



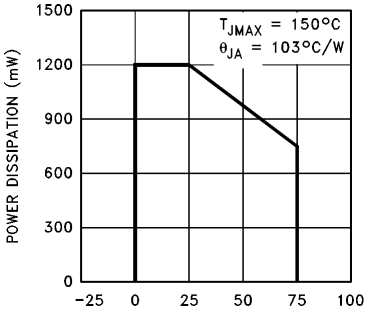
4089-15

Differential Phase vs DC Input Offset; A_V = 2; F_O = 3.58 MHz; R_L = 150Ω



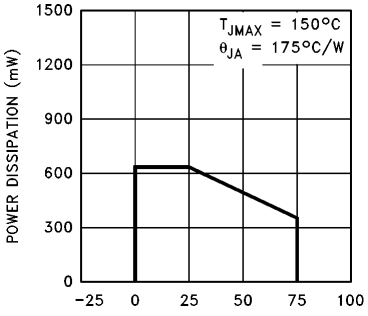
4089-16

8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



4089-17

8-Lead SO Maximum Power Dissipation vs Ambient Temperature



4089-18

Typical Application

The EL4089 can be used to DC-restore a video waveform (see Fig. 1). The above circuit forces the cable driving video amplifier's output to ground when the HOLD pin is at a logic low.

The "correction voltage" is stored on capacitor CX1, an external ceramic capacitor. The capacitor value is chosen from the system requirements. The typical input bias current to the video amplifier is 1 μA, so for a 62 μs hold time, and a 0.01 μF capacitor, the output voltage drift is 6.2 mV in one line.

The S/H amplifier can provide a typical current of 300 μA to charge capacitor CX1, so with a 1.2 μs sampling time, the output can be corrected by 36 mV in each line.

Using a smaller value of CX1 increases both the voltage that can be corrected, and the drift while being held, likewise, using a larger value of CX1, reduces the voltages.

The RX1 resistor is in the circuit purely to simulate some external source impedance, and is not needed as a real component. Likewise for RX2. The 75Ω back terminating resistor RXT is recommended when driving 75Ω cables.

The board layout should have a ground plane underneath the EL4089, with the ground plane cut away from the vicinity of the V_{IN-} pin, (pin 1). This helps to minimize the stray capacitance on pin 1.

Power supply bypassing is important, and a 0.1 μF ceramic capacitor, from each power pin to ground, placed very close to the power pins, together with a 4.7 μF tantalum bead capacitor, is recommended.

When both digital and Analog grounds are on the same board, the EL4089 should be on the Analog ground. The digital ground can be connected to the Analog ground through a 100Ω–300Ω resistor, near the EL4089. This allows the digital signal a return path, while preventing the digital noise from corrupting the analog ground.

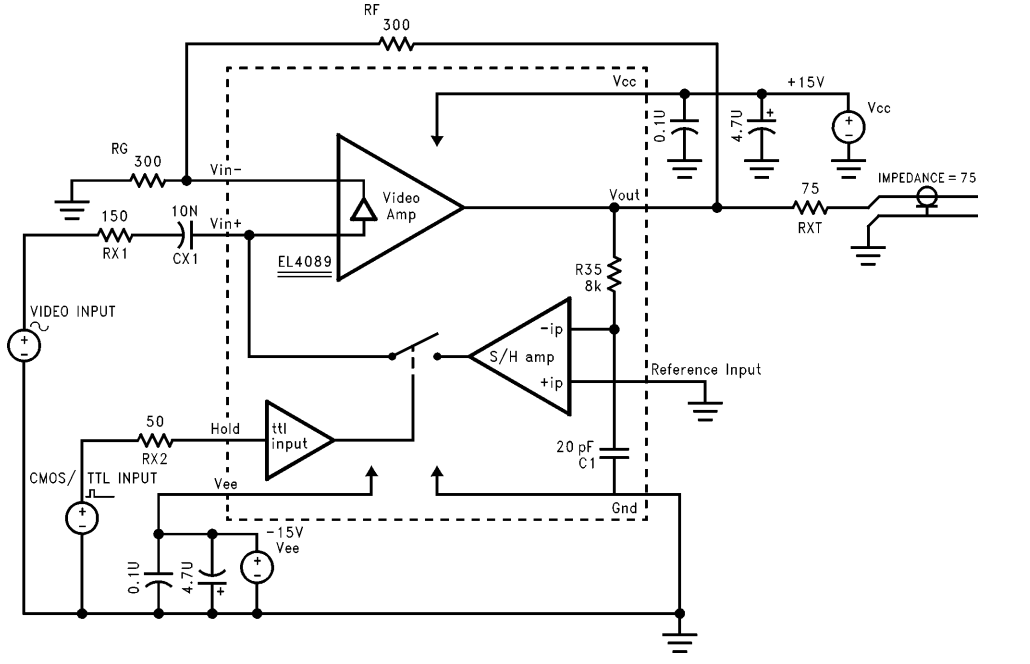


Figure 1

Table of Charge Storage Capacitor vs Droop Charging Rates

Cap Value nF	Droop in 60 μs mV	Charge in 1.2 μs mV	Charge in 4 μs mV
10	6	36	120
33	1.8	11	36
100	0.6	3.6	12

Basic formulae are:
V (droop) = Ib+ * (Line time − Sample time) / Capacitor
and V (charge) = I_{OUT} * Sample time / Capacitor

For best results the source impedance should be kept low, using a buffer for example.

Because the S/H effectively shorts the input signal during Sample, the input should not be sampled during active video. Typically the sample is made during the back porch period of horizontal blanking. For this reason color composite signals, which have color burst on the back porch, can not be passed. See EL2090 or EL4093 for this application.

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