

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4450C

Wideband Four-Quadrant Multiplier

EL4450C

Features

- Complete four-quadrant multiplier with output amp—requires no extra components
- Good linearity of 0.3%
- 90 MHz bandwidth for both X and Y inputs
- Operates on $\pm 5V$ to $\pm 15V$ supplies
- All inputs are differential
- 400V/ μs slew rate

Applications

- Modulation/Demodulation
- RMS computation
- Real-time power computation
- Nonlinearity correction/generation

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4450CN	-40°C to +85°C	14-Pin P-DIP	MDP0031
EL4450CS	-40°C to +85°C	14-Lead SO	MDP0027

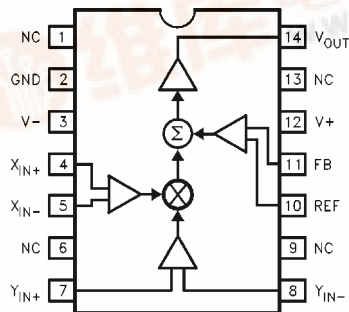
General Description

The EL4450C is a complete four-quadrant multiplier circuit. It offers wide bandwidth and good linearity while including a powerful output voltage amplifier, drawing modest supply current.

The EL4450C operates on $\pm 5V$ supplies and has an analog input range of $\pm 2V$, making it ideal for video signal processing. AC characteristics do not vary over the $\pm 5V$ to $\pm 15V$ supply range.

The multiplier has an operational temperature range of $-40^\circ C$ to $+85^\circ C$ and are packaged in plastic 14-pin P-DIP and SO.

Connection Diagrams



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Absolute Maximum Ratings (T_A = 25 °C)

V+	Positive Supply Voltage	16.5V	I _{OUT}	Output Current	30 mA
V _S	V+ to V- Supply Voltage	33V	P _D	Maximum Power Dissipation	See Curves
V _{IN}	Voltage at any Input or Feedback	V+ to V-	T _A	Operating Temperature Range	-40°C to +85°C
V _{IN}	Difference between Pairs of Inputs or Feedback	6V	T _S	Storage Temperature Range	-60°C to +150°C
I _{IN}	Current into any Input or Feedback Pin	4 mA			

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore T_J = T_C = T_A.

Test Level Test Procedure

- I** 100% production tested and QA sample tested per QA test plan QCX0002.
- II** 100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
- III** QA sample tested per QA test plan QCX0002.
- IV** Parameter is guaranteed (but not tested) by Design and Characterization Data.
- V** Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics

Power Supplies at ±5V, T_A = 25°C, V_{FB} = V_{OUT}.

Parameter	Description	Min	Typ	Max	Test Level	Units
V _{DIFF}	Differential Input Voltage—Clipping	1.8	2.0		I	V
	0.2% nonlinearity		1.0		V	V
V _{CM}	Common-Mode Range of V _{DIFF} = 0, V _S = ±5V	±2.5	±2.8		I	V
	V _S = ±15V	±12.5	±12.8		I	V
V _{OS}	Input Offset Voltage		8	35	I	mV
I _B	Input Bias Current		9	20	I	μA
I _{OS}	Input Offset Current between X _{IN+} and X _{IN-} , Y _{IN+} and Y _{IN-} , REF and FB		0.5	4	I	μA
Gain	Gain Factor of V _{OUT} = Gain × X _{IN+} × Y _{IN}	0.45	0.5	0.55	I	V/V ²
NL _X	Nonlinearity of X Input; X _{IN} between -1V and +1V		0.3	0.7	I	%
NL _Y	Nonlinearity of Y Input; Y _{IN} between -1V and +1V		0.2	0.35	I	%
R _{IN}	Input resistance	X _{IN+} to X _{IN-} , Y _{IN+} to Y _{IN-} ,	230		V	kΩ
		REF to FB	90			
CMRR	Common-Mode Rejection Ratio, X _{IN} and Y _{IN}	70	90		I	dB
PSRR	Power-Supply Rejection Ratio, FB	60	72		I	dB
V _O	Output Voltage Swing (V _{IN} = 0, V _{REF} Varied)	V _S = ±5V	±2.5	±2.8	I	V
		V _S = ±15V	±12.5	±12.8		
I _{SC}	Output Short-Circuit Current	40	85		I	mA
I _S	Supply Current, V _S = ±15V		15.4	18	I	mA

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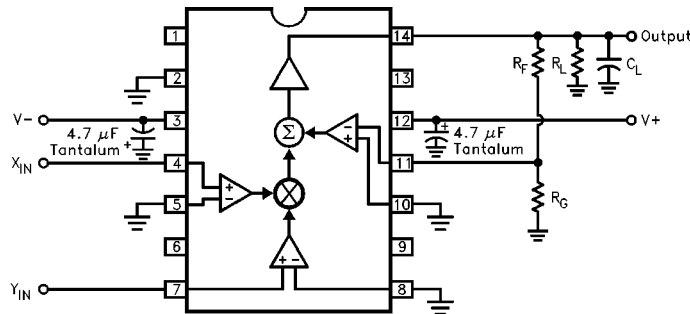
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Closed-Loop AC Electrical Characteristics

Power Supplies at $\pm 12V$, $T_A = 25^\circ C$, $R_L = 500\%$, $C_L = 15pF$

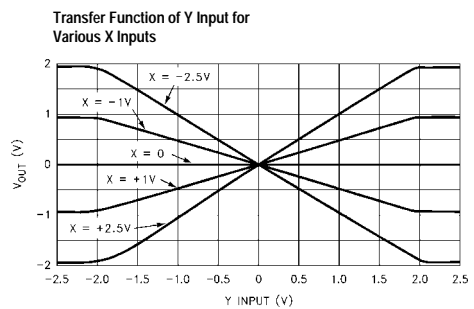
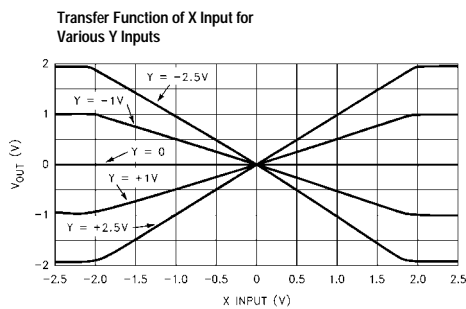
Parameter	Description	Min	Typ	Max	Test Level	Units
BW, -3 dB	-3 dB Small-Signal Bandwidth, X or Y		90		V	MHz
BW, ± 0.1 dB	0.1 dB Flatness Bandwidth		10		V	MHz
Peaking	Frequency Response Peaking		1.0		V	dB
SR	Slew Rate, V_{OUT} between -2V and +2V	300	400		I	V/ μs
V_N	Input-Referred Noise Voltage Density		100		V	nV/Hz

Test Circuit



Note: For typical performance curves, $R_F = 0$, $R_G = \infty$, $V_S = \pm 5V$, $R_L = 500\%$, and $C_L = 15 pF$ unless otherwise noted.

Typical Performance Curves

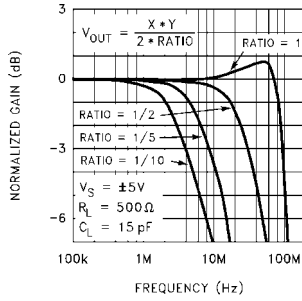


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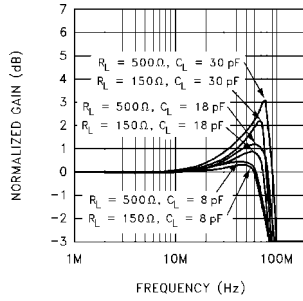
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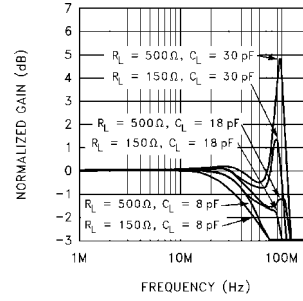
Frequency Response for Various Feedback Divider Ratios



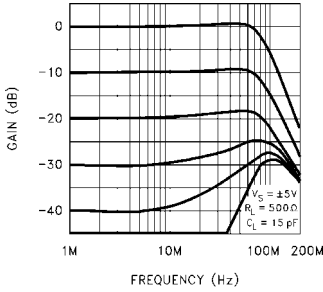
Frequency Response for Various R_L, C_L $V_S = \pm 5V$



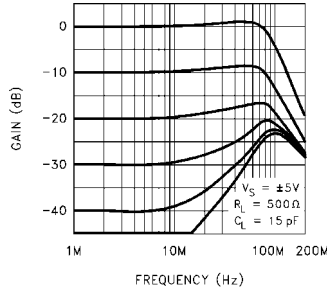
Frequency Response for Various R_L, C_L $V_S = \pm 15V$



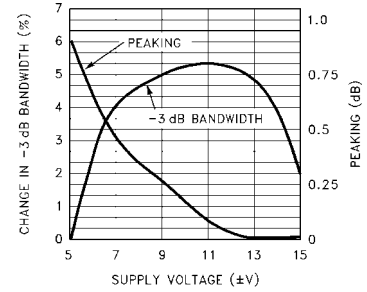
X Input Frequency Response for Various Y DC Inputs



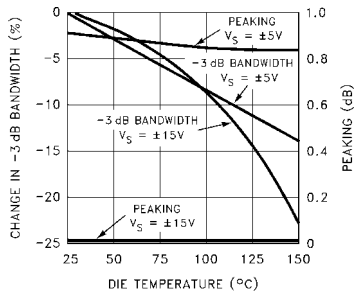
Y Input Frequency Response for Various X DC Inputs



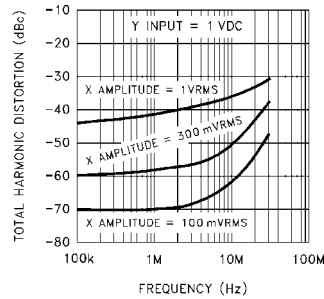
-3 dB Bandwidth and Peaking vs Supply Voltage



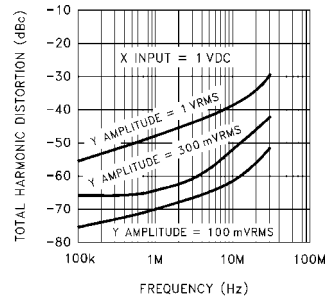
Change in Bandwidth and Peaking vs Temperature



Total Harmonic Distortion of X Input vs Frequency

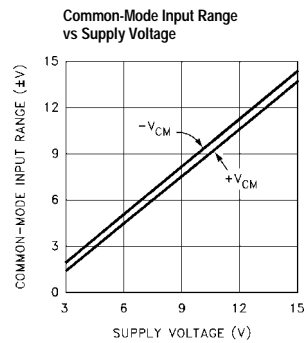
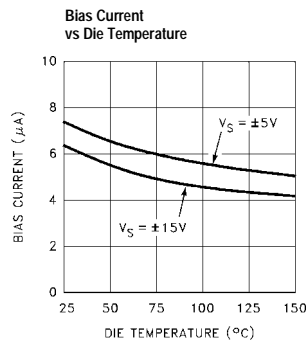
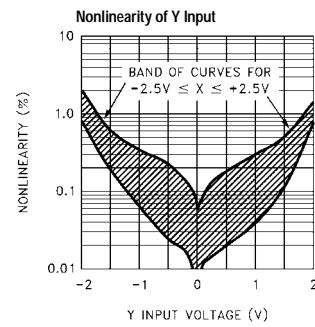
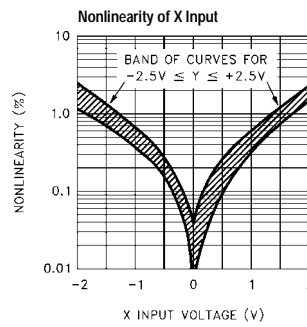
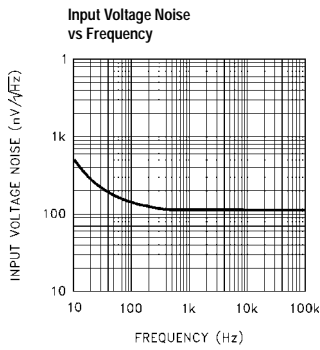
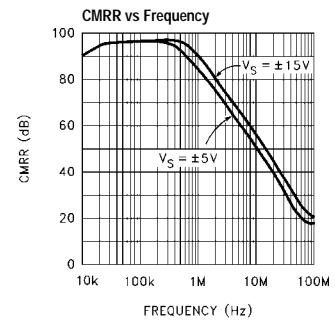
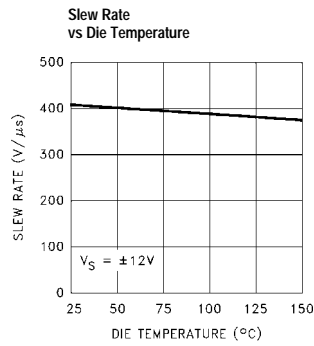
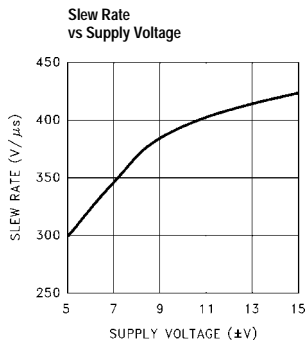


Total Harmonic Distortion of Y Input vs Frequency



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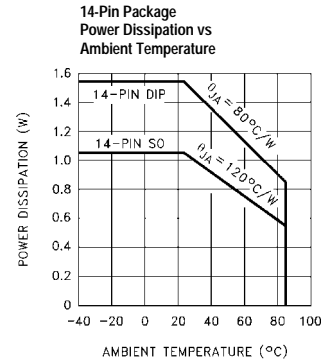
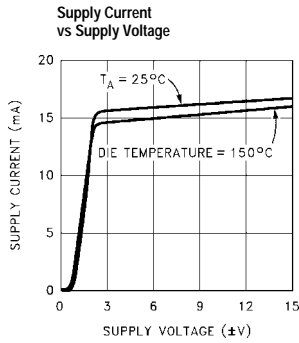
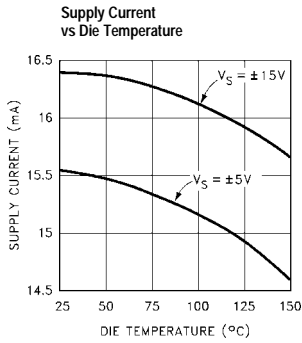
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Applications Information

The EL4450 is a complete four-quadrant multiplier with 90 MHz bandwidth. It has three sets of inputs; a differential multiplying X-input, a differential multiplying Y-input, and another differential input which is used to

complete a feedback loop with the output. Here is a typical connection:

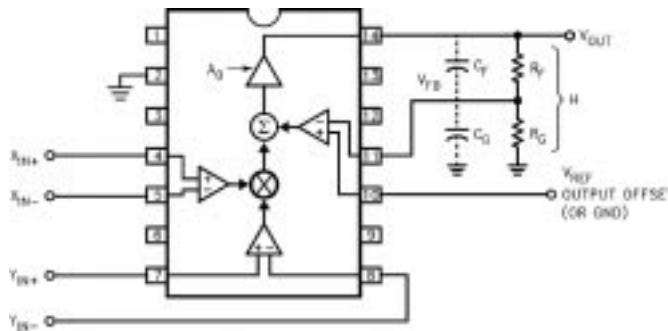


Figure 1.

The gain of the feedback divider is H, and $H = R_G / (R_G + R_F)$. The transfer function of the part is

$$V_{OUT} = A_O \times (1/2 \times ((V_{INX+} - V_{INX-}) \times (V_{INY+} - V_{INY-})) + (V_{REF} - V_{FB})).$$

V_{FB} is connected to V_{OUT} through a feedback network, so $V_{FB} = H \times V_{OUT}$. A_O is the open-loop gain of the amplifier, and is about 600. The large value of A_O drives

$$(1/2 \times ((V_{INX+} - V_{INX-}) \times (V_{INY+} - V_{INY-})) + (V_{REF} - V_{FB})) \rightarrow 0.$$

Rearranging and substituting for V_{REF}

$$V_{OUT} = (1/2 \times ((V_{INX+} - V_{INX-}) \times (V_{INY+} - V_{INY-})) + V_{REF}) / H, \text{ or}$$

$$V_{OUT} = (XY/2 + V_{REF}) / H$$

Thus the output is equal to one-half the product of X and Y inputs and offset by V_{REF} , all gained up by the feedback divider ratio. The EL4450 is stable for a direct connection between V_{OUT} and FB, and the feedback divider may be used for higher output gain, although with the traditional loss of bandwidth.

It is important to keep the feedback divider's impedance at the FB terminal low so that stray capacitance does not diminish the loop's phase margin. The pole caused by the parallel impedance of the feedback resistors and stray capacitance should be at least 150 MHz; typical strays

of 3 pF thus require a feedback impedance of $360^{3/4}$ or less. Alternatively, a small capacitor across R_F can be

used to create more of a frequency-compensated divider. The value of the capacitor should scale with the parasitic capacitance at the FB input. It is also practical to place small capacitors across both the feedback resistors (whose values maintain the desired gain) to swamp out parasitics. For instance, two 10 pF capacitors across equal divider resistors for a maximum gain of 1 will dominate parasitic effects and allow a higher divider resistance.

The REF pin can be used as the output's ground reference, or for DC offsetting of the output, or it can be used to sum in another signal.

Input Connections

The input transistors can be driven from resistive and capacitive sources, but are capable of oscillation when presented with an inductive input. It takes about 80 nH of series inductance to make the inputs actually oscillate, equivalent to four inches of unshielded wiring or about 6 of unterminated input transmission line. The oscillation has a characteristic frequency of 500 MHz. Placing one's finger (via a metal probe) or an oscilloscope probe on the input will kill the oscillation. Normal high-frequency construction obviates any such problems, where the input source is reasonably close to the input. If this is

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not possible, one can insert series resistors of around to 51 $\frac{3}{4}$ to de-Q the inputs.

Signal Amplitudes

Signal input common-mode voltage must be between (V-) + 2.5V and (V+) -2.5V to ensure linearity. Additionally, the differential voltage on any input stage must be limited to $\pm 6V$ to prevent damage. The differential signal range is $\pm 2V$ in the EL4450C. The input range is substantially constant with temperature.

The Ground Pin

The ground pin draws only 6 μA maximum DC current, and may be biased anywhere between (V-) +2.5V and (V+) -3.5V. The ground pin is connected to the IC's substrate and frequency compensation components. It serves as a shield within the IC and enhances input stage CMRR over frequency, and if connected to a potential other than ground, it must be bypassed.

Power Supplies

The EL4450C works well on supplies from $\pm 3V$ to $\pm 15V$. The supplies may be of different voltages as long as the requirements of the GND pin are observed (see the Ground Pin section for a discussion). The supplies should be bypassed close to the device with short leads. 4.7 μF tantalum capacitors are very good, and no smaller bypasses need be placed in parallel. Capacitors as low as 0.01 μF can be used if small load currents flow.

Single-polarity supplies, such as +12V with +5V can be used, where the ground pin is connected to +5V and V- to ground. The inputs and outputs will have to have their levels shifted above ground to accommodate the lack of negative supply.

The power dissipation of the EL4450C increases with power supply voltage, and this must be compatible with the package chosen. This is a close estimate for the dissipation of a circuit:

$$P_D = 2 \cdot I_{S,max} \cdot V_S + (V_S - V_O) \cdot V_O / R_{PAR}$$

where

- $I_{S,max}$ is the maximum supply current
- V_S is the \pm supply voltage (assumed equal)
- V_O is the output voltage

- R_{PAR} is the parallel of all resistors loading the output
- For instance, the EL4450C draws a maximum of 18 mA. With light loading, $R_{PAR} \rightarrow \infty$ and the dissipation with $\pm 5V$ supplies is 180 mW. The maximum supply voltage that the device can run on for a given P_D and the other parameters is

$$V_{S,max} = (P_D + V_O^2 / R_{PAR}) / (2I_{S,max} + V_O / R_{PAR})$$

The maximum dissipation a package can offer is

$$P_{D,max} = (T_{J,max} - T_{A,max}) / \theta_{JA}$$

Where $T_{J,max}$ is the maximum junction temperature, 150°C for reliability, less to retain optimum electrical performance

$T_{A,max}$ is the ambient temperature, 70°C for commercial and 85°C for industrial range

θ_{JA} is the thermal resistance of the mounted package, obtained from data sheet dissipation curves

The more difficult case is the SO-14 package. With a maximum junction temperature of 150°C and a maximum ambient temperature of 85°C, the 65°C temperature rise and package thermal resistance of 120°/W gives a dissipation of 542 mW at 85°C. This allows the full maximum operating supply voltage unloaded, but reduced if loaded significantly.

Output Loading

The output stage is very powerful. It typically can source 85 mA and sink 120 mA. Of course, this is too much current to sustain and the part will eventually be destroyed by excessive dissipation or by metal traces on the die opening. The metal traces are completely reliable while delivering the 30 mA continuous output given in the Absolute Maximum Ratings table in this data sheet, or higher purely transient currents.

Gain accuracy degrades only 0.2% from no load to 100% load. Heavy resistive loading will degrade frequency response and video distortion for loads $< 100\%$.

Capacitive loads will cause peaking in the frequency response. If a capacitive load must be driven, a small-valued series resistor can be used to isolate it. 12 $\frac{3}{4}$ to 51 $\frac{3}{4}$ should suffice. A 22 $\frac{3}{4}$ series resistor will limit peaking to 2.5 dB with even a 220 pF load.

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Mixer Applications

Because of its lower distortion levels, the Y input is the better choice for a mixer's signal port. The X input would receive oscillator amplitudes of about 1V RMS maximum. Carrier suppression is initially limited by the offset voltage of the Y input, 20 mV maximum, and is

about 37 dB worst-case. Better suppression can be obtained by nulling the offset of the X input. Similarly, nulling the offset of the Y input will improve signal-port suppression. Driving an input differentially will also maximize feedthrough suppression at frequencies beyond 10 MHz.

AC Level Detectors

Square-law converters are commonly used to convert AC signals to DC voltages corresponding to the original amplitude in subsystems like automatic gain controls (AGC's) and amplitude-stabilized oscillators. Due to the controlled AC amplitudes, the inputs of the multiplier

will see a relatively constant signal level. Best performance will be obtained for inputs between 200 mVRMS and 1 VRMS. The traditional use of the EL4450C as an AGC detector and control loop would be:

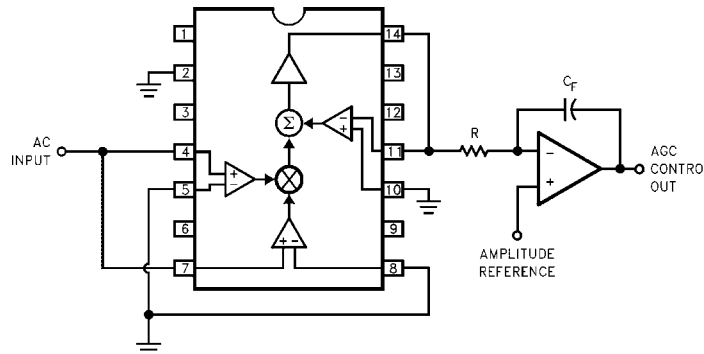


Figure 2. Traditional AGC Detector/DC Feedback Circuit

The EL4450C simply provides an output equal to the square of the input signal and an integrator filters out the AC component, while comparing the DC component to an amplitude reference. The integrator output is the DC control voltage to the variable-gain sections of the AGC (not shown). If a negative polarity of reference is required, one of the multiplier input terminal pairs is reversed, inverting the multiplier output. In-

put bias current will cause input voltage offsets due to source impedances; putting a compensating resistor in series with the grounded inputs of the EL4450C will reduce this offset greatly.

This control system will attempt to force

$$V_{IN,RMS}^2/4 = V_{REF}$$

The extra op-amp can be eliminated by using this circuit:

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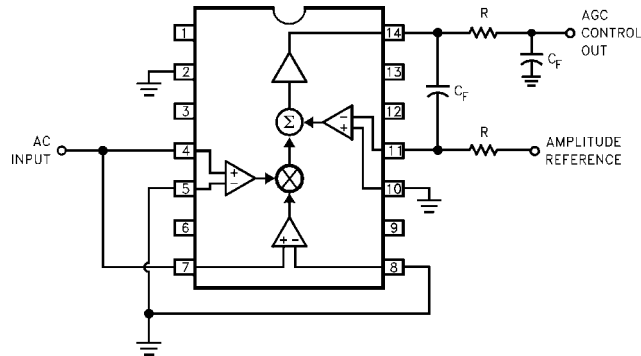


Figure 3. Simplified AGC Detector/DC Feedback Circuit

Here the internal op-amp of the EL4450C replaces the external amplifier. The feedback capacitor C_F does not provide a perfect integration action; a zero occurs at a frequency of $1/2\pi RC_F$. This is canceled by including another RC_F pair at the AGC control output. If the reference voltage must be negative, the resistor at pin 11 is connected to ground rather than the reference and pin 10 connected to the reference.

The amplitude reference will have to support some AC currents flowing through R. If this is a problem, several changes can be made to

eliminate it. The reference is connected to pin 10 and the resistor R connected to pin 11 reconnected to ground, and one of the multiplier input connections are reversed.

Square-law detectors have a restricted input range, about 10:1, because the output rapidly disappears into the DC errors as signal amplitudes reduce. This circuit gives a multiplier output that is the absolute value of the input, thus increasing range to 100:1:

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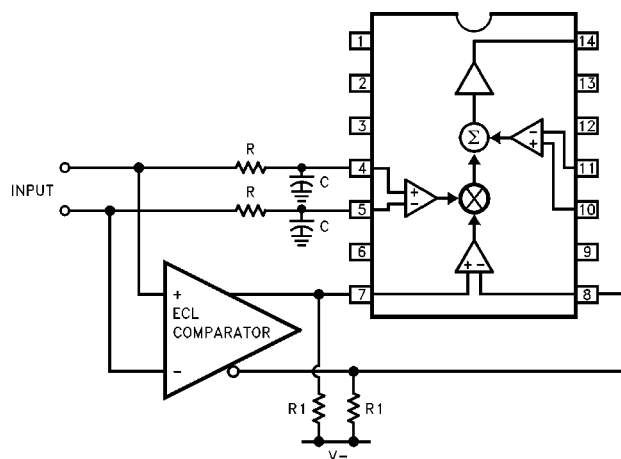


Figure 4. Absolute-Value Input Circuitry

An ECL comparator produces an output corresponding to the sign of the input, which when multiplied by the input produces an effective

absolute-value function. The RC product connected to the X inputs simply emulates the time delay of the comparator to maintain circuit accuracy at higher frequencies.

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Nonlinear Function Generation

The REF pin of the EL4450C can be used to sum in various quantities of polynomial function generators. For instance, this sum of REF allows a linear signal path

which can have various amounts of squared signal added:

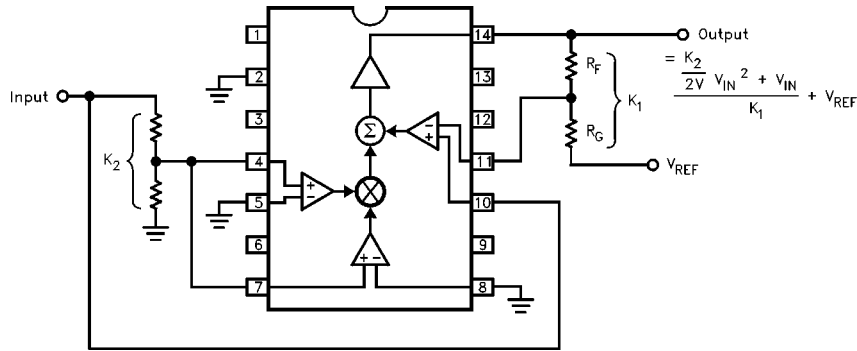


Figure 5. Polynomial Function Generator

The polarity of the squared signal can be reversed by swapping one of the X or Y input pairs.

The REF and FB pins also simplify feedback schemes that allow square-rooting:

The diode and I_{pulldown} assure that the output will always produce the positive square-root of the input signal. I_{pulldown} should be large enough to assure that the diode be forward-biased for any load current. In this configuration, the bandwidth of the circuit will reduce for smaller input signals.

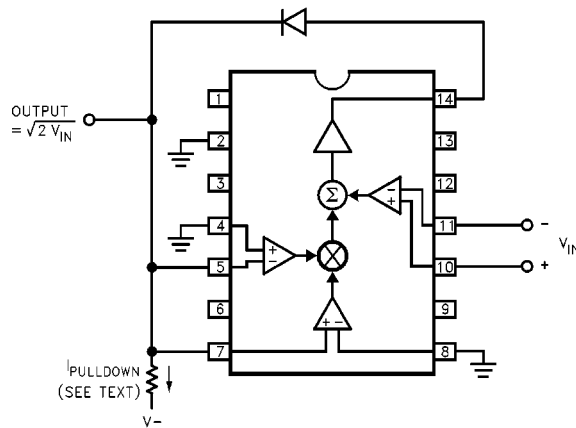


Figure 6. Square-Rooter

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The REF and FB terminals can also be used to implement division:

The output frequency response reduces for smaller values of V_X , but is not affected by V_{REF} .

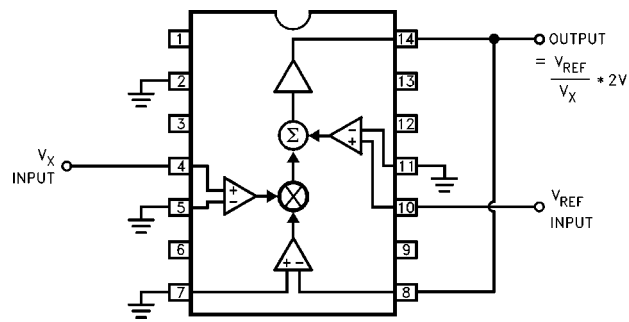


Figure 7. Divider Connection

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General Disclaimer

Specifications contained in this data sheet are in effect as of the publication date shown. Elantec, Inc. reserves the right to make changes in the circuitry or specifications contained herein at any time without notice. Elantec, Inc. assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Elantec, Inc.

1996 Tarob Court
Milpitas, CA 95035
Telephone: (408) 945-1323
(800) 333-6314
Fax: (408) 945-9305
European Office: 44-71-482-4596

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