

Horizontal Genlock, 4F_{SC}

The EL4584 is a PLL (Phase Lock Loop) sub system, designed for video applications but also suitable for general purpose use up to 36MHz. In video applications, this device generates a TTL/CMOS compatible Pixel Clock (CLK OUT) which is a multiple of the TV horizontal scan rate and phase locked to it.

The reference signal is a horizontal sync signal, TTL/CMOS format, which can be easily derived from an analog composite video signal with the EL4583 Sync Separator. An input signal to "coast" is provided for applications where periodic disturbances are present in the reference video timing such as VTR head switching. The Lock detector output indicates correct lock.

The divider ratio is four ratios for NTSC and four similar ratios for the PAL video timing standards, by external selection of three control pins. These four ratios have been selected for common video applications including 4F_{SC}, 3F_{SC}, 13.5MHz (CCIR 601 format) and square picture elements used in some workstation graphics. To generate 8F_{SC}, 6F_{SC}, 27MHz (CCIR 601 format) etc. use the EL4585, which includes an additional divide-by-two stage.

For applications where these frequencies are inappropriate or for general purpose PLL applications the internal divider can be bypassed and an external divider chain used.

FREQUENCIES AND DIVISORS

FUNCTION	3F _{SC} (NOTE 1)	CCIR 601 (NOTE 2)	SQUARE (NOTE 3)	4F _{SC}
Divisor	851	864	944	1135
PAL F _{OSC} (MHz)	13.301	13.5	14.75	17.734
Divisor	682	858	780	910
NTSC F _{OSC} (MHz)	10.738	13.5	12.273	14.318

NOTES:

- 3F_{SC} numbers do not yield integer divisors.
- CCIR 601 Divisors yield 720 pixels in the portion of each line for NTSC and PAL.
- Square pixels format gives 640 pixels for NTSC and 768 pixels for PAL in the active portion.

Features

- 36MHz, general purpose PLL
- 4F_{SC} based timing (use the EL4585 for 8F_{SC})
- Compatible with EL4583 sync separator
- VCXO, Xtal, or LC tank oscillator
- < 2ns jitter (VCXO)
- User controlled PLL capture and lock
- Compatible with NTSC and PAL TV formats
- 8 pre-programmed TV scan rate clock divisors
- Selectable external divide for custom ratios
- Single 5V, low current operation
- Pb-Free plus anneal available (RoHS compliant)

Applications

- Pixel clock regeneration
- Video compression engine (MPEG) clock generator
- Video capture or digitization
- PIP (Picture in Picture) timing generator
- Text or graphics overlay timing

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL4584CN	16-Pin PDIP	-	MDP0031
EL4584CS	16-Pin SO (0.150")	-	MDP0027
EL4584CS-T7	16-Pin SO (0.150")	7"	MDP0027
EL4584CS-T13	16-Pin SO (0.150")	13"	MDP0027
EL4584CSZ (See Note)	16-Pin SO (0.150") (Pb-free)	-	MDP0027
EL4584CSZ-T7 (See Note)	16-Pin SO (0.150") (Pb-free)	7"	MDP0027
EL4584CSZ-T13 (See Note)	16-Pin SO (0.150") (Pb-free)	13"	MDP0027

*For 6F_{SC} and 8F_{SC} clock frequencies, see EL4585 datasheet.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Demo Board

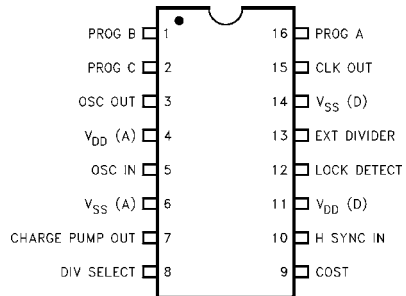
A demo PCB is available for this product.



EL4584

Pinout

EL4584
(16-PIN SO, PDIP)
TOP VIEW



EL4584

Absolute Maximum Ratings (T_A = 25°C)

V _{CC} Supply 7V	Oscillator Frequency 36MHz
Operating Junction Temperature 125°C	Pin Voltages -0.5V to V _{CC} +0.5V
Storage Temperature -65°C to +150°C	Operating Ambient Temperature Range -40°C to +85°C
Power Dissipation 400mW	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T_J = T_C = T_A

DC Electrical Specifications V_{DD} = 5V, T_A = 25°C unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I _{DD}	V _{DD} = 5V (Note 1)		2	4	mA
V _{IL} Input Low Voltage				1.5	V
V _{IH} Input High Voltage		3.5			V
I _{IL} Input Low Current	All inputs except COAST, V _{IN} = 1.5V	-100			nA
I _{IH} Input High Current	All inputs except COAST, V _{IN} = 3.5V			100	nA
I _{IL} Input Low Current	COAST pin, V _{IN} = 1.5V	-100	-60		μA
I _{IH} Input High Current	COAST pin, V _{IN} = 3.5V		60	100	μA
V _{OL} Output Low Voltage	Lock Det, I _{OL} = 1.6mA			0.4	V
V _{OH} Output High Voltage	Lock Det, I _{OH} = -1.6mA	2.4			V
V _{OL} Output Low Voltage	CLK, I _{OL} = 3.2mA			0.4	V
V _{OH} Output High Voltage	CLK, I _{OH} = -3.2mA	2.4			V
V _{OL} Output Low Voltage	OSC Out, I _{OL} = 200μA			0.4	V
V _{OH} Output High Voltage	OSC Out, I _{OH} = -200μA	2.4			V
I _{OL} Output Low Current	Filter Out, V _{OUT} = 2.5V	200	300		μA
I _{OH} Output High Current	Filter Out, V _{OUT} = 2.5V		-300	-200	μA
I _{OL} /I _{OH} Current Ratio	Filter Out, V _{OUT} = 2.5V	1.05	1.0	0.95	
I _{LEAK} Filter Out	Coast Mode, V _{DD} > V _{OUT} > 0V	-100	±1	100	nA

NOTE:

1. All inputs to 0V, COAST floating.

AC Electrical Specifications V_{DD} = 5V, T_A = 25°C unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VCO Gain @ 20MHz	Test circuit 1		15.5		dB
H _{SYNC} S/N Ratio	V _{DD} = 5V (Note 1)	35			dB
Jitter	VCXO oscillator		1		ns
Jitter	LC oscillator (Typ)		10		ns

NOTE:

1. Noisy video signal input to EL4583, H_{SYNC} input to EL4584. Test for positive signal lock.

EL4584

Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION
1, 2, 16	PROG A,B,C	Digital inputs to select ÷ N value for internal counter. See table below for values.
3	OSC/VCO OUT	Output of internal inverter/oscillator. Connect to external crystal or LC tank VCO circuit.
4	VDD (A)	Analog positive supply for oscillator, PLL circuits.
5	OSC/VCO IN	Input from external VCO.
6	VSS (A)	Analog ground for oscillator, PLL circuits.
7	CHARGE PUMP OUT	Connect to loop filter. If the H _{SYNC} phase is leading or H _{SYNC} frequency > CLK ÷ N, current is pumped into the filter capacitor to increase VCO frequency. If H _{SYNC} phase is lagging or frequency < CLK ÷ N, current is pumped out of the filter capacitor to decrease VCO frequency. During coast mode or when locked, charge pump goes to a high impedance state.
8	DIV SELECT	Divide select input. When high, the internal divider is enabled and EXT DIV becomes a test pin, outputting CLK ÷ N. When low, the internal divider is disabled and EXT DIV is an input from an external ÷ N.
9	COAST	Tri-state logic input. Low (<1/3*V _{CC}) = normal mode, Hi Z (or 1/3 to 2/3*V _{CC}) = fast lock mode, High (>2/3*V _{CC}) = coast mode.
10	HSYNC IN	Horizontal sync pulse (CMOS level) input.
11	VDD (D)	Positive supply for digital, I/O circuits.
12	LOCK DET	Lock Detect output. Low level when PLL is locked. Pulses high when out of lock.
13	EXT DIV	External Divide input when DIV SEL is low, internal ÷N output when DIV SEL is high.
14	VSS (D)	Ground for digital, I/O circuits.
15	CLK OUT	Buffered output of the VCO.

TABLE 1. VCO DIVISORS

PROG A (PIN 16)	PROG B (PIN 1)	PROG C (PIN 2)	DIV VALUE (N)
0	0	0	851
0	0	1	864
0	1	0	944
0	1	1	1135
1	0	0	682
1	0	1	858
1	1	0	780
1	1	1	910

Timing Diagrams

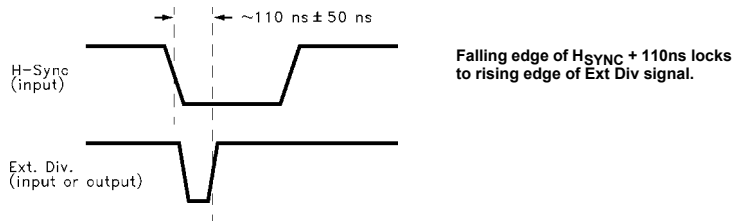


FIGURE 1. PLL LOCKED CONDITION (PHASE ERROR = 0)

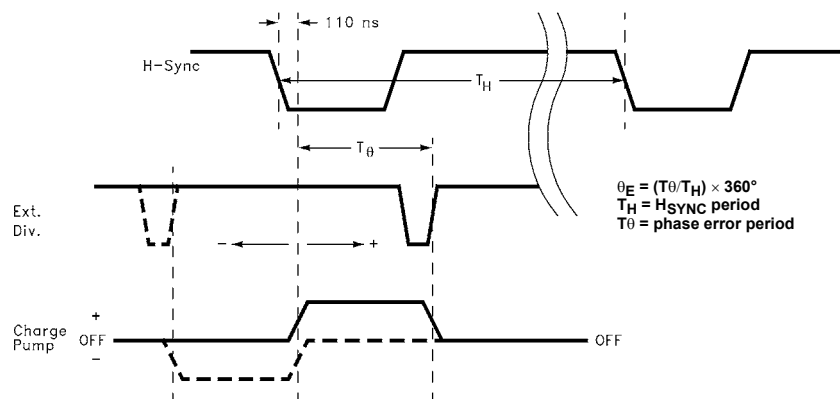


FIGURE 2. OUT OF LOCK CONDITION

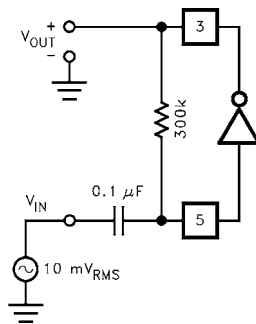
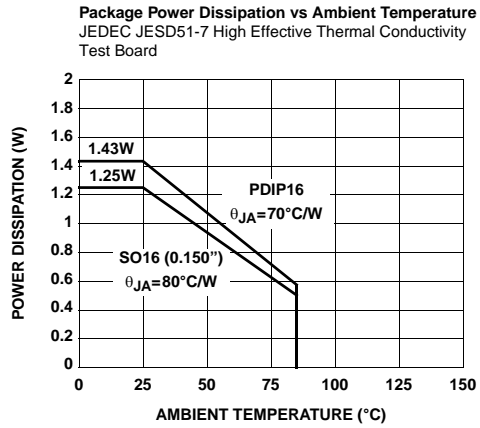
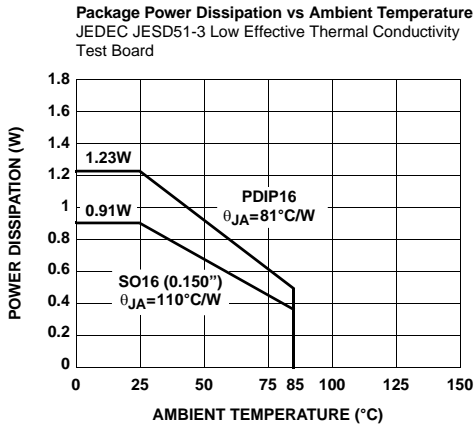
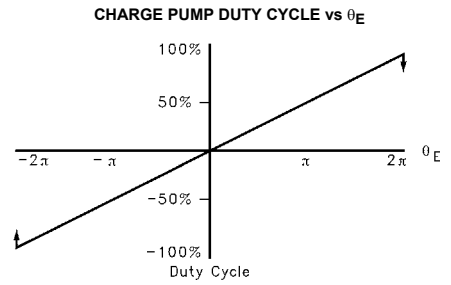
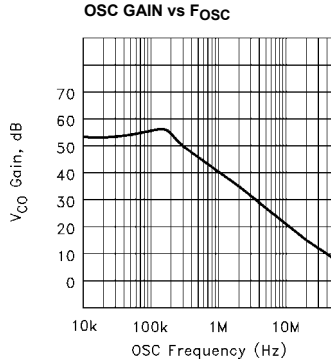
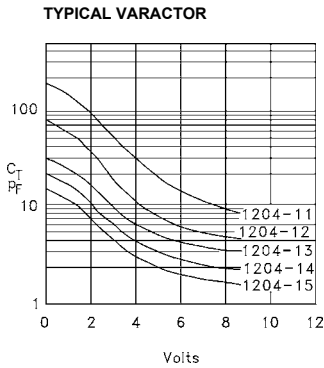
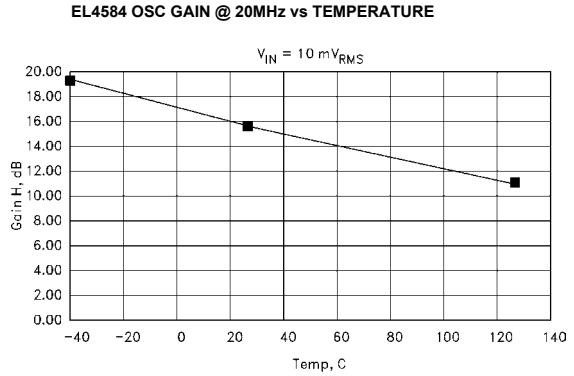
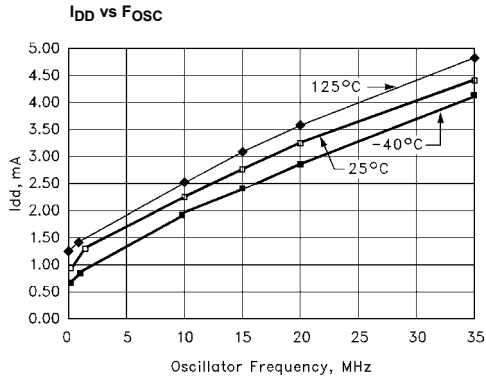


FIGURE 3. TEST CIRCUIT 1

EL4584

Typical Performance Curves



of a long pendulum. Due to parasitic effects of PCB traces and component variables, it will take some trial and error experimentation to determine the best values to use for any given situation. Use the component tables as a starting point, but be aware that deviation from these values is not out of the ordinary.

External Divide

DIV SEL (pin 8) controls the use of the internal divider. When high, the internal divider is enabled and EXT DIV (pin 13) outputs the CLK out divided by N. This is the signal to which the horizontal sync input will lock. When divide select is low, the internal divider output is disabled, and external divide becomes an input from an external divider, so that a divisor other than one of the 8 pre-programmed internal divisors can be used.

Normal Mode

Normal mode is enabled by pulling COAST (pin 9) low (below $1/3 \cdot V_{CC}$). If HSYNC and $CLK \div N$ have any phase or frequency difference, an error signal is generated and sent to the charge pump. The charge pump will either force current into or out of the filter capacitor in an attempt to modulate the VCO frequency. Modulation will continue until the phase and frequency of $CLK \div N$ exactly match the HSYNC input. When the phase and frequency match (with some offset in phase that is a function of the VCO characteristics), the error signal goes to zero, lock detect no longer pulses high, and the charge pump enters a high impedance state. The clock is now locked to the HSYNC input. As long as phase and frequency differences remain small, the PLL can adjust the VCO to remain locked and lock detect remains low.

Fast Lock Mode

Fast Lock mode is enabled by either allowing coast to float, or pulling it to mid supply (between $1/3$ and $2/3 \cdot V_{CC}$). In this mode, lock is achieved much faster than in normal mode, but the clock divisor is modified on the fly to achieve this. If the phase detector detects an error of enough magnitude, the clock is either inhibited or reset to attempt a "fast" lock of the signals.

Forcing the clock to be synchronized to the HSYNC input this way allows a lock in approximately 2 H-cycles, but the clock spacing will not be regular during this time. Once the near lock condition is attained, charge pump output should be very close to its lock-on value and placing the device into normal mode should result in a normal lock very quickly. Fast Lock mode is intended to be used where HSYNC becomes irregular, until a stable signal is again obtained.

Coast Mode

Coast mode is enabled by pulling COAST (pin 9) high (above $2/3 \cdot V_{CC}$). In coast mode the internal phase detector is disabled and filter out remains in high impedance mode to keep filter out voltage and VCO frequency as constant a

possible. VCO frequency will drift as charge leaks from the filter capacitor, and the voltage changes the VCO operating point. Coast mode is intended to be used when noise or signal degradation result in loss of horizontal sync for many cycles. The phase detector will not attempt to adjust to the resultant loss of signal so that when horizontal sync returns, sync lock can be re-established quickly. However, if much VCO drift has occurred, it may take as long to re-lock as when restarting.

Lock Detect

Lock detect (pin 12) will go low when lock is established. Any DC current path from charge pump out will skew EXT DIV relative to HSYNC in, tending to offset or add to the 110ns internal delay, depending on which way the extra current is flowing. This offset is called static phase error, and is always present in any PLL system. If, when the part stabilizes in a locked mode, lock detect is not low, adding or subtracting from the loop filter series resistor R_2 will change this static phase error to allow LDET to go low while in lock. The goal is to put the rising edge of EXT DIV in sync with the falling edge of HSYNC + 110ns. (See timing diagrams.) Increasing R_2 decreases phase error, while decreasing R_2 increases phase error. (Phase error is positive when EXT DIV lags HSYNC.) The resistance needed will depend on VCO design or VCXO module selection.

Applications Information

Choosing External Components

1. To choose LC VCO components, first pick the desired operating frequency. For our example we will use 14.31818MHz, with an HSYNC frequency of 15.734kHz.
2. Choose a reasonable inductor value (10–20 μ H works well). We choose 15 μ H.
3. Calculate C_T needed to produce F_{OSC} .

$$F_{OSC} = \frac{1}{2\pi\sqrt{LC_T}}$$

$$C_T = \frac{1}{4\pi^2 F^2 L} = \frac{1}{4\pi^2 (14.318e6)^2 (15e-6)} = 8.2pF$$

4. From the varactor data sheet find C_V @ 2.5V, the desired lock voltage. $C_V = 23pF$ for our SMV1204-12, for example.
5. C_2 should be about $10C_V$, so we choose $C_2 = 220pF$ for our example.
6. Calculate C_1 . Since:

$$C_T = \frac{C_1 C_2 C_V}{(C_1 C_2) + (C_1 C_V) + (C_2 C_V)}$$

then:

$$C_1 = \frac{C_2 C_T C_V}{(C_2 C_V) - (C_2 C_T) - (C_T C_V)}$$

EL4584

For our example, $C_1 = 14\text{pF}$. (A trim cap may be used for fine tuning.) Examples for each frequency using the internal divider follow.

Typical Application

Horizontal genlock provides clock for an analog to digital converter, digitizing analog video.

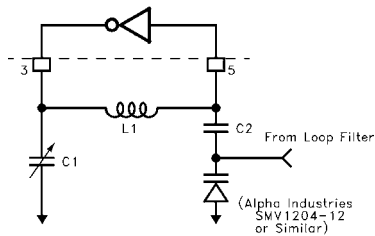
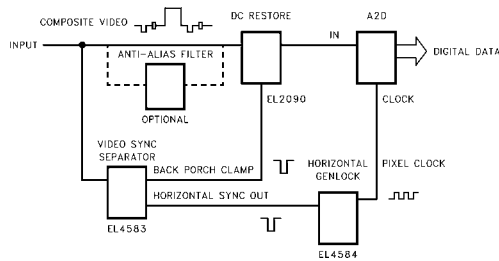


FIGURE 4. TYPICAL LC VCO

LC VCO COMPONENT VALUES (APPROXIMATE) (NOTE)

FREQUENCY (MHZ)	L ₁ (μH)	C ₁ (pF)	C ₂ (pF)
13.301	15	18	220
13.5	15	17	220
14.75	12	18	220
17.734	12	10	220
10.738	22	20	220
12.273	18	17	220
14.318	15	14	220

NOTE: Use shielded inductors for optimum performance.

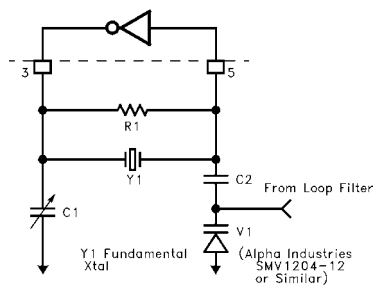


FIGURE 5. TYPICAL XTAL VCO

XTAL VCO COMPONENT VALUES (APPROXIMATE)

FREQUENCY (MHZ)	R ₁ (kΩ)	C ₁ (pF)	C ₂ (μF)
13.301	300	15	0.001
13.5	300	15	0.001
14.75	300	15	0.001
17.734	300	15	0.001
10.738	300	15	0.001
12.273	300	15	0.001
14.318	300	15	0.001

The above oscillators are arranged as Colpitts oscillators, and the structure is redrawn here to emphasize the split capacitance used in a Colpitts oscillator. It should be noted that this oscillator configuration is just one of literally hundreds possible, and the configuration shown here does not necessarily represent the best solution for all applications. Crystal manufacturers are very informative sources on the design and use of oscillators in a wide variety of applications, and the reader is encouraged to become familiar with them.

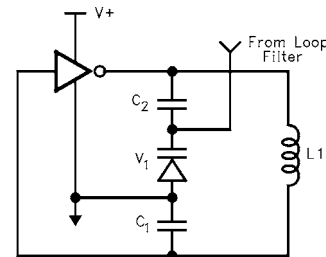


FIGURE 6. COLPITTS OSCILLATOR

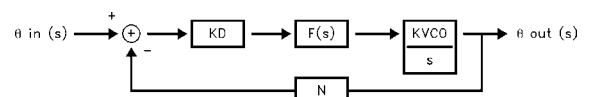
C_1 is to adjust the center frequency, C_2 DC isolates the control from the oscillator, and V_1 is the primary control device. C_2 should be much larger than C_V so that V_1 has maximum modulation capability. The frequency of oscillation is given by:

$$F = \frac{1}{12\pi\sqrt{LC_T}}$$

$$C_T = \frac{C_1 C_2 C_V}{(C_1 C_2) + (C_1 C_V) + (C_2 C_V)}$$

Choosing Loop Filter Components

The PLL, VCO, and loop filter can be described as:



Where:

K_d = phase detector gain in A/rad

$F(s)$ = loop filter impedance in V/A

K_{VCO} = VCO gain in rad/s/V

N = internal or external divisor

It can be shown that for the loop filter shown below:

$$C_3 = \frac{K_d K_{VCO}}{N \omega_n^2}, C_4 = \frac{C_3}{10}, R_3 = \frac{2N\zeta\omega_n}{K_d K_{VCO}}$$

$$C_3 = \frac{K_d K_{VCO}}{N \omega_n^2} = \frac{(4.77e-5)(6.05e6)}{(910)(5000)^2} = 0.01 \mu F$$

$$C_4 = \frac{C_3}{10} = 0.0001 \mu F$$

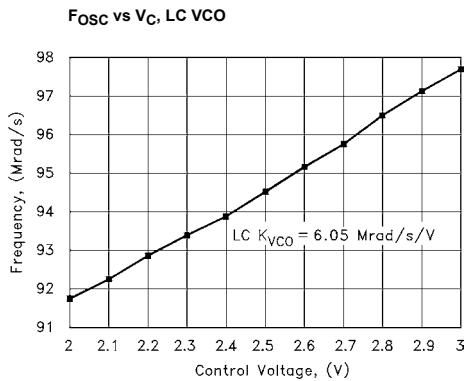
$$R_3 = \frac{2N\zeta\omega_n}{K_d K_{VCO}} = \frac{(2)(910)(1)(5000)}{(4.77e-5)(6.05e6)} = 31.5 k\Omega$$

Where ω_n = loop filter bandwidth, and ζ = loop filter damping factor.

- $K_d = 300 \mu A / 2\pi \text{ rad} = 4.77e-5 A/\text{rad}$ for the EL4584.
- The loop bandwidth should be about H_{SYNC} frequency/20, and the damping ratio should be 1 for optimum performance. For our example, $\omega_n = 15.734 \text{ kHz} / 20 = 787 \text{ Hz} \approx 5000 \text{ rad/S}$.
- $N = 910$ from table 1.

$$N = \frac{VCO \text{ frequency}}{H - SYNC \text{ frequency}} = \frac{14.31818 \text{ M}}{15.73426 \text{ k}} = 910$$

- K_{VCO} represents how much the VCO frequency changes for each volt applied at the control pin. It is assumed (but probably is not) linear about the lock point (2.5V). Its value depends on the VCO configuration and the varactor transfer function $C_V = F(V_C)$, where V_C is the reverse bias control voltage, and C_V is varactor capacitance. Since $F(V_C)$ is nonlinear, it is probably best to build the VCO and measure K_{VCO} about 2.5V. The results of one such measurement are shown below. The slope of the curve is determined by linear regression techniques and equals K_{VCO} . For our example, $K_{VCO} = 6.05 \text{ Mrad/S/V}$.



- Now we can solve for C_3 , C_4 , and R_3 .

We choose $R_3 = 30 k\Omega$ for convenience.

- Notice R_2 has little effect on the loop filter design. R_2 should be large, around 100k, and can be adjusted to compensate for any static phase error $T\theta$ at lock, but if made too large, will slow loop response. If R_2 is made smaller, $T\theta$ (see timing diagrams) increases, and if R_2

increases, $T\theta$ decreases. For LDET to be low at lock, $|T\theta| < 50 \text{ ns}$. C_4 is used mainly to attenuate high frequency noise from the charge pump.

Lock Time

Let $T = R_3 C_3$. As T increases, damping increases, but so does lock time. Decreasing T decreases damping and speeds up loop response, but increases overshoot and thus increases the number of hunting oscillations before lock. Critical damping ($\zeta = 1$) occurs at minimum lock time. Because decreased damping also decreases loop stability, it is sometimes desirable to design slightly overdamped ($\zeta > 1$), trading lock time for increased stability.

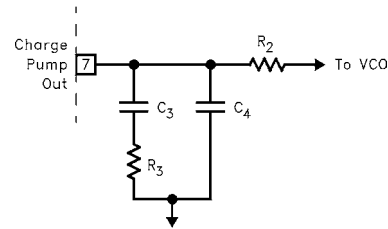


FIGURE 7. TYPICAL LOOP FILTER

LC LOOP FILTER COMPONENTS (APPROXIMATE)

FREQUENCY (MHZ)	R ₂ (kΩ)	R ₃ (kΩ)	C ₃ (μF)	C ₄ (μF)
13.301	100	30	0.01	0.001
13.5	100	30	0.01	0.001
14.75	100	33	0.01	0.001
17.734	100	39	0.01	0.001
10.738	100	22	0.01	0.001
12.273	100	27	0.01	0.001
14.318	100	30	0.01	0.001

EL4584

XTAL LOOP FILTER COMPONENTS (APPROXIMATE)

FREQUENCY (MHz)	R ₂ (kΩ)	R ₃ (MΩ)	C ₃ (pF)	C ₄ (pF)
13.301	100	4.3	68	6.8
13.5	100	4.3	68	6.8
14.75	100	4.3	68	6.8
17.734	100	4.3	68	6.8
10.738	100	4.3	68	6.8
12.273	100	4.3	68	6.8
14.318	100	4.3	68	6.8

PCB Layout Considerations

It is highly recommended that power and ground planes be used in layout. The oscillator and filter sections constitute a feedback loop and thus care must be taken to avoid any feedback signal influencing the oscillator except at the control input. The entire oscillator/filter section should be surrounded by copper ground to prevent unwanted influences from nearby signals. Use separate paths for

analog and digital supplies, keeping the analog (oscillator section) as short and free from spurious signals as possible. Careful attention must be paid to correct bypassing. Keep lead lengths short and place bypass caps as close to the supply pins as possible. If laying out a PCB to use discrete components for the VCO section, care must be taken to avoid parasitic capacitance at the OSC pins 3 and 5, and FILTER out (pin 7). Remove ground and power plane copper above and below these traces to avoid making a capacitive connection to them. It is also recommended to enclose the oscillator section within a shielded cage to reduce external influences on the VCO, as they tend to be very sensitive to "handwaving" influences, the LC variety being more sensitive than crystal controlled oscillators. In general, the higher the operating frequency, the more important these considerations are. Self contained VCXO or VCO modules are already mounted in a shielding cage and therefore do not require as much consideration in layout. Many crystal manufacturers publish informative literature regarding use and layout of oscillators which should be helpful.

Demo Board

