Monolithic 600mA Step-Down Regulator with Low Quiescent Current

The EL7530 is a synchronous, integrated FET 600mA step-down regulator with internal compensation. It operates with an input voltage range from 2.5V to 5.5V, which accommodates supplies of 3.3V, 5V, or a Li-Ion battery source. The output can be externally set from 0.8V to V_{IN} with a resistive divider.

The EL7530 features automatic PFM/PWM mode control, or PWM mode only. The PWM frequency is typically 1.4MHz and can be synchronized up to 12MHz. The typical no load quiescent current is only 120µA. Additional features include a Power-Good output, <1µA shut-down current, short-circuit protection, and over-temperature protection.

The EL7530 is available in the 10-pin MSOP package, making the the entire converter occupy less than 0.18in^2 of PCB area with components on one side only. The 10-pin MSOP package is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER (BRAND)	PACKAGE	TAPE & REEL	PKG. DWG. #
EL7530IY (BYAAA)	10-Pin MSOP	-	MDP0043
EL7530IY-T7 (BYAAA)	10-Pin MSOP	7”	MDP0043
EL7530IY-T13 (BYAAA)	10-Pin MSOP	13”	MDP0043
EL7530IYZ (BAADA) (Note)	10-Pin MSOP (Pb-free)	-	MDP0043
EL7530IYZ-T7 (BAADA) (Note)	10-Pin MSOP (Pb-free)	7”	MDP0043
EL7530IYZ-T13 (BAADA) (Note)	10-Pin MSOP (Pb-free)	13”	MDP0043

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

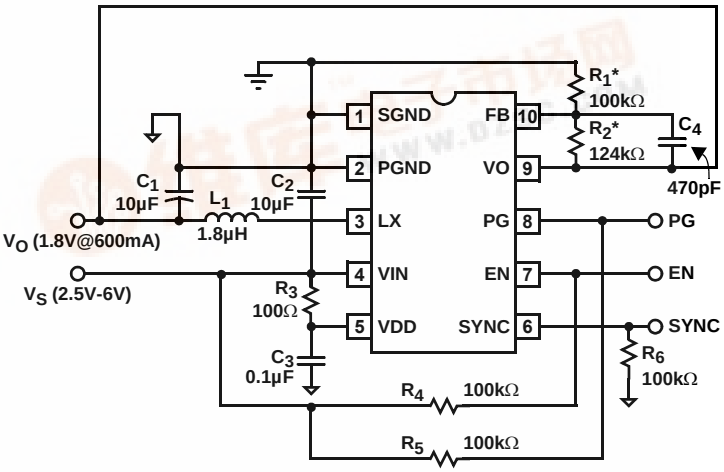
- Less than 0.18in^2 footprint for the complete 600mA converter
- Components on one side of PCB
- Max height 1.1mm MSOP10
- Power-Good (PG) output
- Internally-compensated voltage mode controller
- Up to 95% efficiency
- <1µA shut-down current
- 120µA quiescent current
- Overcurrent and over-temperature protection
- External synchronizable up to 12MHz
- Pb-Free plus anneal available (RoHS compliant)

Applications

- PDA and pocket PC computers
- Bar code readers
- Cellular phones
- Portable test equipment
- Li-Ion battery powered devices
- Small form factor (SFP) modules

Pinout and Typical Application Diagram

EL7530
TOP VIEW



* $V_O = 0.8V * (1 + R_2 / R_1)$

Absolute Maximum Ratings (T_A = 25°C)

V_{IN}, V_{DD}, PG to SGND . . . . . -0.3V to +6.5V
LX to PGND . . . . . -0.3V to (V_{IN} + +0.3V)
SYNC, EN, V_O, FB to SGND . . . . . -0.3V to (V_{IN} + +0.3V)
PGND to SGND . . . . . -0.3V to +0.3V
Peak Output Current 800mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
MSOP10 Package (Note 1)	115

Operating Ambient Temperature . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

Electrical Specifications

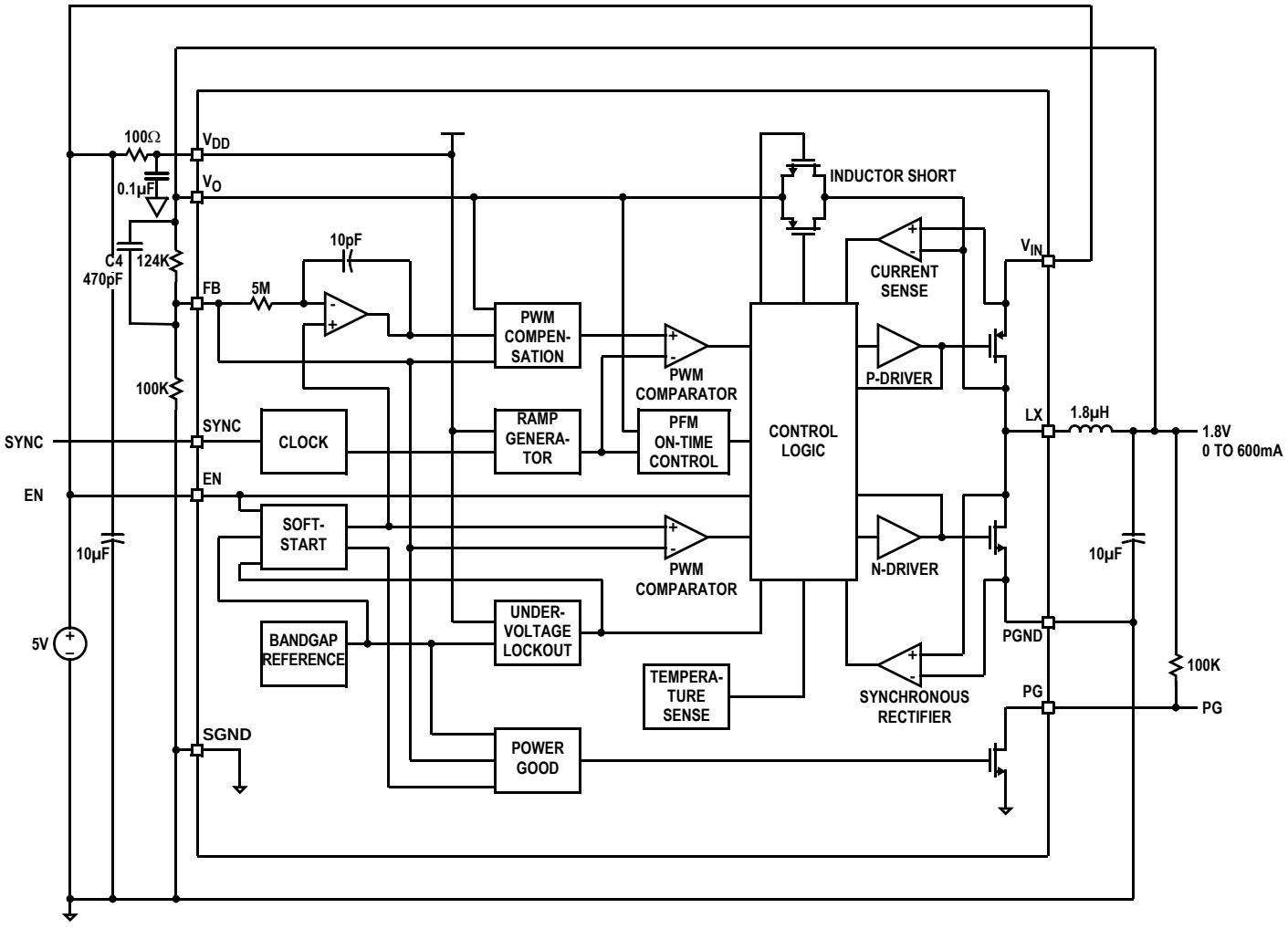
$V_{DD} = V_{IN} = V_{EN}$ = 3.3V, C1 = C2 = 10µF, L = 1.8µH, V_O = 1.8V (as shown in Typical Application Diagram), unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
V_{FB}	Feedback Input Voltage	PWM Mode	790	800	810	mV
I_{FB}	Feedback Input Current				100	nA
V_{IN}, V_{DD}	Input Voltage		2.5		5.5	V
$V_{IN,OFF}$	Minimum Voltage for Shutdown	V_{IN} falling	2		2.2	V
$V_{IN,ON}$	Maximum Voltage for Startup	V_{IN} rising	2.2		2.4	V
I_S	Input Supply Quiescent Current					
	Active - PFM Mode	V_{SYNC} = 0V		120	145	µA
	Active - PWM Mode	V_{SYNC} = 3.3V		6.5	7.5	mA
I_{DD}	Supply Current	PWM, $V_{IN} = V_{DD}$ = 5V		400	500	µA
		EN = 0, $V_{IN} = V_{DD}$ = 5V		0.1	1	µA
$R_{DS(ON)-PMOS}$	PMOS FET Resistance	V_{DD} = 5V, wafer test only		70	100	mΩ
$R_{DS(ON)-NMOS}$	NMOS FET Resistance	V_{DD} = 5V, wafer test only		45	75	mΩ
I_{LMAX}	Current Limit			1.2		A
$T_{OT,OFF}$	Over-temperature Threshold	T rising		145		°C
$T_{OT,ON}$	Over-temperature Hysteresis	T falling		130		°C
I_{EN}, I_{SYNC}	EN, SYNC Current	V_{EN}, V_{RSI} = 0V and 3.3V	-1		1	µA
V_{EN1}, V_{SYNC1}	EN, SYNC Rising Threshold	V_{DD} = 3.3V			2.4	V
V_{EN2}, V_{SYNC2}	EN, SYNC Falling Threshold	V_{DD} = 3.3V	0.8			V
V_{PG}	Minimum V_{FB} for PG, WRT Targeted V_{FB} Value	V_{FB} rising			95	%
		V_{FB} falling	86			%
V_{OLPG}	PG Voltage Drop	I_{SINK} = 3.3mA		35	70	mV
AC CHARACTERISTICS						
F_{PWM}	PWM Switching Frequency		1.25	1.4	1.6	MHz
t_{SYNC}	Minimum SYNC Pulse Width	Guaranteed by design	25			ns
t_{SS}	Soft-start Time			650		µs

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	SGND	Negative supply for the controller stage
2	PGND	Negative supply for the power stage
3	LX	Inductor drive pin; high current digital output with average voltage equal to the regulator output voltage
4	VIN	Positive supply for the power stage
5	VDD	Power supply for the controller stage
6	SYNC	SYNC input pin; when connected to HI, regulator runs at forced PWM mode; when connected to Low, auto PFM/PWM mode; when connected to external sync signal, at external PWM frequency up to 12MHz
7	EN	Enable
8	PG	Power-Good open drain output
9	VO	Output voltage sense
10	FB	Voltage feedback input; connected to an external resistor divider between V_O and SGND for variable output

Block Diagram



Performance Curves and Waveforms

All waveforms are taken at V_{IN}=3.3V, V_O=1.8V, I_O=600mA with component values shown on page 1 at room ambient temperature, unless otherwise noted.

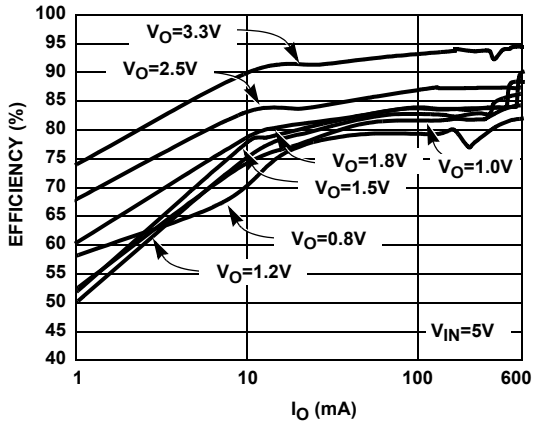


FIGURE 1. EFFICIENCY vs I_O (PFM/PWM MODE)

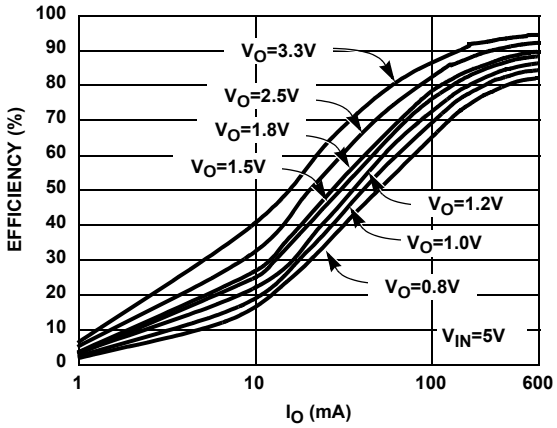


FIGURE 2. EFFICIENCY vs I_O (PWM MODE)

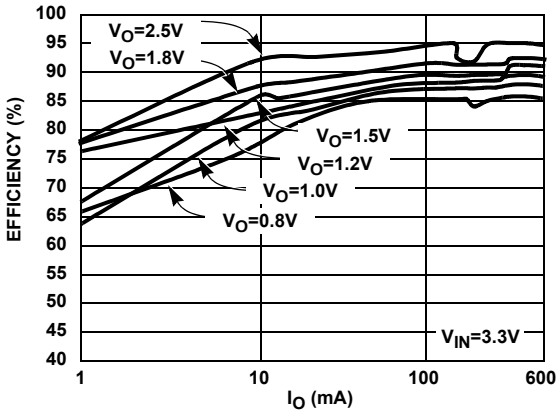


FIGURE 3. EFFICIENCY vs I_O (PFM/FWM MODE)

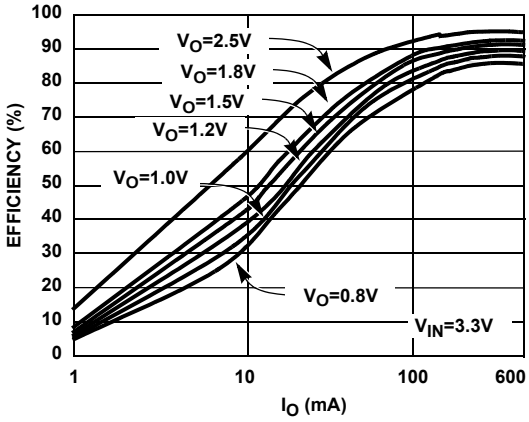


FIGURE 4. EFFICIENCY vs I_O (PWM MODE)

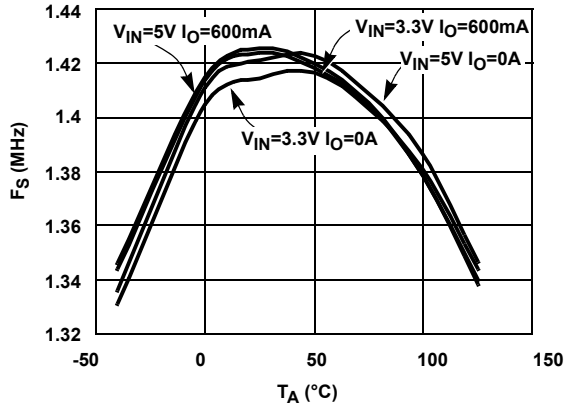


FIGURE 5. F_S vs JUNCTION TEMPERATURE (PWM MODE)

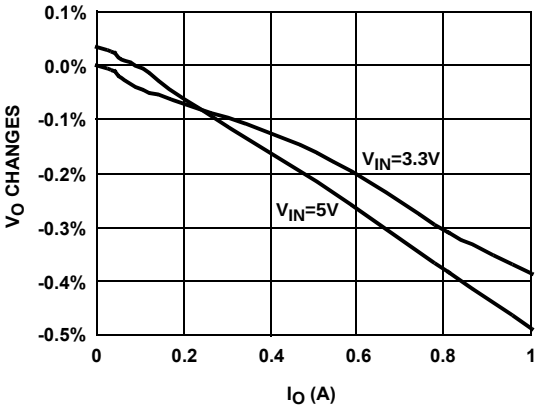


FIGURE 6. LOAD REGULATIONS (PWM MODE)

Performance Curves and Waveforms (Continued)

All waveforms are taken at V_{IN}=3.3V, V_O=1.8V, I_O=600mA with component values shown on page 1 at room ambient temperature, unless otherwise noted.

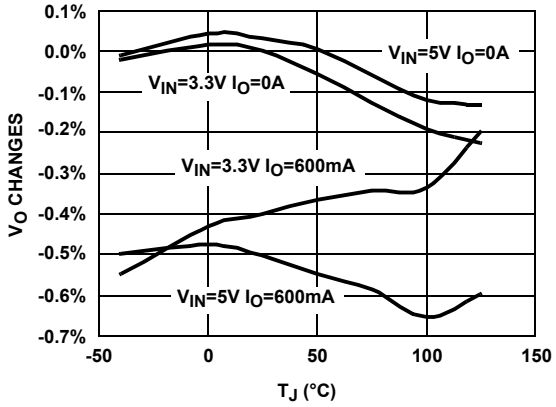


FIGURE 7. PWM MODE LOAD/LINE REGULATIONS vs JUNCTION TEMPERATURE

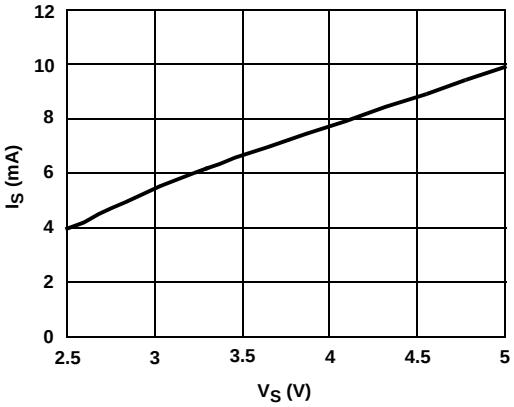


FIGURE 8. NO LOAD QUIESCENT CURRENT (PWM MODE)

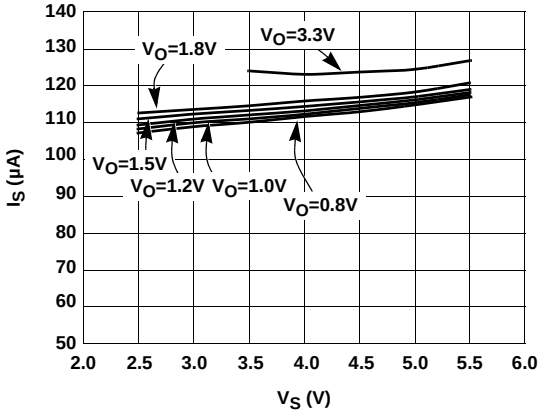
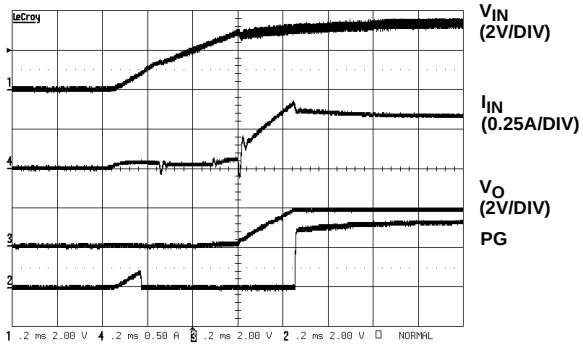


FIGURE 9. NO LOAD QUIESCENT CURRENT (PFM MODE)

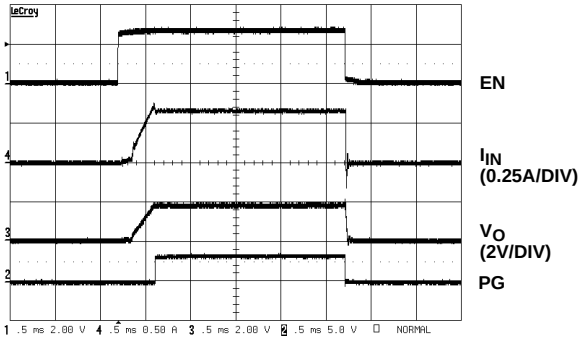
1



200µs/DIV

FIGURE 10. START-UP AT I_O = 600mA

2



500µs/DIV

FIGURE 11. ENABLE AND SHUT-DOWN

Performance Curves and Waveforms (Continued)

All waveforms are taken at V_{IN}=3.3V, V_O=1.8V, I_O=600mA with component values shown on page 1 at room ambient temperature, unless otherwise noted.

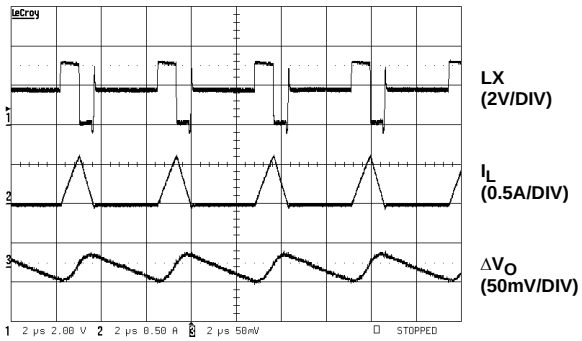


FIGURE 12. PFM STEADY-STATE OPERATION WAVEFORM (I_O = 100mA)

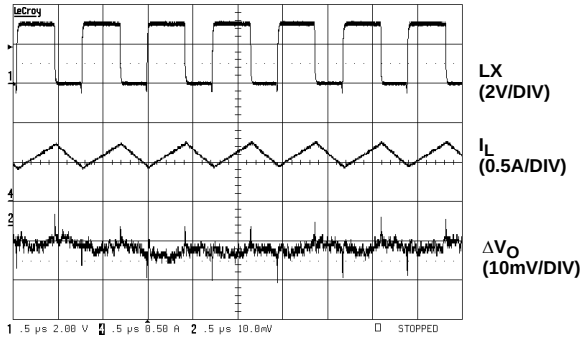


FIGURE 13. PWM STEADY-STATE OPERATION (I_O = 600mA)

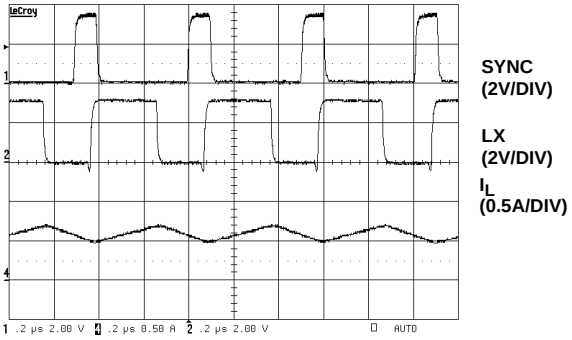


FIGURE 14. EXTERNAL SYNCHRONIZATION TO 2MHz

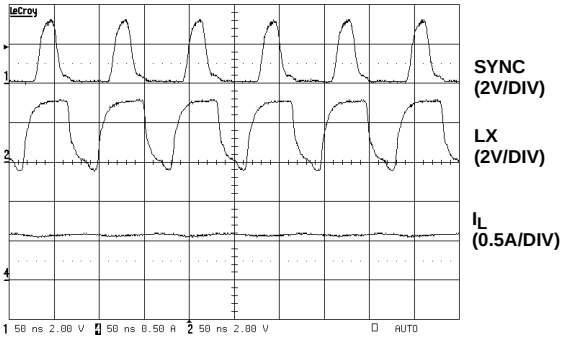


FIGURE 15. EXTERNAL SYNCHRONIZATION TO 12MHz

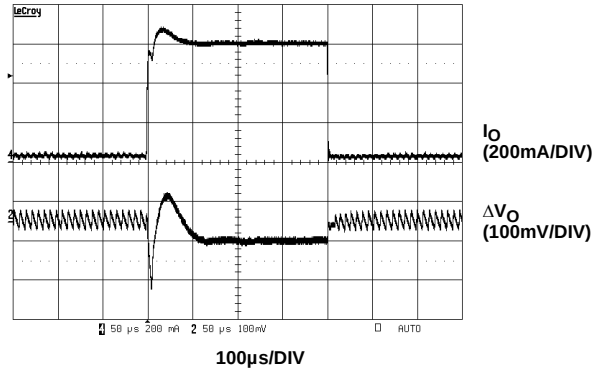


FIGURE 16. LOAD TRANSIENT RESPONSE (22mA to 600mA)

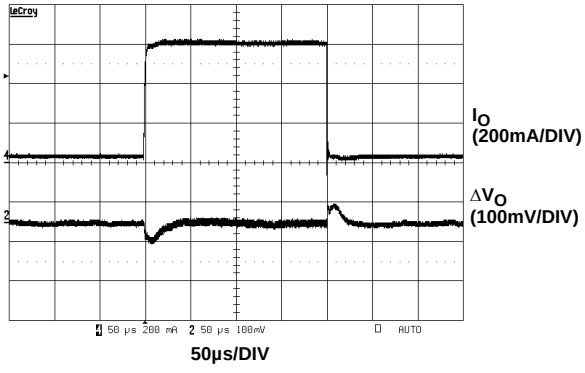


FIGURE 17. PWM LOAD TRANSIENT RESPONSE (30mA TO 600mA)

Performance Curves and Waveforms (Continued)

All waveforms are taken at V_{IN}=3.3V, V_O=1.8V, I_O=600mA with component values shown on page 1 at room ambient temperature, unless otherwise noted.

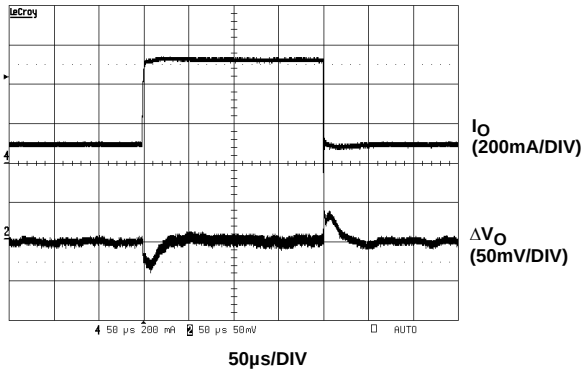


FIGURE 18. PWM LOAD TRANSIENT RESPONSE (100mA TO 500mA)

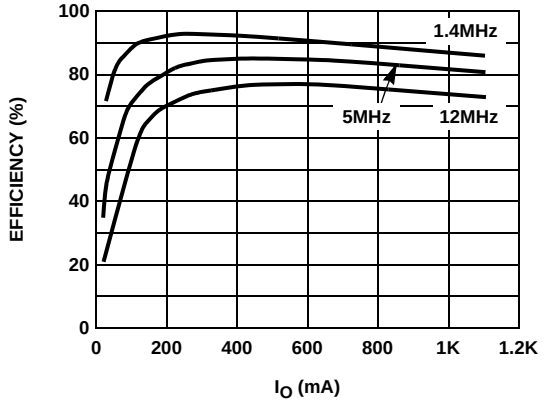


FIGURE 19. EFFICIENCY vs I_O (PWM MODE)

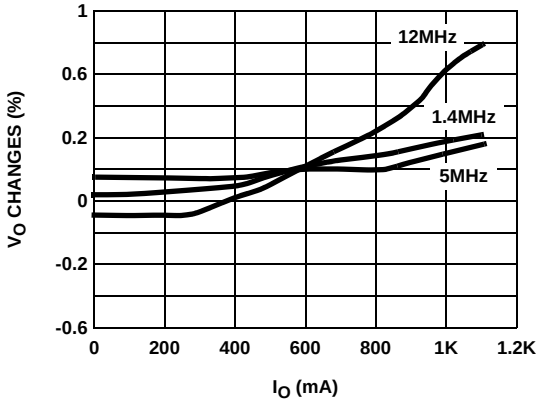


FIGURE 20. LOAD REGULATION (PWM MODE)

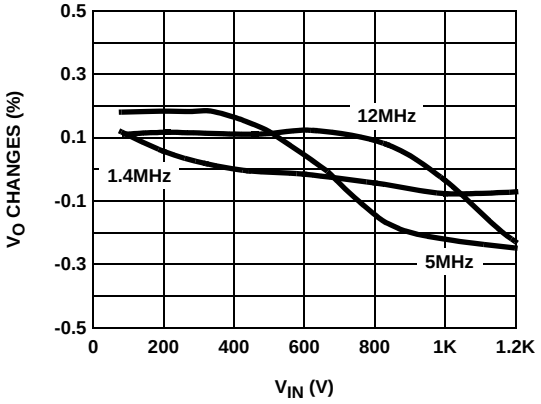


FIGURE 21. LINE REGULATION @ 500mA (PWM MODE)

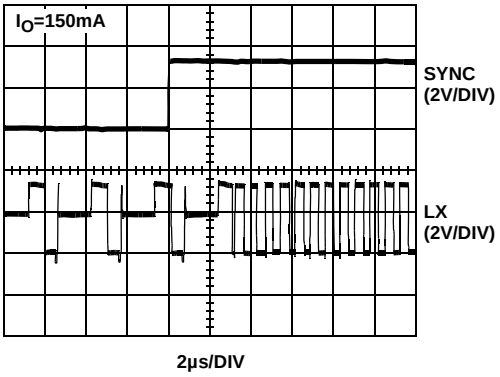


FIGURE 22. PFM-PWM TRANSITION TIME

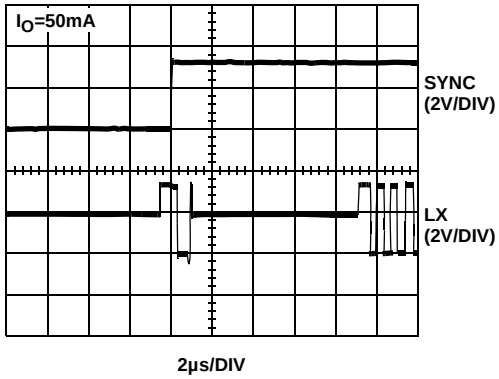


FIGURE 23. PFM-PWM TRANSITION TIME

Performance Curves and Waveforms (Continued)

All waveforms are taken at V_{IN}=3.3V, V_O=1.8V, I_O=600mA with component values shown on page 1 at room ambient temperature, unless otherwise noted.

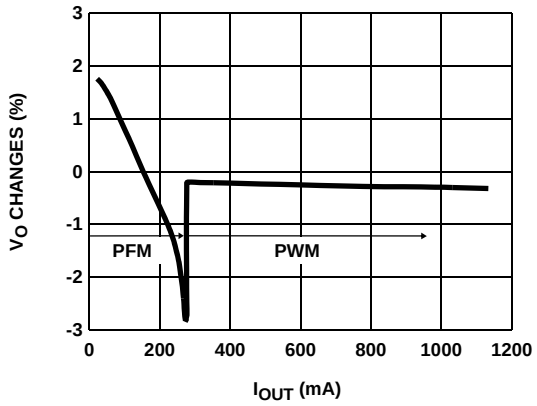


FIGURE 24. PFM-PWM LOAD REGULATION

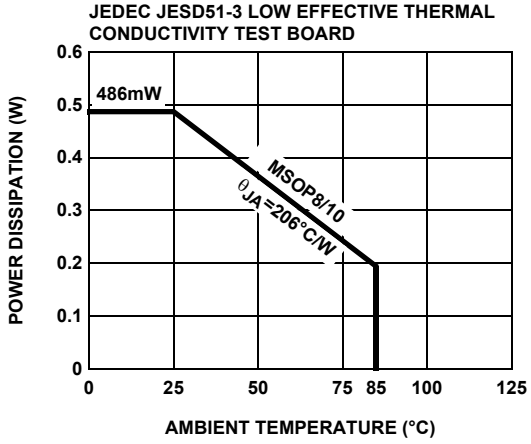


FIGURE 25. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

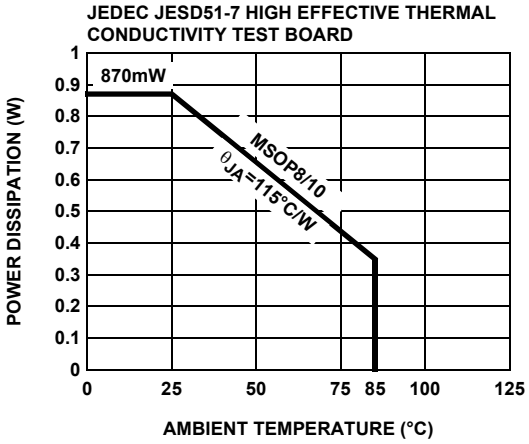


FIGURE 26. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Product Description

The EL7530 is a synchronous, integrated FET 600mA step-down regulator which operates from an input of 2.5V to 5.5V. The output voltage is user-adjustable with a pair of external resistors.

When the load is very light, the regulator automatically operates in the PFM mode, thus achieving high efficiency at light load (>70% for 1mA load). When the load increases, the regulator automatically switches over to a voltage-mode PWM operating at nominal 1.4MHz switching frequency. The efficiency is up to 95%.

It can also operate in a fixed PWM mode or be synchronized to an external clock up to 12MHz for improved EMI performance.

PFM Operation

The heart of the EL7530 regulator is the automatic PFM/PWM controller.

If the SYNC pin is connected to ground, the regulator operates automatically in either the PFM or PWM mode, depending on load. When the SYNC pin is connected to V_{IN}, the regulator operates in the fixed PWM mode. When the pin is connected to an external clock ranging from 1.6MHz to 12MHz, the regulator is in the fixed PWM mode and synchronized to the external clock frequency.

In the automatic PFM/PWM operation, when the load is light, the regulator operates in the PFM mode to achieve high efficiency. The top P channel MOSFET is turned on first. The inductor current increases linearly to a preset value before it is turned off. Then the bottom N channel MOSFET turns on, and the inductor current linearly decreases to zero current. The N channel MOSFET is then turned off, and an anti-ringing MOSFET is turned on to clamp the VLX pin to VO. The inductor current looks like triangular pulses. The frequency of the pulses is mainly a function of output current. The higher the load, the higher the frequency of the pulses until the inductor current becomes continuous. At this point, the controller automatically changes to PWM operation.

PWM Operation

The regulator operates the same way in the forced PWM or synchronized PWM mode. In this mode, the inductor current is always continuous and does not stay at zero.

In this mode, the P channel MOSFET and N channel MOSFET always operate complementary. When the PMOSFET is on and the NMOSFET off, the inductor current increases linearly. The input energy is transferred to the output and also stored in the inductor. When the P channel MOSFET is off and the N channel MOSFET on, the inductor current decreases linearly, and energy is transferred from the inductor to the output. Hence, the average current through the inductor is the output current. Since the inductor and the output capacitor act as a low pass filter, the duty cycle ratio is approximately equal to V_O divided by V_{IN}.

The output LC filter has a second order effect. To maintain the stability of the converter, the overall controller must be compensated. This is done with the fixed internally compensated error amplifier and the PWM compensator. Because the compensations are fixed, the values of input and output capacitors are 10µF to 22µF ceramic and inductor is 1.5µH to 2.2µH.

Forced PWM Mode/SYNC Input

Pulling the SYNC pin HI (>2.5V) forces the converter into PWM mode in the next switching cycle regardless of output current. The duration of the transition varies depending on the output current. Figures 22 and 23 (under two different loading conditions) show the device goes from PFM to PWM mode.

Start-Up and Shut-Down

When the EN pin is tied to V_{IN}, and V_{IN} reaches approximately 2.4V, the regulator begins to switch. The inductor current limit is gradually increased to ensure proper soft-start operation.

When the EN pin is connected to a logic low, the EL7530 is in the shut-down mode. All the control circuitry and both MOSFETs are off, and V_{OUT} falls to zero. In this mode, the total input current is less than 1µA.

When the EN reaches logic HI, the regulator repeats the start-up procedure, including the soft-start function.

Current Limit and Short-Circuit Protection

The current limit is set at about 1.2A for the PMOS. When a short-circuit occurs in the load, the preset current limit restricts the amount of current available to the output, which causes the output voltage to drop below the preset voltage. In the meantime, the excessive current heats up the regulator until it reaches the thermal shut-down point.

Thermal Shut-Down

Once the junction reaches about 145°C, the regulator shuts down. Both the P channel and the N channel MOSFETs turn off. The output voltage will drop to zero. With the output MOSFETs turned off, the regulator will soon cool down. Once the junction temperature drops to about 130°C, the regulator will restart again in the same manner as EN pin connects to logic HI.

Thermal Performance

The EL7530 is available in a fused-lead MSOP10. Compared with regular MSOP10 package, the fused- lead package provides lower thermal resistance. The θ_{JA} is 100°C/W on a 4-layer board and 125°C/W on 2-layer board. Maximizing the copper area around the pins will further improve the thermal performance.

Output Voltage Selection

Users can set the output voltage of the variable version with a resister divider, which can be chosen based on the following formula:

$$V_O = 0.8 \times \left(1 + \frac{R_2}{R_1}\right)$$

Component Selection

Because of the fixed internal compensation, the component choice is relatively narrow. For a regulator with fixed output voltage, only two capacitors and one inductor are required. We recommend 10µf to 22µF multi-layer ceramic capacitors with X5R or X7R rating for both the input and output capacitors, and 1.5µH to 2.2µH for the inductor.

The RMS current present at the input capacitor is decided by the following formula:

$$I_{INRMS} = \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}} \times I_O$$

This is about half of the output current I_O for all the V_O. This input capacitor must be able to handle this current.

The inductor peak-to-peak ripple current is given as:

$$\Delta I_{IL} = \frac{(V_{IN} - V_O) \times V_O}{L \times V_{IN} \times f_S}$$

L is the inductance

f_S the switching frequency (nominally 1.4MHz)

The inductor must be able to handle I_O for the RMS load current, and to assure that the inductor is reliable, it must handle the 2A surge current that can occur during a current limit condition.

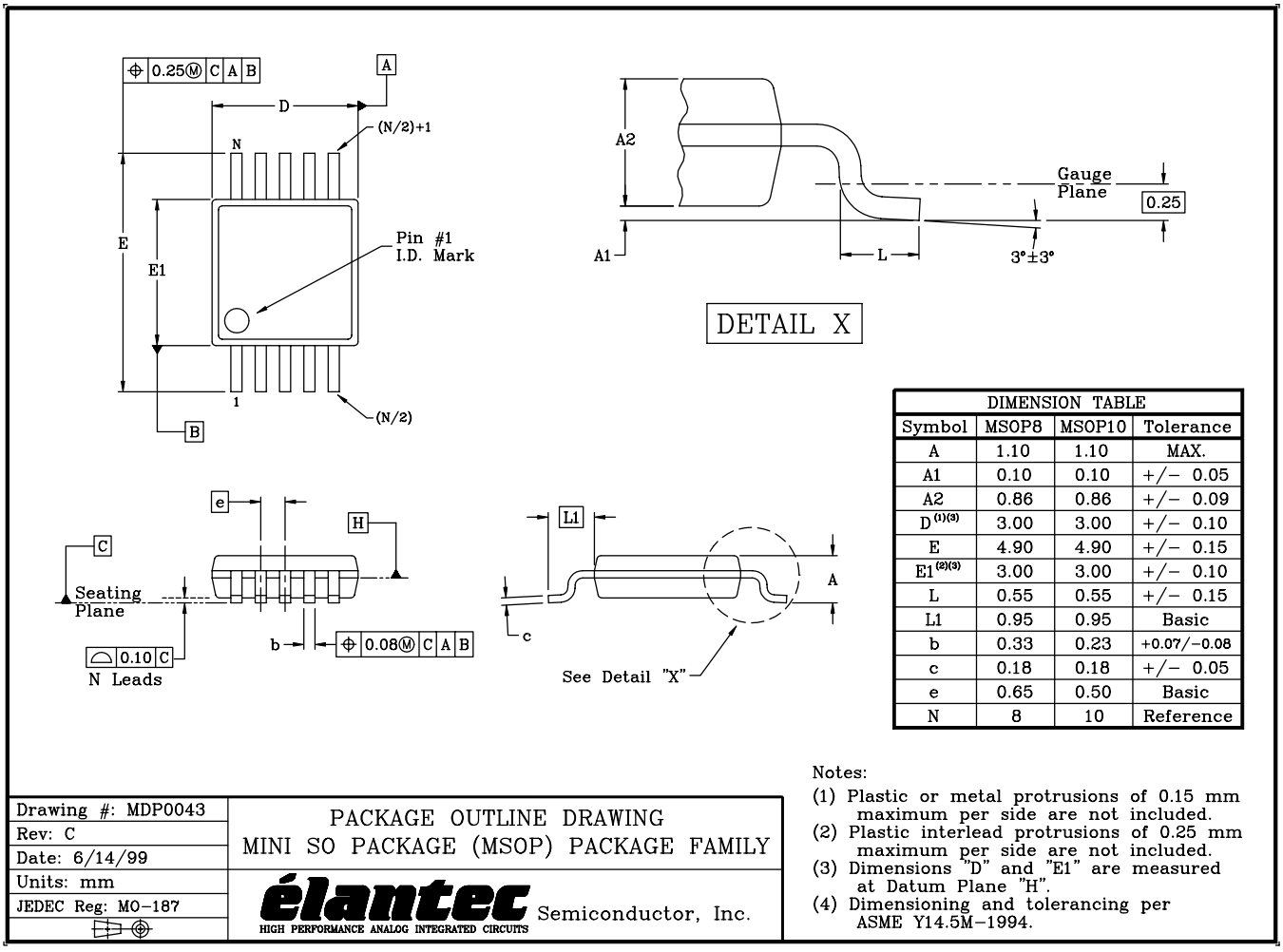
Layout Considerations

The layout is very important for the converter to function properly. The following PC layout guidelines should be followed:

1. Separate the Power Ground (⏚) and Signal Ground (⏚); connect them only at one point right at the pins
2. Place the input capacitor as close to V_{IN} and PGND pins as possible
3. Make the following PC traces as small as possible:
4. from LX pin to L
5. from C_O to PGND
6. If used, connect the trace from the FB pin to R_1 and R_2 as close as possible
7. Maximize the copper area around the PGND pin
8. Place several via holes under the chip to additional ground plane to improve heat dissipation

The demo board is a good example of layout based on this outline. Please refer to the EL7530 Application Brief.

MSOP Package Outline Drawing



DIMENSION TABLE			
Symbol	MSOP8	MSOP10	Tolerance
A	1.10	1.10	MAX.
A1	0.10	0.10	+/− 0.05
A2	0.86	0.86	+/− 0.09
D (1)(3)	3.00	3.00	+/− 0.10
E	4.90	4.90	+/− 0.15
E1 (2)(3)	3.00	3.00	+/− 0.10
L	0.55	0.55	+/− 0.15
L1	0.95	0.95	Basic
b	0.33	0.23	+0.07/−0.08
c	0.18	0.18	+/− 0.05
e	0.65	0.50	Basic
N	8	10	Reference

Drawing #: MDP0043	PACKAGE OUTLINE DRAWING MINI SO PACKAGE (MSOP) PACKAGE FAMILY
Rev: C	
Date: 6/14/99	
Units: mm	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MO−187	

Notes:
(1) Plastic or metal protrusions of 0.15 mm maximum per side are not included.
(2) Plastic interlead protrusions of 0.25 mm maximum per side are not included.
(3) Dimensions "D" and "E1" are measured at Datum Plane "H".
(4) Dimensioning and tolerancing per ASME Y14.5M−1994.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>