Micropower Single Supply Rail-to-Rail Input-Output Precision Op Amp

The EL8176 is a micropower precision operational amplifier optimized for single supply operation at 5V and can operate down to 2.4V.

The EL8176 draws minimal supply current while meeting excellent DC-accuracy noise and output drive specifications. Competing devices seriously degrade these parameters to achieve micropower supply current. Offset current, voltage and current noise, slew rate, and gain-bandwidth product are all two to ten times better than on previous micropower op amps.

The EL8176 can be operated from one lithium cell or two Ni-Cd batteries. The input range includes both positive and negative rail. The output swings to both rails.

Ordering Information

PART NUMBER	PART MARKING	PACKAGE	TAPE & REEL	PKG. DWG. #
EL8176AIW-T7	BBGA	6 Ld SOT-23	7” (3K pcs)	MDP0038
EL8176AIW-T7A	BBGA	6 Ld SOT-23	7” (250 pcs)	MDP0038
EL8176AIWZ-T7 (Note)	BBNA	6 Ld SOT-23 (Pb-free)	7” (3K pcs)	MDP0038
EL8176AIWZ-T7A (Note)	BBNA	6 Ld SOT-23 (Pb-free)	7” (250 pcs)	MDP0038
EL8176BIW-T7	BBGA	6 Ld SOT-23	7” (3K pcs)	MDP0038
EL8176BIW-T7A	BBGA	6 Ld SOT-23	7” (250 pcs)	MDP0038
EL8176BIWZ-T7 (Note)	BBNA	6 Ld SOT-23 (Pb-free)	7” (3K pcs)	MDP0038
EL8176BIWZ-T7A (Note)	BBNA	6 Ld SOT-23 (Pb-free)	7” (250 pcs)	MDP0038
EL8176ISZ (Note)	8176ISZ	8 Ld SO (Pb-free)	-	MDP0027
EL8176ISZ-T7 (Note)	8176ISZ	8 Ld SO (Pb-free)	7”	MDP0027
EL8176ISZ-T13 (Note)	8176ISZ	8 Ld SO (Pb-free)	13”	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

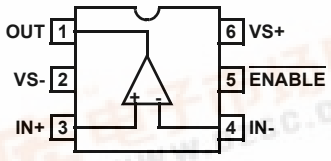
- 55µA supply current
- 100µV max offset voltage
- 500pA input bias current
- 400kHz gain-bandwidth product
- 1MHz -3dB bandwidth
- 0.13V/µs slew rate
- Single supply operation down to 2.4V
- Rail-to-rail input and output
- Output sources and sinks 26mA load current
- Pb-free plus anneal available (RoHS compliant)

Applications

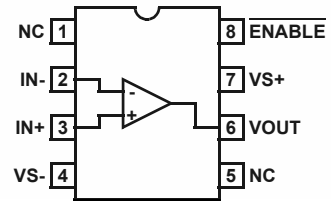
- Battery- or solar-powered systems
- 4mA to 20mA current loops
- Handheld consumer products
- Medical devices
- Thermocouple amplifiers
- Photodiode pre amps
- pH probe amplifiers

Pinouts

EL8176
(6 LD SOT-23)
TOP VIEW



EL8176
(8 LD SO)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage 5.5V
Differential Input Current 5mA
Input Voltage . . . . . -0.5V to V_S + 0.5V
Output Short-Circuit Duration . . . . . Indefinite
Ambient Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	Grade A		50	100	µV
		Grade B		110	400	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			TBD		µV/Mo
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Drift vs Temperature	EL8176IW		0.7		µV/°C
		EL8176IS		0.3		µV/°C
I_{OS}	Input Offset Current			0.4	1.2	nA
I_B	Input Bias Current			0.5	2	nA
e_N	Input Noise Voltage Density	f_O = 1kHz		25		nV/√Hz
i_N	Input Noise Current Density	f_O = 1kHz		0.1		pA/√Hz
CMIR	Input Voltage Range	Guaranteed by CMRR test	0		5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	90	110		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.4V to 5V	90	110		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V, R_L = 100kΩ	200	500		V/mV
		V_O = 0.5V to 4.5V, R_L = 1kΩ		25		V/mV
V_{OUT}	Maximum Output Voltage Swing	Output low, R_L = 100kΩ		3	6	mV
		Output low, R_L = 1kΩ		130	200	mV
		Output high, R_L = 100kΩ	4.994	4.997		V
		Output high, R_L = 1kΩ	4.8	4.88		V
SR	Slew Rate		0.09	0.13	0.17	V/µs
GBW	Gain Bandwidth Product	f_O = 100kHz		400		kHz
BW	-3dB Bandwidth	Unity gain, C_{LOAD} = 27pF, R_F = 100Ω		1		MHz
$I_{S,ON}$	Supply Current, Enabled		40	55	75	µA
$I_{S,OFF}$	Supply Current, Disabled			3	10	µA
I_O+	Short Circuit Output Current	R_L = 10Ω	18	31		mA
I_O-	Short Circuit Output Current	R_L = 10Ω	17	26		mA
V_S	Minimum Supply Voltage			2.2	2.4	V
V_{INH}	Enable Pin High Level				2	V
V_{INL}	Enable Pin Low Level		0.8			V
I_{ENH}	Enable Pin Input Current	V_{EN} = 5V	0.25	0.7	2	µA
I_{ENL}	Enable Pin Input Current	V_{EN} = 0V	-0.5	0	+0.5	µA

Typical Performance Curves

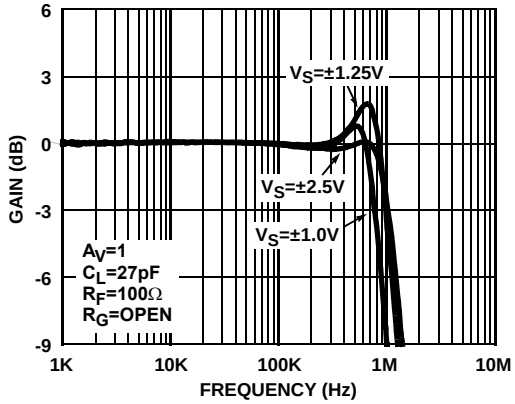


FIGURE 1. UNITY GAIN FREQUENCY RESPONSE vs SUPPLY VOLTAGE

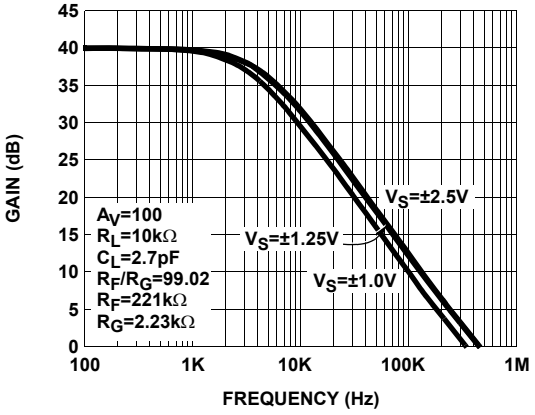


FIGURE 2. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

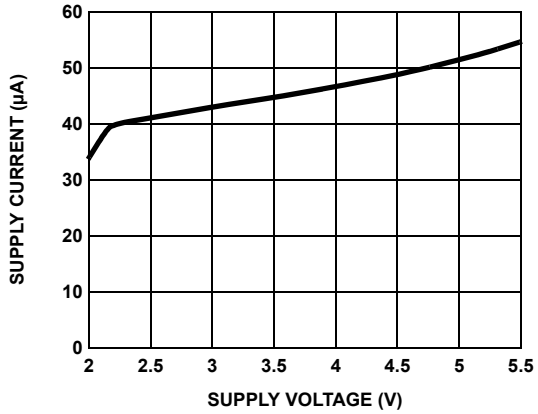


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

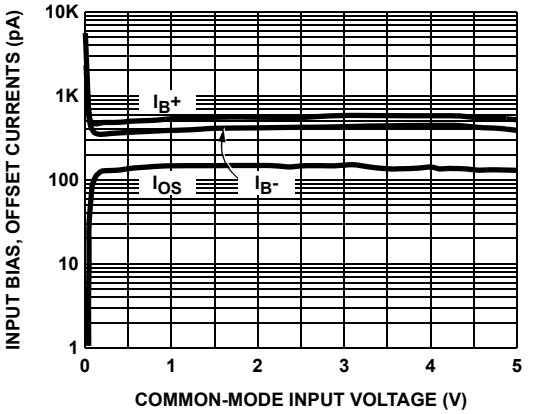


FIGURE 4. INPUT BIAS + OFFSET CURRENTS vs COMMON-MODE INPUT VOLTAGE

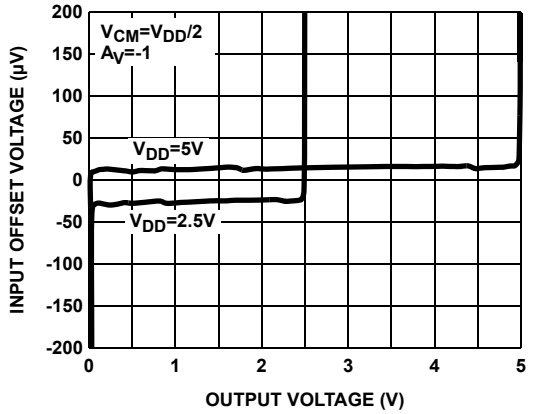


FIGURE 5. INPUT OFFSET VOLTAGE vs OUTPUT VOLTAGE

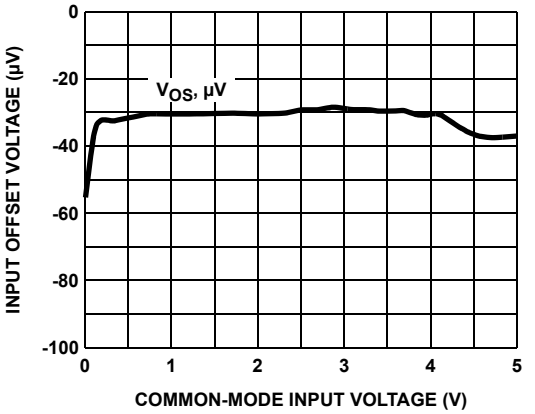


FIGURE 6. INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

Typical Performance Curves (Continued)

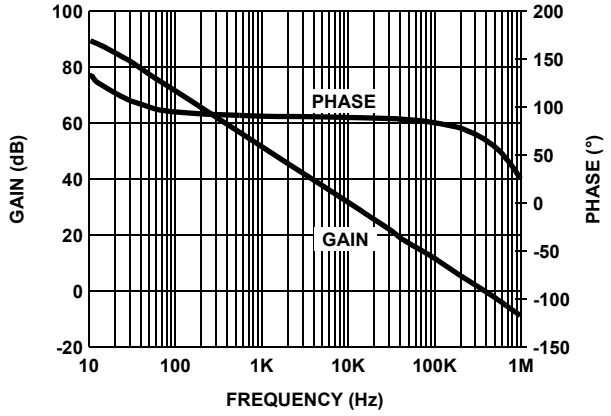


FIGURE 7. A_{VOL} vs FREQUENCY @ 1kΩ LOAD

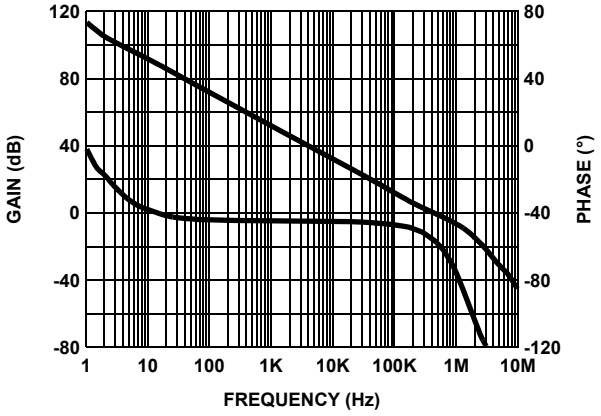


FIGURE 8. A_{VOL} vs FREQUENCY @ 100kΩ LOAD

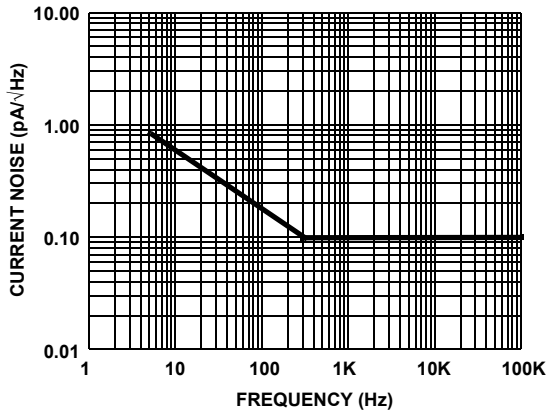


FIGURE 9. CURRENT NOISE vs FREQUENCY

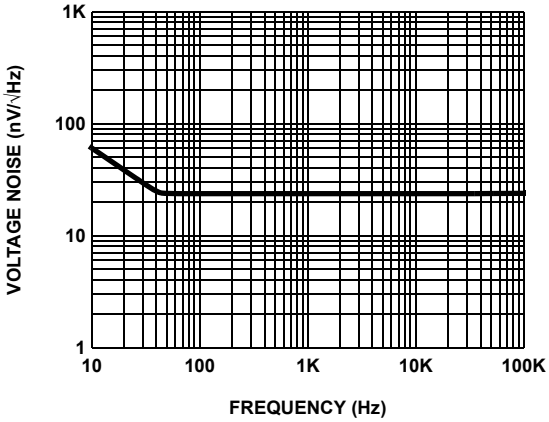


FIGURE 10. VOLTAGE NOISE vs FREQUENCY

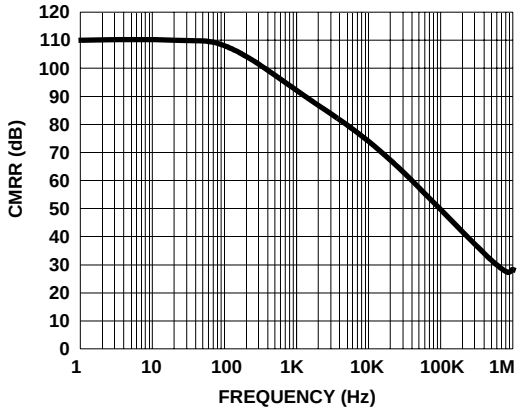


FIGURE 11. CMRR vs FREQUENCY

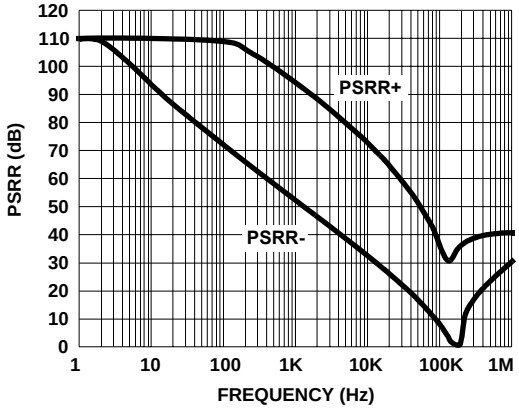


FIGURE 12. PSRR vs FREQUENCY

Typical Performance Curves (Continued)

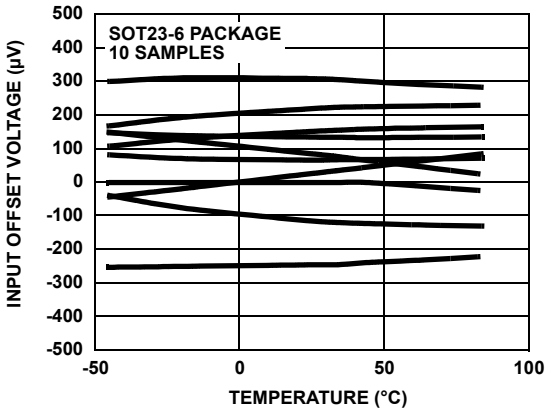


FIGURE 13. V_{OS} vs TEMPERATURE

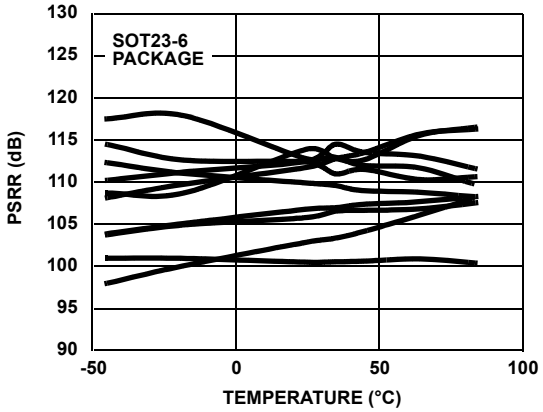


FIGURE 14. PSRR vs TEMPERATURE

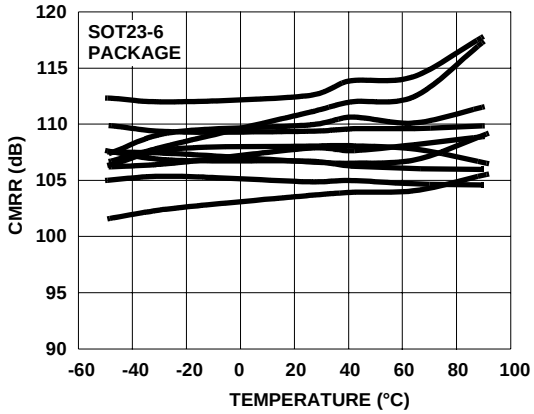


FIGURE 15. CMRR vs TEMPERATURE

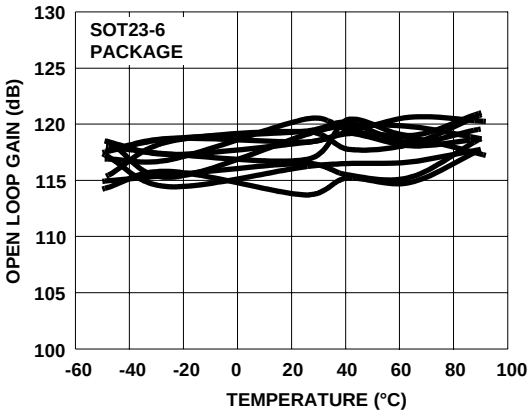


FIGURE 16. A_{VOL} vs TEMPERATURE

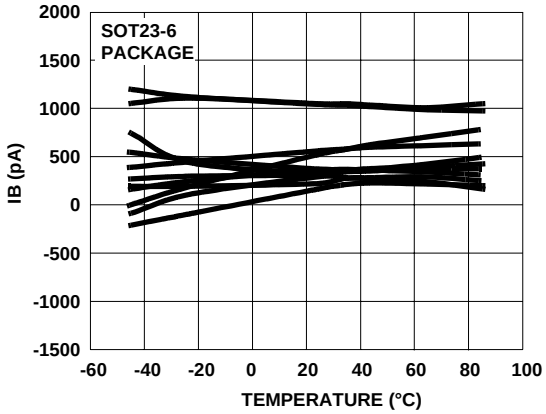


FIGURE 17. IB vs TEMPERATURE

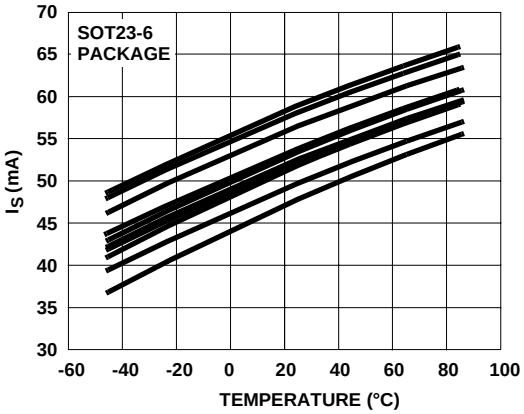


FIGURE 18. I_S vs TEMPERATURE

Typical Performance Curves (Continued)

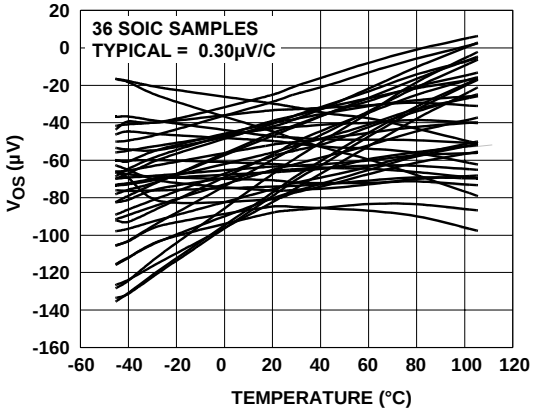


FIGURE 19. EL8176SOIC V_{OS} vs TEMPERATURE (V_S = 5V)

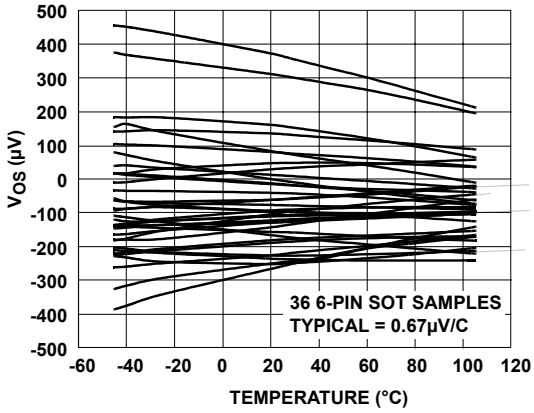


FIGURE 20. EL8176SOT V_{OS} vs TEMPERATURE (V_S = 5V)

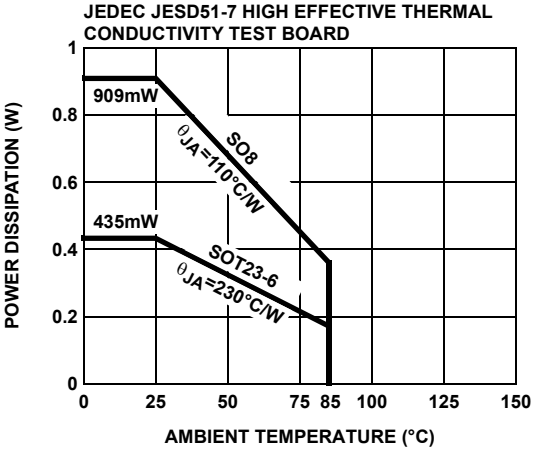


FIGURE 21. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

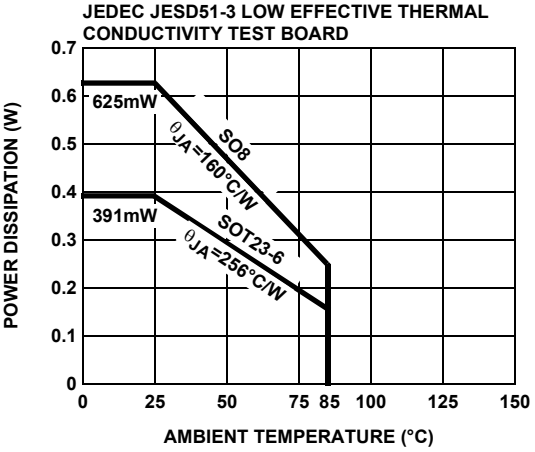


FIGURE 22. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Introduction

The EL8176 is a rail-to-rail input and output micro-power precision single supply operational amplifier with an enable feature. The device achieves rail-to-rail input and output operation and eliminates the concerns introduced by a conventional rail-to-rail I/O operational amplifier.

Rail-to-Rail Input

The input common-mode voltage range of the EL8176 goes from negative supply to positive supply without introducing offset errors or degrading performance associated with a conventional rail-to-rail input operational amplifier. Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The EL8176 achieves input rail-to-rail without sacrificing important precision specifications and without degrading distortion performance. The EL8176's input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range for the EL8176 gives us an undistorted behavior from typically 10mV above the negative rail all the way up to the positive rail. 10mV above the negative rail to the positive rail is the range of operation of yet another feature of the EL8176, input bias current compensation.

Input Bias Current Compensation

The input bias currents of the EL8176 are decimated down to a typical of 500pA while maintaining an excellent bandwidth for a micro-power operational amplifier. Inside the EL8176 is an input bias canceling circuit. The input stage

transistors are still biased with an adequate current for speed but the canceling circuit sinks most of the base current, leaving a small fraction as input bias current. The input bias current compensation/cancellation operates from typically 10mV to the positive supply rail and also from -40°C to 85°C.

Rail-to-Rail Output

A pair of complementary MOSFET devices achieves rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. The EL8176 with a 100kΩ load will swing to within 3mV of the supply rails.

Enable/Disable Feature

The EL8176 offers an EN pin. The active low enable pin disables the device when pulled up to at least 2.2V. Upon disable the part consumes typically 3µA, while the output is in a high impedance state. The EN also has an internal pull down. If left open, the EN pin will pull to negative rail and the device will be enabled by default. The high impedance at output during disable allows multiple EL8176s to be connected together as a MUX. The outputs are tied together in parallel and a channel can be selected by the EN pin.

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance and low offset voltage of the EL8176, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 23 shows how the guard ring should be configured and Figure 24 shows the top view of how a surface mount layout can be arranged. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.

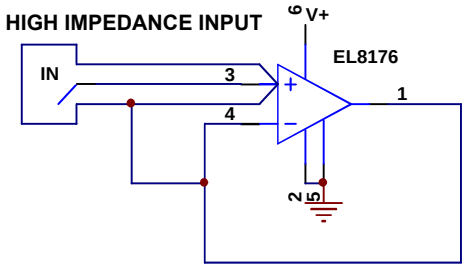


FIGURE 23.

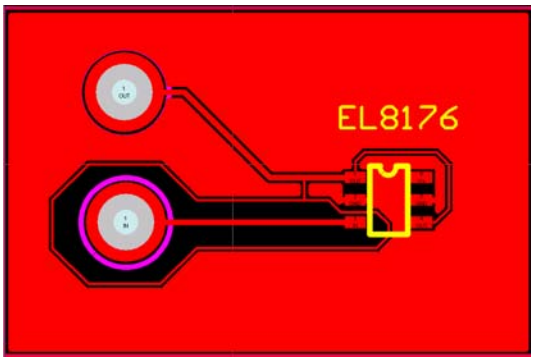


FIGURE 24.

Typical Applications

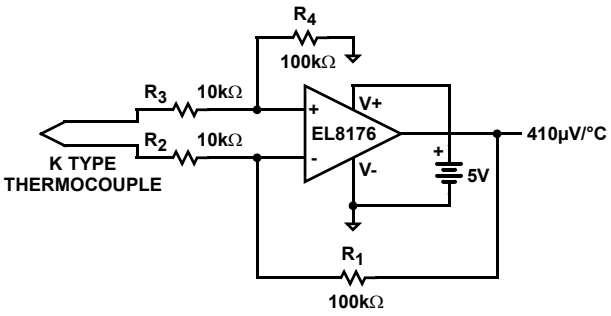
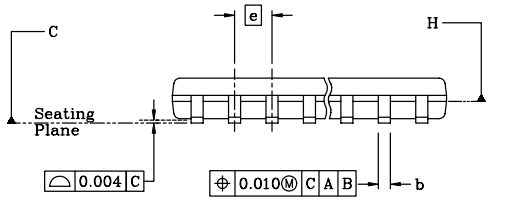
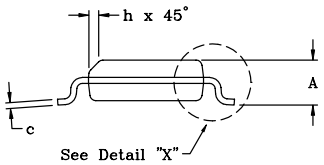


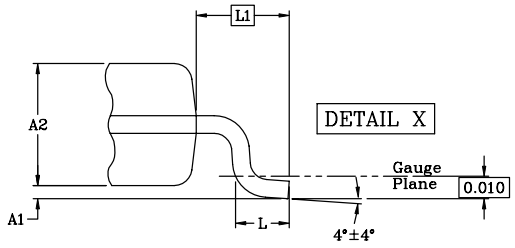
FIGURE 25. THERMOCOUPLE AMPLIFIER

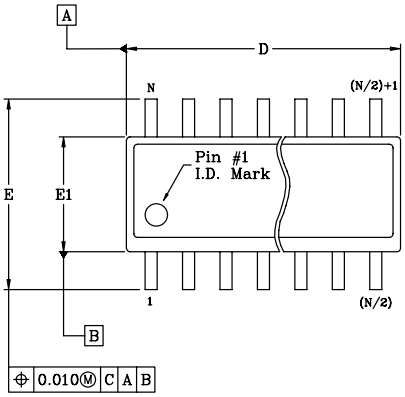
Thermocouples are the most popular temperature-sensing device because of their low cost, interchangeability, and ability to measure a wide range of temperatures. The EL8176 is used to convert the differential thermocouple voltage into single-ended signal with 10X gain. The EL8176's rail-to-rail input characteristic allows the thermocouple to be biased at ground and the converter to run from a single 5V supply.

SO Package Outline Drawing









DIMENSION TABLE								
Symbol	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	Tolerance
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX.
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	+/- 0.003
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	+/- 0.002
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	+/- 0.003
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	+/- 0.001
D (1)(3)	0.193	0.341	0.390	0.406	0.504	0.606	0.704	+/- 0.004
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	+/- 0.008
E1 (2)(3)	0.154	0.154	0.154	0.295	0.295	0.295	0.295	+/- 0.004
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	+/- 0.009
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference
N	8	14	16	16	20	24	28	Reference

Drawing #: MDP0027	PACKAGE OUTLINE DRAWING SMALL OUTLINE (SO) PACKAGE FAMILY
Rev: L	
Date: 2/15/01	
Units: Inches	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MS-012/013	

Notes:

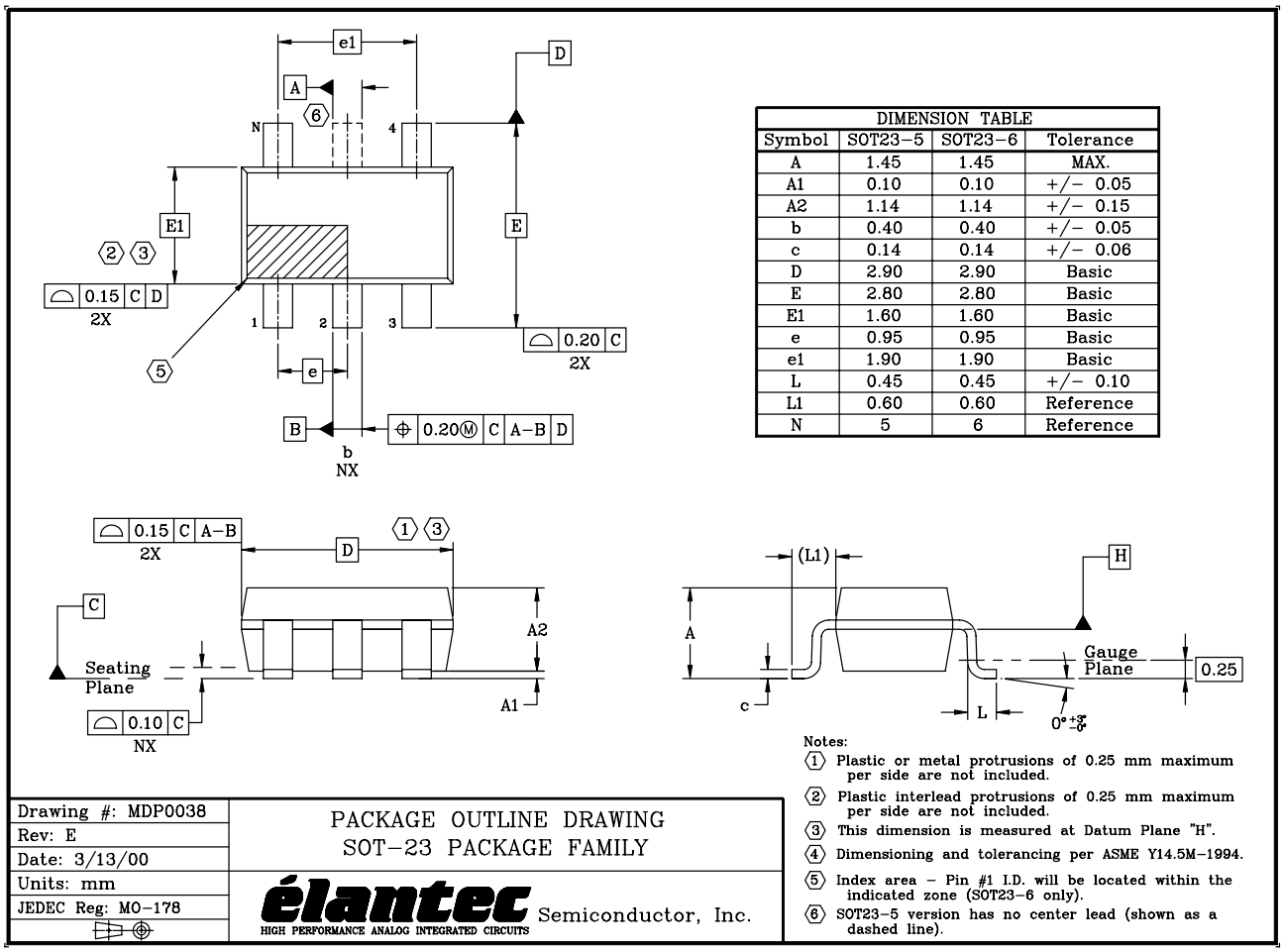
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.

(2) Plastic interlead protrusions of 0.010" maximum per side are not included.

(3) Dimensions "D" and "E1" are measured at Datum Plane "H".

(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

SOT-23 Package Outline Drawing



DIMENSION TABLE			
Symbol	SOT23-5	SOT23-6	Tolerance
A	1.45	1.45	MAX.
A1	0.10	0.10	+/- 0.05
A2	1.14	1.14	+/- 0.15
b	0.40	0.40	+/- 0.05
c	0.14	0.14	+/- 0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	+/- 0.10
L1	0.60	0.60	Reference
N	5	6	Reference

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at http://www.intersil.com/design/packages/index.asp