Triple Differential Receiver/Equalizer

The EL9111 and EL9112 are triple channel differential receivers and equalizers. They contains three high speed differential receivers with five programmable poles. The outputs of these pole blocks are then summed into an output buffer. The equalization length is set with the voltage on a single pin. The EL9111 and EL9112 also contain a 3-statable output, enabling multiple devices to be connected in parallel and used in a multiplexing application.

The gain can be adjusted up or down on each channel by 6dB using its V_{GAIN} control signal. In addition, a further 6dB of gain can be switched in to provide a matched drive into a cable.

The EL9111 and EL9112 have a bandwidth of 150MHz and consume just 108mA on ±5V supply. A single input voltage is used to set the compensation levels for the required length of cable.

The EL9111 is a special version of the EL9112 that decodes syncs encoded onto the common modes of three pairs of CAT-5 cable by the EL4543. (Refer to the EL4543 datasheet for details.)

The EL9111 and EL9112 are available in a 28-pin QFN package and are specified for operation over the full -40°C to +85°C temperature range.

Features

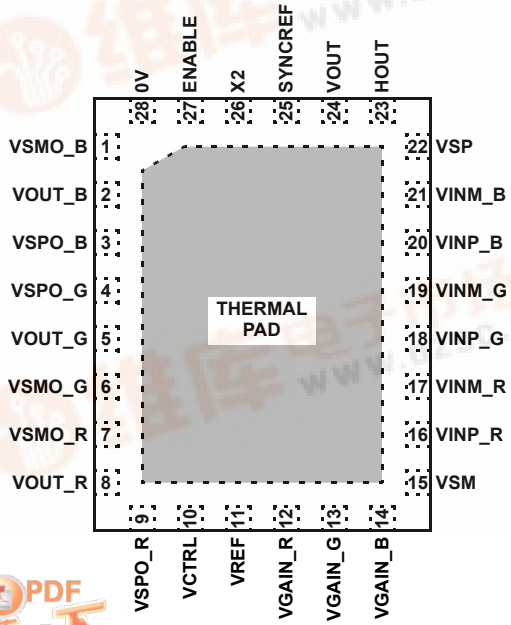
- 150MHz -3dB bandwidth
- CAT-5 compensation
  - 50MHz @ 1000 ft
  - 125MHz @ 500 ft
- 108mA supply current
- Differential input range 3.2V
- Common mode input range -4V to +3.5V
- ±5V supply
- Output to within 1.5V of supplies
- Available in 28-pin QFN package
- Pb-free available (RoHS compliant)

Applications

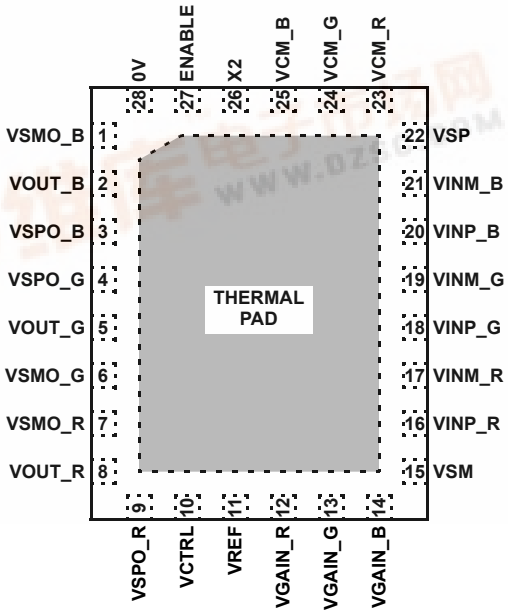
- Twisted-pair receiving/equalizer
- KVM (Keyboard/Video/Mouse)
- VGA over twisted-pair
- Security video

Pinouts

EL9111
(28-PIN QFN)
TOP VIEW



EL9112
(28-PIN QFN)
TOP VIEW



Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL9111IL	28-Pin QFN	-	MDP0046
EL9111IL-T7	28-Pin QFN	7”	MDP0046
EL9111IL-T13	28-Pin QFN	13”	MDP0046
EL9111ILZ (Note)	28-Pin QFN (Pb-Free)	-	MDP0046
EL9111ILZ-T7 (Note)	28-Pin QFN (Pb-Free)	7”	MDP0046
EL9111ILZ-T13 (Note)	28-Pin QFN (Pb-Free)	13”	MDP0046

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL9112IL	28-Pin QFN	-	MDP0046
EL9112IL-T7	28-Pin QFN	7”	MDP0046
EL9112IL-T13	28-Pin QFN	13”	MDP0046
EL9112ILZ (Note)	28-Pin QFN (Pb-Free)	-	MDP0046
EL9112ILZ-T7 (Note)	28-Pin QFN (Pb-Free)	7”	MDP0046
EL9112ILZ-T13 (Note)	28-Pin QFN (Pb-Free)	13”	MDP0046

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S+ and V_S- 12V
Maximum Continuous Output Current per Channel 30mA
Power Dissipation . . . . . See Curves
Pin Voltages . . . . . V_S- -0.5V to V_S+ +0.5V

Storage Temperature . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Die Junction Temperature . . . . . 150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{SA}+ = V_A+ = +5V, V_{SA}- = V_A- = -5V, T_A = 25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	Bandwidth	(See Figure 1)		150		MHz
SR	Slew Rate	V_{IN} = -1V to +1V, V_G = 0.39, V_C = 0, R_L = 75 + 75Ω		1.5		kV/µs
THD	Total Harmonic Distortion	10MHz $2V_{P-P}$ out, V_G = 1V, X2 gain, V_C = 0		-50		dBc
DC PERFORMANCE						
$V(V_{OUT})_{OS}$	Offset Voltage	X2 = high, no equalization	-110	-10	+78	mV
ΔV_{OS}	Channel-to-Channel Offset Matching	X2 = high, no equalization	-100	0	+100	mV
INPUT CHARACTERISTICS						
CMIR	Common-mode Input Range			-4/+3.5		V
O_{NOISE}	Output Noise	V_G = 0V, V_C = 0V, X2 = HIGH, R_{LOAD} = 150Ω, Input 50Ω to GND, 10MHz		-110		dBm
CMRR	Common-mode Rejection Ratio	Measured at 10kHz		-80		dB
CMRR	Common-mode Rejection Ratio	Measured at 10MHz		-55		dB
CMBW	CM Amplifier Bandwidth	10K || 10pF load		50		MHz
CM_{SLEW}	CM Slew Rate	Measured @ +1V to -1V		100		V/µs
C_{INDIFF}	Differential Input Capacitance	Capacitance V_{INP} to V_{INM}		600		fF
R_{INDIFF}	Differential Input Resistance	Resistance V_{INP} to V_{INM}	1	2.4		MΩ
C_{INCM}	CM Input Capacitance	Capacitance V_{INP} = V_{INM} to GND		1.2		pF
R_{INCM}	CM Input Resistance	Resistance V_{INP} = V_{INM} to GND	1	2.8		MΩ
$+I_{IN}$	Positive Input Current	DC bias @ V_{INP} = V_{INM} = 0V		1		µA
$-I_{IN}$	Negative Input Current	DC bias @ V_{INP} = V_{INM} = 0V		1		µA
V_{INDIFF}	Differential Input Range	V_{INP} - V_{INM} when slope gain falls to 0.9	2.5	3.2		V
OUTPUT CHARACTERISTICS						
$V(V_{OUT})$	Output Voltage Swing	R_L = 150Ω		±3.5		V
$I(V_{OUT})$	Output Drive Current	R_L = 10Ω, V_{INP} = 1V, V_{INM} = 0V, X2 = high, V_G = 0.39	50	60		mA
$R(V_{CM})$	CM Output Resistance of VCM_R/G/B (EL9112 only)	at 100kHz		30		Ω
Gain	Gain	V_C = 0, V_G = 0.39, X2 = 5, R_L = 150Ω	0.85	1.0	1.1	
ΔGain	Channel-to-Channel Gain Matching	V_C = 0, V_G = 0.39, X2 = 5, R_L = 150Ω		3	6	%
$V(SYNC)_{HI}$	High Level output on V/H_{OUT} (EL9111 only)		$V(V_{SP})$ - 0.1V		$V(V_{SP})$	

Electrical Specifications $V_{SA}+ = V_A+ = +5V$, $V_{SA}- = V_A- = -5V$, $T_A = 25°C$, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$V(SYNC)_{LO}$	Low Level output on V/H_{OUT} (EL9111 only)		0		V(SYNC REF) + 0.1V	
SUPPLY						
I_{SON}	Supply Current per Channel	$V_{ENBL} = 5$, $V_{INM} = 0$	32	36	39	mA
I_{SOFF}	Supply Current per Channel	$V_{ENBL} = 0$, $V_{INM} = 0$	0.2		0.4	mA
PSRR	Power Supply Rejection Ratio	DC to 100kHz, ±5V supply		65		dB
LOGIC CONTROL PINS (ENABLE, X2)						
V_{HI}	Logic High Level	V_{IN} - V_{LOGIC} ref for guaranteed high level	1.35			V
V_{LOW}	Logic Low Level	V_{IN} - V_{LOGIC} ref for guaranteed low level			0.8	V
I_{LOGICH}	Logic High Input Current	$V_{IN} = 5V$, $V_{LOGIC} = 0V$			50	µA
I_{LOGICL}	Logic Low Input Current	$V_{IN} = 0V$, $V_{LOGIC} = 0V$			15	µA

Pin Descriptions

PIN NUMBER	EL9111IL PIN NAME	EL9111IL PIN FUNCTION	EL9112IL PIN NAME	EL9112IL PIN FUNCTION
1	VSMO_B	-5V to blue output buffer	VSMO_B	-5V to blue output buffer
2	VOUT_B	Blue output voltage referenced to 0V pin	VOUT_B	Blue output voltage referenced to 0V pin
3	VSPO_B	+5V to blue output buffer	VSPO_B	+5V to blue output buffer
4	VSPO_G	+5V to green output buffer	VSPO_G	+5V to green output buffer
5	VOUT_G	Green output voltage referenced to 0V pin	VOUT_G	Green output voltage referenced to 0V pin
6	VSMO_G	-5V to green output buffer	VSMO_G	-5V to green output buffer
7	VSMO_R	-5V to red output buffer	VSMO_R	-5V to red output buffer
8	VOUT_R	Red output voltage referenced to 0V pin	VOUT_R	Red output voltage referenced to 0V pin
9	VSPO_R	+5V to red output buffer	VSPO_R	+5V to red output buffer
10	VCTRL	Equalization control voltage (0V to 1V)	VCTRL	Equalization control voltage (0V to 1V)
11	VREF	Reference voltage for logic signals, V_{CTRL} and V_{GAIN} pins	VREF	Reference voltage for logic signals, V_{CTRL} and V_{GAIN} pins
12	VGAIN_R	Red channel gain voltage (0V to 1V)	VGAIN_R	Red channel gain voltage (0V to 1V)
13	VGAIN_G	Green channel gain voltage (0V to 1V)	VGAIN_G	Green channel gain voltage (0V to 1V)
14	VGAIN_B	Blue channel gain voltage (0V to 1V)	VGAIN_B	Blue channel gain voltage (0V to 1V)
15	VSM	-5V to core of chip	VSM	-5V to core of chip
16	VINP_R	Red positive differential input	VINP_R	Red positive differential input
17	VINM_R	Red negative differential input	VINM_R	Red negative differential input
18	VINP_G	Green positive differential input	VINP_G	Green positive differential input
19	VINM_G	Green negative differential input	VINM_G	Green negative differential input
20	VINP_B	Blue positive differential input	VINP_B	Blue positive differential input
21	VINM_B	Blue negative differential input	VINM_B	Blue negative differential input
22	VSP	+5V to core of chip	VSP	+5V to core of chip
23	HOUT	Decoded Horizontal sync referenced to SYNCREF	VCM_R	Red common-mode voltage at inputs
24	VOUT	Decoded Vertical sync referenced to SYNCREF	VCM_G	Green common-mode voltage at inputs
25	SYNCREF	Reference level for H_{OUT} and V_{OUT} logic outputs	VCM_B	Blue common-mode voltage at inputs

Pin Descriptions (Continued)

PIN NUMBER	EL9111IL PIN NAME	EL9111IL PIN FUNCTION	EL9112IL PIN NAME	EL9112IL PIN FUNCTION
26	X2	Logic signal for x1/x2 output gain setting	X2	Logic signal for x1/x2 output gain setting
27	ENABLE	Chip enable logic signal	ENABLE	Chip enable logic signal
28	0V	0V reference for output voltage	0V	0V reference for output voltage

Typical Performance Curves

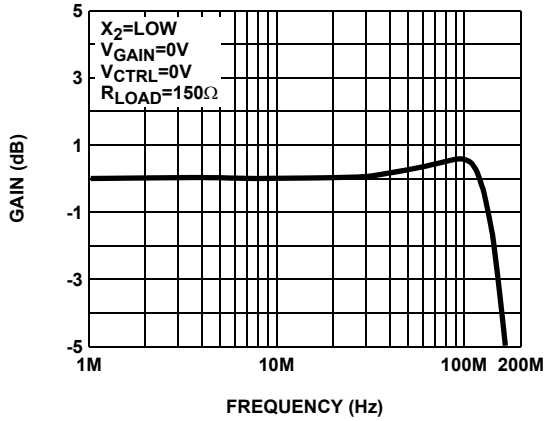


FIGURE 1. FREQUENCY RESPONSE OF ALL CHANNELS

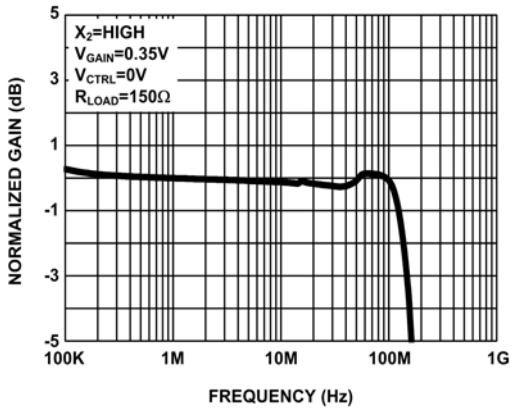


FIGURE 2. GAIN vs FREQUENCY ALL CHANNELS

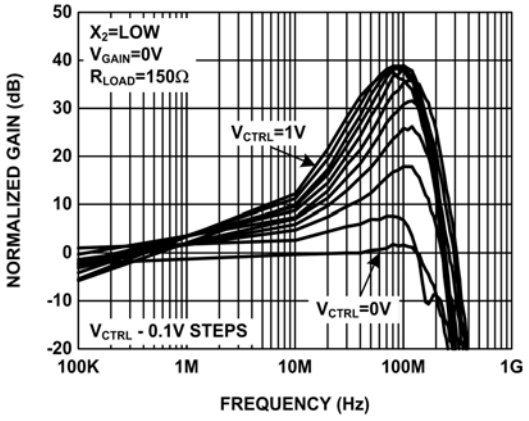


FIGURE 3. GAIN vs FREQUENCY FOR VARIOUS V_{CTRL}

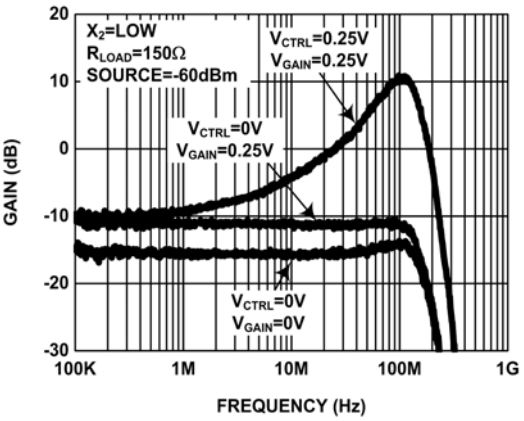


FIGURE 4. GAIN vs FREQUENCY FOR VARIOUS V_{CTRL} & V_{GAIN}

Typical Performance Curves (Continued)

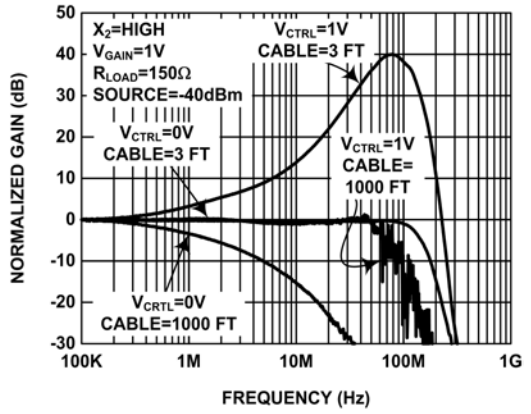


FIGURE 5. GAIN vs FREQUENCY FOR VARIOUS V_{CTRL} & CABLE LENGTHS

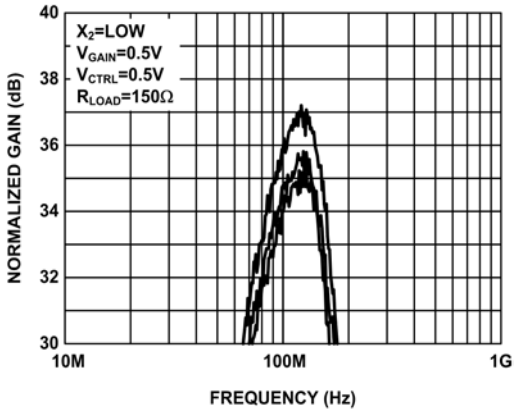


FIGURE 6. CHANNEL MISMATCH

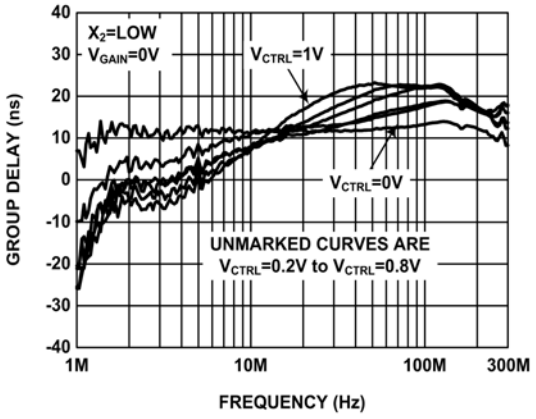


FIGURE 7. GROUP DELAY vs FREQUENCY FOR VARIOUS V_{CTRL}

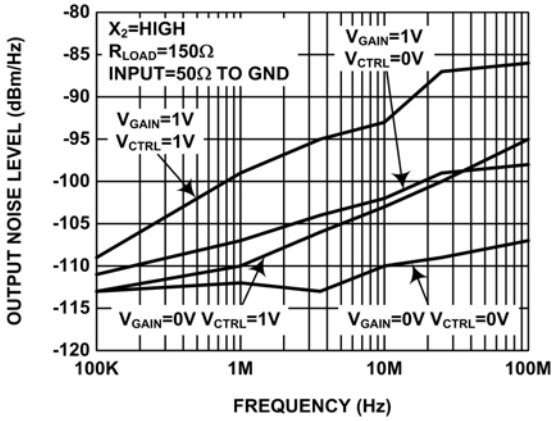


FIGURE 8. OUTPUT NOISE

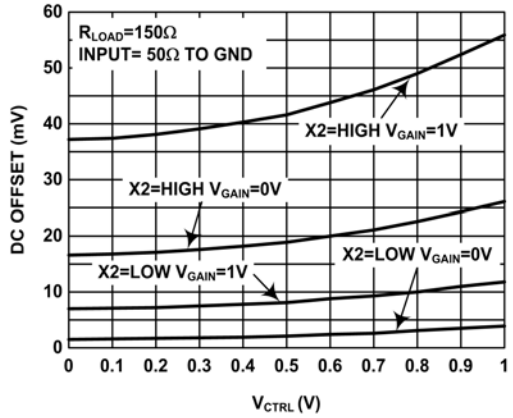


FIGURE 9. OFFSET vs V_{CTRL}

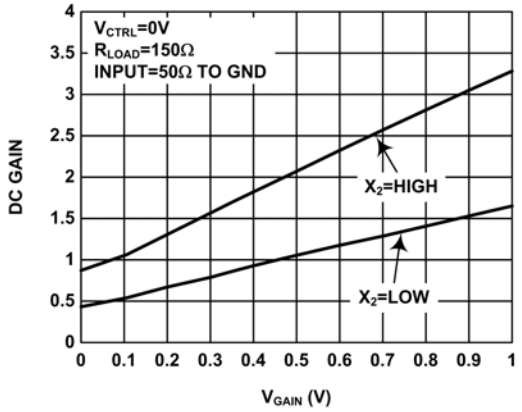


FIGURE 10. DC GAIN vs V_{GAIN}

Typical Performance Curves (Continued)

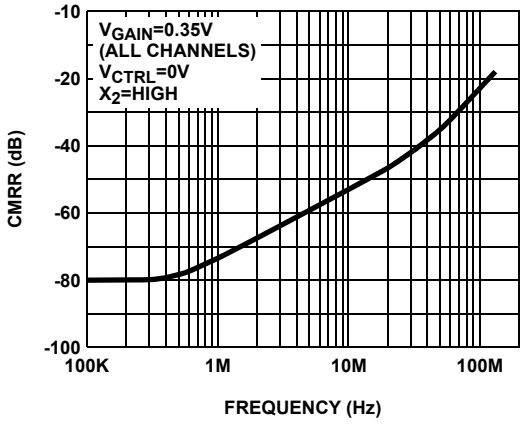


FIGURE 11. COMMON-MODE REJECTION

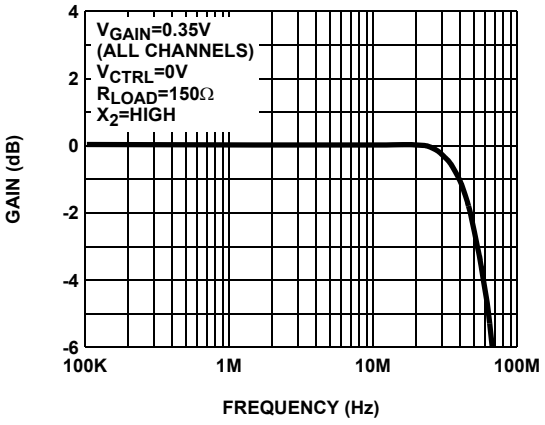


FIGURE 12. CM AMPLIFIER BANDWIDTH

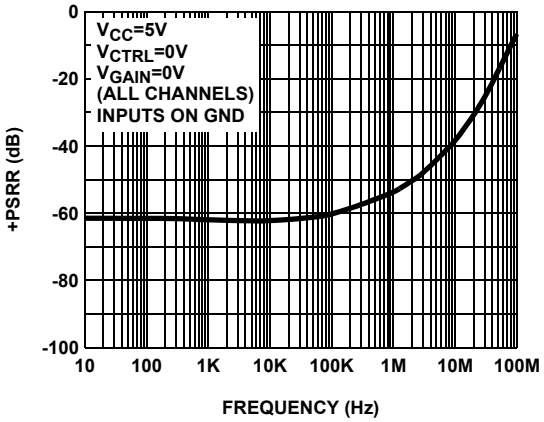


FIGURE 13. (+)PSRR vs FREQUENCY

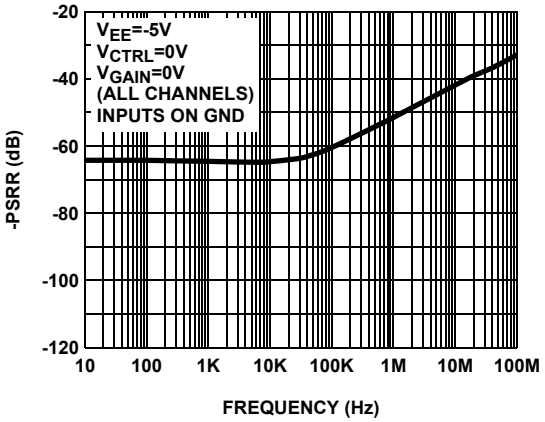


FIGURE 14. (-)PSRR vs FREQUENCY

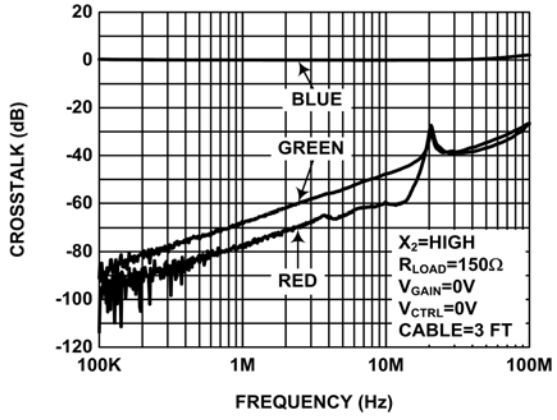


FIGURE 15. BLUE CROSSTALK

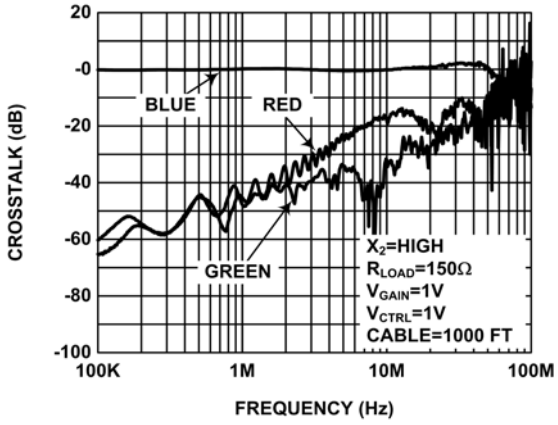


FIGURE 16. BLUE CROSSTALK

Typical Performance Curves (Continued)

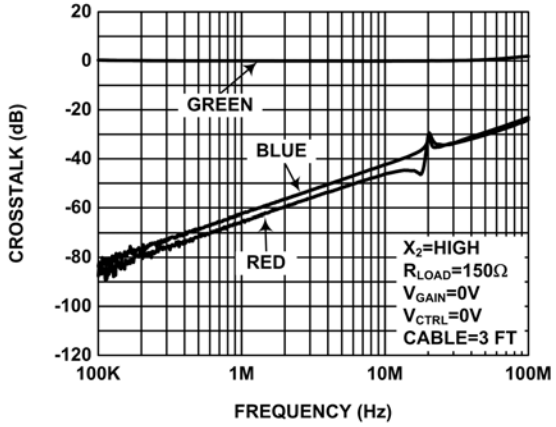


FIGURE 17. GREEN CROSSTALK

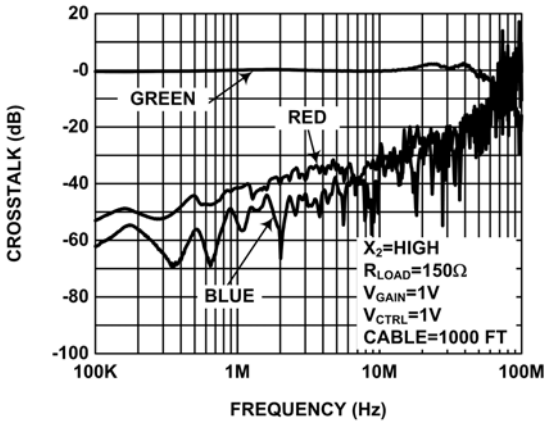


FIGURE 18. GREEN CROSSTALK

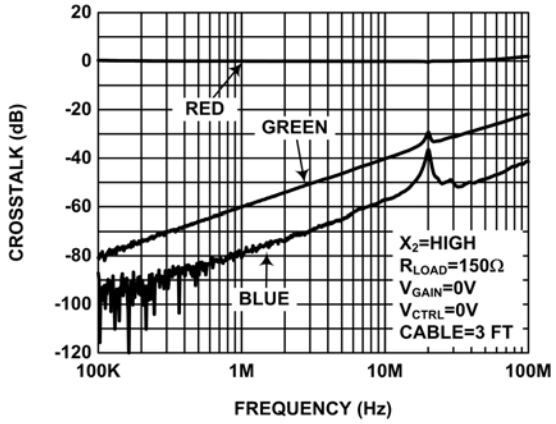


FIGURE 19. RED CROSSTALK

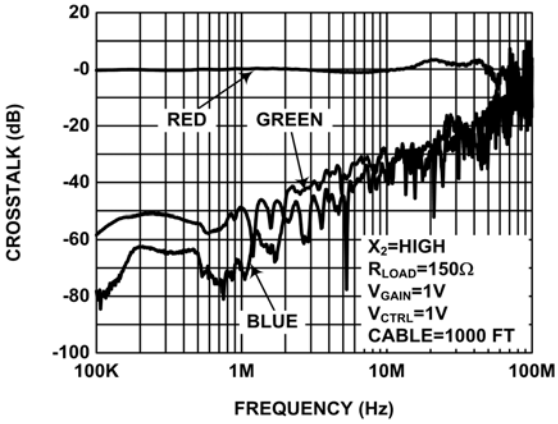


FIGURE 20. RED CROSSTALK

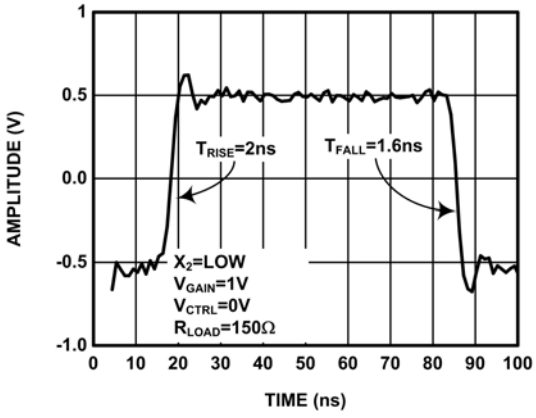


FIGURE 21. RISE TIME AND FALL TIME

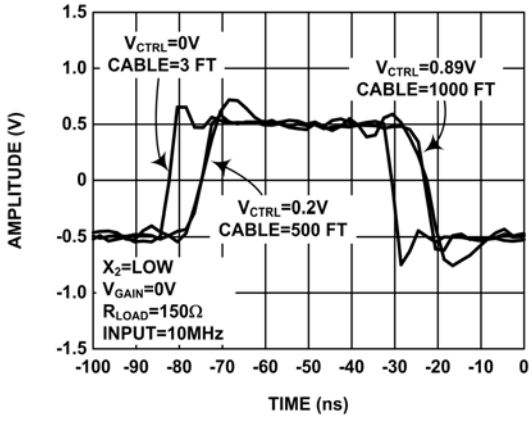


FIGURE 22. PULSE RESPONSE FOR VARIOUS CABLE LENGTHS

Typical Performance Curves (Continued)

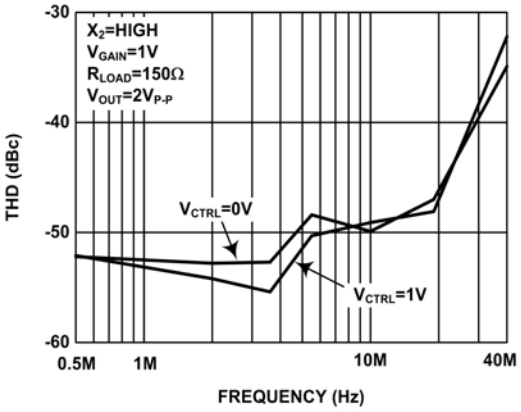


FIGURE 23. TOTAL HARMONIC DISTORTION

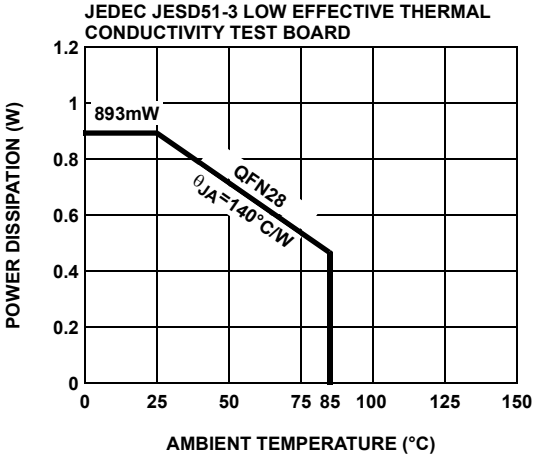


FIGURE 24. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

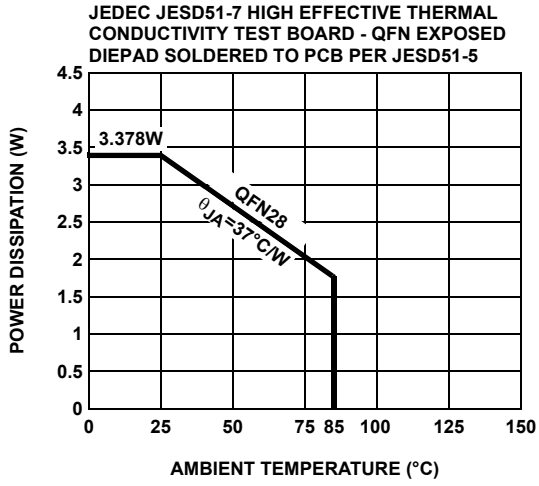


FIGURE 25. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Logic Control

The EL9112 has two logical input pins, Chip Enable (ENABLE) and Switch Gain (X2). The logic circuits all have a nominal threshold of 1.1V above the potential of the logic reference pin (VREF). In most applications it is expected that this chip will run from a +5V, 0V, -5V supply system with logic being run between 0V and +5V. In this case the logic reference voltage should be tied to the 0V supply. If the logic is referenced to the -5V rail, then the logic reference should be connected to -5V. The logic reference pin sources about 60µA and this will rise to about 200µA if all inputs are true (positive).

The logic inputs all source up to 10µA when they are held at the logic reference level. When taken positive, the inputs sink a current dependent on the high level, up to 50µA for a high level 5V above the reference level.

The logic inputs, if not used, should be tied to the appropriate voltage in order to define their state.

Control Reference and Signal Reference

Analog control voltages are required to set the equalizer and contrast levels. These signals are voltages in the range 0V - 1V, which are referenced to the control reference pin. It is expected that the control reference pin will be tied to 0V and the control voltage will vary from 0V to 1V. It is; however, acceptable to connect the control reference to any potential between -5V and 0V to which the control voltages are referenced.

The control voltage pins themselves are high impedance. The control reference pin will source between 0µA and 200µA depending on the control voltages being applied.

The control reference and logic reference effectively remove the necessity for the 0V rail and operation from ±5V (or 0V and 10V) only is possible. However we still need a further reference to define the 0V level of the single ended output signal. The reference for the output signal is provided by the 0V pin. The output stage cannot pull fully up or down to either supply so it is important that the reference is positioned to allow full output swing. The 0V reference should be tied to a 'quiet ground' as any noise on this pin is transferred directly to the output. The 0V pin is a high impedance pin and draws dc bias currents of a few µA and similar levels of AC current.

Equalizing

When transmitting a signal across a twisted pair cable, it is found that the high frequency (above 1MHz) information is attenuated more significantly than the information at low frequencies. The attenuation is predominantly due to resistive skin effect losses and has a loss curve which depends on the resistivity of the conductor, surface condition of the wire and the wire diameter. For the range of high performance twisted pair cables based on 24awg copper wire (CAT-5 etc.) these parameters vary only a little between cable types, and in general cables exhibit the same frequency dependence of loss. (The lower loss cables can be compared with somewhat longer lengths of their more lossy brothers.) This enables a single equalizing law equation to be built into the EL9112.

With a control voltage applied between pins V_{CTRL} and V_{REF}, the frequency dependence of the equalization is shown in Figure 8. The equalization matches the cable loss up to about 100MHz. Above this, system gain is rolled off rapidly to reduce noise bandwidth. The roll-off occurs more rapidly for higher control voltages, thus the system (cable + equalizer) bandwidth reduces as the cable length increases. This is desirable, as noise becomes an increasing issue as the equalization increases.

Contrast

By varying the voltage between pins V_{GAIN} and V_{REF}, the gain of the signal path can be changed in the ratio 4:1. The gain change varies almost linearly with control voltage. For normal operation it is anticipated the X2 mode will be selected and the output load will be back matched. A unity gain to the output load will then be achieved with a gain control voltage of about 0.35V. This allows the gain to be trimmed up or down by 6dB to compensate for any gain/loss errors that affect the contrast of the video signal. Figure 26 shows an example plot of the gain to the load with gain control voltage.

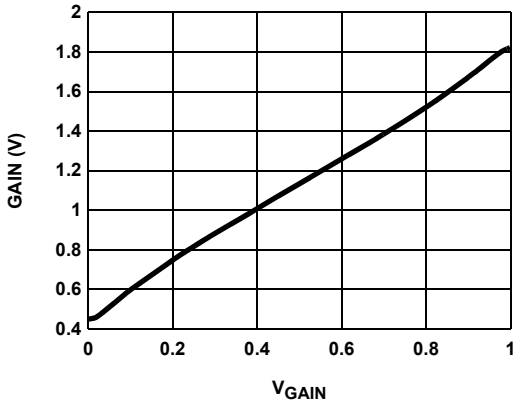


FIGURE 26. VARIATION OF GAIN WITH GAIN CONTROL VOLTAGE

Common Mode Sync Decoding

The EL9111 features common mode decoding to allow horizontal and vertical synchronization information, which has been encoded on the three differential inputs by the EL4543, to be decoded. The entire RGB video signal can therefore be transmitted, along with the associated synchronization information, by using just three twisted pairs.

Decoding is based on the EL4543 encoding scheme, as described in Figure 27 and Table 1. The scheme is a three-level system, which has been designed such that the sum of the common mode voltages results in a fixed average DC level with no AC content. This eliminates the effect of EMI radiation into the common mode signals along the twisted pairs of the cable

The common mode voltages are initially extracted by the EL9111 from the three input pairs. These are then passed to an internal logic decoding block to provide Horizontal and Vertical sync output signals (H_{OUT} and V_{OUT}).

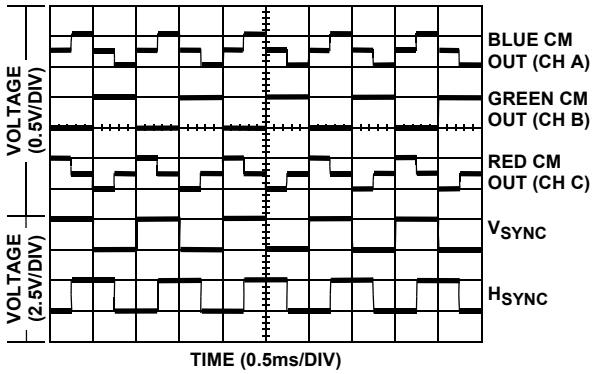


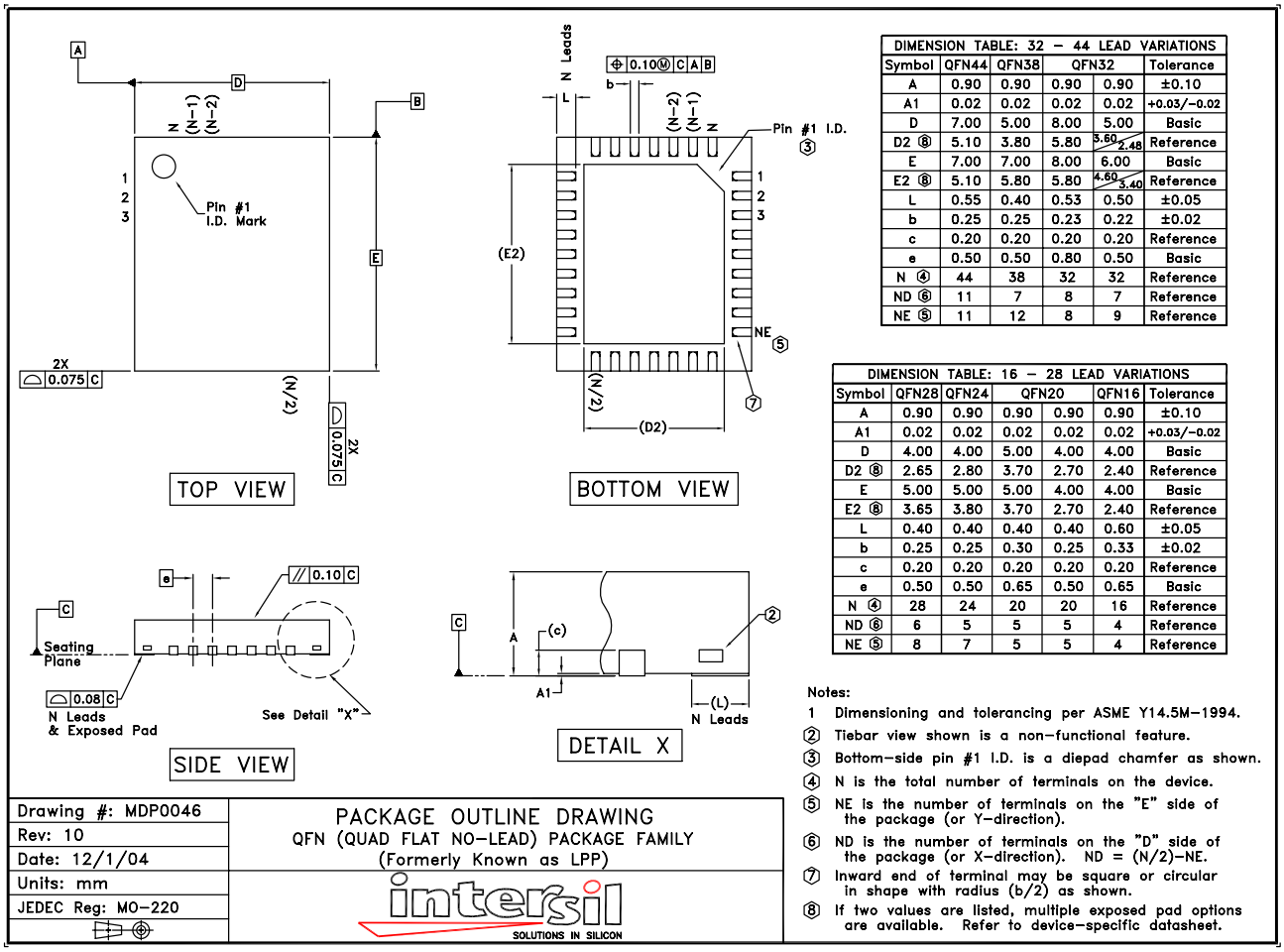
FIGURE 27. H & V SYNCS ENCODED

TABLE 1. H AND V SYNC DECODING

RED CM	GREEN CM	BLUE CM	H_{SYNC}	V_{SYNC}
Mid	High	Low	Low	Low
High	Low	Mid	Low	High
Low	High	Mid	High	Low
Mid	Low	High	High	High

NOTE: Level ‘Mid’ is halfway between ‘High’ and ‘Low’

Package Outline Drawing



DIMENSION TABLE: 32 – 44 LEAD VARIATIONS					
Symbol	QFN44	QFN38	QFN32		Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/–0.02
D	7.00	5.00	8.00	5.00	Basic
D2 (8)	5.10	3.80	5.80	3.60 / 2.48	Reference
E	7.00	7.00	8.00	6.00	Basic
E2 (8)	5.10	5.80	5.80	4.60 / 3.40	Reference
L	0.55	0.40	0.53	0.50	±0.05
b	0.25	0.25	0.23	0.22	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.80	0.50	Basic
N (4)	44	38	32	32	Reference
ND (6)	11	7	8	7	Reference
NE (5)	11	12	8	9	Reference

DIMENSION TABLE: 16 – 28 LEAD VARIATIONS					
Symbol	QFN28	QFN24	QFN20	QFN16	Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/–0.02
D	4.00	4.00	5.00	4.00	4.00	Basic
D2 (8)	2.65	2.80	3.70	2.70	2.40	Reference
E	5.00	5.00	5.00	4.00	4.00	Basic
E2 (8)	3.65	3.80	3.70	2.70	2.40	Reference
L	0.40	0.40	0.40	0.40	0.60	±0.05
b	0.25	0.25	0.30	0.25	0.33	±0.02
c	0.20	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.65	0.50	0.65	Basic
N (4)	28	24	20	20	16	Reference
ND (6)	6	5	5	5	4	Reference
NE (5)	8	7	5	5	4	Reference

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M–1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y-direction).
6. ND is the number of terminals on the "D" side of the package (or X-direction). ND = (N/2)–NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at http://www.intersil.com/design/packages/index.asp