GENERAL DESCRIPTION

EM19100 is an 8-bit CMOS A/D converter for video use. The adoption of a 2-step parallel system achieves low consumption at a maximum conversion speed of 20 MSPS typical.

FEATURES

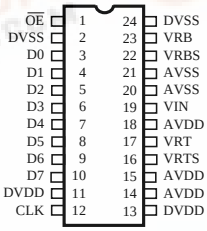
- 20MSPS maximum conversion speed
- Build-in sampling and hold circuit
- Internal self-bias reference voltage
- 90mW power dissipation at 20MSPS
- +5V single power supply
- Available in 24 pin SOP
- Series
  EM19100M for 300 mil SOP
  EM19100S for 209 mil SOP

APPLICATION

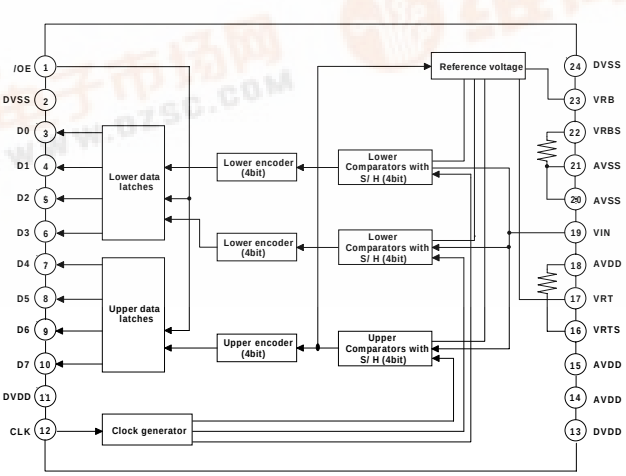
TV,VCR digital systems and a wide range of fields where high speed A/D conversion is required.

PIN ASSIGNMENT

EM19100

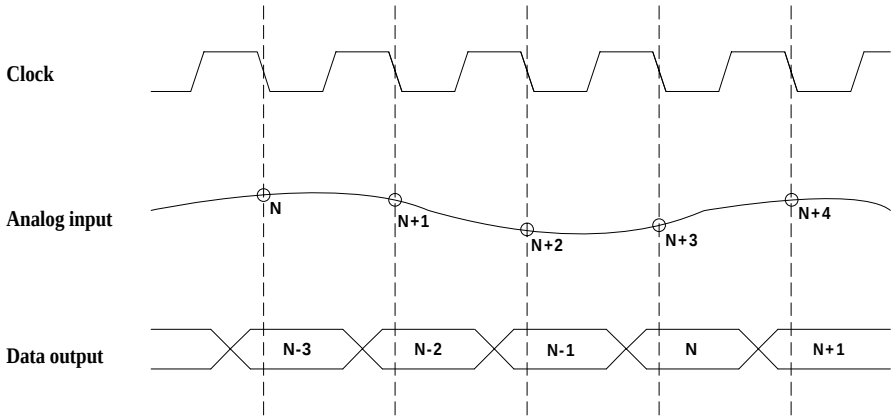


FUNCTIONAL BLOCK DIAGRAM



OUTPUT CODING

Step	Analog Input (V)	Digital Output Code	Conditions
0	0.607815	00000000	VRB=0.6V
1	0.607815~0.6156250	00000001	VRT=2.6V
2	0.6156250~0.6234375	00000010	1LSB=7.8125mV
....	....	....	
124	1.6000000~1.6078125	10000000	
125	1.6078125~1.6156250	10000001	
....	....	....	
254	2.5843750~2.5921875	11111110	
255	2.5921875~	11111111	



ABSOLUTE MAXIMUM RATINGS (T_A=25°C)

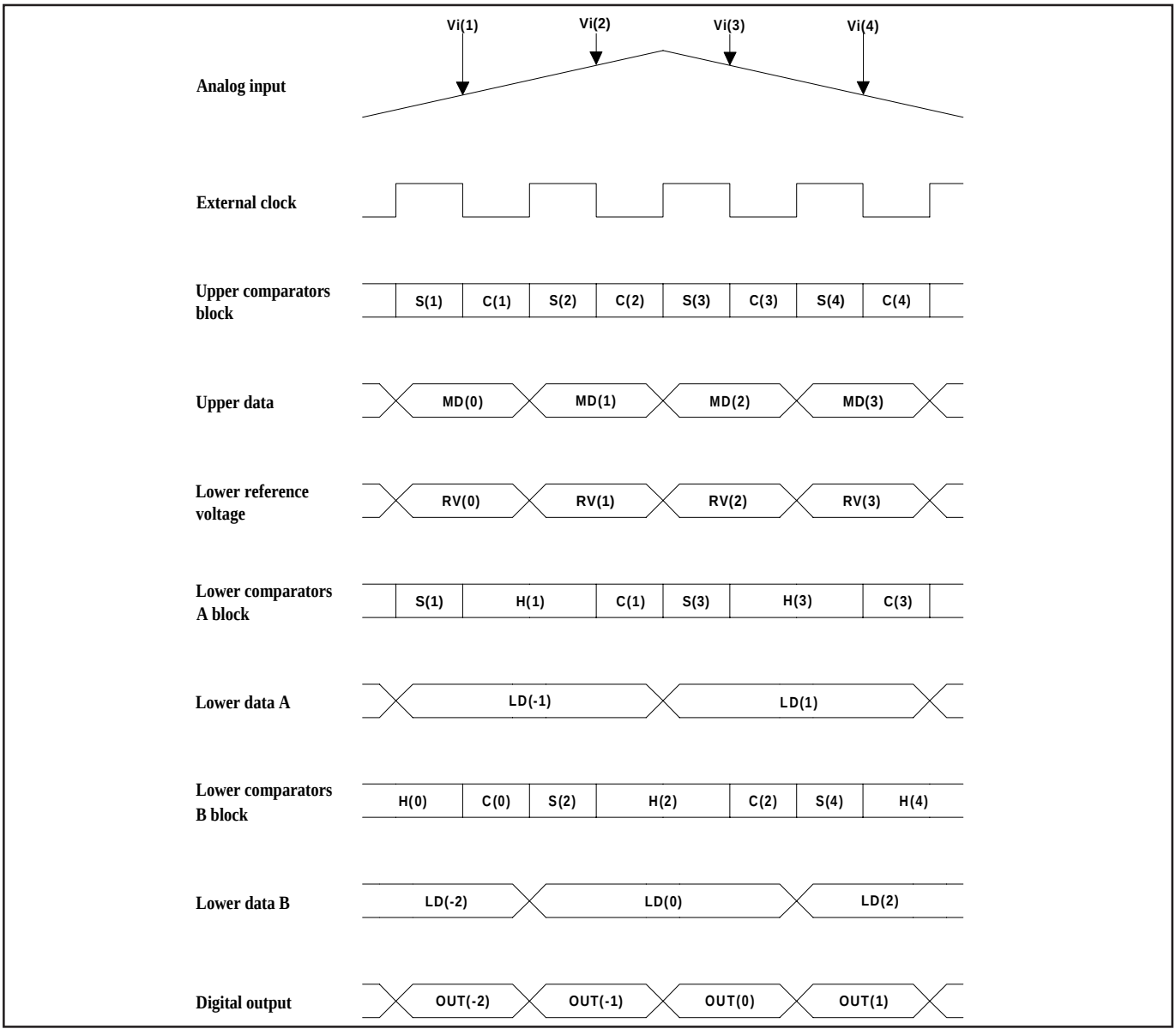
Items	Sym.	Rating	Unit
Supply voltage	V_{DD}	7	V
Operating temperature	T_{OPR}	-20 to +65	°C
Input voltage	V_{IN}	V_{SS} to V_{DD}	V
Ref, Input voltage	V_{RT},V_{RB}	V_{SS} to V_{DD}	V

(F_C=20MPS,V_{DD}=5V,V_{RB}=0.5V,V_{RT}=2.5V,Ta=25 deg.)

Parameter	Sym.	Conditions	Min.	Typ.	Max.	Unit
Maximum Conversion Speed	F_C	Vin=0.6V to 2.6V fin=1kHz ramp		20		MSPS
Supply current	I_{DD}	F_C=20MSPS NTSC ramp wave input		12	17	mA
Reference pin current	I_{REF}		5.7	8.0	9.1	mA
Analog input bandwidth	BW			10		MHz
Analog input capacitance	C_{IN}	V_{IN}=1.5V+0.07Vrms		11		pF
Reference resistance	R_{REF}		220	250	350	Ω
Internal bias	V_{RB}	Short V_{RB} and V_{RBS}	0.55	0.6	0.65	V
	V_{RT}-V_{RB}	Short V_{RT} and V_{RTS}	1.9	2.0	2.1	
Offset Voltage	E_{OT}		-10	-35	-60	mV
	E_{OB}		0	15	45	
Digital input voltage	V_{IH}		4.0			V
	V_{IL}				1.0	
Digital input current	I_{IH}	V_{DD}=max. V_{IH}=V_{DD}			5	uA
	I_{IL}	V_{IL}=0V			5	

Parameter	Sym.	Conditions	Min.	Typ.	Max.	Unit
Digital output current	I_{OH}	$\overline{OE}$=V_{SS},V_{OH}=V_{DD}-0.5V	-1.1			mA
	I_{OL}	V_{DD}=min. V_{OL}=0.4V	3.7			
Digital output current	I_{OZH}	$\overline{OE}$=V_{DD}, V_{OH}=V_{DD}			16	uA
		V_{OL}=0V			16	
Output data delay	T_{DL}			18	30	ns
Integral nonlinearity	EL	F_C=20MSPS V_{IN}=0.6V to 2.6V		0.5	1.3	LSB
Differential nonlinearity	ED	F_C=20MSPS V_{IN}=0.6V to 2.6V		±0.3	±0.5	LSB
Differential gain error	DG	NTSC 40 IRE mod ramp, F_C=14.3MSPS		1.0		%
Differential phase error	D_P			0.5		deg
Aperture jitter	t_{AJ}			30		ps
Sampling delay	t_{DS}			4		ns

Timing



Timing explanation

EM19100 is a 2-step parallel system A/D converter featuring a 4-bit upper comparators group and 2 lower comparators groups of 4-bit each. The reference voltage that is equal to the voltage between V_{RT}-V_{RB}/16 is constantly applied to the upper 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data. V_{RTS} and V_{RBS} pins serve for the self generation of V_{RT} (Reference voltage top) and V_{RB}(Reference voltage bottom).

This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.

The operation of respective parts is as indicated in the chart. For instance input voltage Vi(1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block. The upper comparators block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV(1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as Out(1) with the rising edge the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Application Note

V_{DD},V_{SS}

To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog V_{DD} pins, use a ceramic capacitor of about 0.1uF set as close as possible to the pin to bypass to the respective GND's.

Analog input

Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100Ω in series between the amplifier output and A/D input.

Clock input

The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits

Reference input

Voltage between V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. Bypassing V_{RT} and V_{RB} pins to GND, by means of a capacitor about 0.1μF, stable characteristics are obtained. By shorting V_{RT} and V_{RTS}, V_{RB} and VRBS, the self bias function that generates V_{RT}=2.6V and V_{RB}=0.6V, is activated.

Timing

Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and

with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.

$\overline{OE}$ pin

By connecting $\overline{OE}$ to GND output mode is obtained. By connecting to V_{DD} high impedance is obtained.

About latch up

It is necessary that AV_{DD} and DV_{DD} pins be the common source of power supply. This is to avoid latch up due to the voltage difference between AV_{DD} and DV_{DD} pins when power is ON.

Application Circuit