



EM77565

ADPCM with PCM CODEC

Version A1.0



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1. GENERAL DESCRIPTION

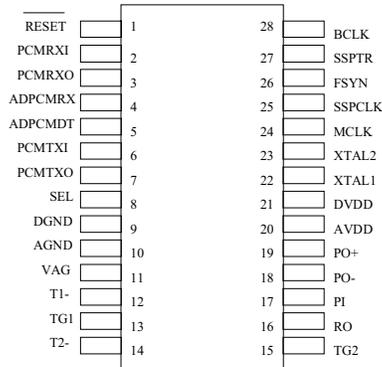
This ADPCM Codec is a single channel chip incorporating a 64 Kbps Mu-Law PCM codec filter with a 32 Kbps ADPCM transcoder specified by CCITT G.721. The chip also includes a serial setup port (SSP) interface with a five byte control registers for gain control, tone generator and battery test. A microcontroller can setup different gains through the SSP interface. This chip allows full-duplex operation over a single 3 volt voltage and its low power consumption makes it ideal for battery applications. In addition, this chip also consists of some OP amplifiers integrated with a PCM codec-filter to allow for easy control of the analog interface.

2. FEATURES

- Single 3.0 volt power supply
- Master clock rate: 19.2 MHz oscillator typically
- Max power consumption of 42 mW with 350 Ω load for 3 volt; power down of 0.6 mW
- Full-duplex single channel speech codec
- Built-in PCM codec-filter for A/D and D/A converter with Mu-Law companding
- Mu-PCM transcoder with 64 Kbps bit rates
- ADPCM transcoder with 32 Kbps bit rates Complied with CCITT G.721
- Serial Bit Clock transfer data rate from 64 Kbps to 2048 Kbps
- Five Control registers with 8 bits wide for Gain setup, Tone Generator and Battery Test applications
- Analog input: two single-end OP amplifier with external gain adjustment for microphone interface
- Analog output: Differential power driver with 350 Ω +120 nF load and external gain adjustment
- Packaged in 28-pin SOP



3. PIN CONFIGURATION



4. PIN DESCRIPTIONS

4.1. Power Control Interface

PIN Name	PIN No.	I/O	FUNCTION
AVDD	20	I	This pin is the analog power supply between 2.7 and 3.3 vol, 3 volt typically.
DVDD	21	I	This pin is the digital power supply between 2.7 and 3.3 vol, 3 volt typically.
DGND	9	I	This pin is digital ground and typically is connected to 0 volt.
AGND	10	I	This pin is analog ground and typically is connected to 0 volt.
VAG	11	O	This is the analog ground output pin which supplies a 1.35 volt reference voltage for all analog signal processing. This pin should be decoupled to AGND with 0.1 μ F capacitor. This pin is still 1.35 volt when the chip enters the power down mode.



4.2. Analog Interface

Pin Name	PIN No.	I/O	FUNCTION
TI-	12	I	This pin is the inverting input of the transmit input amplifier 1.
TG1	13	O	This pin is the analog output of the transmit input amplifier 1. It can be used to set the gain by external resistors.
T2-	14	I	This pin is the inverting input of the transmit input amplifier 2.
TG2	15	O	This pin is the analog output of the transmit input amplifier 2. It can be used to set the gain by external resistors.
RO	16	O	This pin is the non-inverting analog output of the receive smoothing filter. This pin can typically drive a 20 K Ω load to 1.3 volt peak –peak referenced to the VAG pin.
PI	17	I	This pin is the inverting input to the PO- (pin-18) power amplifier. This pin and PO- are used to set the gain by using external resistors.
PO-	18	O	This pin is the inverting power amplifier output. This pin can drive a 350 Ω +120 nF load differentially with PO+ pin.
PO+	19	O	This pin is the non-inverting power amplifier output. This pin can drive a 350 Ω +120 nF load differentially with PO- pin.



4.3. Digital Interface

PIN Name	PIN No.	I/O	FUNCTION
/RESET	1	I	This pin is reset input pin. When it is logic "0", the device is in the reset state. When it switches from logic 0 to logic 1, this chip is active and resets the ADPCM transcoder and all circuits.
XTAL1	22	I	This pin is the oscillator input and the system master clock input pin. For the crystal input, the XTAL2 pin must be tied to the other side. For the oscillator input, the pin should be connected to the ground.
XTAL2	23	O	This pin is the oscillator output. For the crystal input, the XTAL1 pin must be tied to the other side. For the oscillator input, the pin is floating.
MCLK	24	I	This pin is the system master clock input pin. It typically accepts 19.2 MHz. For the oscillator input, the pin is connected to external clock source.
FSYN	26	I	This pin is an 8 KHz frame syncs for transmit and receive ADPCM and PCM data. This pin is synchronized with the input and output of the serial PCM and ADPCM data stream.
BCLK	28	I	The bit clock is for transmission and receive ADPCM/PCM data. It shifts out the data on the rising edge and shift into the data on the falling edge. The frequency may vary from 32K to 2048 KHz.
PCMTXI	6	I	The pin inputs PCM data into device for ADPCM encoder. In application, this pin should be connected to PCMTXO pin.
PCMTXO	7	O	This pin outputs PCM data, either Mu-law or linear selected by SEL pin.
ADPCMDT	5	O	This pin transmits the ADPCM serial data. It is an open drain output with a pull-up resistor about 3K Ω . When the device is power down, the pin enters a high impedance.
PCMRXI	2	I	This pin inputs PCM data into device in order to bypass ADPCM decoder. In application, this pin should be connected to PCMRXO pin.
PCMRXO	3	O	This pin outputs PCM data after ADPCM decoder, either Mu-law or linear selected by SEL pin
ADPCMRX	4	I	This pin is the receive ADPCM data controlled by the FSYN and BCLK pins.
SEL	8	I	This pin selects Mu-law or linear data. If it is logic-0, the device selects Mu-law signal; otherwise, it selects the linear data.
SSPCLK	25	I	This pin is the clock for SSP setup. Note that data is shifted out of the SSP on the falling edge of this pin, and shifted into the SSP on the rising edge. The SSPCLK can be any frequency from 0 to 2048 KHz.
SSPTR	27	I/O	This pin is bidirectional serial data for SSP receive and transmission controlled by the SSPCLK pin (pin-25).

5. BLOCK DIAGRAM

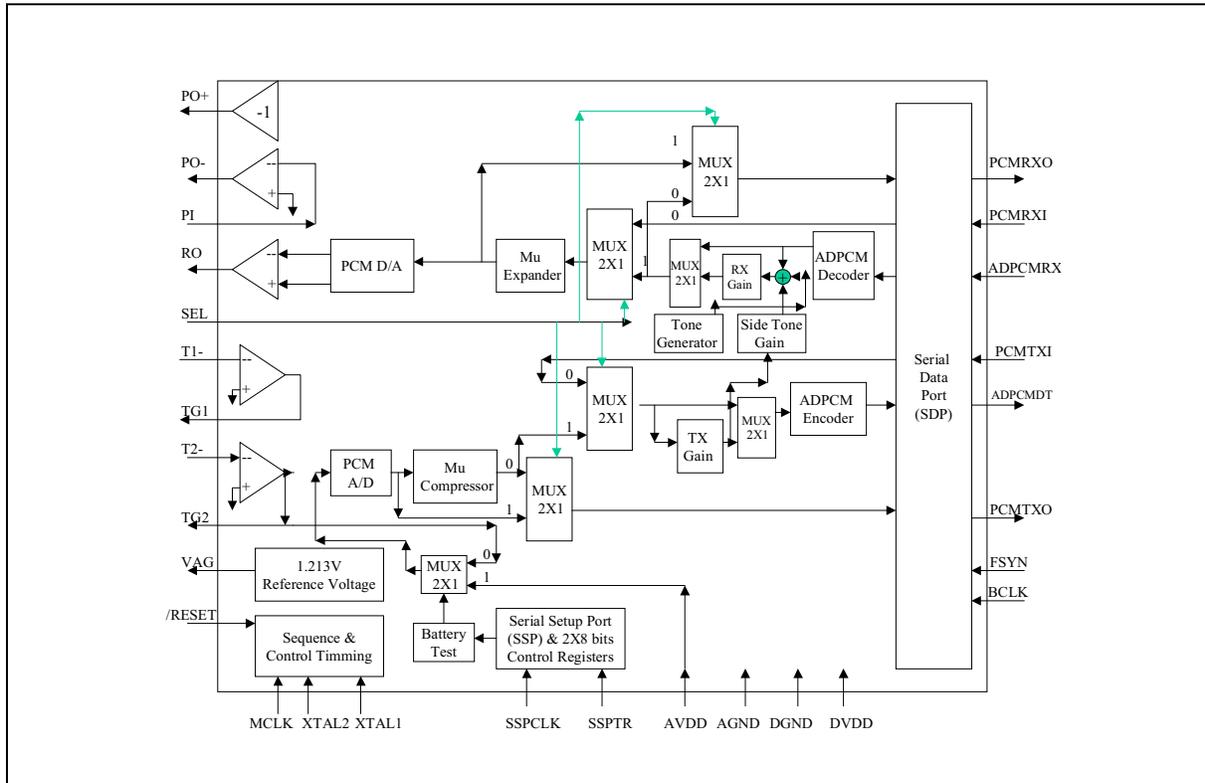


Figure 5-1 EM77565 ADPCM Codec Block Diagram

6. FUNCTIONAL DESCRIPTIONS

Figure 5-1 illustrates the functional blocks of EM77565 ADPCM codec. In this block there is a 3-volt power supply system, VDD pin, for all analog block and digital signal processing. Moreover, the analog ground is supplied with the AGND pin; and the digital ground is supplied with the DGND pin. AVDD should be decoupled to AGND and DVDD is decoupled to DGND pin with a 0.1 μ F capacitor. In addition, all analog reference voltages such as OP and power amplifier TG1, TG2, RO, PO are 1.35 volt.

This device has a built in linear 14-bit PCM codec with a Mu-Law compander. In the transmission path, an analog signal input is passed to the first OP amplifier (T1+, T1-, TG1) and/or the second OP amplifier (T2+, T2-, TG2) driving a typical 20 K Ω load externally to amplify the input analog signal. The analog signal is converted into a linear 14-bit A/D data via PCM A/D block. Then it can be compressed into 8-bit Mu-law data. By SEL pin, user can select the 14-bit linear data or 8-bit Mu-Law data on PCMTXO pin. Normally, the PCMTXO should be connected to PCMTXI pin. In the meantime, the 4-bit data after ADPCM encoder through transmit gain control is outputted on ADPCMDT pin every 8KHz frame sync, FSYN pin. In the tone generator mode, the input of the ADPCM encoder comes from the output of the tone generator, not from the transmit path in the PCM A/D. The ADPCM encoder outputs the tone ADPCM signal through pin ADPCMDT.

In the receive path, the 4-bit ADPCM data on the ADPCMRX pin is inputted into ADPCM decoder to



reconstruct the signal into 14-bit linear data. Once moreover, by SEL pin, user can control the output format, either 14-bit linear or 8-bit Mu-law data, on PCMRXO pin. Normally, the PCMRXO should be connected to PCMRXI pin. If the SEL pin is logic-0, the PCM data format is 8-bit Mu-Law data; otherwise, the PCM format is 14-bit linear data. Finally, the 14-bit linear data after through side tone gain and receive gain control is converted into analog signal by PCM D/A block. Then the analog output signal is sent to the power amplifier, RO, which is capable of driving a 20 K Ω load connected to the VAG pin. Note the device provides an differential power amplifier, PO+ & PO-, connected in a push-pull configuration with a 350 Ω + 120 nF load. If the device enables the tone generator, the function of the ADPCM decoder will be disabled. The tone generator can be used to generate DTMF tones, different ringing tones, and call progress tones for handset applications. In telephone line applications, this tone generator can be used for signaling on the line. In addition, If the user enable the battery test mode in control register CR0, the VDD pin, not TG2 pin, will be sampled by PCM A/D converter and the high pass filter is disable. In the meantime, the 8-bit linear data is stored into control register CR4.

The frame sync operation uses the long frame sync for transfer of the ADPCM and PCM data words, as shown in Fig 6-1 and 6-2. For the PCM data, the device shifts out the data on the PCMTXO and PCMRXO pin at the BCLK rising edge. As for the ADPCM data, the device shifts out the data on the ADPCMDT pin at the BCLK rising edge and shifts in the data on the ADPCMRX pin at the BCLK falling edge.

The device builds up the five 8-bit wide control registers, CR0—CR4, for different functional setup via the serial setup port. The serial port is a two wire interface given as SSPTR and SSPCLK to communicate with an external micro-controller. When SSPCLK, i.e., the data rate, is clocking into the chip, the data is reading from the SSP port or writing into the SSP port by the following protocol.

The SSP port first monitors 4 subsequent logic 1, “1111”, as the starting bits. Then the following bit is R/W bit, logic 1 as read status and logic 0 as write status. In the following the 3 subsequent bits, (A2:A0), are address bits; and the final 8 bits, (D7:D0), are data bits for CR0—CR4 found in the chapter 7 in more detail. The timing for read/write are shown in the Fig.6-3 and Fig 6-4.

For the sequence and control, the master clock MCLK, divided by 2 internally, which supports the clock of the DSP engine, may be asynchronous to all other blocks. Its frequency is typically 19.2 MHz. The frequency can be from crystal or oscillator (external clock). If master clock is from external clock, XTAL1 pin should be connected to the ground, XTAL2 floating, and use the MCLK pin as external clock source. As for the crystal application, user can connect 19.2 MHz crystal between XTAL1 and XTAL2, and MCLK is connected to XTAL2 without any capacitor. In addition, the /RESET pin can be controlled to reset and power down the device. Note if the device is power down, the values of control registers should be pre-store. And when the device is power up from reset/power down mode (/RESET pin is from logic-0 to logic1), the control registers must be re-written by pre-stored values.

For the digital I/O of Mu-law code, the full scale and zero words are shown in Table 6-1. For analog signal processing, the maximum transmit level is 3.17 dBm0 for Mu-Law.



	MU-LAW		
Level	Sign	Segment Bits	Step Bits
+ max. scale	1	000	0000
+Zero	1	111	1111
- Zero	0	111	1111
- max. scale	0	000	0000

Tabl6-1 Digital I/O for Mu-Law

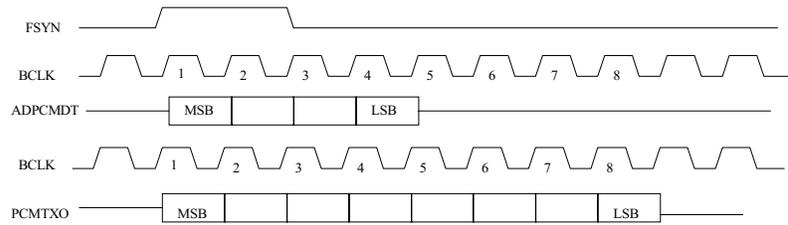


Fig. 6-1 Long Frame Sync for Transmission Timing

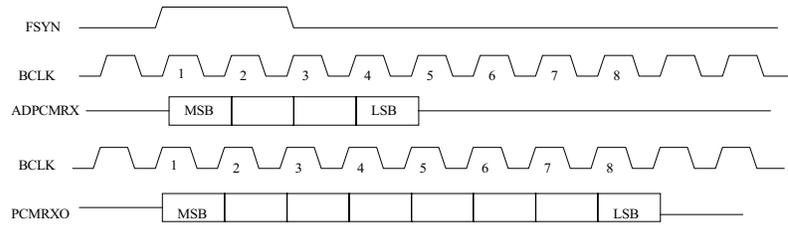


Fig. 6-2 Long Frame Sync for Receive Timing

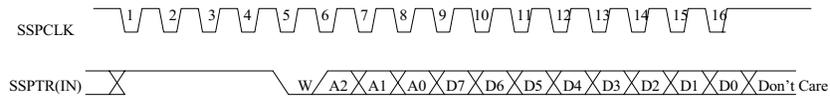


Fig. 6-3 SSP Writing Interface Timing

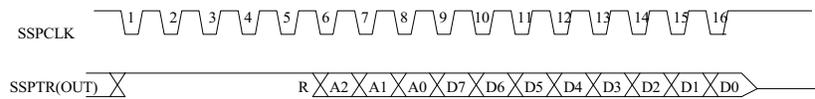


Fig. 6-4 SSP Reading Interface Timing



7. CONTROL REGISTERS

7.1. Introduction

There are 5x8-bit control registers for controlling the chip via the internal SSP port (Serial Setup Port) from external micro-controller. These registers are labeled CR0 and CR1. These descriptions are as follows. Note that "setting" is corresponding to logic "1" and "clearing" is corresponding to logic "0". In addition, the **res** bit indicates the reserved bit and must be logic-0.

The map of control registers for the software mode is shown in Table 7-1.

Control Register	R/W Status	B7	B6	B5	B4	B3	B2	B1	B0
CR0	W	Bat_test	En_Gain	Txgain[2]	Txgain[1]	Txgain[0]	Rxgain[2]	Rxgain[1]	Rxgain[0]
CR1	W	Stgain[2]	Stgain[1]	Stgain[0]	En_tone	Dis_coef	Encodtone	Para[1]	Para[0]
CR2	W	Tdata[11]	Tdata[10]	Tdata[9]	Tdata[8]	Tdata[7]	Tdata[6]	Tdata[5]	Tdata[4]
CR3	W	Tdata[3]	Tdata[2]	Tdata[1]	Tdata[0]	Res(test)	Res(test)	Res(test)	Res(test)
CR4	R	res							

Table 7-1 5x8-bit Control Registers Map

7.2. Control Register 0 (CR0)

This is a gain control for transmit and receive path and power detection setup. The CR0 register is configured as **0X1B** in hexadecimal format when the RESET pin is set to logic zero or power-on reset in initial.

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	Bat_test	En_gain	Txgain[2]	Txgain[1]	Txgain[0]	Rxgain[2]	Rxgain[1]	Rxgain[0]

Bat_test (B7):

When the bit is setting, the VDD pin is sampled by A/D converter and the high pass filter is disable for A/D path. In the meantime, the 8-bit linear result is stored into CR4. **Note when the function is enable, the speech path is disable via TG1 and TG2.**

EN_gain (B6):

If user wants to define different gain for transmit, receive and side tone, the bit must be logic-1.

Txgain[2:0](B[5:3]):

These three bits are used to control transmit gain as shown in Table 7-2 .



Txgain[2]	Txgain[1]	Txgain[0]	Transmit Gain Control(dB)
0	0	0	-6
0	0	1	-4
0	1	0	-2
0	1	1	0
1	0	0	+2
1	0	1	+4
1	1	0	+6
1	1	1	+8

Table 7-2 Transmit Gain Control

Rxgain[2:0](B[2:0]):

These three bits are used to control receive gain as shown in Table 7-3 .

Rxgain[2]	Rxgain[1]	Rxgain[0]	Receive Gain Control(dB)
0	0	0	-6
0	0	1	-4
0	1	0	-2
0	1	1	0
1	0	0	+2
1	0	1	+4
1	1	0	+6
1	1	1	+8

Table 7-3 Receive Gain Control

7.3. Control Register 1 (CR1)

This is a side tone gain control and Tone enable and setup. The CR1 register is configured as 0X00 in hexadecimal format when the RESET pin is set to logic zero or power-on reset in initial.

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	Stgain[2]	Stgain[1]	Stgain[0]	En_Tone	En_Coef	Encodtone	Para[1]	Para[0]

Stgain[2:0](B[7:5]):

These three bits are used to control sidetone gain as shown in Table 7-4 .



Stgain[2]	Stgain[1]	Stgain[0]	Side Tone Gain Control(dB)
0	0	0	OFF
0	0	1	-21
0	1	0	-19
0	1	1	-17
1	0	0	-15
1	0	1	-13
1	1	0	-11
1	1	1	-9

Table 7-4 Side Tone Gain Control

En tone (B4):

Setting this bit performs the tone generator routine instead of the ADPCM decoder. The result of the tone generator will be passed to the ADPCM encoder to compress the tone and transmit the encoded result to the ADPCMDT pin.

Dis coef (B3):

When the tone generator is initial for defining the frequency and gain, the bit should be logic-0. After the initialization, the bit must be setting up logic-1 for normal tone generator.

Encodtone (B2):

Setting this bit will turn on the ADPCM encoder for tone generator. In default, the encoder of tone generator will be disable.

Para[1:0](B[1:0]):

These two bits contain the four frequencies or tone generator attenuation coefficients. The 8-bit MSBs are placed in CR2[7:0]. And the last four LSBs are placed in the CR3[b7:b4] register. Switching between the frequency and attenuation factor is determined by table 7-5.

PARA[1] (B1)	PARA[0] (B0)	TONE PARAMETER SELECTION
0	0	Frequency of Tone 1
0	1	Attenuation of Tone 1
1	0	Frequency of Tone 2
1	1	Attenuation of Tone 2

Table 7-5 Tone generator Address Parameters



7.4. Control Register 2 (CR2)

This is a MSB tone parameters for frequency and attenuation data. The CR2 register is configured as 0X00 in hexadecimal format when the RESET pin is set to logic zero or power-on reset in initial.

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	Tdata[11]	Tdata[10]	Tdata[9]	Tdata[8]	Tdata[7]	Tdata[6]	Tdata[5]	Tdata[4]

Tdata[7:0](B[7:0]):

These eight bits contain the eight MSB frequencies or tone generator attenuation coefficients.

7.5. Control Register 3 (CR3)

This is a LSB tone parameters for frequency and attenuation data. The CR3 register is configured as 0X00 in hexadecimal format when the RESET pin is set to logic zero or power-on reset in initial.

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	Tdata[3]	Tdata[2]	Tdata[1]	Tdata[0]	Res(test)	Res(test)	Res(test)	Res(test)

Tdata[3:0](B[7:4]):

These four bits contain the last LSB frequencies or tone generator attenuation coefficients.

Res(test) (B[3:0]):

These bits are reserved for test mode. User cannot program them. The default values are zero.

7.6. Control Register 4 (CR4)

This register is reserved and cannot be controlled.



8. ELECTRICAL CHARACTERISTICS

8.1. Absolute Maximum Ratings

(Voltage Referenced to AGND and DGND pin)

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	VDD	-0.3 to +4.0	V
Analog Input Voltage	---	-0.3 to VDD + 0.3	V
Digital Input Voltage	---	-0.3 to VDD + 0.3	V
Operating Temperature	TOP	0 to +70	°C
Storage Temperature	TSTG	-55 to +85	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8.2. DC Characteristics

(AGND=DGND = 0 volt ,TOP =0 to +70 ° C)

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	VEXT	----	2.7	3.0	3.6	V
Operating Current	IEXT	MCLK=19.2 MHz, VDD=3.0 V with 350 Ω Loading	---	---	14	mA
Power Down Current	IPWDN	MCLK Off, /reset=0, VDD=3.0V	---	---	0.2	mA
Input High Voltage	VIH	All digital input pins	2.0	---	----	V
Input Low Voltage	VIL	All digital input pins	--	----	0.8	V
Output High Voltage	VOH	All digital output pins	2.4	----	----	V
Output Low Voltage	VOL	All digital output pins	--	---	0.4	V
Input High Current	IIL	VSS ≤ Vin ≤ VEXT	---	---	+10	uA
Input Low Current	IiH	VSS ≤ Vin ≤ VEXT	---	---	+10	uA



8.3. Analog Transmission Characteristics

(VDD = +3V ±5%, AGND=DGND = 0 volt , Top = 0 to +70 ° C ; all analog signal referenced to VAG; 64 Kbps Mu-Law PCM; FSYN = 8 KHz; BCLK = 2.048 MHz; MCLK = 19.2 MHz; Unless otherwise noted)

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT		RECEIVE		UNIT
				MIN.	MAX.	MIN.	MAX.	
Absolute Level	LABS	0 dBm0= -7.7 dBm @ 600 Ω	0.320	---	---	---	---	Vrms
Max. Transmit Level	TXMAX	-----	1.300	---	---	---	---	Vpp
Frequency Response, Relative to 0 dbm0 @ 1020Hz	GRTV	60 Hz	---	---	-23.5	-0.25	+0.25	dB
		300 to 3000 Hz	---	-0.16	+0.16	-0.16	+0.16	
		3400 Hz	---	-0.86	0	-0.86	0	
		4000 Hz	---	---	-23	---	-31	
Total Distortion vs. Level Tone (1020 Hz, Mu-Law, C- Message)	DLT	+3 dBm0	---	36	---	34	---	dBC
		0 to -30 dBm0	---	36	---	36	---	
		-40 dBm0	---	29	---	30	---	
		-45 dBm0	---	25	---	25	---	
Gain Variation vs. Level Tone (1020 Hz relative to - 10 dBm0)	GLT	+3 to -40 dBm0	---	-0.3	+0.3	-0.2	+0.2	dB
		-40 to -50 dBm0	---	-1.0	+1.0	-0.4	+0.4	
		-50 to -55 dBm0	---	-1.6	+1.6	-0.8	+0.8	
Idle Channel with Equipment Noise	NIDE	Mu-Law, C-Message	---	---	19	---	+11	dBm
Spurious Out-of-Band at RO (300 to 3400 Hz @ 0 dBm0)	NRO	4600 to 7600 Hz	---	---	---	---	-70	dB
		8400 to 100,000 Hz	---	---	---	---	-60	

8.4. Analog Electrical Characteristics

(OP Amplifier TG1, TG2, RO; Power Amplifier PO; VDD = +3V ±5%, AGND=DGND = 0V; Top = 0 to +70 ° C)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset voltage of TG1, TG2, PI	VOFIN	T1-, T2-, PI	---	---	±25	mV
Load Resistance to VAG for TG1, TG2, RO	RLD	TG1, TG2, RO	20	---	---	KΩ
Load Capacitance for RO	CLRO	RO	---	---	100	pF
VAG Output Voltage	VAG	to AGND	---	1.35	---	V
Load Resistance differentially for PO	Rldap	PO- to PO+	350	---	---	Ω
Load Capacitance for PO	Clap	PO- to PO+	---	---	100	pF
Power Supply Rejection Ratio (0 to 50 KHz @ 50m Vrms to VDD)	PSRRdd	---	40	--	---	dB



8.5. Digital Switching Characteristics

(VDD = +3V ±5%, AGND=DGND = 0V; Top = 0 to +70 ° C)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Master Clock Frequency	TMCK	MCLK,XTAL1, XTAL2	-0.01%	19.2	+0.01%	MHz
Bit Clock Frequency for ADPCM/PCM	TBKA	BCLK	32	---	2048	KHz
Frame Sync. Frequency	TSYN	FSYN	---	8	--	KHz
Clock Duty Cycle	CDC	MCLK,BCLK	30	50	70	%
Rise Time	TIR	All digital input pins	---	---	50	nS
Fall Time	TIF	All digital input pins	---	---	50	nS
Frame Sync. Pulse Width	TFSY	FSYN	1	---	---	BCLK
Frame Sync. Timing	Txs Tsx	BCLK to FSYN FSYN to BCLK	100 100	---	---	nS
Setup Time for ADPCMRX	TST	---	100	---	---	nS
Hold Time for ADPCMRX	THD	---	100	---	---	nS
Output Delay for Data Valid(I)	TdV1	BCLK to ADPCM/PCM Data Output	50	---	200	nS
Output Delay for Data Valid(II)	TdV2	FSYN to ADPCM/PCM Data Output	50	---	200	nS
SSP Clock Frequency	TSSPC	SSPCLK	---	---	2.048	MHz
Clock Duty Cycle of SSP	DSSP	SSPCLK	40	50	60	%
SSP Rx Valid Timing	Tsu THD	Setup Time Hold Time	50 50	---	---	nS
Output Delay Time for SSPTR Valid	Tdvc	SSPCLK to SSPTR	---	---	100	nS

Note: these parameters are shown in Figure 8-1, 8-2, 8-3 and 8-4.

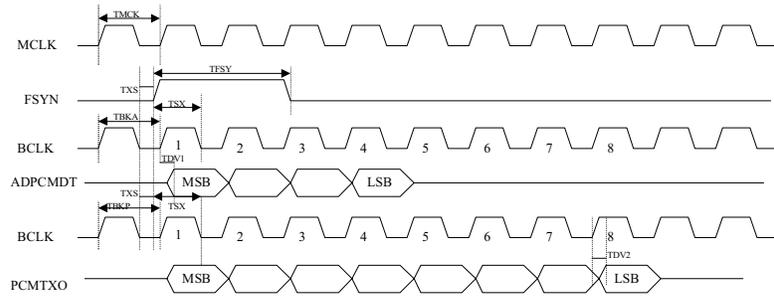


Fig. 8-1 Frame Sync for Transmission Timing

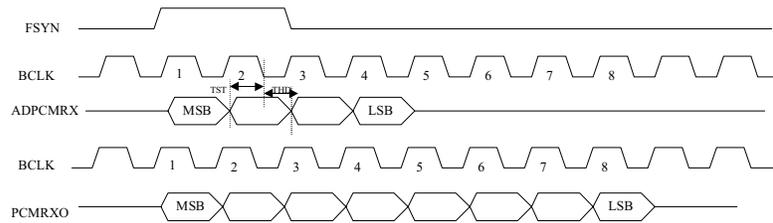


Fig. 8-2 Frame Sync for Receive Timing

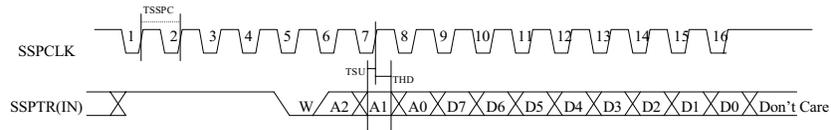


Fig. 8-3 SSP Writing Interface Timing

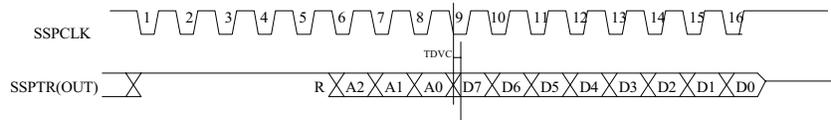
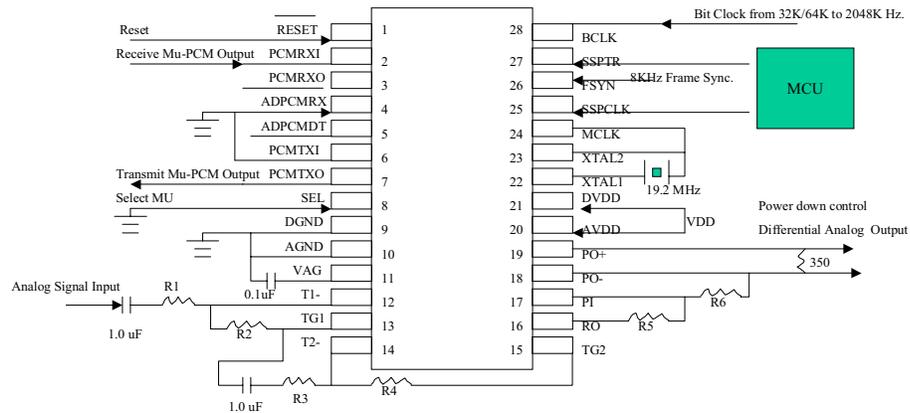


Fig. 8-4 SSP Reading Interface Timing



9. APPLICATION INFORMATIONS

For this application of PCM, VDD is supplied with a 3.0 volt typically. Meanwhile, the PCMRXO,ADPCMDT are floating(no connection). The output power amplifier pins PO- and PO+ can drive a load with $350 \Omega + 120 \text{ nF}$. The PCM codec only supports Mu-law PCM when the device is under PCM application. Note if the device is power down, the values of control registers should be pre-stored. And when the device is power up from reset/power down mode/RESET pin is from logic-0 to logic1), the control register must be re-written by pre-stored values.

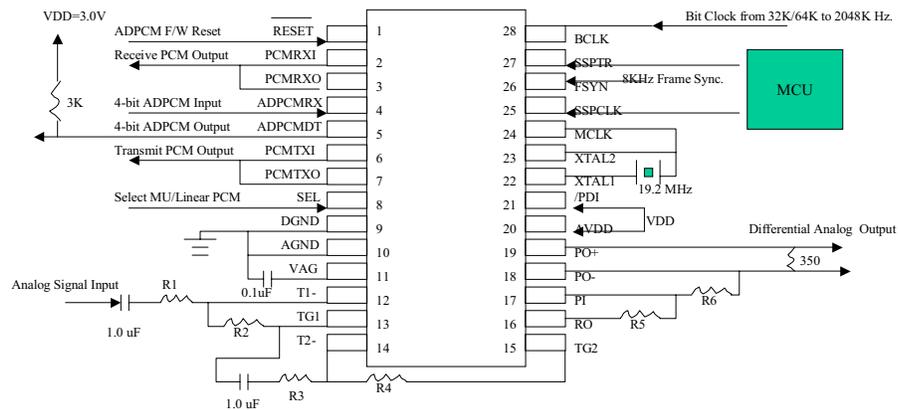


* Transmit Gain= $(R2/R1) * (R4/R3)$

* Receive Gain = $R6/R5$



As for this application of ADPCM, VDD is supplied with a 3.0 volt typically. Meanwhile, the ADPCMDT pin should be connected a pull-up resistor about 3K Ω . The output power amplifier pins PO- and PO+ can drive a load with 350 Ω + 120 nF.



* Transmit Gain = $(R2/R1) * (R4/R3)$

* Receive Gain = $R6/R5$



10. PROGRAMMING DUAL TONE GENERATOR

10.1 Introduction

Setting CR1(b4) to logic "1" is that the dual tone generator will be enabled. In the meantime, the ADPCM decoder will be disabled.

The procedure for programming the dual tone generator is as follows.

- (1) Setting CR1(b[4:3]) to logic "10" turns on the tone generator and setup the 12-bit coefficients for frequency and attenuation once every FSYN cycle(125 μ s). The 8 most significant bits(MSB) of 12-bit coefficients must be written into CR2(b[7:0]) and the 4 least significant bits(LSB) of 12-bit coefficients will be written into CR3(b[7:4]). In the meantime, user must setup CR1(b[1:0]) for frequency and attenuation value. In other words, the 12 bit coefficients stored in CR2(b[7:0]) and CR3(b[7:4]) are corresponding to CR1(b[1:0]) shown in table 7-5. The user must wait at least 125 us before writing another 12-bit coefficient for CR2 and CR3.
- (2) Repeat (1) 4 times until frequency1, attenuation1, frequency2, and attenuation2 setup OK..
- (3) Setting CR1(b[4:3]) to logic "11" is to get the dual tone generator.
- (4) If the only single tone is selected by this device, the other attenuation must be cleared into zero. The device always executes dual tone generator in tone generation mode.

10.2 Tone Frequency Coefficient Calculation

The tone frequency coefficient is calculated by the function " $\cos(2*PI*f/8000 \text{ radian})$ " where $PI = 3.14159$, and f is frequency (Hz). The number will then be converted into a 12-bit coefficient whose MSB is the sign and whose remaining 11 bits are the fractional part found by multiplying by 2048 and rounding off the number. For example, if the frequency is 1000 Hz, the frequency number is as followed.

$$\text{Cos}(2*3.14159*1000/8000) = 0.7071073$$

The converted binary number is 010110101000 and the hex number 5A8, where CR2 = 5A and CR3 = 80.

10.3 Tone Attenuation Coefficient Calculation

The tone attenuation coefficient is calculated by the function " $x/0.6545 \text{ Vp}$ " where x is the amplitude (Vp). The number will be converted into a 12-bit coefficient whose MSB is the sign and whose remaining 11 bits are the fractional part, found by multiplying by 2048 and rounding off the number. For example, if the attenuation is -11 dBm (600 Ω) Hz, first change the dBm units into Vp format as follows.

$$\text{sqrt}[10*\exp(-11/10)*600*0.001] * \text{sqrt}(2) = 0.3087384 \text{ Vp}$$

The attenuation is " $0.3087384/0.6545 = 0.4717164$ " the binary number is 001111000110 and the hex number is 3C6 where CR2 = 3C and CR3 = 60.



10.4 Frequency and Attenuation Coefficients for the DTMF Signal

Table 10-1 shows the 12-bit frequency coefficients for the DTMF signal. The 8 most significant bits are stored in CR2(b[7:0]), the 4 least significant bits are stored in CR3(b[7:4]). Table 10-2 illustrates the 12-bit attenuation coefficients for the DTMF signal such as -9 dBm (600 Ω) or -6 dBm (600 Ω) for column tone and -11 dBm (600 Ω) or -8 dBm (600 Ω) for row tone.

FREQUENCY (HZ)	CR2 (HEX)	CR3 (HEX)
697	6D	50
770	69	50
852	64	60
941	5E	A0
1209	4A	80
1336	3F	C0
1477	33	20
1633	24	60

Table 10-1 Frequency Coefficients for the DTMF Signal

ATTENUATION (DBM@600 Ω)	PEAK VALUE (VP)	CR2 (HEX)	CR3 (HEX)
-11	0.308738	3C	60
-9	0.388679	4C	00
-8	0.436105	55	50
-6	0.549023	6B	60

Table 10-2 Attenuation Coefficients for the DTMF Signal

11. PACKAGE DIMENSIONS

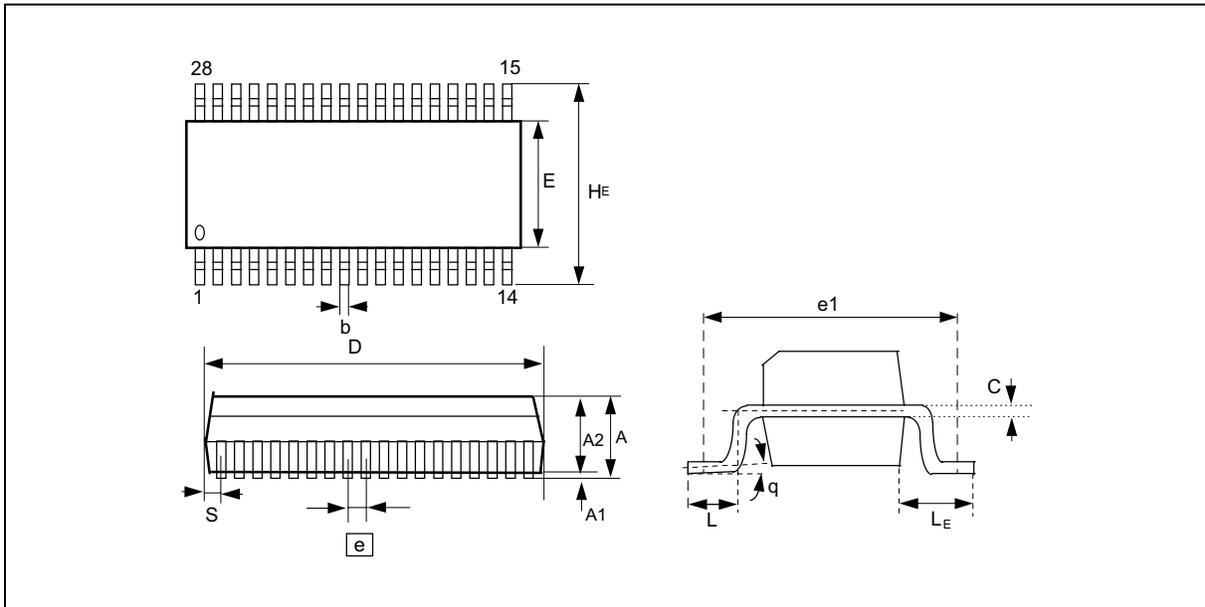


Figure 9. 28-Lead Plastic SOP Package

SYMBOL	DIMENSION IN INCH	DIMENSION IN MM
A	0.110 Max.	2.794 Max.
A1	0.004 Min.	0.102 Min.
A2	0.093 ±0.005	2.362 ±0.127
b	0.016 +0.004 -0.002	0.406 +0.102 -0.051
c	0.010 +0.004 -0.002	0.254 +0.102 -0.051
D	0.705 TYP. (0.725 Max.)	17.90 TYP. (18.415 Max.)
E	0.295 ±0.005	7.493 ±0.127
e	0.050 ±0.006	1.270 ±0.152
e1	0.370 Nom.	9.396 Nom.
HE	0.406 ±0.012	10.312 ±0.305
L	0.036 ±0.006	0.914 ±0.203
LE	0.055 ±0.006	1.397 ±0.203
S	0.043 Max.	0.102 Max.
θ	0–10 degree	0–10 degree