EM78869

8-Bit RISC Type Microprocessor

Product Specification

VERSION 1.0

ELAN MICROELECTRONICS CORP.

July 2004

Specification Revision Chronology		
Version	Revision Description	Date
1.0	Initial version	2004/07/12

Trademark Acknowledgments
IBM is a registered trademark and PS/2 is a trademark of IBM.
Microsoft, MS, MS-DOS, and Windows are registered trademarks of Microsoft Corporation.

Printed in Taiwan, ROC, 07/12/2004 (Version 1.0)

ELAN MICROELECTRONICS CORPORATION

Headquarters:
No. 12, Innovation Road 1
Science-based Industrial Park
Hsinchu, Taiwan, R.O.C. 30077
Tel: +886 3 563-9977
Fax: +886 3 563-9966
http://www.emc.com.tw

Hong Kong:
Elan (HK) Microelectronics Corporation, Ltd.
Rm. 1005B, 10/F Empire Centre
68 Mody Road, Tsimshatsui
Kowloon , HONG KONG
Tel: +852 2723-3376
Fax: +852 2723-7780
http://www.elanhk.com.hk

USA:
Elan Information Technology Group
10062 Miller Ave., Suite 100
Cupertino, CA 95014
USA
Tel: +1 048 366-8223
Fax: +1 048 366-8220

Europe:
Elan Microelectronics Corp. (Europe)
Dubendorfstrasse 4
8051 Zurich, SWITZERLAND
Tel:+41 43 299-4060
Fax:+41 43 299-4079
http://www.elan-europe.com

Shenzhen:
Elan (Shenzhen) Microelectronics Corporation, Ltd.
Rm. 420/4Fl., Fuxing Garden
Fuxing Rd, Futian Dist., Shenzhen
Guandong, CHINA 518031
Tel: +86 755 2601-0565
Fax: +86 755 2601-0500

Shanghai:
Elan Electronics (Shanghai) Corporation, Ltd.
23/Bldg. 115, Lane 572, Bibo Road
Zhangliang Hi-Tech Park
Shanghai, CHINA
Tel: +86 021 5080-3866
Fax: +86 021 5080-4600

Contents

1 General Description

The EM78869 is an 8-bit RISC type microprocessor with low power, high speed CMOS technology. Integrated into the single chip are on chip watchdog (WDT), RAM, ROM, programmable real-time clock/counter, internal interrupt, power-down mode, LCD driver, and tri-state I/O. The EM78869 provides a single chip solution for designing DATA-BANK of message display.

The EM78869 is the cost-down version of its predecessor, the EM78862/B. Comparison between the two series is as follows:

Item	EM78862	EM78862B	EM78869
ROM size	16K X 13 bit	16K X 13 bit	8K X 13 bit
RAM size	2.2K X 8 bit	2.2K X 8 bit	0.7K X 8 bit
LCD	60 X 9	60 X 9	40 X 9
LCD RAM	Write only when LCD is enabled. Read/Write when disabled.		
Oscillator	Crystal	Crystal/RC	Crystal/RC
Code option	MCLK	MCLK/OSCSEL	MCLK/ELCD/OSCSEL
Pins number	84	84	64
OTP	EM78P862A	EM78P862A	EM78P862A

2 Features

2.1 CPU

- Operating voltage range: 2.2V ~ 5.5V
- Operating temperature range: –20°C ~ +70°C.
- 32.768KHz Crystal/RC oscillation circuit selected by code option for system clock
- 144 byte general purpose register
- 640 x 8 bits on-chip data RAM
- 8K x 13 on-chip mask type program ROM.
- Up to 29 bi-directional tri-state I/O ports
- 8-level stack for subroutine nesting
- 8-bit real time clock/counter (TCC)
- Programmable free running on-chip watchdog timer
- Port key scan function
- Operation mode: a) Normal mode; b) Green mode; c).Idle mode; d) Sleep mode
- Input port wake-up function (Port 9)
- 7 interrupt sources:
  - 4 external (INT0 ~ INT3)
  - 3 internal (one TCC timer overflow interrupt + two 8-bit counters overflow interrupt)
- 64-pin chip form (EM78869)

2.2 LCD

- Software selectable LCD operation voltage
- Common driver pins: 8 or 9
- Segment driver pins: 40
- 1/4 bias
- 1/8, 1/9 duty
- Adjustable LCD contrast

3 Applications

- Data Bank
- Message display box
- Scientific calculator

4 Pin Configurations

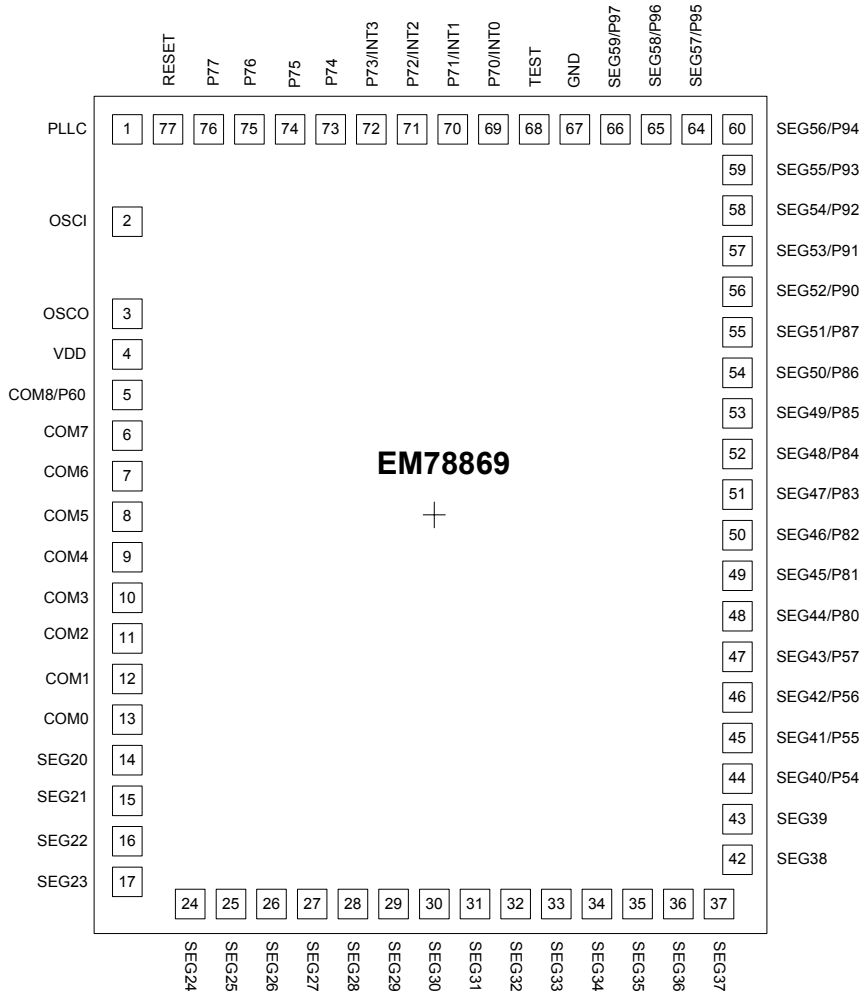


Fig. 1 EM78869 Pin Configuration for Dice Form

4.1 Pin Description

PIN	PIN Number	I/O type	Description
VDD	4	I	Power supply pin
GND	54	I	System ground pin
OSCI	2	I	In crystal mode: crystal input In RC mode: resistor pull high. RC or crystal selection thru OSCSEL bit of code option
OSCO	3	O	In crystal mode: crystal output
COM0 ~ COM8	13 ~ 5	O	Common driver pins of LCD driver
SEG20 ~ SEG59	14 ~ 53	O	Segment driver pins of LCD driver
/RESET	64	I	Low active. If set as /RESET and remains at logic low, the devices will be reset
PLLC	1	I	Phase loop lock capacitor. Connect a capacitor 0.01μ to 0.047μ with GND.
/INT0~/INT3	56 ~ 59	I	Signal can be interrupt signals
P5.4 ~ P5.7	34 ~ 37	I/O	Port 5 (INPUT or OUTPUT port per bit). Shared with LCD segment signals
P6.0	5	I/O	Port 6 (INPUT or OUTPUT port per bit). Shared with LCD common signals
P7.0 ~ P7.7	56~63	I/O	Port 7 (INPUT or OUTPUT port per bit). Internal Pull high function. Key scan function. General purpose I/O pin.
P8.0 ~ P8.7	38~45	I/O	Port 8 (INPUT or OUTPUT port per bit). Shared with LCD segment signals
P9.0 ~ P9.7	46~53	I/O	Port 9 (INPUT or OUTPUT port per bit). “And” can be set as wake-up watchdog timer. “And” is shared with Segment signal.
TEST	55	I	Test pin during test mode only. Normally low

Table 1 Pin Arrangement

5 Functional Block Diagram

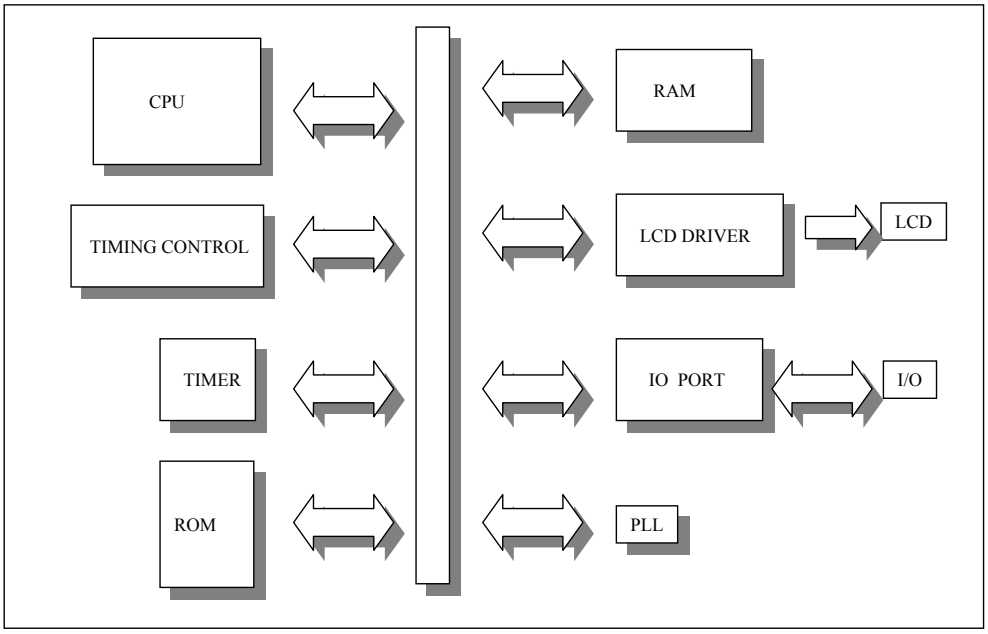


Fig. 2a System Overview Block Diagram

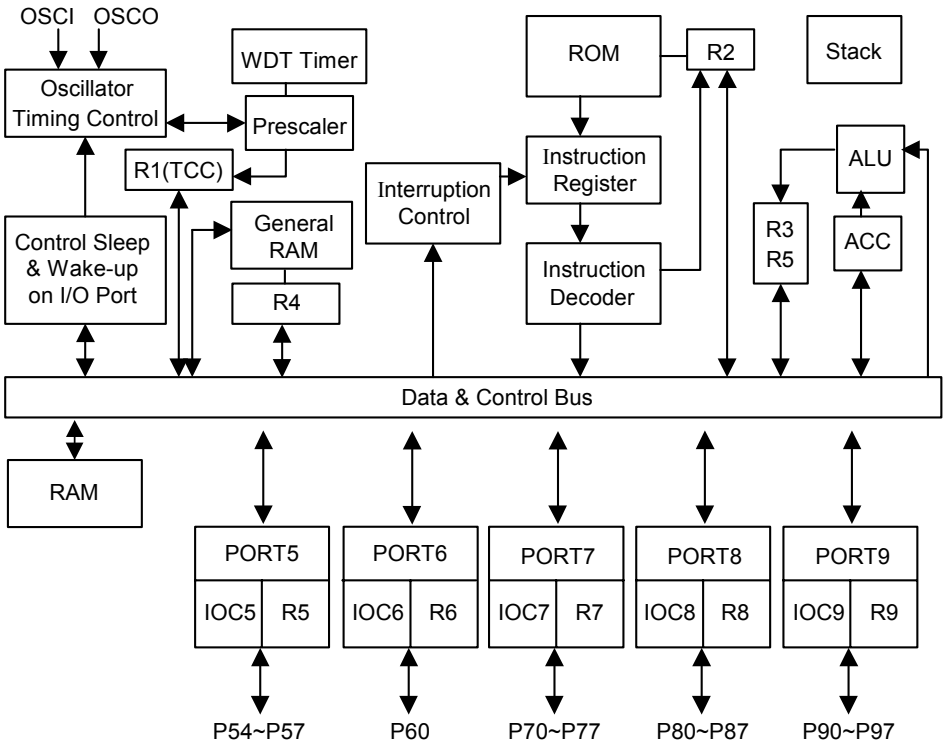


Fig. 2b System Functional Block Diagram

6 Functional Descriptions

6.1 Operational Registers

6.1.1 R0 (Indirect Address Register)

R0 is not a physically implemented register. It is useful as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (TCC)

- Increased by an external signal edge applied to TCC, or by the instruction cycle clock.
- Written and read by the program as any other register.

6.1.3 R2 (Program Counter)

The structure is depicted in Fig. 3 below.

- Generates 8K × 13 on-chip ROM addresses to the relative programming instruction codes.
- "JMP" instruction allows the direct loading of the low 10 program counter bits.
- "CALL" instruction loads the low 10 bits of the PC and PC+1, then push it into the stack.
- "RET" ("RETL k," "RETI") instruction loads the program counter with its contents at the top of stack.
- "MOV R2, A" allows the loading of an address from "A" register to the PC, and the 9th and 10th bits are cleared to "0."
- "ADD R2, A" allows a relative address be added into current PC, and its 9th and 10th bits content are cleared to "0."
- "TBL" allows a relative address to be added into the current PC, and its 9th and 10th bits content do not change. The most significant bit (A10~A13) will be loaded into the status register (R5) with the contents of bits PS0~PS3 upon execution of a "JMP," "CALL," "ADD R2, A," or "MOV R2, A" instruction.

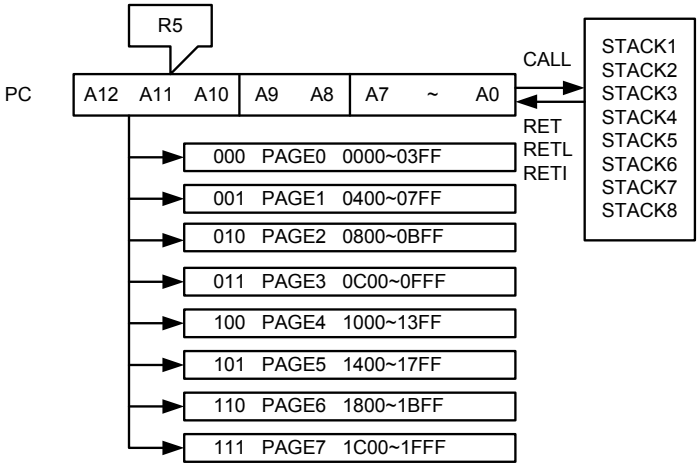


Fig. 3 Program Counter Organization

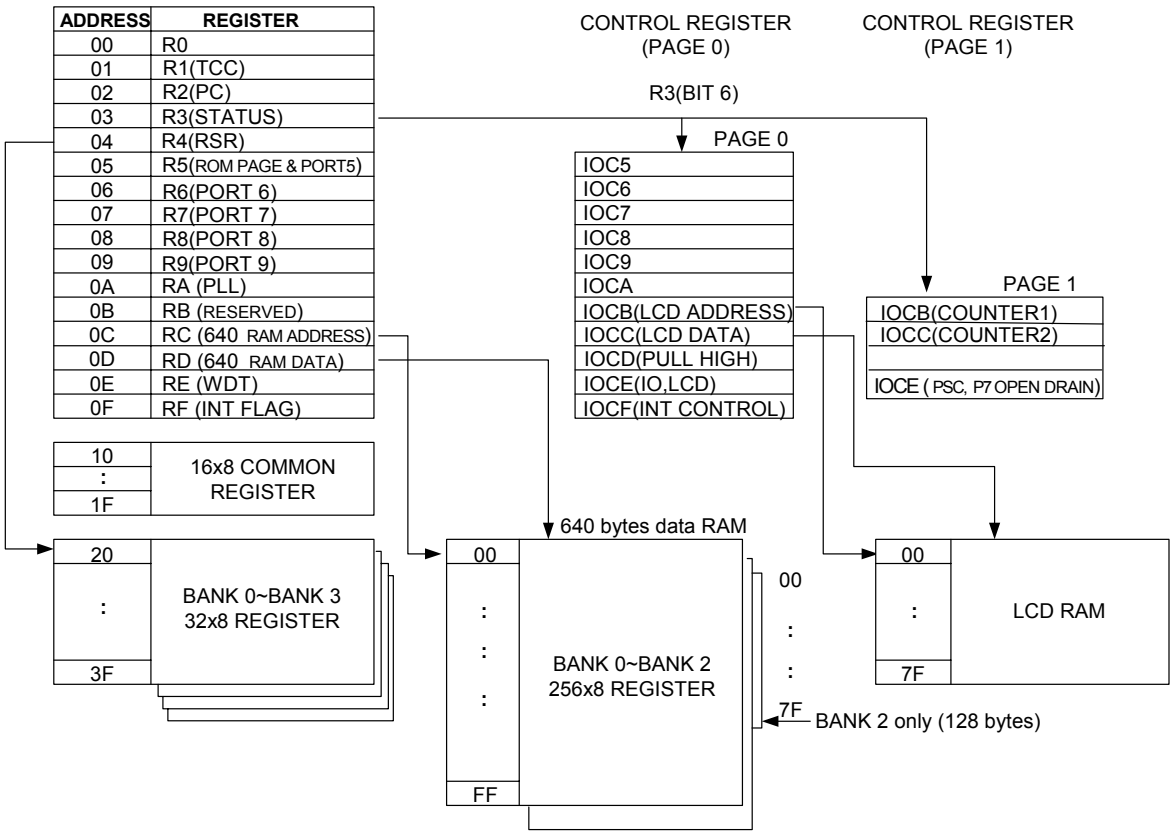


Fig. 4 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	PAGE	0	T	P	Z	DC	C

Bit 0: (C) Carry flag

Bit 1: (DC) Auxiliary carry flag

Bit 2: (Z) Zero flag

Bit 3: (P) Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4: (T) Time-out bit. Set to 1 by the "SLEP" and "WDTC" command or during power up; and reset to 0 by WDT timeout.

Event	T	P	Remark
WDT wake-up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET pin	X	X	X =Don't care

Bit 5: Unused, fixed at "0"

Bit 6: (PAGE) Change IOCB ~ IOCE to another page, 0/1 => page0 / page1

Bit 7: Unused

6.1.5 R4 (Register Bank Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBK1	RBK0	FSR5	FSR4	FSR3	FSR2	FSR1	FSR0

Bits 0 ~ 5: Used to select up to 32 registers in indirect address mode of each bank

Bits 6 ~ 7: Determine which bank is activated among the 4 banks

Refer to Fig. 4; *Data Memory Configuration* (previous page) for configuration of the data memory

6.1.6 R5 (Program Page Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R57	R56	R55	R54	0	PS2	PS1	PS0

Bit 0 ~2: (PS0 ~ PS2) Page select bits as shown below:

PS2	PS1	PS0	Program Memory Page (Address)
0	0	0	Page 0
0	0	1	Page 1
0	1	0	Page 2
:			:
1	1	0	Page 6
1	1	1	Page 7

You can use PAGE instruction to change and maintain program page. Otherwise, use far jump (FJMP) or far call (FCALL) MACRO instructions to program user's code. ÉLAN's complier supports program page maintenance and can change your program by inserting instructions within its program.

Bit 3: Unused. Set to '0'

Bit 4 ~7: 4-bit I/O registers of Port 5

6.1.7 R6 (Port 6)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	-	R60

Bit 0: Port 6 single bit (Bit 0) I/O register

Bit 1 ~7: Unused

6.1.8 R7 (Port 7)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R77	R76	R75	R74	R73	R72	R71	R70

Bit 0 ~7: Port 7 8-bit I/O registers

6.1.9 R8 (Port 8)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R87	R86	R85	R84	R83	R82	R81	R80

Bit 0 ~7: Port 8 8-bit I/O registers

6.1.10 R9 (Port 9)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R97	R96	R95	R94	R93	R92	R91	R90

Bit 0 ~7: Port 9 8-bit I/O registers

6.1.11 RA (Mode Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IDLE	PLLEN	0	1	0	-	-	-

Bit 0 ~2: Unused

Bit 3: Reserved. Clear this bit to '0.'

Bit 4: Reserved. Always set to '1.'

Bit 5: Reserved. Clear this bit to '0'.

Bit 6: (Read/Write) PLL enable signal

0: Disable PLL

1: Enable PLL

The relation between 32.768K and 3.579M (X'TAL) is explained in Fig. 5 below.

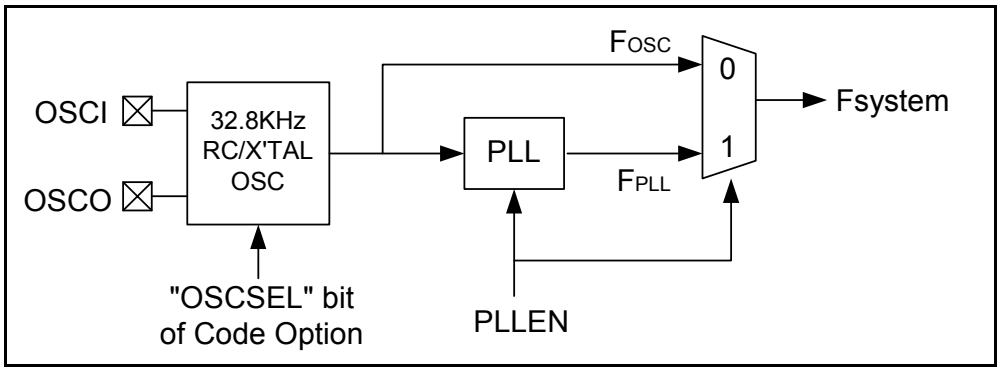


Fig 5 The Relation between 32.768KHz and 3.579MHz

Bit 7: (IDLE) Sleep mode selection bit. This bit defines which SLEP instruction is to be executed.

0: Sleep mode

1: Idle mode

When Sleep mode is defined, program is re-activated by Watch Dog time-out or Port 9 signal input and resume running from the "Start" vector (0H).

When Idle mode is defined, program is re-activated by TCC clock or Watch Dog time-out, or by Port 9, 7.0 ~ 7.3 signal input. Program will continue running from the instruction that follows the "SLEP" instruction.

Wakeup Signal	SLEEP Mode	IDLE Mode	GREEN Mode	NORMAL Mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(1,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC Time-Out	X	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt
WDT Time-Out	RESET	Wake-up + Next instruction	RESET	RESET
Port 9	RESET	Wake-up + Next instruction	X	X
Port 7.0 ~ 7.3	X	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt

NOTES: P7.0 ~ P7.3 wake-up function is controlled by IOCF (1, 2, 3, 7) and ENI instruction.
P7.0 wakeup signal is a rising or falling signal defined by CONT register Bit 7.
Port 9, Port 7.1, Port 7.2, and Port 7.3 wake-up signals are a falling edge signal.
X=Don't care

6.1.12 RB (Reserved)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	1	1	1	1	1

Bit 0 ~7**:** Reserved. Set Bit 7 to Bit 0 to '1'.

6.1.13 RC (640 Bytes RAM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_A7	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0

Bit 0 ~7**:** Select data bank RAM address of up to 256. IOCA is the register for bank selection.

6.1.14 RD (640 Bytes RAM Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0

Bit 0~7**:** 640 bytes RAM data transfer register

NOTE
Refer to Section 6.2.8; ***IOCA Register*** *on how to select RAM bank.*

6.1.15 RE (LCD Driver, WDT Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	WDTE	WUP9H	WUP9L	0	LCD_C2	LCD_C1	LCD_M

Bit 0**:** (LCD_M) LCD_M defines the LCD control methods, including duty (see table next page).

Bit 1~2: (LCD_C#) Defines LCD display mode, enable, disable, or blanking (see following table).

LCD_C2	LCD_C1	LCD_M	LCD Display Control	Duty	Bias
0	0	0	Change duty	1/9	1/4
0	0	1	Disable (turn off LCD)	1/8	1/4
0	1	0	Blanking	1/9	1/4
0	1	1	Blanking	1/8	1/4
1	0	0	(Don't care)	1/9	1/4
1	0	1	(Don't care)	1/8	1/4
1	1	0	LCD display enable	1/9	1/4
1	1	1	LCD display enable	1/8	1/4

Bit 3: Reserved. Clear this bit to '0'.

Bit 4: (WUP9L) Port 9 low nibble Wake-Up Enable. Use to enable the low nibble wake-up function in Port 9.
0: Disable
1: Enable

Bit 5: (WUP9H) Port9 high nibble Wake-Up Enable. Use to enable the high nibble wake-up function in Port 9.
0: Disable
1: Enable

Bit 6: (WDTE = Watch Dog Timer Enable)

Control bit is used to enable Watchdog timer. The relation between Bit 4 to Bit 6 is illustrated in Fig. 6 below.
0: Disable
1: Enable

Bit 7: Reserved. Clear this bit to '0'

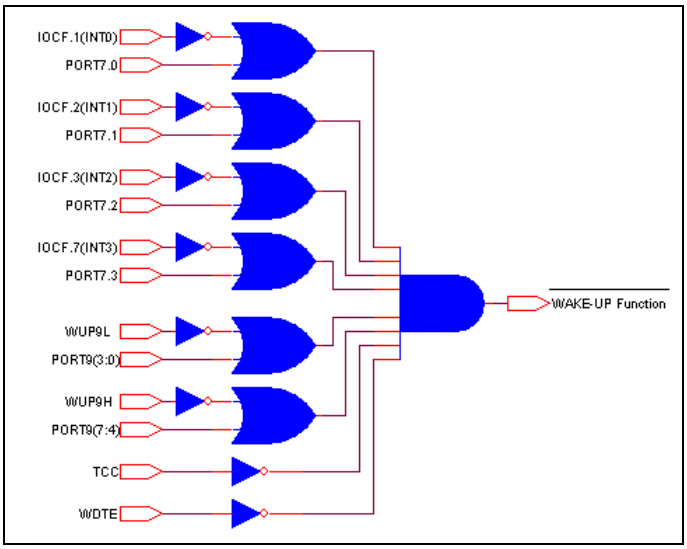


Fig. 6 Wake-up Function and Control Signal

6.1.16 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT3	0	CNT2	CNT1	INT2	INT1	INT0	TCIF

Bit 0**:** (TCIF) TCC timer overflow interrupt flag. Set when TCC timer overflows.

Bit 1**:** (INT0) External INT0 pin interrupt flag

Bit 2**:** (INT1) External INT1 pin interrupt flag

Bit 3**:** (INT2) External INT2 pin interrupt flag

Bit 4**:** (CNT1) Internal Counter 1 underflow interrupts

Bit 5**:** (CNT2) Internal Counter 2 underflow interrupts

Bit 6: Unused. Clear to '0.'

Bit 7**:** (INT3) External INT3 pin interrupt flag

NOTE

1. *"1" means interrupt request; "0" means non-interrupt*
2. *Refer to Section 6.7 (**Interrupt**) for reference on high to low edge trigger*
3. *IOCF is the interrupt mask register. You can read and clear this register.*

6.1.17 R10 ~ R1F and R20 ~ R3F (General Purpose Register)

R10 ~ R1F & R20 ~ R3F (Banks 0~3) are general purpose registers.

6.2 Special Purpose Registers

6.2.1 A (Accumulator, ACC)

Internal data transfer, or instruction operand holding. This is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EDGE	INT	TS	-	PAB	PSR2	PSR1	PSR0

Bit 0 ~2**:** (PSR0) (PSR2) TCC/WDT pre-scaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3: (PAB) Pre-scaler assignment bit
0: For TCC use
1: For WDT use

Bit 4: Unused

Bit 5: (TS) TCC signal source
0: Internal instruction cycle clock
1: 16.384KHz or RC/2 (in RC mode)

Bit 6: (INT) INT enable flag. This bit is read only
0: Interrupt masked by DISI or hardware interrupt
1: Interrupt enabled by ENI/RETI instruction

Bit 7: INT_EDGE
0: P7.0 (INT0) interrupt source is a rising edge signal
1: P7.0 (INT0) interrupt source is a falling edge signal

NOTE
CONT is a readable and writable register.

6.2.3 IOC5 (Port 5 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC57	IOC56	IOC55	IOC54	0	0	0	P5S

Bit 0: P5S is switch register for I/O port or LCD signal switching.
0: Select normal I/O port
1: Select SEG40~SEG43 output as LCD SEGMENT output

Bit 1: Unused.

Bit 2: Unused.

Bit 3: Unused.

Bit 4 ~7: Port 5 I/O direction control registers
0: Set the relative I/O pin as output
1: Set the relative I/O pin into high impedance

6.2.4 IOC6 (Port 6 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	IOC60

Bit 0: Port 6 I/O direction control register
0: Set the relative I/O pins as output
1: Set the relative I/O pin into high impedance

Bit 2 ~7 Unused. Clear to '0'

NOTE
*Refer to Section 6.2.12, **IOCE (Bit 5) Register** on how to switch Port 6 to normal I/O port.*

6.2.5 IOC7 (Port 7 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70

Bit 0 ~7: (IOC70 ~ IOC77) Port 7 I/O direction control register
0: Set the relative I/O pins as output
1: Set the relative I/O pin into high impedance

6.2.6 IOC8 (Port 8 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80

Bit 0 ~7: (IOC80 ~ IOC87) Port 8 I/O direction control register
0: Set the relative I/O pins as output
1: Set the relative I/O pin into high impedance

NOTE
*Refer to Section 6.2.8, **IOCA (Bit6/7) Register** below on how to switch Port 8 to normal I/O port.*

6.2.7 IOC9 (Port 9 I/O Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90

Bit 0 ~7: (IOC90 ~ IOC97) Port 9 I/O direction control register
0: Set the relative I/O pins as output
1: Set the relative I/O pin into high impedance

NOTE
*Refer to Section 6.2.12, **IOCE (Bit6/7) Register** on how to switch Port 9 to normal I/O port.*

6.2.8 IOCA (640 Bytes RAM Bank, Port 8 I/O, or LCD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P8SH	P8SL	0	0	0	RAMBK1	RAMBK0	0

Bit 0: Unused. Clear to '0'

Bit 1 ~2: (RAMBK0~RAMBK1) Select 640 bytes RAM bank.

RAMBK1	RAMBK0	Note (Total Size)
0	0	RAM BANK0 (256 Bytes)
0	1	RAM BANK1 (256 Bytes)
1	0	RAM BANK2 (128 Bytes)
1	1	Reserved

Bit 3 ~ 5: Unused. Clear the bits to '0'

Bit 6: (P8SL) Port 8 low nibble switch
0: Normal I/O port
1: Segment output

Bit 7**:** (P8SH) Port 8 high nibble switch
0: Normal I/O port
1: Segment output

6.2.9 IOCB (LCD Address, Counter 1 Preset Register)

Page 0 (LCD Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	LCDA6	LCDA5	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0

Bit 0 ~ 6**:** (LCDA0~LCDA6) LCD address
The LCD display data is stored in the data RAM. The relation between data area and COM/SEG pin is as follows:

SEGMENT	IOCC (COM7 ~ COM0)								IOCB (Address)	Remarks
Unused	X	X	X	X	X	X	X	X	00 H	
Unused	X	X	X	X	X	X	X	X	01 H	
:	:								:	
:	:								:	
SEG 20									14H	1/8 DUTY
SEG 21									15H	
:										
:										
SEG 58									3AH	
SEG 59									3BH	
Unused									3CH	
Unused									:	
Unused									3FH	
SEGMENT	**IOCC(COM 8)**								**IOCB(Address)**	**Remarks**
Unused	X								40H	
Unused	X								41H	
:	:									
SEG 20									54H	1/9 DUTY
SEG 21									55H	
:										
:										
SEG 58									7AH	
SEG 59									7BH	
Unused	X								7CH	
:	:								:	
Unused	X								7FH	

Bit 7**:** Unused. Fixed at '0'.

NOTE
Write only when LCD is enabled. Read/Write when disabled.

Page 1 (Counter 1 Preset Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C1D7	C1D6	C1D5	C1D4	C1D3	C1D2	C1D1	C1D0

Bit 0 ~7**:** (C1D0~C1D7) 8 bit up counter (COUNTER1) preset and read out register (write = preset). After an interruption, it will count from "0".

6.2.10 IOCC (LCD Data, Counter 2)

Page 0 (LCD Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0

Bit 0 ~7**:** (LCDD0~LCDD7) LCD RAM data register

Page 1 (Counter 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C2D7	C2D6	C2D5	C2D4	C2D3	C2D2	C2D1	C2D0

Bit 0 ~7**:** (C2D0~C2D7) 8 bit up-counter (COUNTER2) preset and read out register. (Write = preset). After an interruption, it will count from "00".

6.2.11 IOCD (Pull-High Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70

Bit 0 ~7**:** (PH70~PH77) Control bit is used to enable the pull-high of Port 7 (#) pin.
0: Disable internal pull-high register
1: Enable internal pull-high register

6.2.12 IOCE (Bias Control Register)

Page 0 (Port9 GPIO/LCD Segment, Port6 GPIO/LCD Com, LCD Bias, Scan Key Signal Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P9SH	P9SL	P6S	BIAS3	BIAS2	BIAS1	0	SC

Bit 0**:** (SC) Scan key signal.
0: Disable scan key signal
1: Enable scan key signal

Once you enable this bit, all of the LCD signal will have a low pulse during a common period. This pulse has 30μs width. Use the following procedures to implement the key scans function**:**

a) Set Port7 as input port

b) Set IOCD Page 0 Port 7 to pull high

c) Enable scan key signal

d) Once a key is pressed, set RA (6)=1, and switch to normal mode

e) Blank LCD. Disable scan key signal

f) Set P9SL = 0, P9SH = 0. Port 9 sent probe signal to Port 7 and read Port 7 to get the key. Note that a probe signal instruction delay will occur before the next instruction is performed.

g) Set P9SH = 1, P9SL =1. Port 9 is defined as LCD signal and enable LCD.

NOTE
This procedure is also applicable to Port 6 and Port 8.

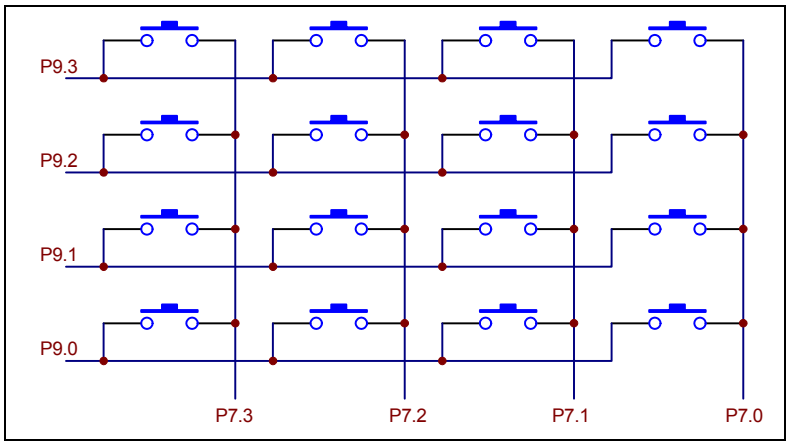


Fig. 7 Key Scans Circuit

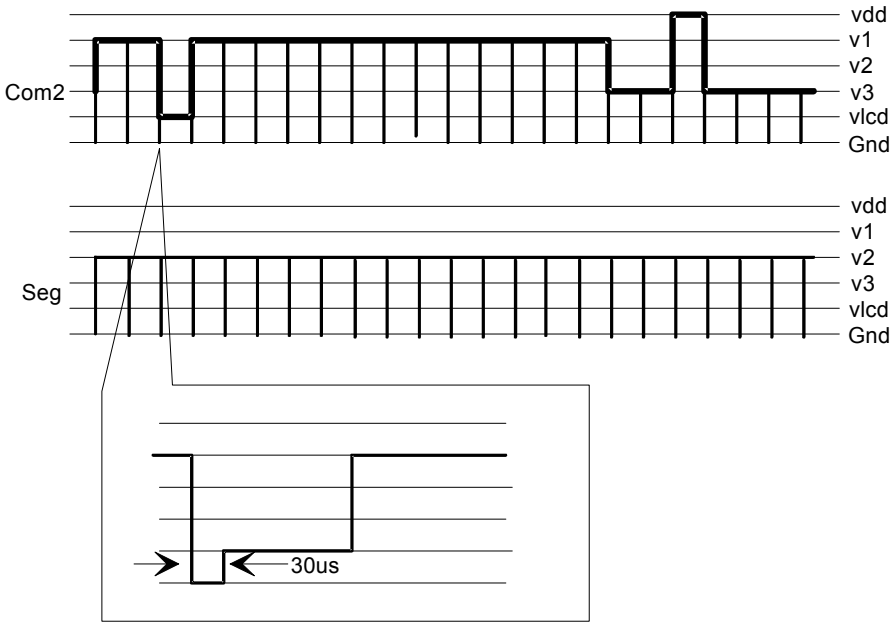


Fig. 8 Key Scan Signal

Bit 1: Port 7 PULL HIGH register option. Use default value.

Bit 2~4: (BIAS1~BIAS3) Control bits are used to choose LCD operation voltage.

BIAS3	BIAS2	BIAS1	LCD Vop (VDD=5V)	LCD Vop(VDD=3V)	Ratio
0	0	0	2.900V	1.740V	0.580 VDD
0	0	1	3.125V	1.875V	0.625 VDD
0	1	0	3.435V	2.061V	0.687 VDD
0	1	1	3.750V	2.250V	0.750 VDD
1	0	0	4.060V	2.436V	0.812 VDD
1	0	1	4.425V	2.655V	0.885 VDD
1	1	0	4.735V	2.841V	0.947 VDD
1	1	1	5.000V	3.000V	1.000 VDD

Bit 5: (P6S) Port 6 switch
0: Normal I/O port
1: Common output of LCD

Bit 6: (P9SL) Port 9 low nibble switch
0: Normal I/O port
1: Segment output of LCD

Bit 7: (P9SH) Port 9 high nibble switch
0: Normal I/O port
1: Segment output of LCD

Page 1 (Port 7 Open Drain, Counter 1/2 Clock Source, Counter 1 Pre-Scaler)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OP77	OP76	C2S	C1S	PSC1	PSC0	0	0

Bit 0: Unused.

Bit 1: Unused.

Bit 2 ~ 3: (PSC0~PSC1) Counter1 prescaler, reset=(0,0)

PSC1	PSC0	Counter 1 Rate
0	0	1:1
0	1	1:4
1	0	1:8
1	1	Reserved

Bit 4: (C1S) Counter 1 source.
0: 32768Hz / RC
1: 3.579MHz, if enable PLL (Crystal mode)

Bit 5: (C2S) Counter 2 source. Scale=1:1
0: 32768Hz / RC
1: 3.579MHz, if enable PLL (Crystal mode)

Bit 6: (OP76) P76 open-drain control
0: Disable
1: Enable

Bit 7**:** (OP77) P77 open-drain control
0: Disable
1: Enable

6.2.13 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT3	0	CNT2	CNT1	INT2	INT1	INT0	TCIF

Bit 0 ~ 5, 7**:** Interrupt enable bit.
0: Disable interrupt
1: Enable interrupt

Bit 6**:** Reserved. Clear the bit to '0'

IOCF register is readable and writable.

6.3 TCC/WDT Pre-Scaler

- An 8-bit counter is available as prescaler for the TCC or WDT. The pre-scaler is available only to either the TCC or WDT at a time.
- An 8-bit counter is available for TCC or WDT as determined by the status of Bit 3 (PAB) of CONT register.
- The prescaler ratio is described in Section 6.2.2 *CONT (Control Register)*.
- The TCC/WDT circuit diagram is shown in Fig. 9 below.
- Both TCC and prescaler are cleared by instructions.
- The prescaler will be cleared by the WDTC and SLEP instructions when running in WDT mode.
- However, prescaler will not be cleared by SLEP instruction when running in TCC mode.

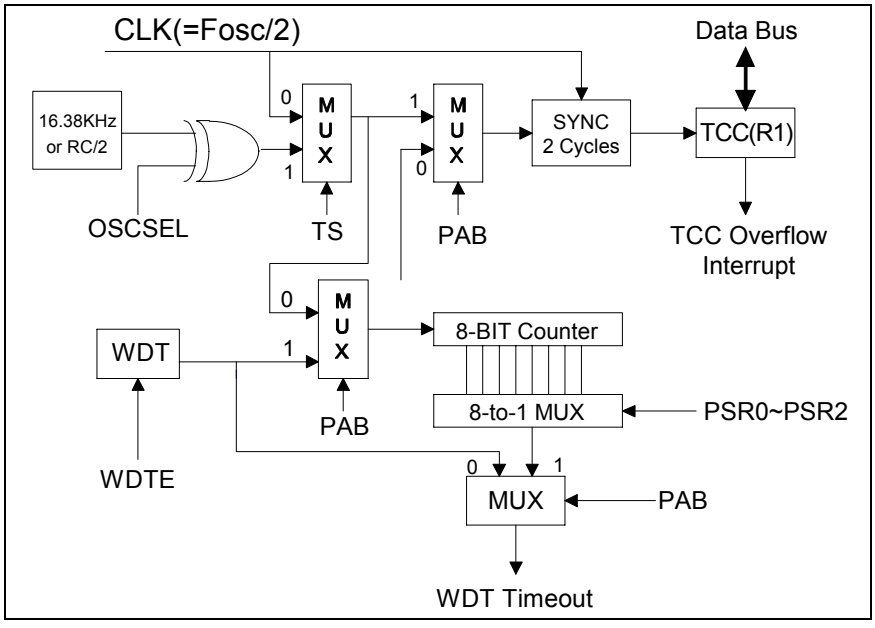


Fig. 9 TCC WDT Block Diagram

6.4 I/O Ports

The I/O registers, (Port 5, Port 6, Port 7, Port 8, and Port 9), are bi-directional tri-state I/O ports. Port 7 can be pulled-high internally by software. Furthermore, P7.6 and P7.7 has its open-drain output also defined through software. Port 9 features an input status changed wake-up function. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC9). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits are shown in Fig. 10 below.

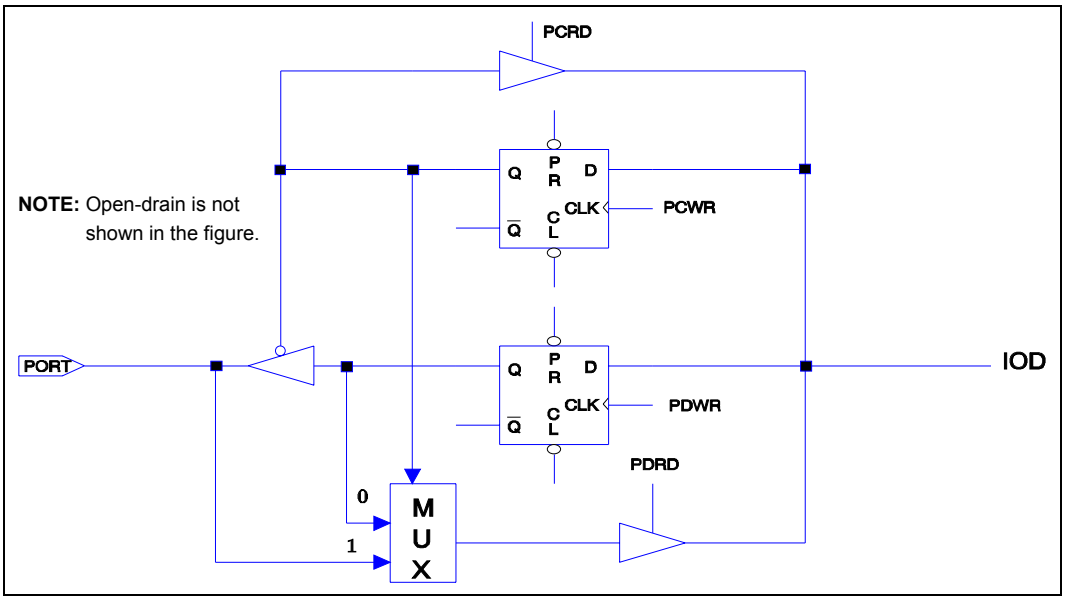


Fig. 10 Port 5, Port 6, Port 7, & Port 8 I/O Port and I/O Control Register Circuit

6.5 RESET and Wake-Up

RESET will occur during any of the following conditions:

- Power on reset
- WDT timeout (if WDT is enable during SLEEP, GREEN, or NORMAL mode)
- /RESET pin pull low

Once a RESET occurs, the following functions are performed:

- The oscillator will continue running
- The Program Counter (R2) is set to all "0"
- All I/O port pins are configured to input mode (high-impedance state)
- The TCC/Watchdog timer and pre-scaler are cleared
- The Watchdog timer is disabled
- When power is switched on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared
- The bits of the CONT register are set to all "1"

■ For other registers (Bit7 & Bit 0), refer below:

R5 = PORT	IOC5 = "11110000"	
R6 = PORT	IOC6 = "11111111"	
R7 = PORT	IOC7 = "11111111"	
R8 = PORT	IOC8 = "11111111"	
R9 = PORT	IOC9 = "11111111"	
RA = "x00x0xxx	IOCA = "00000000"	
RB = "11111111"	Page0 IOCB = "00000000"	Page1 IOCB = "00000000"
RC = "00000000"	Page0 IOCC = "0xxxxxxx"	Page1 IOCC = "00000000"
RD = "xxxxxxxx"	Page0 IOCD = "00000000"	Page1 IOCD = "00000000"
RE = "00000000"	Page0 IOCE = "00000000"	Page1 IOCE = "00000000"
RF = "00000000"	IOCF = "00000000"	

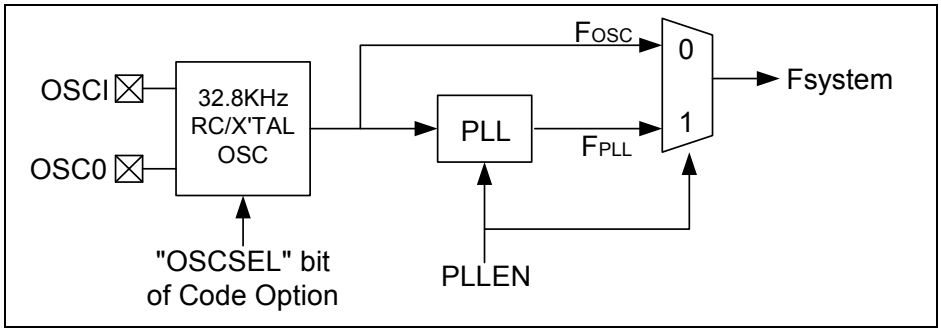
The controller can be awakened from Sleep mode and Idle mode. The wake-up signals are listed below.

Wake-Up Signal	Sleep Mode RA(7,6)=(0,0) + SLEP	Idle Mode RA(7,6)=(1,0) + SLEP	Green Mode RA(7,6)=(x,0) No SLEP	Normal Mode RA(7,6)=(x,1) No SLEP
TCC time out IOCF bit0=1	X	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt
INT0 pin IOCF bit1=1	X	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt
INT1 pin IOCF bit2=1	X	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt
INT2 pin IOCF bit3=1	X	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt
INT3 pin IOCF bit7=1	X	Wake-up + Interrupt + Next instruction	Interrupt	Interrupt
Port9 (input status change wake-up)	RESET	Wake-up + Next instruction	X	X
WDT time out	RESET	Wake-up+ next instruction	RESET	RESET

X=No function

6.6 Oscillator

The oscillator system is used to generate the device clock. The oscillator system is composed of an RC or crystal oscillator and a PLL oscillator as shown in the diagram below.



NOTE: Under RC oscillator mode, the pull-up resistor that connects to OSCI pin and OSC0 pin should be floating.

Under 32768Hz crystal oscillator mode, the crystal is connected between OSCI pin and OSCO pin. A 20~30pF capacitor should be connected between each of the pins and ground.

In Crystal mode, if the RA (Bit 6)=1, the system clock frequency can be tuned to 3.579MHz. The initial value of OSCSEL bit is fixed at '1' (crystal oscillator).

Fig. 11 Oscillator and PLL Function Block.

6.7 Interrupt

The EM78869 IC has two types internal interrupts which are falling edge triggered**:**

- TCC timer overflow interrupt (internal)
- Two 8-bit counters overflow interrupt

If these interrupt sources change signal from high to low, the RF register will generate '1' flag to corresponding register if IOCF register is enabled.

RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the RF register.

NOTE

The interrupt flag bit must be cleared in software before leaving the interrupt service routine in order to prevent and avoid recursive interrupts.

There are four external interrupt pins, i.e., INT0, INT1, INT2, & INT3, and three internal interrupts available**:**

- External interrupt signals (INT0, INT1, INT2, and INT3) are from Port 7 Bit 0 to Bit 3. If IOCF is enabled, then these signals will activate interrupt. Otherwise, these signals will be treated as general input data.
- Internal signals include TCC, CNT1, and CNT2.

After reset, the next instruction will be fetched from Address 000H, and the hardware interrupt is 008H.

After timeout, TCC will go to Address 008H when in GREEN mode or NORMAL mode. When in SLEEP mode, TCC will run the next instruction after "SLEP" instruction. These two conditions will set a RF flag.

NOTE

It is very important to save ACC, R3 and R5 when processing an interruption as illustrated below:

Address	Instruction	Remarks
0x08	DISI	; Disable interrupt
0x09	MOV A_BUFFER, A	; Save ACC
0x0A	SWAP A_BUFFER	
0x0B	SWAPA 0x03	; Save R3 status
0x0C	MOV R3_BUFFER, A	
0x0D	MOV A, 0x05	; Save ROM page register
0x0E	MOV R5_BUFFER, A	
:	:	
:	:	
:	MOV A, R5_BUFFER	; Return R5
:	MOV 0X05,A	
:	SWAPA R3_BUFFER	; Return R3
:	MOV 0X03,A	
:	SWAPA A_BUFFER	; Return ACC
:	RETI	

6.8 LCD Driver

The data bank IC can drive LCD directly and has 40 segments and 9 commons that can drive a total of 40*9 dots. LCD block is made up of LCD driver; display RAM, segment output pins, common output pins, and LCD operating power supply pins.

Duty, bias, the number of segment, the number of common, and frame frequency are determined by LCD mode register and LCD control register.

The basic structure contains a timing control which uses the basic frequency 32.768KHz or RC to generate the proper timing for different duty and display access. RE register is a command register for LCD driver. The LCD display (disable, enable, & blanking) is controlled by LCD_C and the driving duty and bias is decided by LCD_M. The display data is stored in data RAM which address and data access are controlled by registers IOCB and IOCC.

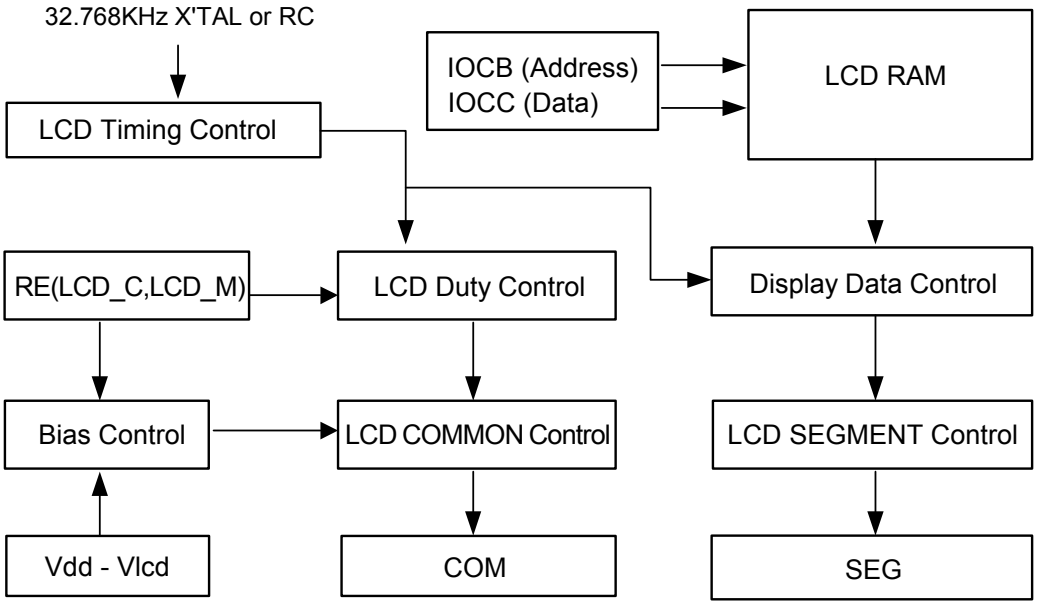


Fig. 12 LCD Driver Control Block

6.8.1 LCD Driver Control

LCD Driver, WDT Control (RE)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	/WDTE	/WUP9H	/WUP9L	0	LCD_C2	LCD_C1	LCD_M

Bit 0: (LCD_M) LCD_M decides the methods, including duty.

Bit 1~2: (LCD_C#) decides the LCD display enable or blanking.

LCD_C2	LCD_C1	LCD_M	LCD Display Control	Duty	Bias
0	0	0	Change duty	1/9	1/4
0	0	1	Disable (turn off LCD)	1/8	1/4
0	1	0	Blanking	1/9	1/4
0	1	1	Blanking	1/8	1/4
1	0	0	X	1/9	1/4
1	0	1	X	1/8	1/4
1	1	0	LCD display enable	1/9	1/4
1	1	1	LCD display enable	1/8	1/4

6.8.2 LCD Display Area

The LCD display data is stored in the data RAM. The relation between data area and COM/SEG pin is as shown below:

SEGMENT	IOCC (COM7 ~ COM0)								IOCB (Address)	Remarks
Unused	X	X	X	X	X	X	X	X	00 H	
Unused	X	X	X	X	X	X	X	X	01 H	
:	:								:	
:	:								:	
SEG 20									14H	1/8 DUTY
SEG 21									15H	
:										
:										
SEG 58									3AH	
SEG 59									3BH	
Unused									3CH	
Unused									:	
Unused									3FH	
SEGMENT	**IOCC (COM 8)**								**IOCB (Address)**	**Remarks**
Unused	X								40H	
Unused	X								41H	
:	:									
SEG 20									54H	1/9 DUTY
SEG 21									55H	
:										
:										
SEG 58									7AH	
SEG 59									7BH	
Unused	X								7CH	
:	:								:	
Unused	X								7FH	

Page 0 (LCD Address, Counter 1 Preset Register (IOCB))

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	LCDA6	LCDA5	LCDA4	LCDA3	LCDA2	LCDA1	LCDA0

Bit 0 ~ 6**:** (LCDA0~LCDA6) LCD address

Bit 7**:** Unused. Fixed at '0'

NOTE
Write only when LCD is enabled. Read/Write when disabled.

Page 0 (LCD Data, Counter 2 (IOCC))

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDD7	LCDD6	LCDD5	LCDD4	LCDD3	LCDD2	LCDD1	LCDD0

Bit 0 ~7**:** (LCDD0~LCDD7) LCD RAM data register

6.8.3 LCD COM and SEG Signal

COM Signal**:** The number of COM pins varies according to the duty cycle in use as shown in the following table. In 1/8 Duty mode COM8 must be opened. In 1/9 Duty mode COM0 ~ COM8 pins must be used.

Duty	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8
1/8	O	O	O	O	O	O	O	O	X
1/9	O	O	O	O	O	O	O	O	O

X = open, O = select

SEG Signal**:** The 40 segment signal pins are connected to the corresponding display RAM address 14h to 3Bh. When Duty mode is at 1/8, the required data address are only those from Com0 ~ Com7 (located within 14h ~ 3Bh). However, when Duty mode is at 1/9, all data address from Com0 ~ Com7 (located within 14h ~ 3Bh) and Com8 (located within 54h ~ 7Bh) are needed.

When a bit of display RAM is 1, a select signal is sent to the corresponding segment pin, and when the bit is 0, a non-select signal is sent to the corresponding segment pin.

COM, SEG, and Select/Non-Select signals are illustrated below.

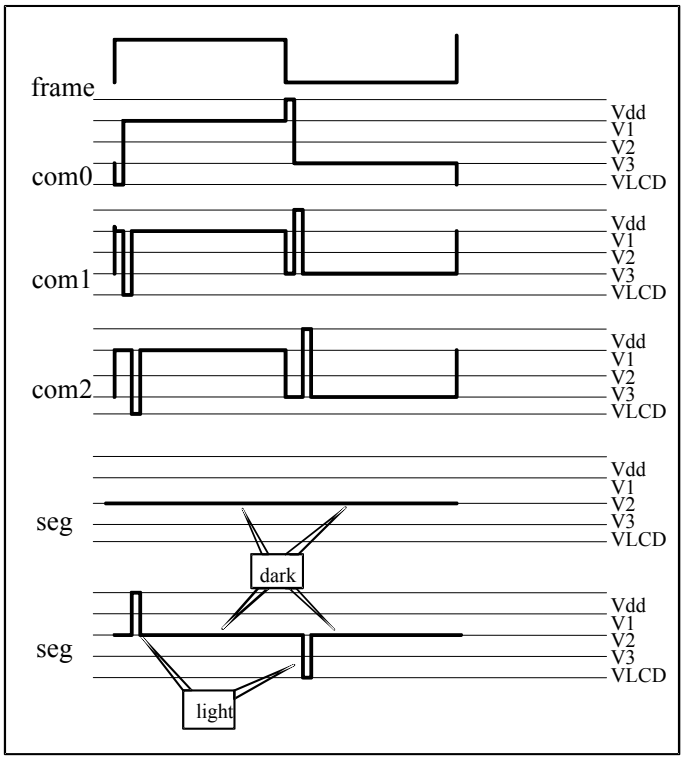


Fig.13 LCD Waveform 1/4 Bias

6.8.4 LCD Bias Control

Bias Control Register (IOCE)

Page 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P9SH	P9SL	P6S	BIAS3	BIAS2	BIAS1	0	SC

Bit 2 ~ 4**:** (BIAS1~BIAS3) Control bits used to choose LCD operation voltage. See Fig. 14 below for the applicable circuit diagram.

BIAS3	BIAS2	BIAS1	LCD Vop (VDD=5V)	LCD Vop(VDD=3V)	Ratio
0	0	0	2.900V	1.740V	0.580 VDD
0	0	1	3.125V	1.875V	0.625 VDD
0	1	0	3.435V	2.061V	0.687 VDD
0	1	1	3.750V	2.250V	0.750 VDD
1	0	0	4.060V	2.436V	0.812 VDD
1	0	1	4.425V	2.655V	0.885 VDD
1	1	0	4.735V	2.841V	0.947 VDD
1	1	1	5.000V	3.000V	1.000 VDD

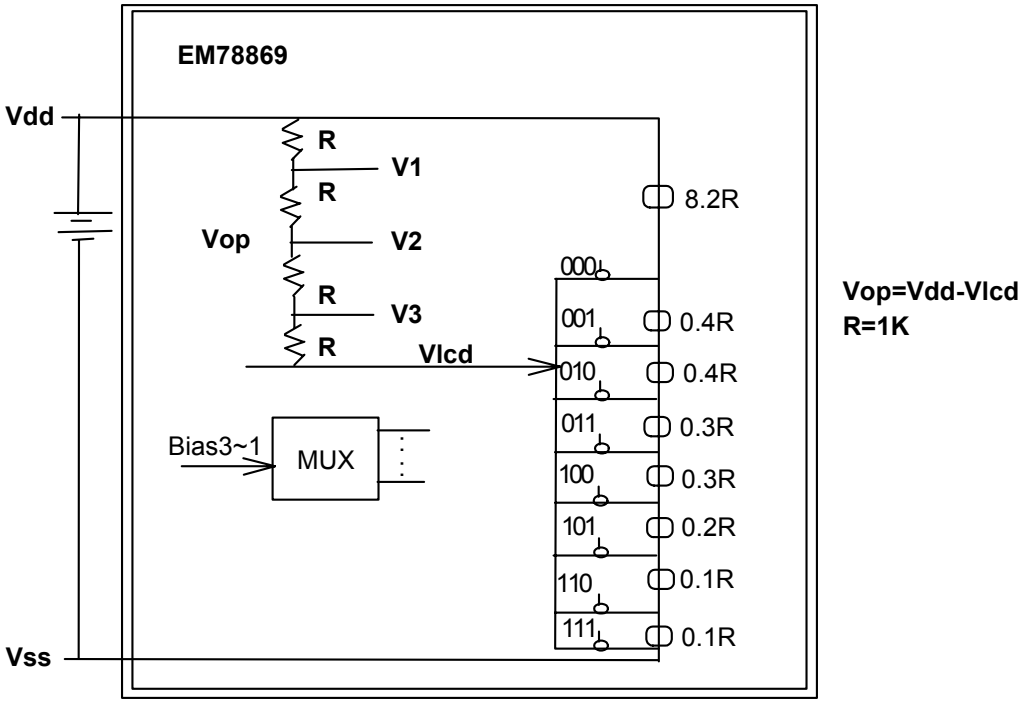


Fig.14 LCD bias circuit

6.9 Code Options

Bit 2	Bit 1	Bit 0
OSCSEL	ELCD	MCLK

The EM78869 IC has one CODE option register that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

Bit 0**:** Main clock selection

0: 3.58MHZ

1: 1.84MHZ

Bit 1 LCD driving current selection

0: LCD resistance low impedance. Provides more current to LCD.

1: LCD resistance high impedance. Saves power consumption.

Bit 2 (OSCSEL)**:** Select RC or crystal oscillator

0: RC oscillator

1: Crystal oscillator

The RC or crystal oscillator is selected by OSCSEL bit of code option.

6.10 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods). Unless the program counter is changed by instructions "MOV R2, A," "ADD R2, A," or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2, A," "BS(C) R2, 6," "CLR R2," etc.). Under this condition, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows**:**

a) Change one instruction cycle to consist of 4 oscillator periods.

b) Execute within two instruction cycles, "JMP," "CALL," "RET," "RETL," & "RETI," or the conditional skip ("JBS," "JBC," "JZ," "JZA," "DJZ," & "DJZA") instructions which were tested to be true. Also execute within two instruction cycles the instructions that are written to the program counter.

Furthermore, the instruction set has the following features**:**

- Every bit of any register can be set, cleared, or tested directly.
- The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" in the instruction set represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. "B" represents a bit field designator that selects the value for the bit, which is located in the register "R", and affects operation. "K" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None [1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None [1]
0 0000 0010 0000	0020	TBL	R2+A → R2, Bits 8~9 of R2 unchanged	Z, C, DC
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R [2]	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R (R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 (A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 (R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 (A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 (R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) (A(n-1), R(0) (C, C (A(7)	C

[1] This instruction is applicable to IOC5 ~ IOC9, IOCA, IOCB, IOCC, IOCD, IOCE, & IOCF only.
[2] Source and destination must be the same.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0110 01rr rrrr	06rr	RRC R	R(n) (R(n-1), R(0) (C, C (R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) (A(n+1), R(7) (C, C (A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) (R(n+1), R(7) (C, C (R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) (A(4-7), R(4-7) (A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) (R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 (A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 (R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 (R(b)	None [3]
0 101b bbrr rrrr	0xxx	BS R,b	1 (R(b)	None [4]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 ([SP], (Page, k) (PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) (PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k (A	None
1 1001 kkkk kkkk	19kk	OR A,k	A (k (A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k (A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A (k (A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k (A, [Top of Stack] (PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A (A	Z, C, DC
1 1110 0000 0010	1E02	INT	PC+1 ([SP], 002H (PC	None
1 1110 1000 0kkk	1E8k	PAGE k	k->R5(2:0)	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A (A	Z, C, DC

[3] This instruction is not recommended for RF operation.
[4] This instruction cannot operate under RF.

7 Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltage	Vdd	–0.3 to 6	V
Input Voltage	Vin	–0.5 to Vdd +0.5	V
Operating Temperature Range	Ta	–20 to 70	C

8 DC Electrical Characteristics

(Ta=0°C ~ 70°C, VDD=5V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Type	Max	Unit
IIL1	Input Leakage Current for input pins	VIN = VDD, VSS	-	-	±1	μA
IIL2	Input Leakage Current for bi-directional pins	VIN = VDD, VSS	-	-	±1	μA
VIH	Input High Voltage	-	2.5	-	-	V
VIL	Input Low Voltage	-	-	-	0.8	V
VIHT	Input High Threshold Voltage	/RESET, TCC, RDET1	2.0	-	-	V
VILT	Input Low Threshold Voltage	/RESET, TCC,RDET1	-		0.8	V
VIHX	Clock Input High Voltage	OSCI	3.5	-	-	V
VILX	Clock Input Low Voltage	OSCI	-		1.5	V
VHscan	Key scan Input High Voltage	Port 6 for key scan	3.5	-	-	V
VLscan	Key scan Input Low Voltage	Port 6 for key scan	-	-	1.5	V
VOH1	Output High Voltage (Port 6, 7, 8)	IOH = –1.6mA	2.4	-	-	V
	(Port 9)	IOH = –6.0mA	2.4	-	-	V
VOL1	Output Low Voltage (Port6, 7, 8)	IOL = 1.6mA	-	-	0.4	V
	(Port 9)	IOL = 6.0mA	-	-	0.4	V
Vlcd	LCD drive reference voltage	Contrast adjustment	-	-	2.2	V
IPH	Pull-high current	Pull-high active input pin at VSS	-	–10	–15	μA
ISB1	Power down current (SLEEP mode)	All input and I/O pin at VDD, output pin floating, WDT disabled	-	0.5	1	μA
ISB2	Power down current (IDLE mode)	All input and I/O pin at VDD, output pin floating, WDT disabled, LCD enabled	-	38	65	μA
ISB3	Low clock current (GREEN mode)	CLK=32.768KHz, all input and I/O pin at VDD, output pin floating, WDT disabled, LCD enabled	-	58	80	μA
ICC	Operating supply current (NORMAL mode)	/RESET=High, CLK=3.579MHz, output pin floating, LCD enabled	-	900	1000	μA

(Ta=0°C ~ 70°C, VDD=3V±5%, VSS=0V)

Symbol	Parameter	Condition	Min	Type	Max	Unit
ISB1	Power down current (SLEEP mode)	All input and I/O pin at VDD, output pin floating, WDT disabled		0.5	1	μA
ISB2	Power down current (IDLE mode)	All input and I/O pin at VDD, output pin floating, WDT disabled, LCD enabled		18	25	μA
ISB3	Low clock current (GREEN mode)	CLK=32.768KHz, all input and I/O pin at VDD, output pin floating, WDT disabled, LCD enabled		25	35	μA
ICC	Operating supply current (NORMAL mode)	/RESET=High, CLK=3.579MHz, output pin floating, LCD enable		450	680	μA

9 AC Electrical Characteristics

(Ta=0°C ~ 70°C, VDD=5V, VSS=0V)

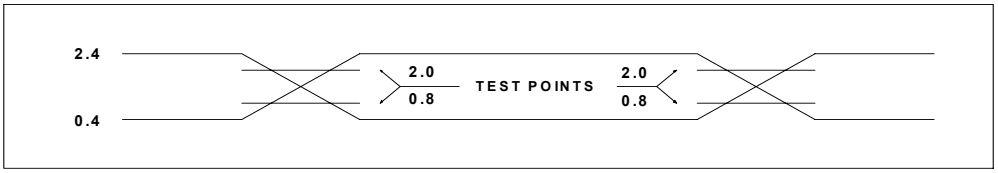
Symbol	Parameter	Conditions	Min	Type	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time	32.768K 3.579M		60 550		μs ns
Tdrh	Device delay hold time			18		ms
Ttcc	TCC input period	*	(Tins+20)/N			ns
Twdt	Watchdog timer period	Ta = 25°C		18		ms

*N= selected prescaler ratio.

Description	Symbol	Min	Type	Max	Unit
OSC start up(32.768KHz) (3.579MHz PLL)	Tosc	--		400 10	ms

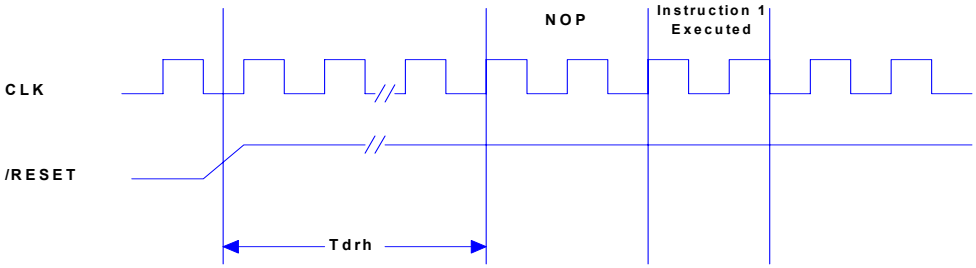
10 Timing Diagram

AC Test Input/Output Waveform

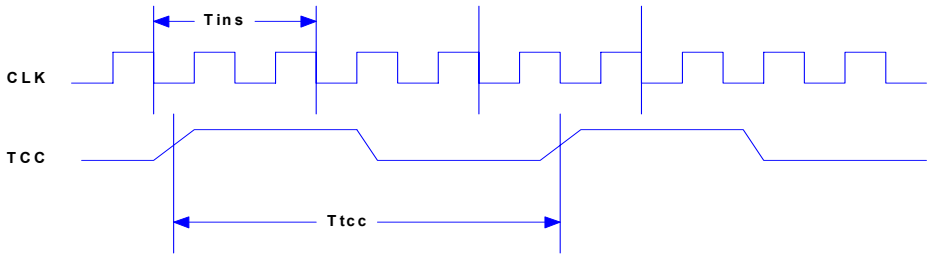


AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



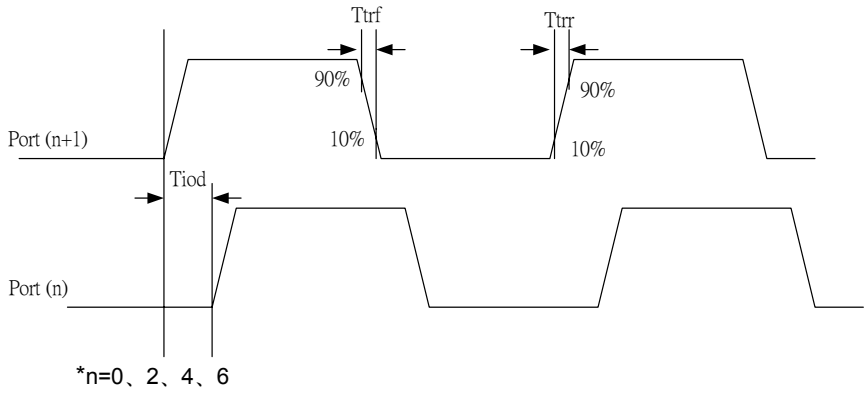


Fig. 15 AC Timing

11 Application Circuit

11.1 Application with Crystal Mode

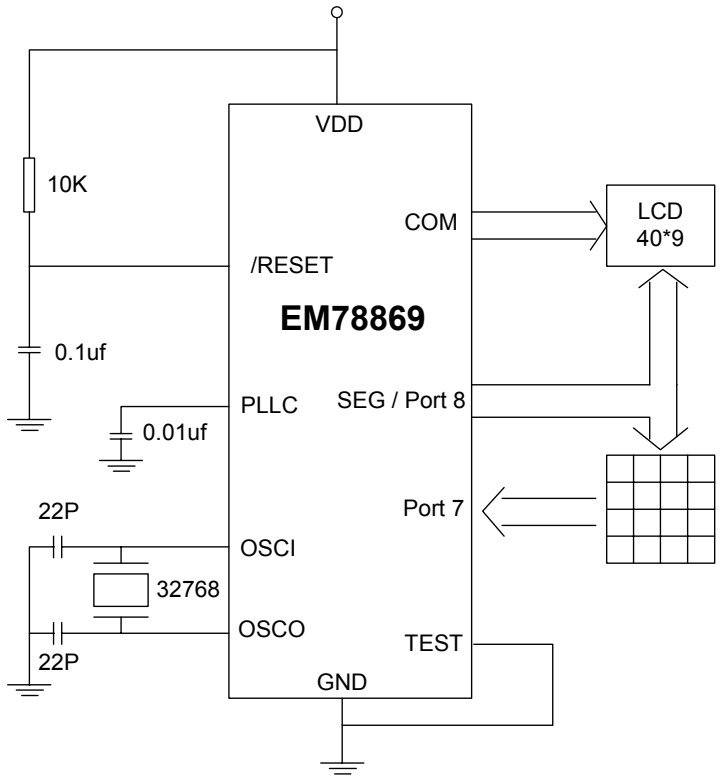


Fig 16. Application with Crystal Mode

11.2 Application with RC Mode

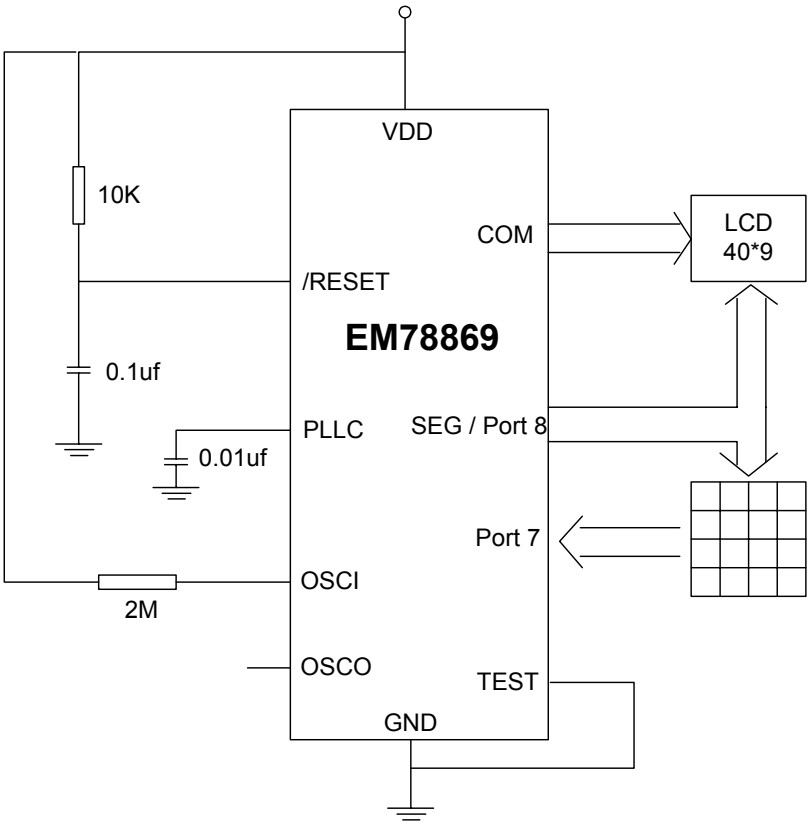


Fig 17. Application with RC Mode