EM78P468N

8-BIT Microcontroller

Product Specification

DOC. VERSION 1.2

ELAN MICROELECTRONICS CORP.

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Specification Revision History		
Version	Revision Description	Date
1.0	Initial version	2004/04/10
1.1	1. Add DC curve vs. Temperature. 2. Remove LVD function	2004/12/09
1.2	1. Add LQFP Package	2005/03/15

1 GENERAL DESCRIPTION

This LSI is an 8-bit RISC type microprocessor with high speed CMOS technology and low power consumption. Integrated onto a single chip are on chip watchdog timer (WDT), Data RAM, ROM, programmable real time clock counter, internal/external interrupt, power down mode, LCD driver, infrared transmitter function, and tri-state I/O. The EM78P468N provides multi-protection bits to protect against intrusion of user's code in the OTP memory and a seven option bits to accommodate user's requirements. It also provides an especial 13 bits customer ID option.

With its OTP-ROM feature, this LSI offers a convenient way of developing and verifying user's programs. Moreover, user developed code can be easily programmed with the ELAN writer.

2 FEATURES

2.1 CPU

- Operating voltage and temperature range:
  - Commercial: 2.2V ~ 5.5 V. (at 0℃~+70℃)
  - Industrial: 2.5V ~ 5.5 V. / (at -40℃~+85℃)
- Operation speed: DC ~ 10MHz clock input.
- Dual clock operation
  - High frequency oscillator can select among Crystal, RC, or PLL (phase lock loop)
  - Low frequency oscillator can select between Crystal or RC mode
- Totally 272 bytes SRAM
  - 144 bytes general purpose register
  - 128 bytes on chip data RAM
- 4K*13 bits OTP - ROM (One Time Programmable - Read Only Memory)
- Up to 28 bi-directional tri-state I/O ports
  - Typically, 12 bi-directional tri-state I/O ports.
  - 16 bi-directional tri-state I/O ports shared with LCD segment output pin.
- 8-level stack for subroutine nesting
- 8-bit real time clock/counter (TCC)
- One infrared transmitter/PWM generator function

- Four sets of 8 bits auto reload down-count timer can be used as interrupt sources
  - Counter 1: independent down-count timer
  - Counter 2, High Pulse Width Timer (HPWT), and Low Pulse Width Timer (LPWT) shared with IR function.
- Programmable free running on chip watchdog timer (WDT). This function can operate on Normal, Green and Idle mode.
- Operation modes:
  - Normal mode: The CPU operated on frequency of main oscillator (Fm)
  - Green mode: The CPU operated on frequency sub-oscillator (Fs) and main oscillator (Fm) stop.
  - Idle mode: CPU idle, LCD display remains working
  - Sleep mode: whole chip stop working.
- Input port wake up function (PORT6, PORT8). Working on Idle and leep mode.
- Eight interrupt sources, three external and five internal.
  - Internal interrupt source : TCC; Counter 1,2; High/Low pulse width timer.
  - External interrupt source : INT0, INT1 and Pin change wake-up (Port 6 and Port 8)
- Packages:
  - Dice form : 59 pin
  - QFP-64 pin : EM78P468NQ (Body 14mm*20mm)
  - LQFP-64 pin : EM78P468NAQ (Body 7mm*7mm)
  - LQFP-44 pin : EM78P468NBQ (Body 10mm*10mm)
  - QFP-44 pin : EM78P468NCQ (Body 10mm*10mm)

2.2 LCD Circuit

- Common driver pins: 4
- Segment driver pins: 32
- LCD Bias: 1/3, 1/2 bias
- LCD Duty: 1/4, 1/3, 1/2 duty

2.3 Applications

- Remote control for air conditioner
- Health care
- Home appliances

3 PIN ASSIGNMENTS

3.1 QFP - 64

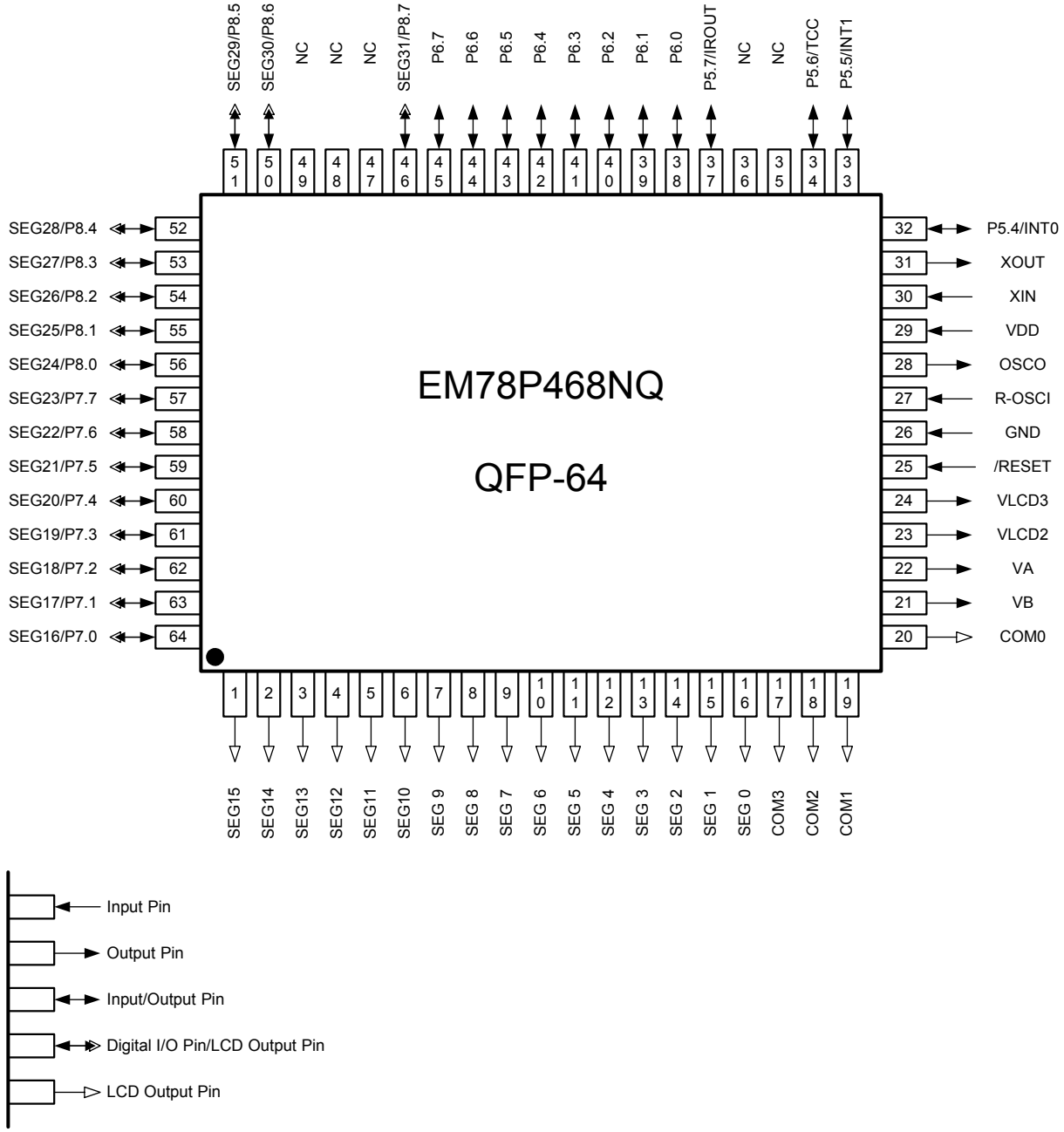


Fig. 1-(a) Pins Configuration for 64 Pin QFP Package

3.2 LQFP - 64

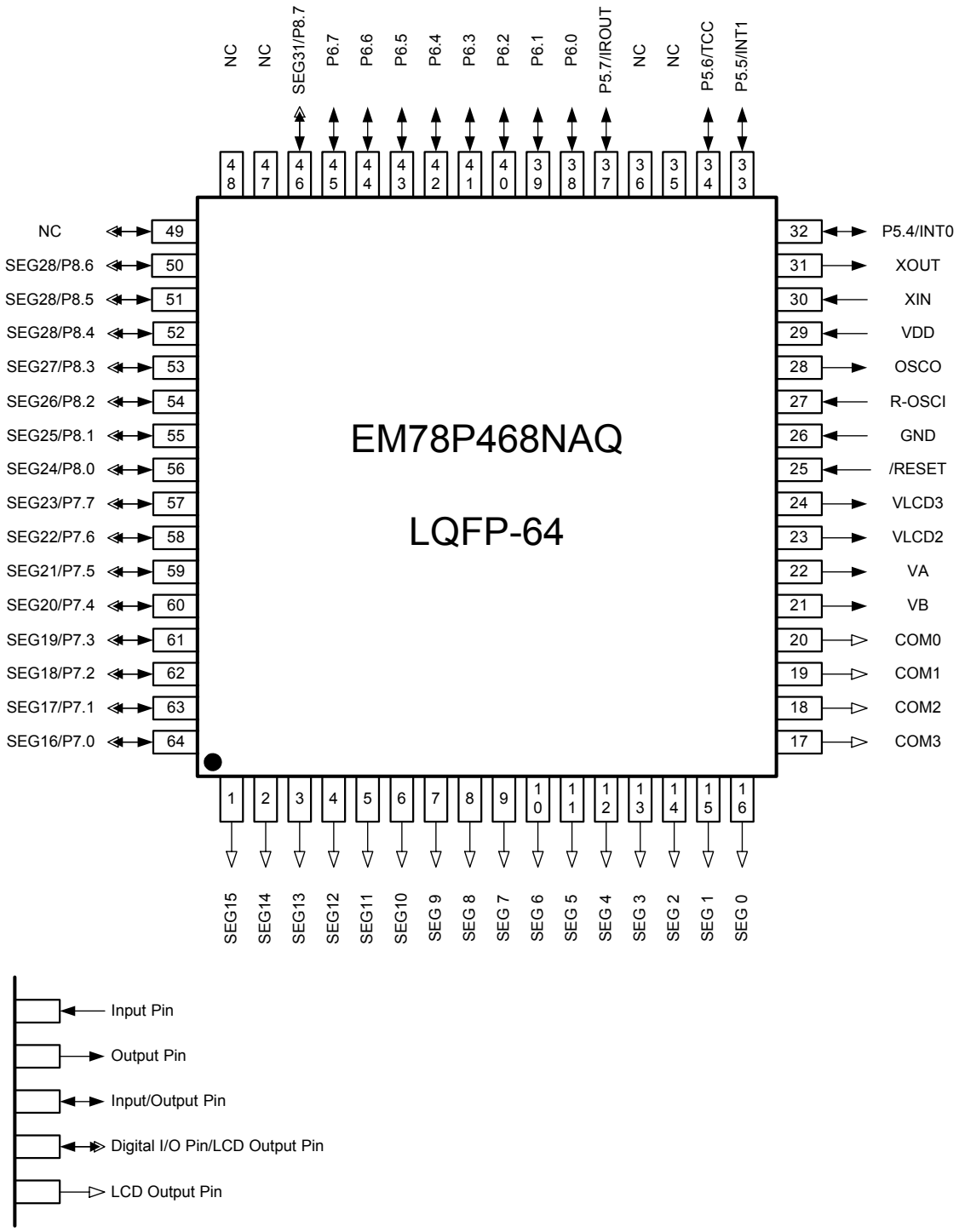


Fig. 1-(b) Pins Configuration for 64 Pin LQFP Package

3.3 LQFP - 44

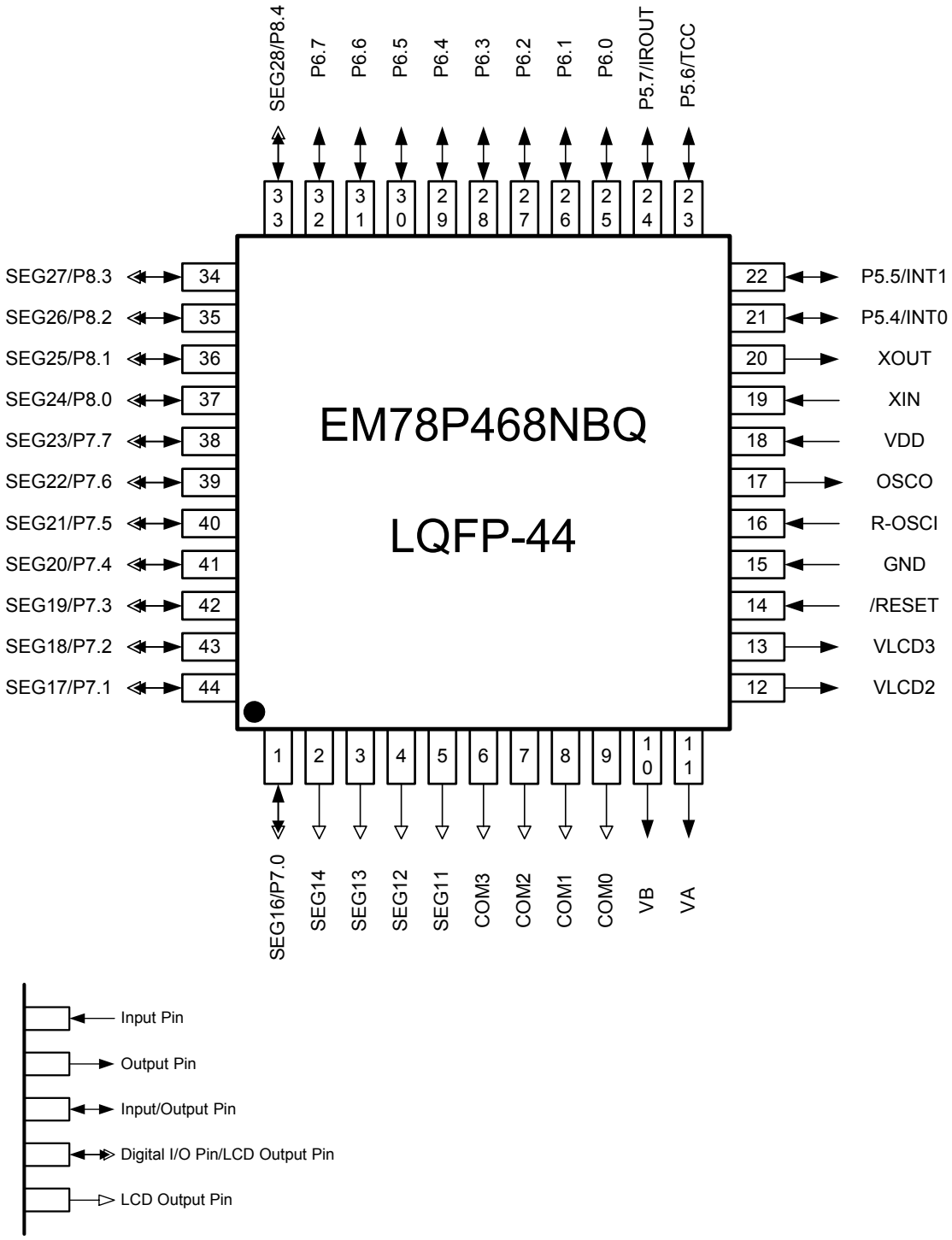


Fig. 1-(c) Pins Configuration for 44 Pin LQFP Package

3.4 QFP - 44

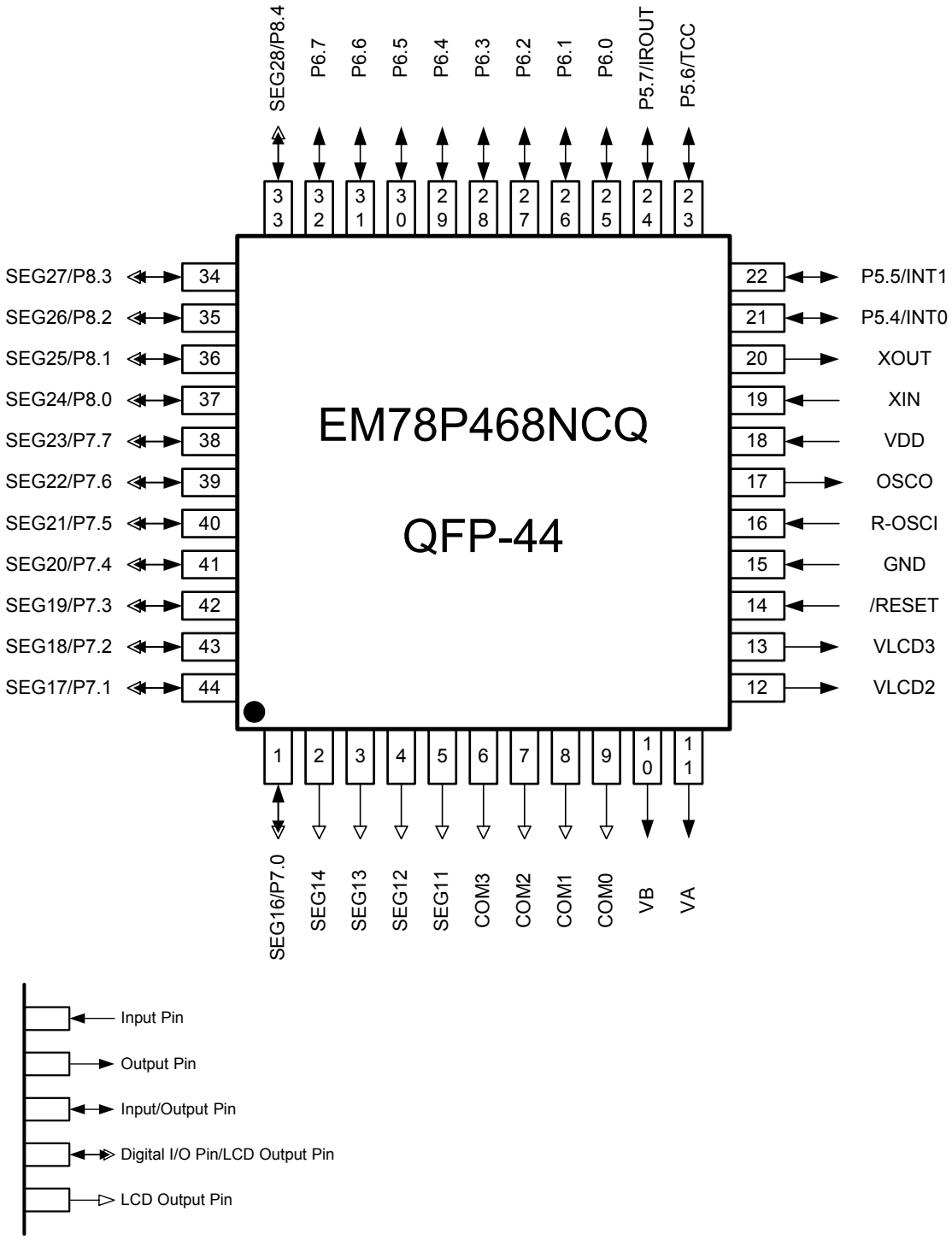


Fig. 1-(d) Pins Configuration for 44 Pin QFP Package

Table 1 (a) Pin Description for Package of QFP64 and LQFP64

PIN	PIN number	I/O type	Description
VDD	29	I	* Power supply pin
GND	26	I	* System ground pin
R-OSCI	27	I	* In crystal mode: crystal input * In RC mode: resistor pull high. * In PLL mode: connect 0.01μF capacitance to GND * Connect 0.01μF capacitor to GND and code option select PLL mode when high oscillator is not use.
OSCO	28	O	* In crystal mode: crystal output * In RC mode: instruction clock output
Xin	30	I	* In crystal mode:Input pin for sub-oscillator. Connect to a 32.768KHz crystal * RC mode: this pin is connected with a resistor to high level.
Xout	31	O	* In crystal: Connect to a 32.768KHz crystal * In RC mode: instruction clock output
/RESET	25	I	* Low active. If set as /RESET and remains at logic low, the devices will be reset
P5.4/INT0	32	I/O	* General purpose I/O pin. /external interrupt. * INT0 interruption source can be set to falling or rising edge by IOC71 register bit 7 (INT_EDGE). * Wake up from sleep mode and idle mode when the pin status changes.
P5.5/INT1	33	I/O	* General purpose I/O pin. /external interrupt. * Interruption source is a falling edge signal. * Wake up from sleep mode and idle mode when the pin status changes.
P5.6/TCC	34	I/O	* General purpose I/O/ external counter input * This pin works in normal/green/idle mode.
P5.7/IROUT	37	I/O	* General purpose I/O pin or IR/PWM mode output pin, * Capable of sinking 20mA/5V.
P6.0 ~ P6.7	38~45	I/O	* General purpose I/O pin. * Pull-high, pull-low and open drain function support. * All pins can wake up from sleep and idle modes when the pin status changes.
COM3~0	17~20	O	* LCD common output pin.
SEG0~SEG15	16~1	O	* LCD segment output pin.
SEG16/P7.0 ~ SEG23/P7.7	64 ~ 57	O/(I/O)	* LCD segment output pin. Can be shared with general purposes I/O pin
SEG24/P8.0 ~ SEG30/P8.6 SEG31/P8.7	56 ~ 50 46	O/(I/O)	* LCD segment output pin. Can be shared with general I/O pin * For general purpose I/O use, can wake up from sleep mode and idle mode when the pin status changes. * For general purposes I/O use, supports pull-high function.
VB	21	O	* Connect capacitors for LCD bias voltage
VA	22	O	* Connect capacitors for LCD bias voltage
VLCD2	23	O	* One of LCD bias voltage
VLCD3	24	O	* One of LCD bias voltage
NC	35~36 47~49		

Table 1 (b) Pin Description for Package of QFP44 and LQFP44

PIN	PIN number	I/O type	Description
VDD	18	I	* Power supply pin
GND	15	I	* System ground pin
R-OSCI	16	I	* In crystal mode: crystal input * In RC mode: resistor pull high. * In PLL mode: connect 0.01μF capacitance to GND * Connect 0.01μF capacitor to GND and code option select PLL mode when high oscillator is not use.
OSCO	17	O	* In crystal mode: crystal output * In RC mode: instruction clock output
Xin	19	I	* In crystal mode:Input pin for sub-oscillator. Connect to a 32.768KHz crystal * RC mode: this pin is connected with a resistor to high level.
Xout	20	O	* In crystal: Connect to a 32.768KHz crystal * In RC mode: instruction clock output
/RESET	14	I	* Low active. If set as /RESET and remains at logic low * the devices will be reset
P5.4/INT0	21	I/O	* General purpose I/O pin. /external interrupt. * INT0 interruption source can be set to falling or rising edge by IOC71 register bit 7 (INT_EDGE). * Wake up from sleep mode and idle mode when the pin status changes.
P5.5/INT1	22	I/O	* General purpose I/O pin. /external interrupt. * Interruption source is a falling edge signal. * Wake up from sleep mode and idle mode when the pin status changes.
P5.6/TCC	23	I/O	* General purpose I/O/ external counter input * This pin works in normal/green/idle mode.
P5.7/IROUT	24	I/O	* General purpose I/O pin or IR/PWM mode output pin, * Capable of sinking 20mA/5V.
P6.0 ~ P6.7	25~32	I/O	* General purpose I/O pin. * Pull-high, pull-low and open drain function support. * All pins can wake up from sleep and idle modes when the pin status changes.
COM3~0	6~9	O	* LCD common output pin.
SEG11~SEG14	5~2	O	* LCD segment output pin.
SEG16/P7.0 SEG17/P7.1 ~ SEG23/P7.7	1 44 ~ 38	O/(I/O)	* LCD segment output pin. Can be shared with general purposes I/O pin
SEG24/P8.0 ~ SEG31/P8.4	37 ~ 33	O/(I/O)	* LCD segment output pin. Can be shared with general I/O pin * For general purpose I/O use, can wake up from sleep mode and idle mode when the pin status changes. * For general purposes I/O use, supports pull-high function.
VB	10	O	* Connect capacitors for LCD bias voltage
VA	11	O	* Connect capacitors for LCD bias voltage
VLCD2	12	O	* One of LCD bias voltage
VLCD3	13	O	* One of LCD bias voltage

4 FUNCTION DESCRIPTION

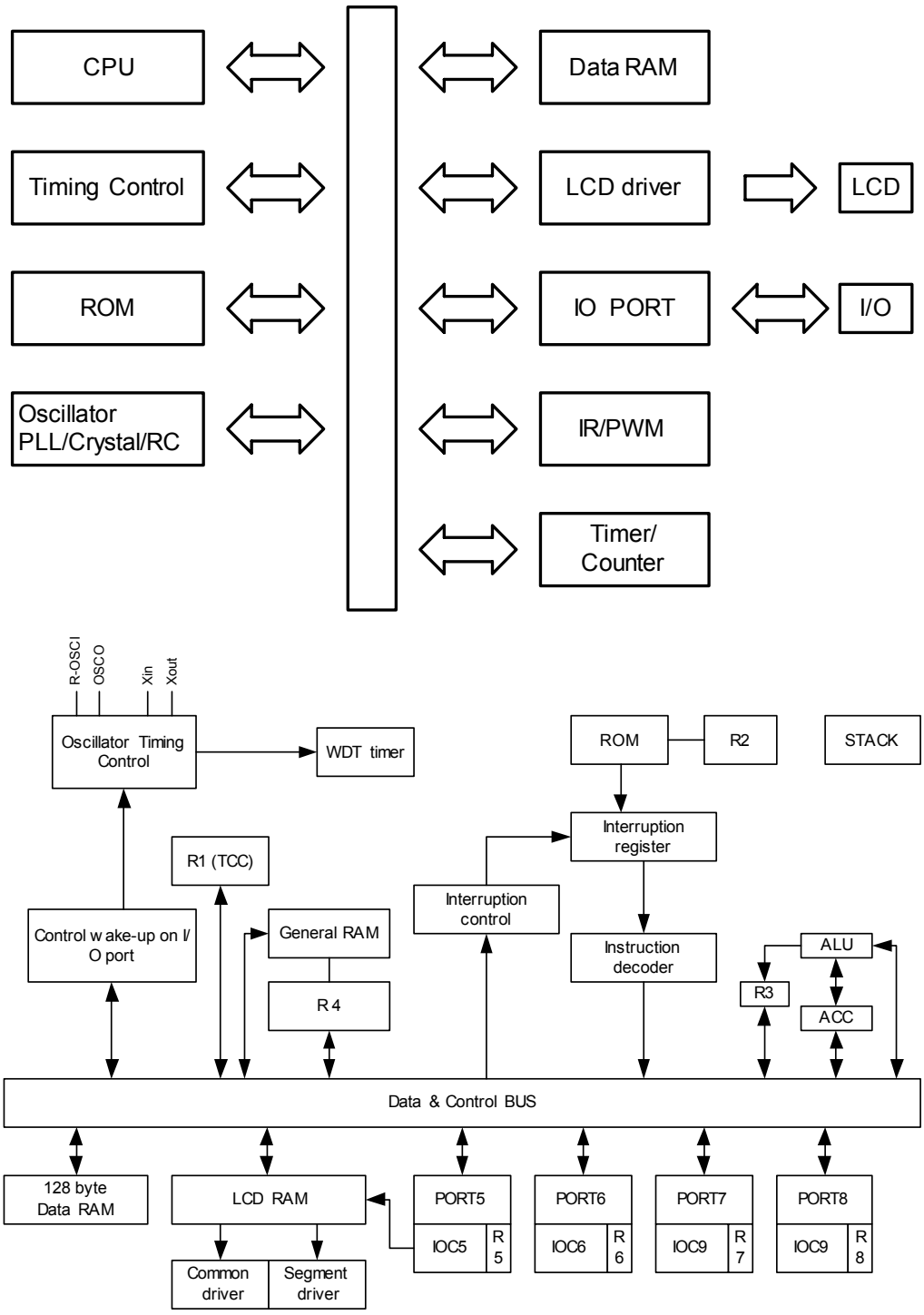


Fig. 2 System Block Diagram

4.1 Operational Registers

4.1.1 R0/IAR (Indirect Addressing Register) (Address: 00h)

R0 is not a physically implemented register. It is used as indirect addressing pointer. Any instruction using R0 as register actually accesses the data pointed by the RAM Select Register (R4).

4.1.2 R1/TCC (Time Clock Counter) (Address: 01h)

Increases by an external signal edge applied to TCC, or by the instruction cycle clock.

Written and read by the program as any other register.

4.1.3 R2/PC (Program Counter) (Address: 02h)

* The structure is depicted in Fig. 3

* Generates 4K × 13 on-chip ROM addresses to the relative programming instruction codes.

* "JMP" instruction allows direct loading of the low 10 program counter bits.

* "CALL" instruction loads the low 10 bits of the PC and PC+1, then push it into the stack.

* "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

* "MOV R2, A" allows the loading of an address from the A register to the PC. The contents of the ninth and tenth bits do not change.

* "ADD R2, A" allows a relative address be added to the current PC.

* The most significant bit (A10~A11) will be loaded with the content of bits PS0~PS1 in the Status register (R3) upon execution of a "JMP" or "CALL" instruction.

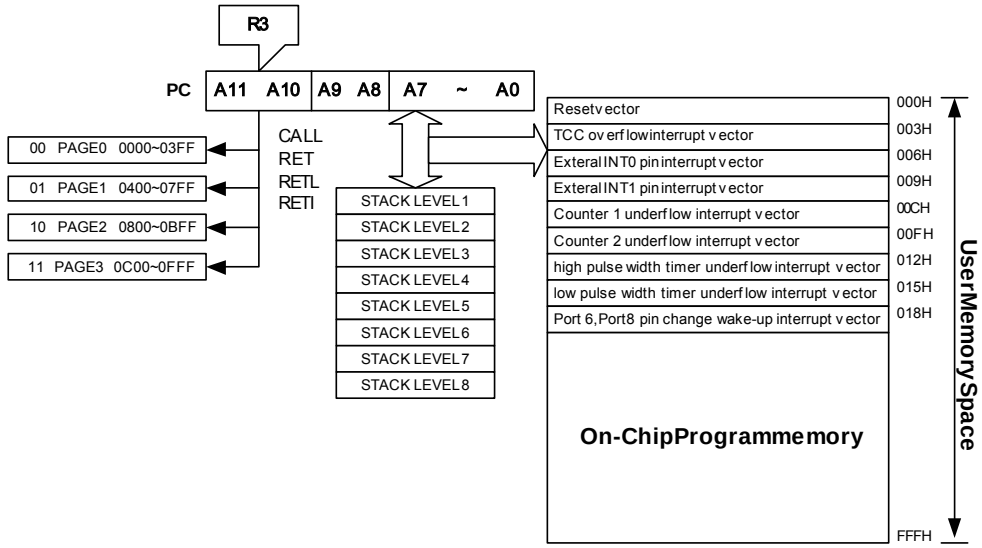


Fig. 3 Program Counter Organization

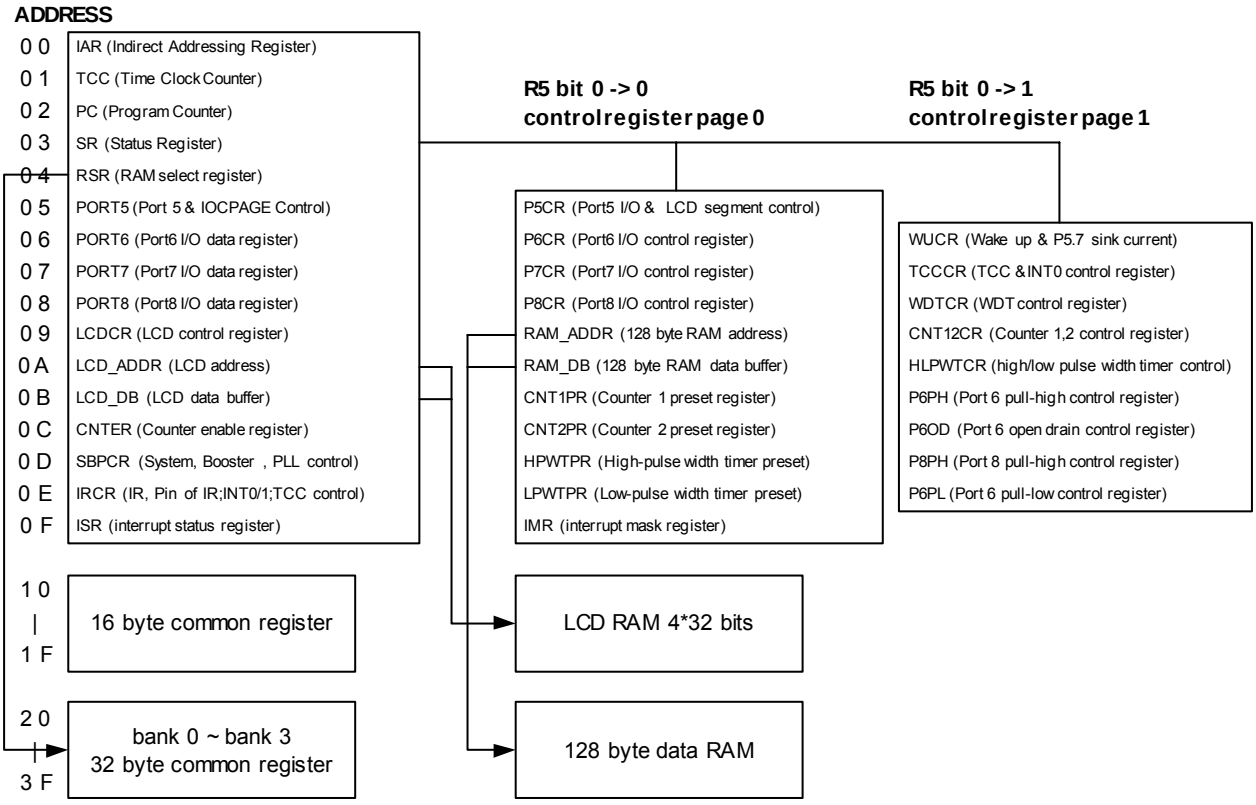


Fig. 4 Data Memory Configuration

4.1.4 R3/SR (Status Register) (Address: 03h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	PS1	PS0	T	P	Z	DC	C

Bit 7 : Not used

Bit 6 ~ 5 (PS1 ~ 0) : Page select bits

PS1	PS0	ROM page (Address)
0	0	Page 0 (000H ~ 3FFH)
0	1	Page 1 (400H ~ 7FFH)
1	0	Page 2 (800H ~ BFFH)
1	1	Page 3 (C00H ~ FFFH)

PS0~PS1 are used to select a ROM page. User can use PAGE instruction (e.g. PAGE 1) or set PS1~PS0 bits to change ROM page. When executing a "JMP", "CALL", or other instructions which causes the program counter to be changed (e.g. MOV R2, A), PS0~PS1 are loaded into the 11th and 12th bits of the program counter where it selects one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS1 bits. That is, the return will always be to the page from where the subroutine was called, regardless of the current setting of PS0~PS1 bits.

Bit 4 (T) : Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands or during power up and reset to 0 by WDT timeout.

EVENT	T	P	REMARK
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	1	1	X: don't care

Bit 3 (P) : Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 2 (Z) : Zero flag

Bit 1 (DC) : Auxiliary carry flag.

Bit 0 (C) : Carry flag

4.1.5 R4/RSR (RAM Select Register) (Address: 04h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBS1	RBS0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0

Bits 7 ~ 6 (RBS1 ~ RBS0) : determine which bank is activated among the 4 banks. See the configuration of the data memory in Fig.4. Use BANK instruction (e.g. BABK 1) to change bank.

Bits 5 ~ 0 (RSR5 ~ RSR0) : are used to select up to 64 registers (address: 00~3F) in the indirect addressing mode. If no indirect addressing is used, the RSR can be used as an 8-bit general purposes read/writer register.

4.1.6 R5/PORT5 (PORT 5 I/O Data and Page of Register Select) (Address: 05h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R57	R56	R55	R54	--	--	--	IOCPAGE

Bit 7~4 : 4-bits I/O registers of PORT5

User can use IOC50 register to define input or output each bit.

Bit 3~1 : Not used

Bit 0 (IOCPAGE) : change IOC5 ~ IOCF to another page

IOCPAGE = "0" : Page 0 (select register of IOC 50 to IOC F0)

IOCPAGE = "1" : Page 1 (select register of IOC 61 to IOC E1)

4.1.7 R6/PORT6 (PORT 6 I/O Data Register) (Address: 06h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R67	R66	R65	R64	R63	R62	R61	R60

Bit 7~0 : 8-bit I/O registers of PORT 6

User can use IOC60 register to define input or output each bit.

4.1.8 R7/PORT7 (PORT 7 I/O Data Register) (Address: 07h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R77	R76	R75	R74	R73	R72	R71	R70

Bit 7~0 : 8-bit I/O registers of PORT 7

User can use IOC70 register to define input or output each bit.

4.1.9 R8/PORT8 (PORT 8 I/O Data Register) (Address: 08h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R87	R86	R85	R84	R83	R82	R81	R80

Bit 7~0 : 8-bit I/O registers of PORT 8

User can use IOC80 register to define input or output each bit.

4.1.10 R9/LCDCR (LCD Control Register) (Address: 09h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BS	DS1	DS0	LCDEN	--	LCDTYPE	LCDF1	LCDF0

Bit 7 (BS): LCD bias select bit,

BS = "0": 1/2 bias

BS = "1": 1/3 bias

Bit 6 ~ 5 (DS1 ~ DS0): LCD duty select

DS1	DS0	LCD duty
0	0	1/2 duty
0	1	1/3 duty
1	X	1/4 duty

Bit 4 (LCDEN) : LCD enable bit

LCDEN = "0" : LCD circuit disable. all common/segment outputs are set to ground (GND) level

LCDEN = "1" : LCD circuit enable.

Bit 3: Not used

Bit 2 (LCDTYPE) : LCD drive waveform type select bit

LCDTYPE = "0" : A type waveform

LCDTYPE = "1" : B type waveform

Bit 1 ~ 0(LCDF1 ~ LCDF0): LCD frame frequency control bits

LCDF1	LCDF0	LCD frame frequency (e.g. Fs=32.768KHz)		
		1/2 duty	1/3 duty	1/4 duty
0	0	Fs/(256*2)=64.0	Fs/(172*3)=63.5	Fs/(128*4) =64.0
0	1	Fs/(280*2)=58.5	Fs/(188*3)=58.0	Fs/(140*4) =58.5
1	0	Fs/(304*2)=53.9	Fs/(204*3)=53.5	Fs/(152*4) =53.9
1	1	Fs/(232*2)=70.6	Fs/(156*3)=70.0	Fs/(116*4) =70.6

Fs: sub-oscillator frequency

4.1.11 RA/LCD_ADDR (LCD Address) (Address: 0Ah)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	LCD_A4	LCD_A3	LCD_A2	LCD_A1	LCD_A0

Bit 7 ~ 5: Not used, fixed to "0"

Bit 4~0 (LCDA4 ~ LCDA0): LCD RAM address

RA (LCD address)	RB (LCD data buffer)					Segment
	Bit 7 ~4	Bit 3 (LCD_D3)	Bit 2 (LCD_D2)	Bit 1 (LCD_D1)	Bit 0 (LCD_D0)	
00H	--					SEG0
01H	--					SEG1
02H	--					SEG2
|			|		|
1DH	--					SEG29
1EH	--					SEG30
1FH	--					SEG31
Common	X	COM3	COM2	COM1	COM0	

4.1.12 RB/LCD_DB (LCD Data Buffer) (Address: 0Bh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	--	--	--	LCD_D3	LCD_D2	LCD_D1	LCD_D0

Bit 7 ~ 4 : Not used

Bit 3~0 (LCD_D3 ~ LCD_D0) : LCD RAM data transfer register

4.1.13 RC/CNTER (Counter Enable Register) (Address: 0Ch)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	--	--	--	LPWTEN	HPWTEN	CNT2EN	CNT1EN

Bit 7,5 : Not used, must fixed to "0"

Bit 6,4 : Not used

Bit 3(LPWTEN): low pulse width timer enable bit,

LPWTEN = "0" : Disable LPWT. Count operation stop.

LPWTEN = "1" : Enable LPWT. Count operation start.

Bit 2(HPWTEN) : high pulse width timer enable bit

HPWTEN = "0" : Disable HPWT. Count operation stop.

HPWTEN = "1" : Enable HPWT. Count operation start.

Bit 1(CNT2EN) : counter 2 enable bit

CNT2EN = "0" : Disable Counter 2. Count operation stop.

CNT2EN = "1" : Enable Counter 2. Count operation start.

Bit 0(CNT1EN) : counter 1 enable bit

CNT1EN = "0" : Disable Counter 1. Count operation stop.

CNT1EN = "1" : Enable Counter 1. Count operation start.

4.1.14 RD/SBPCR (System, Booster and PLL Control Register) (Address: 0Dh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	CLK2	CLK1	CLK0	IDLE	BF1	BF0	CPUS

Bit 7: Not used

Bit 6 ~ 4 (CLK2 ~ CLK0): main clock selection bits for PLL mode (code option select)

CLK2	CLK1	CLK0	Main clock	Example Fs=32.768K
0	0	0	Fs*130	4.26 MHz
0	0	1	Fs*65	2.13 MHz
0	1	0	Fs*65/2	1.065 MHz
0	1	1	Fs*65/4	532 KHz
1	X	X	Fs*244	8 MHz

Bit 3 (IDLE) : idle mode enable bit. This bit will decide the intended mode of the SLEP instruction.

IDLE="0"+SLEP instruction => sleep mode

IDLE="1"+SLEP instruction => idle mode

**** NOP instruction must be added after SLEP instruction.***

Example : IDLE mode : IDLE bit = "1" +SLEP instruction + NOP instruction

SLEEP mode : IDLE bit = "0" +SLEP instruction + NOP instruction

Bit 2,1 (BF1, 0): **LCD booster frequency select bit to adjust VLCD 2,3 driving.**

BF1	BF0	Booster frequency
0	0	Fs
0	1	Fs/4
1	0	Fs/8
1	1	Fs/16

Bit 0 (CPUS): CPU oscillator source select, When CPUS=0, the CPU oscillator select sub-oscillator and the main oscillator is stopped.

CPUS = "0": sub-oscillator (Fs)

CPUS = "1": main oscillator (Fm)

CPU Operation Mode

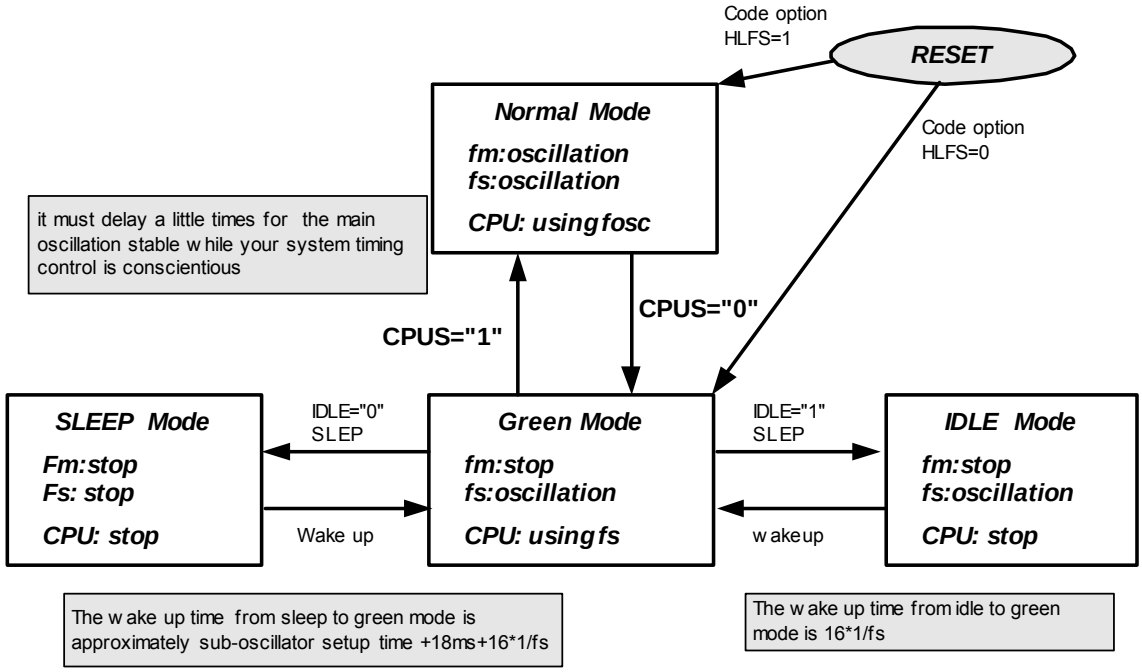


Fig. 5 CPU Operation Mode

4.1.15 RE/IRCR (IR and PORT 5 Setting Control Register) (Address: 0Eh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRE	HF	LGP	--	IROUTE	TCCE	EINT1	EINT0

Bit 7 (IRE): Infrared Remote Enable bit

IRE = "0" : Disable IR/PWM function. The state of P5.7/IROUT pin is determined by bit 7 of IOC 50 if it's for IROUT.

IRE = "1" : Enable IR or PWM function.

Bit 6 (HF) : High carry frequency.

HF = "0" : For PWM application, disable H/W modulator function. IROUT waveform is created according to high-pulse and low-pulse time as determined by the high pulse and low pulse width timers respectively. The counter 2 is an independent auto reload timer.

HF = "1" : For IR application mode, enable H/W modulator function, the low time sections of the generated pulse is modulated with the frequency Fcarrier. The frequency of Fcarrier provide by counter 2.

Bit 5 (LGP) : IROUT for long time of low pulse.

LGP = "0" : The high-pulse width timer register and low-pulse width timer is valid.

LGP = "1" : The high-pulse width timer register is ignored. So the IROUT waveform is dependent on low-pulse width timer register only.

Bit 4 : Not used

Bit 3 (IROUTE) : Define the function of P5.7/IROUT pin.

IROUTE = "0" : for bi-directional general I/O pin.

IROUTE = "1" : for IR or PWM output pin, the control bit of P5.7 (bit 7 of IOC50) must be set to "0"

Bit 2 (TCCE) : Define the function of P5.6/TCC pin.

TCCE = "0" : for bi-directional general I/O pin.

TCCE = "1" : for external input pin of TCC, the control bit of P5.6 (bit 6 of IOC50) must be set to "1"

Bit 1 (EINT1): Define the function of P5.5/INT1 pin.

EINT1 = "0" : for bi-directional general I/O pin.

EINT1 = "1" : for external interrupt pin of INT1, the control bit of P5.5 (bit 5 of IOC50) must be set to "1"

Bit 0 (EINT0) : Define the function of P5.4/INT0 pin.

EINT0 = "0" : for bi-directional general I/O pin.

EINT0 = "1" : for external interrupt pin of INT0, the control bit of P5.4 (bit 4 of IOC50) must be set to "1"

4.1.16 RF/ISR (Interrupt Status Register) (Address: 0Fh)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICIF	LPWTF	HPWTF	CNT2F	CNT1F	INT1F	INT0F	TCIF

These bits are set to "1" when interrupt occurs respectively.

Bit 7 (ICIF) : PORT 6, PORT 8, input status changed interrupt flag. Set when PORT6, PORT8 input changes.

Bit 6 (LPWTF) : interrupt flag of internal low-pulse width timer underflow.

Bit 5 (HPWTF) : interrupt flag of internal high-pulse width timer underflow.

Bit 4 (CNT2F) : interrupt flag of internal counter 2 under-flow.

Bit 3 (CNT1F) : interrupt flag of internal counter 1 underflow.

Bit 2 (INT1F): external INT1 pin interrupt flag.

Bit 1 (INT0F) : external INT0 pin interrupt flag.

Bit 0 (TCIF) : TCC timer overflow interrupt flag. Set when TCC timer overflows.

4.1.17 Address: 10h~3Fh;R10~R3F (General Purpose Register)

R10~R31F and R20~R3F (Banks 0~3) are general purposes register.

4.2 Special Purpose Registers

4.2.1 A (Accumulator)

- Internal data transfer, or instruction operand holding
- This is not an addressable register.

Registers of IOC Page 0 (IOC50 ~ IOCF0, Bit 0 of R5 = "0")

4.2.2 IOC50/P5CR (PORT 5 I/O and PORT 7, 8 for LCD Segment Control Register) (Address: 05h, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC57	IOC56	IOC55	IOC54	P8HS	P8LS	P7HS	P7LS

Bit 7~4(IOC57~54): PORT 5 I/O direction control register

IOC5x = "0": set the relative P5.x I/O pins as output

IOC5x = "1": set the relative P5.x I/O pin into high impedance (input pin)

Bit 3(P8HS): Switch to high nibble I/O of PORT 8 or to LCD segment output as share pins SEGxx/P8.x pins

P8HS = "0": select high nibble of PORT 8 as normal P8.4~P8.7

P8HS = "1": select LCD SEGMENT output as SEG 28~SEG 31 output

Bit 2(P8LS): Switch to low nibble I/O of PORT 8 or to LCD segment output as share pins SEGxx/P8.x pins

P8LS = "0": select low nibble of PORT 8 as normal P8.0~P8.3

P8LS = "1": select LCD SEGMENT output as SEG 24~SEG 27 output

Bit 1(P7HS): Switch to high nibble I/O of PORT 7 or to LCD segment output as share pins SEGxx/P7.x pins

P7HS = "0": select high nibble of PORT 7 as normal P7.4~P7.7

P7HS = "1": select LCD SEGMENT output as SEG 20~SEG 23 output

Bit 0(P7LS): Switch to low nibble I/O of PORT 7 or to LCD segment output as share pins SEGxx/P7.x pins

P7LS = "0": select low nibble of PORT 7 as normal P7.0~P7.3

P7LS = "1": select LCD SEGMENT output as SEG 16~SEG 19 output

4.2.3 IOC60/P6CR (PORT 6 I/O Control Register) (Address: 06h, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60

Bit 7 (IOC67)~Bit 0(IOC60): PORT 6 I/O direction control register

IOC6x =”0”: set the relative PORT6.x I/O pins as output

IOC6x =”1”: set the relative PORT6.x I/O pin into high impedance (input pin)

4.2.4 IOC70/P7CR (PORT 7 I/O Control Register) (Address: 07h, Bit 0 of R5 = “0”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70

Bit 7 (IOC77)~Bit 0(IOC70): PORT 7 I/O direction control register

IOC7x = “0”: set the relative PORT7.x I/O pins as output

IOC7x = “1”: set the relative PORT7.x I/O pin into high impedance (input pin)

4.2.5 IOC80/P8CR (PORT 8 I/O Control Register) (Address: 08h, Bit 0 of R5 = “0”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80

Bit 7 (IOC 87)~Bit 0(IOC 80): PORT 8 I/O direction control register

IOC8x = “0”: set the relative PORT8.x I/O pins as output

IOC8x = “1”: set the relative PORT8.x I/O pin into high impedance (input pin)

4.2.6 IOC90/RAM_ADDR (128 Bytes RAM Address) (Address: 09h, Bit 0 of R5 = “0”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0

Bit 7: Not used, fixed at “0”

Bit 6~0: 128 bytes RAM address

4.2.7 IOCA0/RAM_DB (128 Bytes RAM Data Buffer) (Address: 0Ah, Bit 0 of R5 = “0”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0

Bit 7~0: 128 bytes RAM data transfer register

4.2.8 IOCB0/CNT1PR (Counter 1 Preset Register) (Address: 0Bh, Bit 0 of R5 = “0”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7 ~ Bit 0: All are Counter 1 buffer that user can read and write. The Counter 1 is an 8-bit down-count timer with 8-bit pre-scaler that is used as this register to preset the

counter and read preset value. The pre-scaler is set by IOC91 register. After an interruption, it will auto reload the preset value.

4.2.9 IOCC0/CNT2PR (Counter 2 Preset Register) (Address: 0Ch, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7 ~ Bit 0: All are Counter 2 buffer that user can read and write. The Counter 2 is an 8-bit down-count timer with 8-bit pre-scaler that is used as this register to preset the counter and read preset value. The pre-scaler is set by IOC91 register. After an interruption, it will reload the preset value.

When IR output is enabled, this control register can obtain carrier frequency output.

If the Counter 2 clock source is equal to F_T –

$$\text{Carrier frequency (Fcarrier)} = \frac{F_T}{2 * (\text{preset\_value} + 1) * \text{prescaler}}$$

4.2.10 IOCD0/HPWTPR (High-Pulse Width Timer Preset Register) (Address: 0Dh, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7 ~ Bit 0: All are high-pulse width timer buffer that user can read and write. High-pulse width timer preset register is an eight-bit down-counter with 8-bit pre-scaler that is used as IOCD0 to preset the counter and read preset value. The pre-scaler is set by IOCA1 register. After an interruption, it will reload the preset value.

For PWM or IR application, this control register is set as high pulse width.

If the high-pulse width timer source clock is F_T –

$$\text{High pulse time} = \frac{\text{prescaler} * (\text{preset\_value} + 1)}{F_T}$$

4.2.11 IOCE0/LPWTPR (Low-Pulse Width Timer Preset Register) (Address: 0Eh, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit 7 ~ Bit 0: All are low-pulse width timer buffer that user can read and write. Low-pulse width timer preset is an eight-bit down-counter with 8-bit pre-scaler that is used as IOCE0 to preset the counter and read preset value. The pre-scaler is set by IOCA1 register. After an interruption, it will reload the preset value.

For PWM or IR application, this control register is set as low pulse width.

If the low-pulse width timer source clock is F_T –

$$\text{Low pulse time} = \frac{\text{prescaler} * (\text{preset\_value} + 1)}{F_T}$$

4.2.12 IOCF0/IMR (Interrupt Mask Register) (Address: 0Fh, Bit 0 of R5 = "0")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ICIE	LPWTE	HPWTE	CNT2E	CNT1E	INT1E	INT0E	TCIE

Bit 7~Bit 0: interrupt enable bit. Enable interrupt source respectively.

0: disable interrupt

1: enable interrupt

IOCF0 register is readable and writable.

Registers of IOC Page 1 (IOC61 ~ IOCE1, Bit 0 of R5 = "1")

4.2.13 IOC61/WUCR (Wake Up and sink current of P5.7/IROUT Control Register) (Address: 06h, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IROCS	--	--	--	/WUE8H	/WUE8L	/WUE6H	/WUE6L

Bit 7: IROCS: IROUT/PORT5.7 output sink current set

IROCS	P5.7/IROUT Sink current	
	VDD=5V	VDD=3V
0	10 mA	6 mA
1	20 mA	12 mA

Bit 6,5,4: Not used

Bit 3 (/WUE8H): 0/1=> enable/disable P8.4~P8.7 pin change wake up function

Bit 2 (/WUE8L): 0/1=> enable/disable P8.0~P8.3 pin change wake up function

Bit 1 (/WUE6H): 0/1=> enable/disable P6.4~P6.7 pin change wake up function

Bit 0 (/WUE6L): 0/1=> enable/disable P6.0~P6.3 pin change wake up function

*** Port 6 and Port 8 must avoid input floating when wakeup function is enabled. The initial state of wakeup function is enabled.**

4.2.14 IOC71/TCCCR (TCC Control Register) (Address: 07h, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INT_EDGE	INT	TS	TE	PSRE	TCCP2	TCCP1	TCCP0

Bit 7 (INT_EDGE):

INT_EDGE = "0": Interrupt on rising edge of P5.4/INT0 pin

INT_EDGE = ”1”: Interrupt on falling edge of P5.4/INT0 pin

Bit 6 (INT): INT enable flag, this bit is read only

INT = ”0”: interrupt masked by DISI or hardware interrupt

INT = “1”: interrupt enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

TS = “0”: internal instruction cycle clock

TS = “1”: transition on TCC pin, TCC period > internal instruction clock period

Bit 4 (TE): TCC signal edge

TE = ”0”: increment by TCC pin rising edge

TE = “1”: increment by TCC pin falling edge

Bit 3~0 (PSRE,TCCP2 ~ TCCP0): TCC pre-scaler bits.

PSRE	TCCP2	TCCP1	TCCP0	TCC rate
0	X	X	X	1:1
1	0	0	0	1:2
1	0	0	1	1:4
1	0	1	0	1:8
1	0	1	1	1:16
1	1	0	0	1:32
1	1	0	1	1:64
1	1	1	0	1:128
1	1	1	1	1:256

4.2.15 IOC81/WDTCR (WDT Control Register) (Address: 08h, Bit 0 of R5 = “1”)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	--	--	--	WDTE	WDTP2	WDTP1	WDTP0

Bit 7 ~ 4: Not used

Bit 3 (WDTE): watchdog timer enable. This control bit is used to enable the Watchdog timer,

WDTE = “0”: Disable WDT function.

WDTE = “1”: enable WDT function.

Bit 2 ~ 0 (WDTP2 ~ WDTP0): watchdog timer pre-scaler bits. The WDT source clock is sub-oscillation frequency.

WDTP2	WDTP1	WDTP0	WDT rate
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	0	1	1:64
1	1	1	1:128

4.2.16 IOC91/CNT12CR (Counter 1, 2 Control Register) (Address: 09h, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT2S	CNT2P2	CNT2P1	CNT2P0	CNT1S	CNT1P2	CNT1P1	CNT1P0

Bit 7(CNT2S): Counter 2 clock source select 0/1 => Fs/ Fm*

(*Fs: sub-oscillator clock, Fm: main-oscillator clock)

Bit 6~4(CNT2P2 ~ CNT2P 0): Counter 2 pre-scaler select bits

CNT2P2	CNT2P1	CNT1P0	Counter 2 scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3(CNT1S): Counter 1 clock source select 0/1 => Fs/ Fm*

Bit 2~0 (CNT1P2 ~ CNT1P20): Counter 1 pre-scaler select bits

CNT1P2	CNT1P1	CNT1P0	Counter 1 scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

4.2.17 IOCA1/HLPWTCR (High/Low Pulse Width Timer Control Register) (Address: 0Ah, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LPWTS	LPWTP2	LPWTP1	LPWTP0	HPWTS	HPWTP2	HPWTP1	HPWTP0

Bit 7(LPWTS): low-pulse width timer clock source select 0/1 -> Fs/ Fm*

(*Fs: sub-oscillator clock, Fm: main-oscillator clock)

Bit 6~4 (LPWTP2~ LPWTP0): low-pulse width timer pre-scaler select bits

LPWTP2	LPWTP1	LPWTP0	Low-pulse width timer scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3(HPWTS): high-pulse width timer clock source select 0/1 -> Fs/ Fm*

Bit 2~0(HPWTP2~ HPWTP0): high-pulse width timer pre-scaler select bits

HPWTP2	HPWTP1	HPWTP0	High-pulse width timer scale
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

4.2.18 IOCB1/P6PH (PORT 6 Pull High Control Register) (Address: 0Bh, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60

Bit 7 ~ Bit 0 (PH67 ~ PH60): The enable bits of PORT 6 pull high function.

PH6x = "0": disable pin of P6.x internal pull-high resistor function

PH6x = "1": enable pin of P6.x internal pull-high resistor function

4.2.19 IOCC1/P6OD (PORT 6 Open Drain Control Register) (Address: 0Ch, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OP67	OP66	OP65	OP64	OP63	OP62	OP61	OP60

Bit 7 ~ Bit 0: The enable bits of PORT 6 open drain function.

OD6x = "0": disable pin of P6.x open drain function

OD6x = "1": enable pin of P6.x open drain function

4.2.20 IOCD1/P8PH (PORT 8 Pull High Control Register) (Address: 0Dh, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PH87	PH86	PH85	PH84	PH83	PH82	PH81	PH80

Bit 7 ~ Bit 0: The enable bits of PORT 8 pull-high function.

PH8x = "0": disable pin of P8.x internal pull-high resistor function

PH8x = "1": enable pin of P8.x pull-high resistor function

4.2.21 IOCE1/P6PL (PORT 6 Pull-Low Control Register) (Address: 0Eh, Bit 0 of R5 = "1")

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60

Bit 7 ~ Bit 0: The enable bits of PORT 6 pull low function.

PL6x = "0": disable pin of P6.x internal pull-low resistor function

PL6x = "1": enable pin of P6.x internal pull-low resistor function

4.3 TCC and WDT Pre-scaler

Two 8-bit counters are available as pre-scalers for the TCC (Time Clock Counter) and WDT (Watch Dog Timer). The TCCP2~TCCP0 bits of the IOC71 register are used to determine the ratio of the TCC pre-scaler. Likewise, the WDTP2~WDTP0 bits of the IOC81 register are used to determine the WDT pre-scaler. The TCC pre-scaler (TCCP2~TCCP0) is cleared by the instructions each time they are written into TCC, while the WDT pre-scaler is cleared by the "WDTC" and "SLEP" instructions. Fig.7 depicts the circuit diagram of TCC and WDT.

R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be selected by internal instruction clock or external signal input (edge selectable from the TCC control register). If TCC signal source is from internal instruction clock, TCC will increase by 1 at every instruction cycle (without pre-scaler). If TCC signal source is from external clock input, TCC will increase by 1 at every falling edge or rising edge of the TCC pin.

The watchdog timer is a free running on sub-oscillator. The WDT will keep on running even after the oscillator driver has been turned off. During Normal mode, Green mode, or

Idle mode operation, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the Normal mode and Green mode by software programming. Refer to WDTE bit of IOC81 register. The WDT time-out period is equal to (pre-scaler*256/ (Fs/2)).

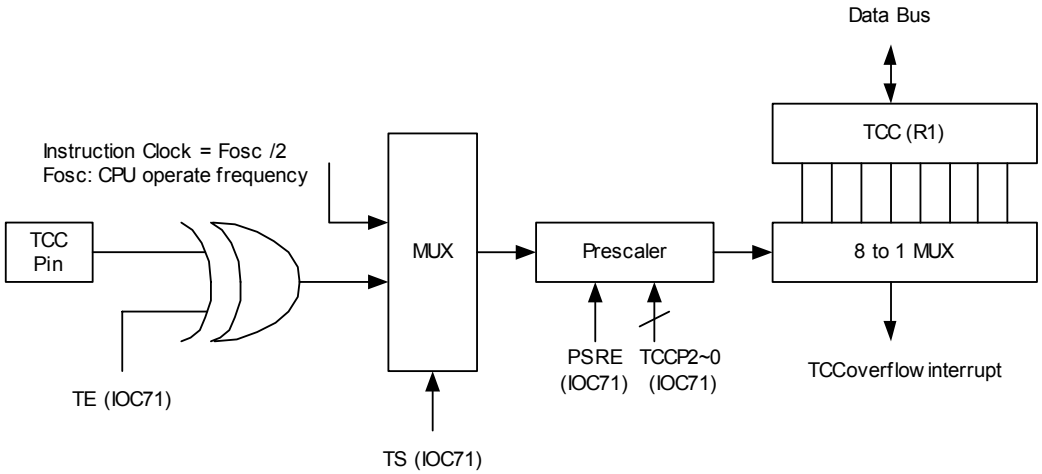


Fig. 7(a) Block Diagram of TCC

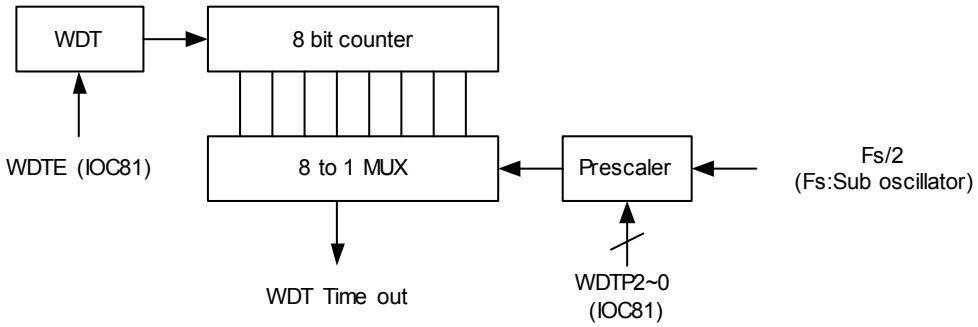
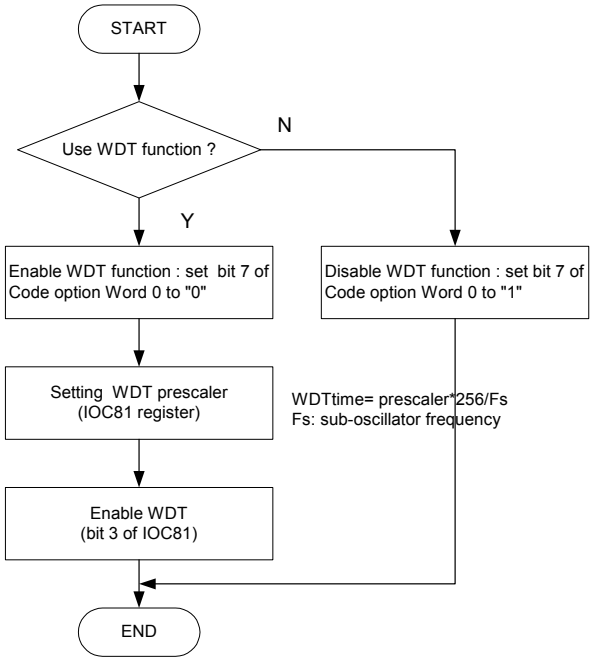
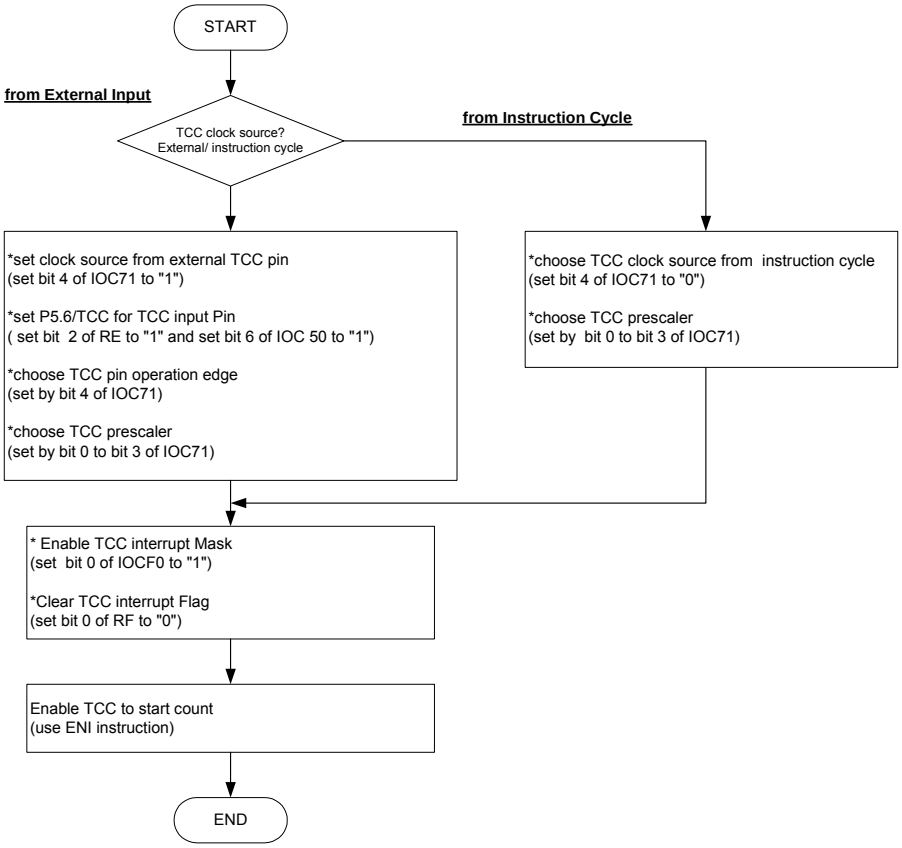


Fig. 7(b) Block Diagram of WDT

WDT setting flowchart

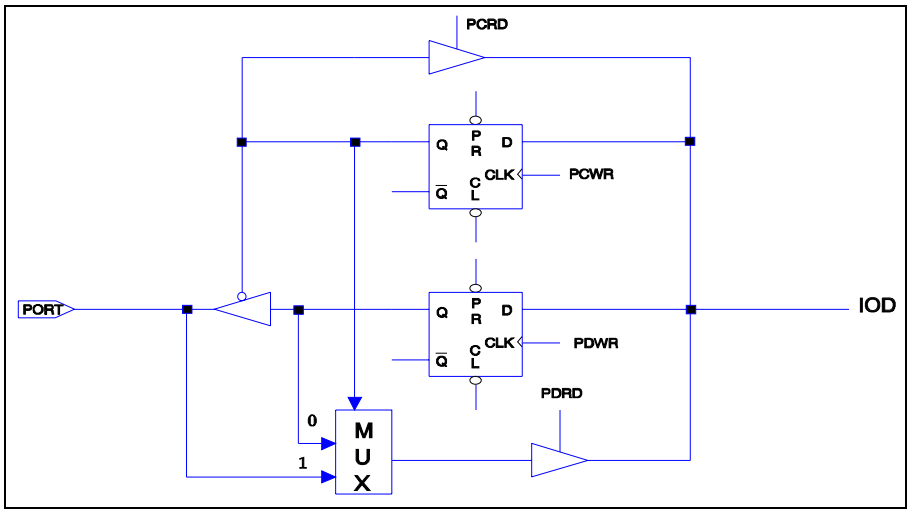


TCC setting flowchart



4.4 I/O Ports

The I/O registers, (PORT 5, PORT 6, PORT 7and PORT 8), are bi-directional tri-state I/O ports. PORT 6 and PORT 8 are pulled-high internally by software; PORT 6 is also pulled-low internally by software. Furthermore, PORT 6 has its open-drain output also through software. PORT 6 and PORT 8 features an input status changed interrupt (or wake-up) function and is pulled-high by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC50 ~ IOC80). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits are shown in Fig. 8



NOTE: *Open-drain, pull high, and pull down are not shown in the figure.*

Fig. 8 The Circuit of I/O Port and I/O Control Register for PORT 5 ~ 8

4.5RESET and Wake-up

A reset can be activated by

- POR (Power On Reset)
- WDT timeout. (if enabled)
- /RESET pin go to low.

Note: *The power on reset circuit is always enabled. It will reset CPU at about 1.9V.*

Once reset occurs, the following functions are performed

- The oscillator is running, or will be started.
- The program counter (R2/PC) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The TCC/Watchdog timer and pre-scaler are cleared.
- When power on, the Bit 5, 6 of R3 and the upper 2 bits of R4 are cleared.
- Bits of the IOC71 register are set to all "1" except for Bit 6 (INT flag).
- For other registers, see Table 2 below.

Table 2 Summary of the Initialized Values for Registers

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	IOC50 (P5CR)	Bit Name	IOC57	IOC56	IOC55	IOC54	P8HS	P8LS	P7HS	P7LS
		Power-On	1	1	1	1	0	0	0	0
		/RESET and WDT	1	1	1	1	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x06	IOC60 (P6CR)	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x07	IOC70 (P7CR)	Bit Name	IOC77	IOC76	IOC75	IOC74	IOC73	IOC72	IOC71	IOC70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x08	IOC80 (P8CR)	Bit Name	IOC87	IOC86	IOC85	IOC84	IOC83	IOC82	IOC81	IOC80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x09	IOC90 (RAM_ADDR)	Bit Name	X	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0A	IOCA0 (RAM_DB)	Bit Name	RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0B	IOCB0 (CNT1PR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0C	IOCC0 (CNT2PR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD0 (HPWTPR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE0 (LPWTPR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0F	IOCF0 (IMR)	Bit Name	ICIE	LPWTE	HPWTE	CNT2E	CNT1E	INT1E	INT0E	TCIE
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x06	IOC61 (WUCR)	Bit Name	IROCS	X	X	X	/WUE8H	/WUE8L	/WUE6H	/WUE6L
		Power-On	0	U	U	U	0	0	0	0
		/RESET and WDT	0	U	U	U	0	0	0	0
		Wake-Up from Pin Change	P	U	U	U	P	P	P	P
0x07	IOC71 (TCCCR)	Bit Name	INT_EDGE	INT	TS	TE	PSRE	TCCP2	TCCP1	TCCP0
		Power-On	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x08	IOC81 (WDTCR)	Bit Name	X	X	X	X	WDTE	WDTP2	WDTP1	WDTP0
		Power-On	U	U	U	U	0	1	1	1
		/RESET and WDT	U	U	U	U	0	1	1	1
		Wake-Up from Pin Change	U	U	U	U	P	P	P	P
0x09	IOC91 (CNT12CR)	Bit Name	CNT2S	CNT2P2	CNT2P1	CNT2P0	CNT1S	CNT1P2	CNT1P1	CNT1P0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0A	IOCA1 (HLPWTCR)	Bit Name	LPWTS	LPWTP2	LPWTP1	LPWTP0	HPWTS	HPWTP2	HPWTP1	HPWTP0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0B	IOCB1 (P6PH)	Bit Name	PH67	PH66	PH65	PH64	PH63	PH62	PH61	PH60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0C	IOCC1 (P6OD)	Bit Name	OP67	OP66	OP65	OP64	OP63	OP62	OP61	OP60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0D	IOCD1 (P8PH)	Bit Name	PH87	PH86	PH85	PH84	PH83	PH82	PH81	PH80
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x0E	IOCE1 (P6PL)	Bit Name	PL67	PL66	PL65	PL64	PL63	PL62	PL61	PL60
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (TCC)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	Jump to address 0x0018 or continue to execute next instruction							
0x03	R3 (SR)	Bit Name	X	PS1	PS0	T	P	Z	DC	C
		Power-On	U	0	0	1	1	U	U	U
		/RESET and WDT	U	0	0	t	t	P	P	P
		Wake-Up from Pin Change	U	P	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	Bank1	Bank0	--	--	--	--	--	--
		Power-On	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x05	R5 (PORT5)	Bit Name	R57	R56	R55	R54	X	X	X	IOCPAGE
		Power-On	1	1	1	1	U	U	U	0
		/RESET and WDT	1	1	1	1	U	U	U	0
		Wake-Up from Pin Change	P	P	P	P	U	U	U	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06	R6 (PORT6)	Bit Name	R67	R66	R65	R64	R63	R62	R61	R60
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x7	R7 (PORT7)	Bit Name	R77	R76	R75	R74	R73	R62	R71	R70
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x8	R8 (PORT8)	Bit Name	R87	R86	R85	R84	R83	R82	R81	R80
		Power-On	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0x9	R9 (LCDCR)	Bit Name	BS	DS1	DS0	LCDEN	X	LCDTYPE	LCDF1	LCDF0
		Power-On	1	1	0	0	U	0	0	0
		/RESET and WDT	1	1	0	0	U	0	0	0
		Wake-Up from Pin Change	P	P	P	P	U	P	P	P
0xA	RA (LCD_ADDR)	Bit Name	X	X	X	LCD_A4	LCD_A3	LCD_A2	LCD_A1	LCD_A0
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P
0xB	RB (LCD_DB)	Bit Name	X	X	X	X	LCD_D 3	LCD_D 2	LCD_D 1	LCD_D 0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	P	P	P	P
		Wake-Up from Pin Change	U	U	U	U	P	P	P	P
0xC	RC (CNTER)	Bit Name	X	X	X	X	LPWTEN	HPWTEN	CNT2EN	CNT1EN
		Power-On	0	1	0	0	0	0	0	0
		/RESET and WDT	0	1	0	0	0	0	0	0
		Wake-Up from Pin Change	P	P	0	P	P	P	P	P
0xD	RD (SBPCR)	Bit Name	X	CLK2	CLK1	CLK0	IDLE	BF1	BF0	CPUS
		Power-On	U	0	0	0	1	0	0	*1
		/RESET and WDT	U	0	0	0	1	0	0	*1
		Wake-Up from Pin Change	U	P	P	P	P	P	P	P
0xE	RE (IRCR)	Bit Name	IRE	HF	LGP	X	IROUTE	TCCE	EINT1	EINT0
		Power-On	0	0	0	U	0	0	0	0
		/RESET and WDT	0	0	0	U	0	0	0	0
		Wake-Up from Pin Change	P	P	P	U	P	P	P	P
0xF	RF (ISR)	Bit Name	ICIF	LPWTF	HPWTF	CNT2F	CNT1F	INT1F	INT0F	TCIF
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-Up from Pin Change	N	P	P	P	P	P	P	P
0x10~0x3F	R10~R3F	Bit Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-On	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-Up from Pin Change	P	P	P	P	P	P	P	P

X: not used. **U:** unknown or don't care. **P:** previous value before reset. **–:** Not defined

t : check R3 register explain. **N:** Monitors interrupt operation status.

Note 1: *This bit is equal to code option HLFS bit data*

The controller can be awakened from sleep mode and idle mode. The wake-up signals are listed as follows:

Wakeup signal	Sleep mode	Idle mode	Green mode	Normal mode
TCC time out IOCF0 bit0=1	X	*1 Wake-up + interrupt + next instruction	Interrupt	Interrupt
INT0 pin IOCF0 bit1=1	Wake-up + interrupt + next instruction	Wake-up + interrupt + next instruction	Interrupt	Interrupt
INT1 pin IOCF0 bit2=1	Wake-up + interrupt + next instruction	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Counter 1 IOCF0 bit3=1	X	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Counter 2 IOCF0 bit4=1	X	Wake-up + interrupt + next instruction	Interrupt	Interrupt
High-pulse timer IOCF0 bit5=1	X	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Low-pulse timer IOCF0 bit6=1	X	Wake-up + interrupt + next instruction	Interrupt	Interrupt
Port6, Port 8 (input status change wake-up) Bit 7 of IOCF0 = “0”	Wake-up + next instruction	Wake-up + next instruction	X	X
Port6, Port 8 (input status change wake-up) Bit 7 of IOCF0 = “1”	Wake-up + interrupt + next instruction	Wake-up + interrupt + next instruction	X	X
WDT time out	X	RESET	RESET	RESET

Note 1: Only external TCC pin can Wake-up from idle mode.

4.6 Oscillator

4.6.1 Oscillator Modes

This LSI can operate in the three different oscillator modes from main oscillator (R-OSCI, OSCO), such as RC oscillator with external resistor and Internal capacitor mode (ERIC); crystal oscillator mode; and PLL operation mode (R-OSCI connected 0.01μF capacitor to Ground). User can select one of them by programming FMMD1 and FMMD0 in the CODE options register. The sub-oscillator can be operated in crystal mode and ERIC mode. Table 3 below shows how these three modes are defined.

Table 3 Oscillator Modes as defined by FSMD, FMMD1, FMMD0.

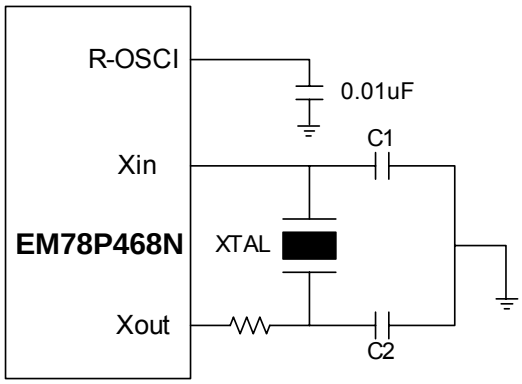
FSMD	FMMD1	FMMD0	Main clock	Sub-clock
0	0	0	RC type (ERIC)	RC type (ERIC)
0	0	1	Crystal type	RC type (ERIC)
0	1	X	PLL type	RC type (ERIC)
1	0	0	RC type (ERIC)	Crystal type
1	0	1	Crystal type	Crystal type
1	1	X	PLL type	Crystal type

Table 4 Summary of maximum operating speeds

Conditions	VDD	Fxt max.(MHz)
Two clocks	2.3	4
	3.0	8
	5.0	10

4.6.2 Phase Lock Loop (PLL Mode)

When operate on PLL mode, the High frequency determined by sub-oscillator. We can choose RD register to change high oscillator frequency. The relation between high frequency (Fm) and sub-oscillator is shown as below table:



Circuit for PLL mode

Bit 6~4 (CLK2~0) of RD: main clock selection bits for PLL mode (code option select)

CLK2	CLK1	CLK0	Main clock	Example Fs=32.768K
0	0	0	Fs*130	4.26 MHz
0	0	1	Fs*65	2.13 MHz
0	1	0	Fs*65/2	1.065 MHz
0	1	1	Fs*65/4	532 KHz
1	X	X	Fs*244	8 MHz

4.6.3 Crystal Oscillator/Ceramic Resonators (XTAL)

This LSI can be driven by an external clock signal through the R-OSCI pin as shown in Fig.9 below.

In most applications, the R-OSCI pin and the OSCO pin can be connected with a crystal or ceramic resonator to generate oscillation. Fig. 10 depicts such circuit. Table 5 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

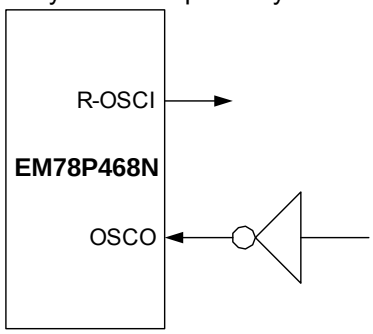


Fig.9 Circuit for External Clock Input

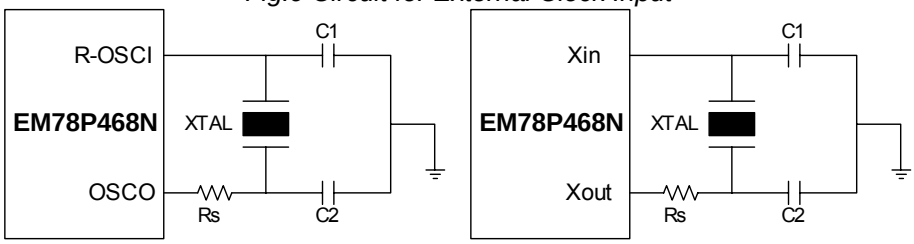


Fig. 10 Circuit for Crystal/Resonator

Table 5 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonators

Oscillator source	Oscillator Type	Frequency	C1 (pF)	C2 (pF)
Main oscillator	Ceramic Resonators	455 kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0MHz	10~30	10~30
	Crystal Oscillator	455KHz	20~40	20~150
		1.0MHz	15~30	15~30
		2.0MHz	15	15
		4.0MHz	15	15
Sub-oscillator	Crystal Oscillator	32.768kHz	25	25

4.6.4 RC Oscillator Mode with Internal Capacitor

If both precision and cost are taken into consideration, This LSI also offers a special oscillation mode, which is equipped with an internal capacitor and an external resistor connected to VDD. The internal capacitor functions as temperature compensator. In order to obtain more accurate frequency, a precise resistor is recommended.

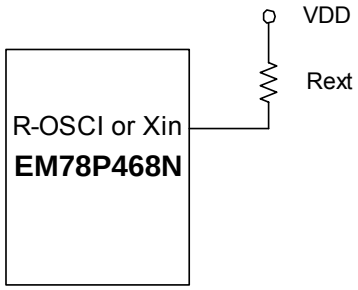


Fig. 11 Circuit for Internal C Oscillator Mode

Table 6 RC Oscillator Frequencies

Pin	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
R-OSCI	51k	2.2221 MHz	2.1972 MHz
	100k	1.1345 MHz	1.1203 MHz
	300k	381.36KHz	374.77 KHz
Xin	2.2M	32.768KHz	32.768KHz

Note: Measured from QFP packages with frequency drift of about ±30%. Values are provided for design reference only.

4.7 Power-on Considerations

Any microcontroller (as with this LSI) is not warranted to start operating properly before the power supply stabilizes in steady state. This LSI is equipped with Power On Reset (POR) with detection level range of 1.9V to 2.1V. The circuitry eliminates the extra external reset circuit but will work well only if the VDD rises quickly enough (50 ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

4.7.1 External Power-on Reset Circuit

This circuit implements an external RC to produce a reset pulse (see Fig.12). The pulse width (time constant) should be kept long enough to allow VDD to reach minimum operation voltage. This circuit is used when the power supply rise time is slow. Because the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be great than 40K. In this way, the voltage at Pin /RESET is held below 0.2V. The diode (D) acts as a short circuit at power-down. The capacitor, C, is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

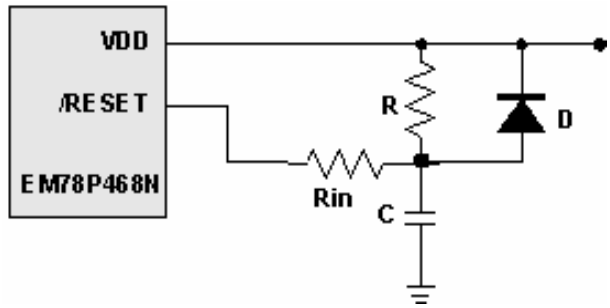


Fig. 12 External Power on Reset Circuit

4.7.2 Residue-Voltage Protection

When battery is replaced, device power (VDD) is disconnected but residue-voltage remains. The residue-voltage may trips below minimum VDD, but above zero. This condition may cause poor power on reset. Fig.13 and Fig.14 show how to build a residue-voltage protection circuit

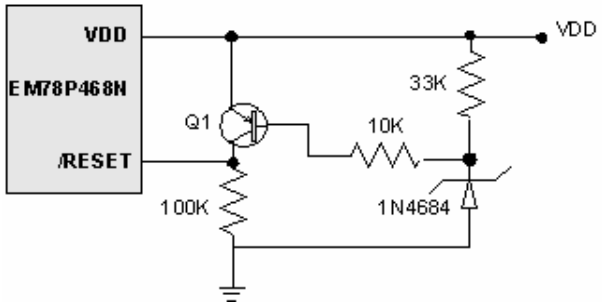


Fig. 13 Circuit 1 for the Residue Voltage Protection

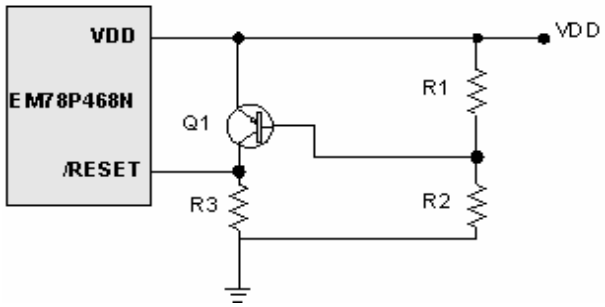


Fig. 14 Circuit 2 for the Residue Voltage Protection

4.8 Interrupt

This LSI has eight interrupt sources as listed below:

- TCC overflow interrupt.
- External interrupt P5.4/INTO pin
- External interrupt P5.5/INT1 pin
- Counter 1 underflow interrupt
- Counter 2 underflow interrupt
- High-pulse width timer underflow interrupt
- Low-pulse width timer underflow interrupt
- Port 6, Port 8 input status change wake-up

This IC has internal interrupts which are falling edge triggered or as follows**:**

- TCC timer overflow interrupt,
- Four 8-bits down counter/timer underflow interrupt

If these interrupt sources change signal from high to low, the RF register will generate “1” flag to corresponding register if the IOCF0 register is enabled.

RF is the interrupt status register. It records the interrupt request in flag bit. IOCF0 is the interrupt mask register. Global interrupt is enabled by ENI instruction and disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it will cause the next instruction to be fetch from address 0003H~0018H according to interrupt source.

With this LSI, each individual interrupt source has its own interrupt vector as depicted in Table 3. Before the interrupt subroutine is executed, the contents of ACC and the R3 register are initially saved by hardware. After the interrupt service routine is completed, ACC and R3 are restored. The existing interrupt service routine does not allow other interrupt service routine to be executed. So if other interrupts occur while the existing interrupt service routine is being executed, the hardware will save the later interrupts. Only after the existing interrupt service routine is completed that the next interrupt service routine is executed.

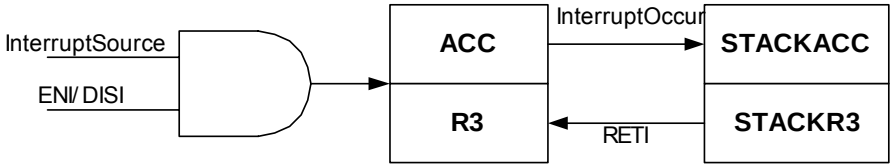


Fig. 15. Interrupt Backup Diagram

Table 3 Interrupt Vector

Interrupt Vector	Interrupt Status
0003H	TCC overflow interrupt.
0006H	External interrupt P5.4/INT0 pin
0009H	External interrupt P5.5/INT1 pin
000CH	Counter 1 underflow interrupt
000FH	Counter 2 underflow interrupt
0012H	High-pulse width timer underflow interrupt
0015H	Low-pulse width timer underflow interrupt
0018H	PORT 6, PORT 8 input status change wake-up

4.9 LCD Driver

This LSI can drive LCD of up to 32 segments and 4 commons that can drive a total of 4*32 dots. LCD block is made up of LCD driver, display RAM, segment output pins, common output pins, and LCD operating power supply pins. This circuit works on normal mode, green mode and idle mode. The LCD duty; bias; the number of segment; the number of common and frame frequency are determined by the LCD controller register.

The basic structure contains a timing control that uses a subsystem clock to generate the proper timing for different duty and display accesses. The R9 register is a command register for LCD driver which includes LCD enable/disable, bias (1/2 and 1/3), duty (1/2, 1/3, 1/4), and LCD frame frequency control. The register RA is an LCD contrast and LCD RAM address control register. The register RB is an LCD RAM data buffer. LCD booster circuit can change operation frequency to improve VLCD2 and VLCD3 drive capability. The control register is explained as follows.

R9/LCDCR (LCD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BS	DS1	DS0	LCDEN	--	LCDTYPE	LCDF1	LCDF0

Bit 7 (BS): LCD bias select bit, 0/1=>(1/2 bias) / (1/3 bias)

Bit 6 ~ 5 (DS1 ~ DS0): LCD duty select

DS1	DS0	LCD Duty
0	0	1/2 duty
0	1	1/3 duty
1	X	1/4 duty

Bit 4 (LCDEN): LCD enable bit: 0/1 -> LCD circuit disable/enable

When LCD function is disabled, all common/segment output is set to ground (GND) level

Bit 3: Not used

Bit 2 (LCDTYPE): LCD drive waveform type select bit

LCDTYPE = "0": "A" type waveform

LCDTYPE = "1": "B" type waveform

Bit 1 ~ 0(LCDF1 ~ LCDF0): LCD frame frequency control bits

LCDF1	LCDF0	LCD frame frequency (e.g. Fs=32.768KHz)		
		1/2 duty	1/3 duty	1/4 duty
0	0	Fs/(256*2)=64.0	Fs/(172*3)=63.5	Fs/(128*4) =64.0
0	1	Fs/(280*2)=58.5	Fs/(188*3)=58.0	Fs/(140*4) =58.5
1	0	Fs/(304*2)=53.9	Fs/(204*3)=53.5	Fs/(152*4) =53.9
1	1	Fs/(232*2)=70.6	Fs/(156*3)=70.0	Fs/(116*4) =70.6

Fs: sub-oscillator frequency

RA/LCD_ADDR (LCD Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	LCD_A4	LCD_A3	LCD_A2	LCD_A1	LCD_A0

Bit 7 ~ 5: Not used, fixed to "0"

Bit 4 ~ 0 (LCDA4 ~ LCDA0): LCD RAM address

RA (LCD address)	RB (LCD data buffer)					Segment
	Bit 7 ~4	Bit 3 (LCD_D3)	Bit 2 (LCD_D2)	Bit 1 (LCD_D1)	Bit 0 (LCD_D0)	
00H	--					**SEG0**
01H	--					**SEG1**
02H	--					**SEG2**
|			|			|
1DH	--					**SEG29**
1EH	--					**SEG30**
1FH	--					**SEG31**
Common	**X**	**COM3**	**COM2**	**COM1**	**COM0**	

RB/LCD_DB (LCD Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	--	--	--	LCD_D 3	LCD_D 2	LCD_D 1	LCD_D 0

Bit 7 ~ 4: Not used

Bit 3 ~ 0 (LCD_D3 ~ LCD_D0): LCD RAM data transfer registers

RD/SBPCR (System, Booster and PLL Control Registers)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
--	CLK2	CLK1	CLK0	IDLE	BF1	BF0	CPUS

Bit 2 ~ 1 (BF1 ~ 0): LCD booster frequency select bits

BF1	BF0	Booster frequency
0	0	Fs
0	1	Fs/4
1	0	Fs/8
1	1	Fs/16

The initial setting flowchart for LCD function

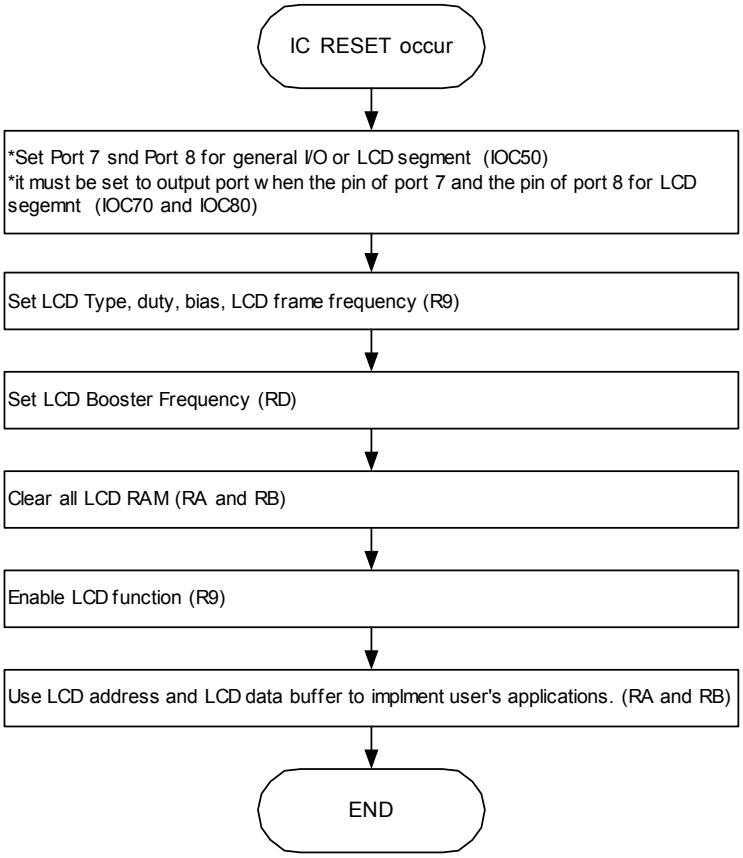
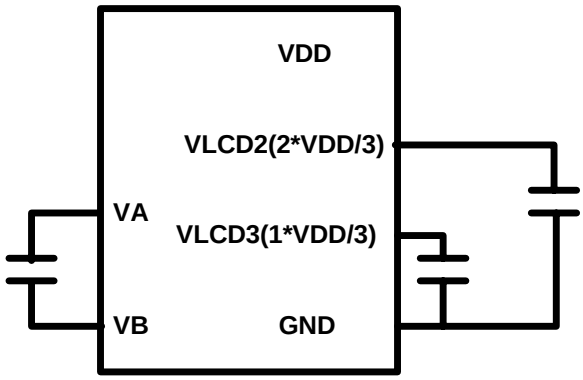
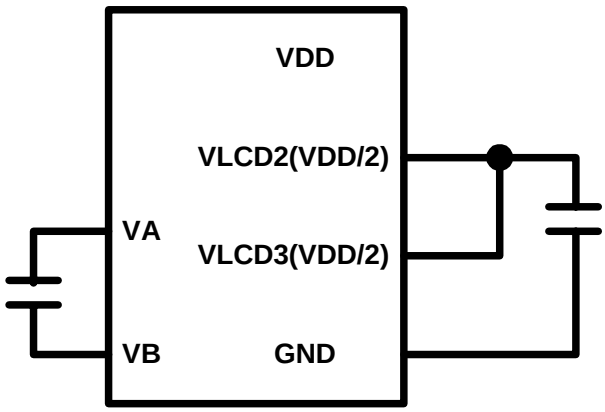


Fig.16. The Initial Setting Flowchart for LCD Function

The connecting of boosting circuits for LCD voltage is as below:



External circuit for 1/3 Bias



External circuit for 1/2 Bias

*Fig. 17 The Connection of Charge Bump Circuit (**Cext=0.1uf**)*

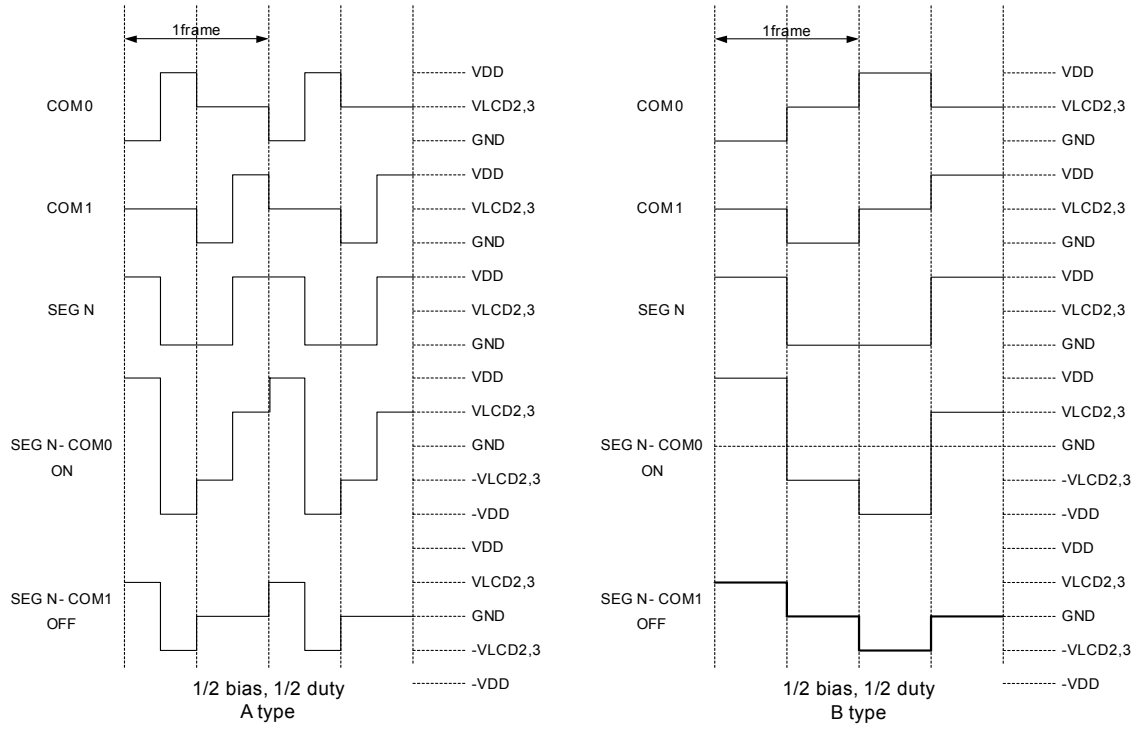


Fig. 18 LCD Waveform for 1/2 Bias, 1/2 Duty

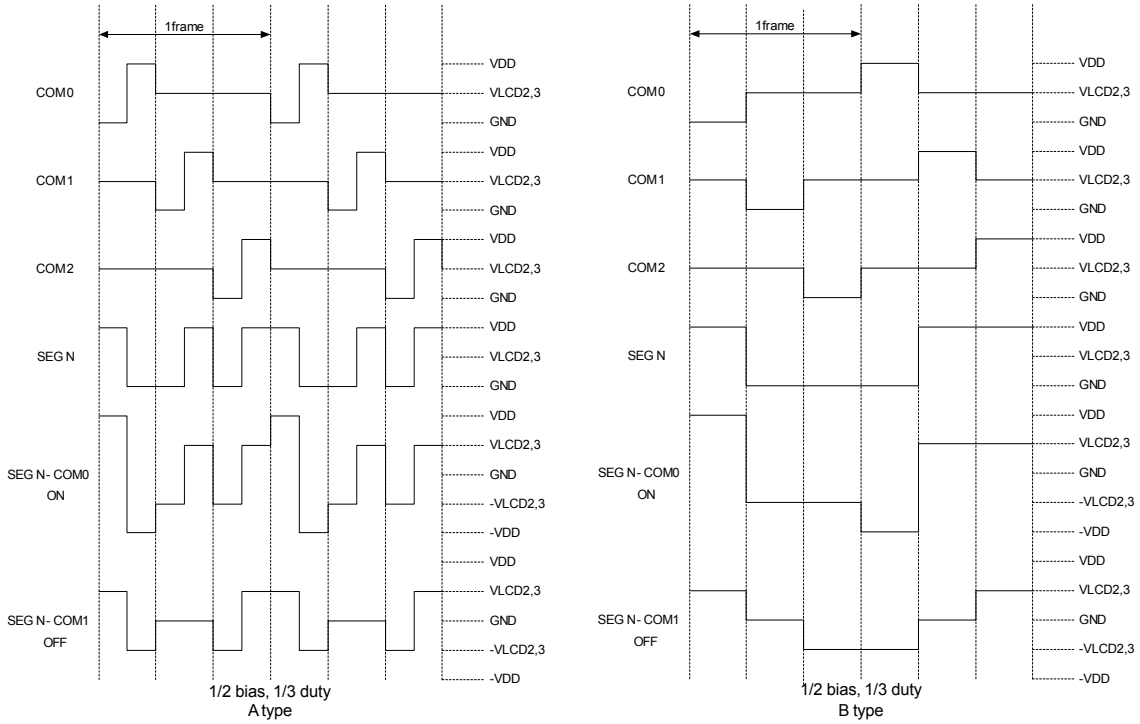


Fig. 19 LCD Waveform for 1/2 Bias, 1/3 Duty

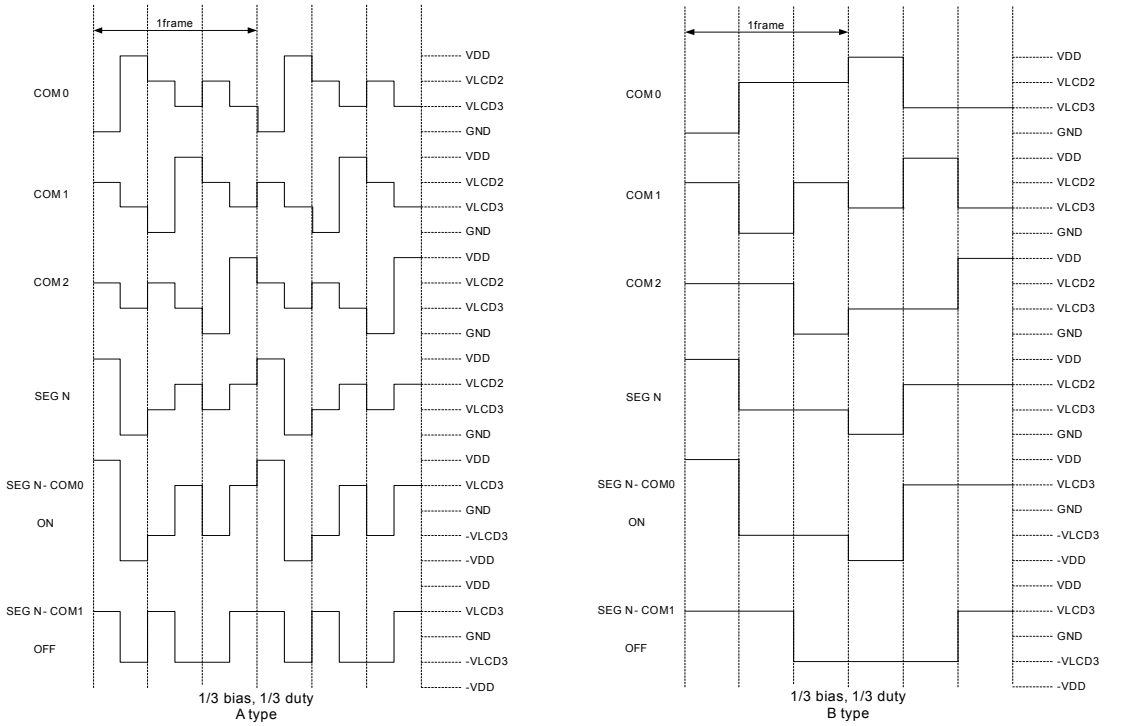


Fig. 20 LCD Waveform for 1/3 Bias, 1/3 Duty

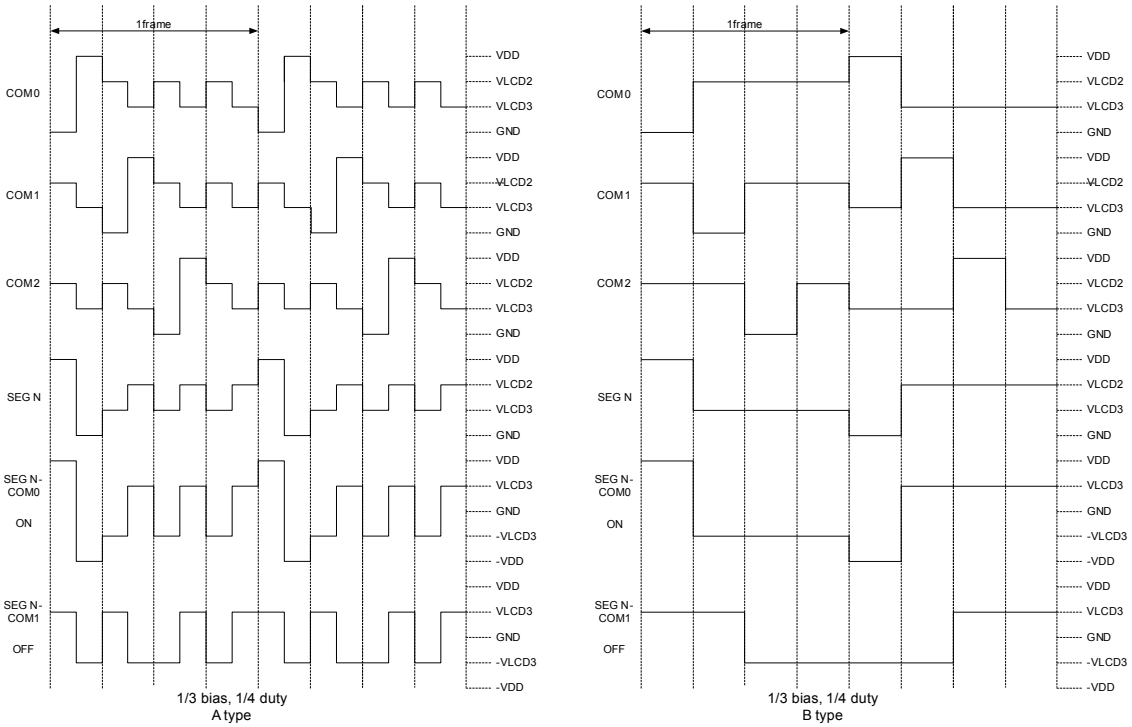


Fig. 21 LCD Waveform for 1/3 Bias, 1/4 Duty

4.10 Infrared Remote Control Application / PWM Waveform Generate

This LSI can output infrared carrier in a friendly manner or in PWM standard waveform. The IR and PWM waveform generated functions include an 8-bit down count timer/counter, high-pulse width timer, low-pulse width timer, and IR control register. The IR system block diagram is show in Fig.21, The IROUT pin waveform is determined by IR control register (RE), IOC90 (Counter 1, 2 control register), IOCA0 (high-pulse width timer, low-pulse width timer control register), IOCC0 (Counter 2 preset), IOCD0 (high-pulse width timer preset register), and IOCE0 (low-pulse width timer preset register). Details on Fcarrier, high-pulse time, and low pulse time are explained as follows:

If Counter 2 source clock is F_T (this clock source can set by IOC91);

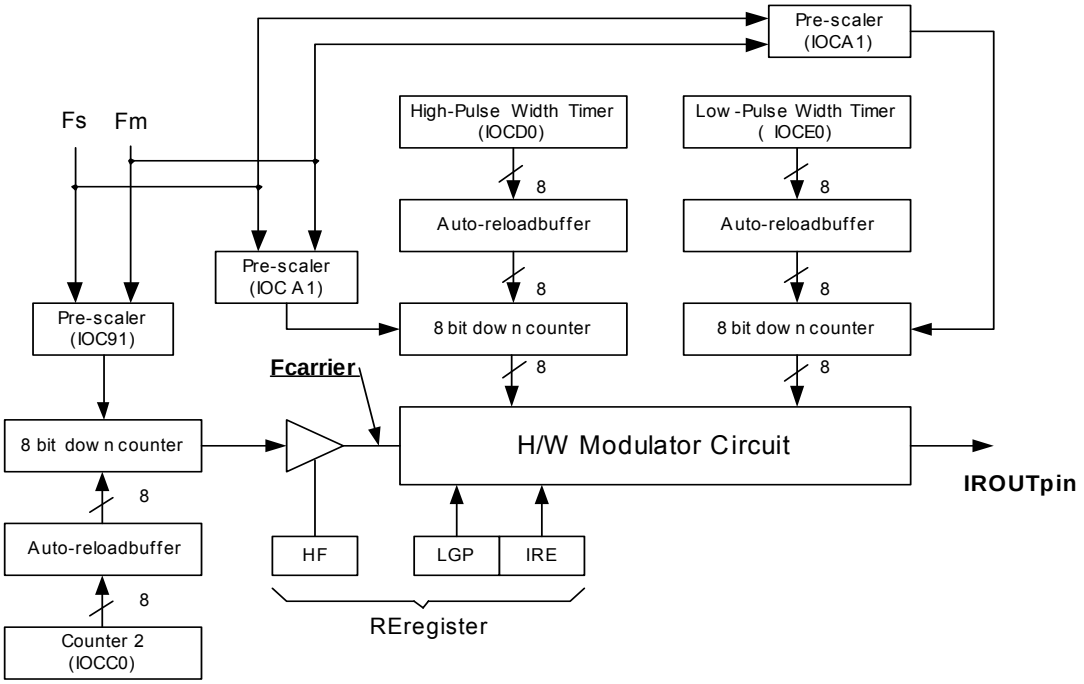
$$F_{carrier} = \frac{F_T}{2 * (1 + \text{decimal of counter2 preset value(IOCC0)}) * \text{prescaler}}$$

If high-pulse width timer source clock is FT (this clock source can set by IOCA1);

$$T_{\text{high pulse time}} = \frac{\text{prescaler} * (1 + \text{decimal of high pulse width timer value(IOCD0)})}{F_T}$$

If low-pulse width timer source clock is FT (this clock source can set by IOCA1);

$$T_{\text{low pulse time}} = \frac{\text{prescaler} * (1 + \text{decimal of low pulse width timer value(IOCE0)})}{F_T}$$



Fm: *main oscillator frequency*; **Fs:** *sub-oscillator frequency*

Fig. 21 IR/PWM System Block Diagram

The IROUT output waveform is further explained in the following figures:

Fig. 22 LGP=0, HF=1, the IROUT waveform can modulate Fcarrier waveform when in low-pulse width time.

Fig. 23 LGP=0, HF=0, the IROUT waveform cannot modulate Fcarrier waveform when in low-pulse width time. So IROUT waveform is determined by high-pulse time and low-pulse time. This mode can produce standard PWM waveform

Fig. 24 LGP=0, HF=1, the IROUT waveform can modulate Fcarrier waveform when in low-pulse width time. When IRE goes from high to low, the output waveform of IROUT will keep on transmitting till high-pulse width timer interrupt occurs.

Fig. 25 LGP=0, HF=0, the IROUT waveform can not modulate Fcarrier waveform when in low-pulse width time. So IROUT waveform is determined by high-pulse time and low-pulse time. This mode can produce standard PWM waveform. When IRE goes from high to low, the output waveform of IROUT will keep on transmitting till high-pulse width timer interrupt occurs.

Fig.26 LGP=1, when this bit is set to high level, the high-pulse width timer is ignored. So IROUT waveform output from low-pulse width timer is established.

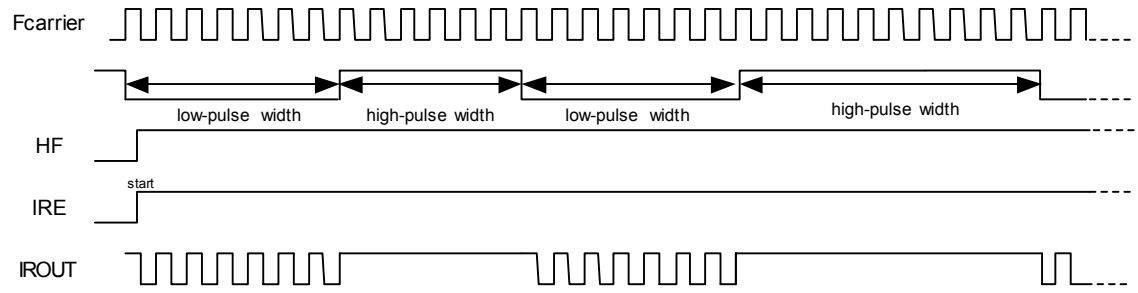


Fig. 22 LGP=0, IROUT Pin Output Waveform

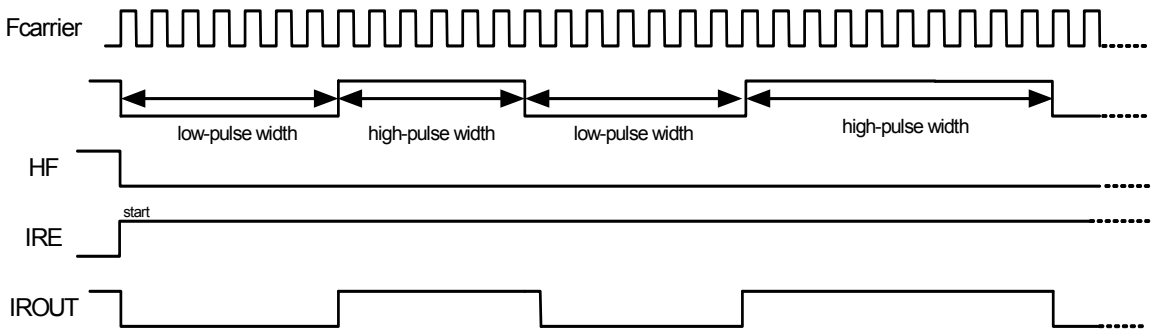


Fig. 23 LGP=0, IROUT Pin Output Waveform

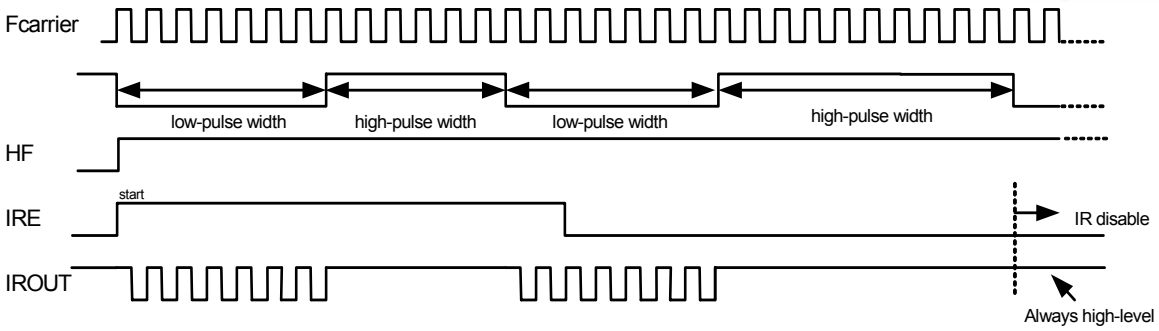


Fig. 24 LGP=0, IROUT Pin Output Waveform

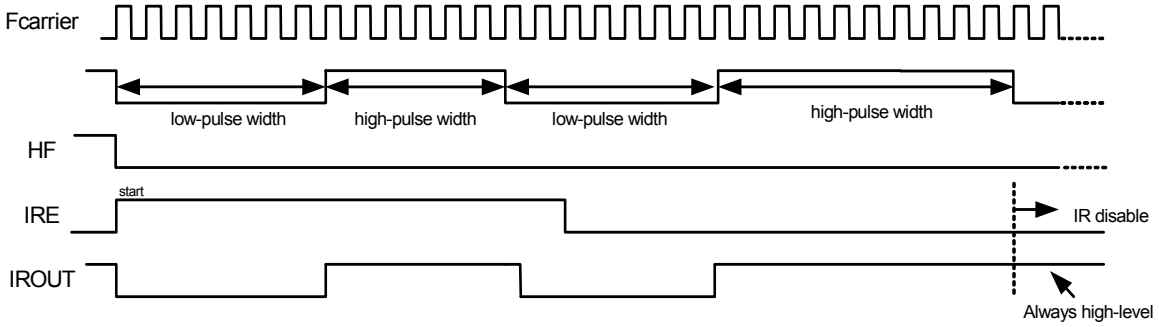


Fig. 25 LGP=0, IROUT Pin Output Waveform

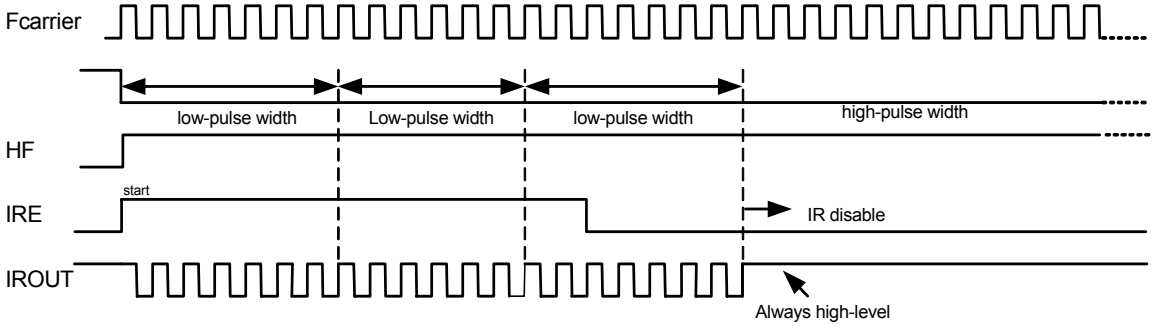


Fig. 26 LGP=1, IROUT Pin Output Waveform

IR/PWM function enable flowchart

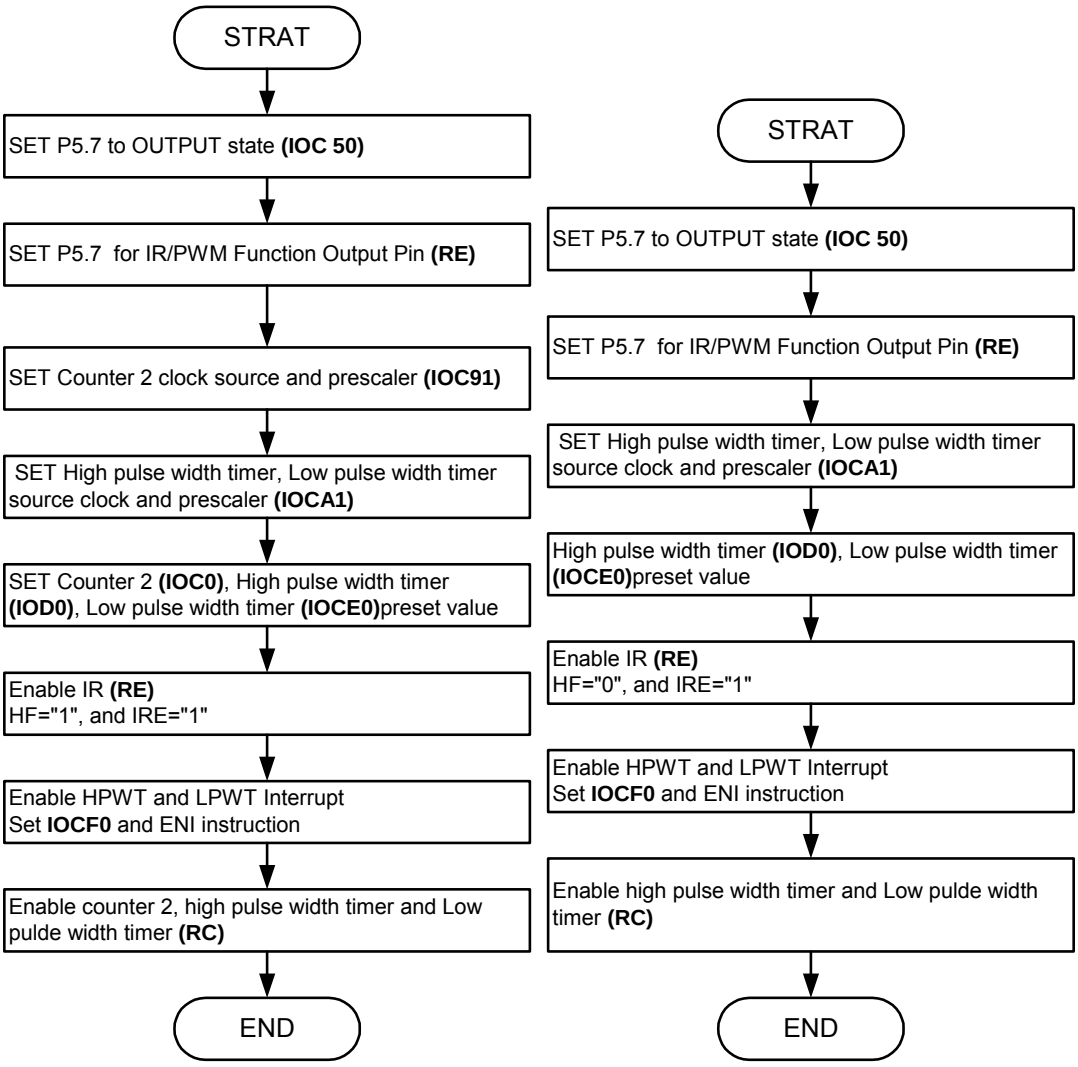


Fig. 27 IR/PWM Function Enable Flowchart

4.11 Code Options

The EM78P468N has one Code Option word that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

Word1 of code options is for customer ID code application.

Word 1
Bit12~Bit 0

Word 0 of Code Options is for IC function setting. The following are the settings for OTP IC programming**:**

Word 0										
Bit12~10	**Bit9**	**Bit8**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
1	CYES	HLFS	ENWDTB	FSMD	FMMD1	FMMD0	HLP	PR2	PR1	PR0

• **Bit 12 ~ 10:** Not used.

These bits are set to "1" all the time.

• **Bit 9 (CYES):** Cycle select for JMP and CALL instructions

CYES = "0": only one instruction cycle (JMP or CALL) can be executed

CYES = "1": two instructions cycles (JMP and CALL) can be executed

• **Bit 8 (HLFS):** main or sub-oscillator select

HLFS = "0": CPU is set to select sub-oscillator when reset occurs.

HLFS = "1": CPU is set to select main-oscillator when reset occurs.

• **Bit 7(ENWDTB):** Watchdog timer enable/disable bit.

ENWDTB = "0": Enable watchdog timer.

ENWDTB = "1": Disable watchdog timer.

• **Bit 6 (FSMD):** sub-oscillator type selection.

• **Bit 5, 4 (FMMD1, 0):** main Oscillator type selection.

FSMD	FMMD1	FMMD0	Main Oscillator Type	Sub Oscillator Type
0	0	0	RC type	RC type
0	0	1	XTAL type	RC type
0	1	X	PLL type	RC type
1	0	0	RC type	XTAL type
1	0	1	XTAL type	XTAL type
1	1	X	PLL type	XTAL type

• **Bit 3 (HLP):** Power consumption selection. If your system usually runs in green mode, it must be set to low power consumption to help support the energy saving issue. We recommend that low power consumption mode is slected.

HLP = "0": Low power consumption mode

HLP = "1": High power consumption mode

Bit 2~0 (PR2~PR0): Protect Bit

PR2~PR0 are protect bits as explained below:

PR2	PR1	PR0	Protect
1	1	1	Disable
Others			Enable

4.12 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", ····). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows**:**

Execute within two instruction cycles the "JMP", "CALL", "RET", "RETL", & "RETI" instructions, or the conditional skip instructions ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") which were tested to be true. Also execute within two instruction cycles the instructions that are written to the program counter.

Additionally, the instruction set offers the following features**:**

(1)Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The symbol "R" represents a register designator that specifies which one of the registers (including operational registers and general purpose registers) is to be utilized by the instruction. "b" represents a bit field designator that selects the value for the bit that is located in the register "R", and affects operation. "k" represents an 8 or 10-bit constant or literal value.

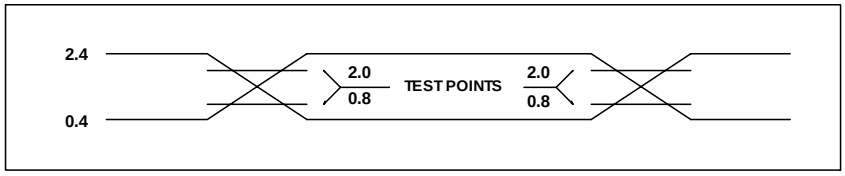
INSTRUCTION BINARY				HEX	MNEMONIC			OPERATION	STATUS AFFECTED
0	0000	0000	0000	0000	NOP			No Operation	None
0	0000	0000	0001	0001	DAA			Decimal Adjust A	C
0	0000	0000	0011	0003	SLEP			0 → WDT, Stop oscillator	T, P
0	0000	0000	0100	0004	WDTC			0 → WDT	T, P
0	0000	0000	rrrr	000r	IOW	R		A → IOCR	None <Note1>
0	0000	0001	0000	0010	ENI			Enable Interrupt	None
0	0000	0001	0001	0011	DISI			Disable Interrupt	None
0	0000	0001	0010	0012	RET			[Top of Stack] → PC	None
0	0000	0001	0011	0013	RETI			[Top of Stack] → PC, Enable Interrupt	None
0	0000	0001	rrrr	001r	IOR	R		IOCR → A	None <Note1>
0	0000	01rr	rrrr	00rr	MOV	R,	A	A → R	None
0	0000	1000	0000	0080	CLRA			0 → A	Z
0	0000	11rr	rrrr	00rr	CLR	R		0 → R	Z
0	0001	00rr	rrrr	01rr	SUB	A,	R	R-A → A	Z, C, DC
0	0001	01rr	rrrr	01rr	SUB	R,	A	R-A → R	Z, C, DC
0	0001	10rr	rrrr	01rr	DECA	R		R-1 → A	Z
0	0001	11rr	rrrr	01rr	DEC	R		R-1 → R	Z
0	0010	00rr	rrrr	02rr	OR	A,	R	A ∨ R → A	Z
0	0010	01rr	rrrr	02rr	OR	R,	A	A ∨ R → R	Z
0	0010	10rr	rrrr	02rr	AND	A,	R	A & R → A	Z
0	0010	11rr	rrrr	02rr	AND	R,	A	A & R → R	Z
0	0011	00rr	rrrr	03rr	XOR	A,	R	A ⊕ R → A	Z
0	0011	01rr	rrrr	03rr	XOR	R,	A	A ⊕ R → R	Z
0	0011	10rr	rrrr	03rr	ADD	A,	R	A + R → A	Z, C, DC
0	0011	11rr	rrrr	03rr	ADD	R,	A	A + R → R	Z, C, DC
0	0100	00rr	rrrr	04rr	MOV	A,	R	R → A	Z
0	0100	01rr	rrrr	04rr	MOV	R,	R	R → R	Z
0	0100	10rr	rrrr	04rr	COMA	R		/R → A	Z
0	0100	11rr	rrrr	04rr	COM	R		/R → R	Z
0	0101	00rr	rrrr	05rr	INCA	R		R+1 → A	Z
0	0101	01rr	rrrr	05rr	INC	R		R+1 → R	Z
0	0101	10rr	rrrr	05rr	DJZA	R		R-1 → A, skip if zero	None
0	0101	11rr	rrrr	05rr	DJZ	R		R-1 → R, skip if zero	None
0	0110	00rr	rrrr	06rr	RRCA	R		R(n) → A(n-1), R(0) → C, C → A(7)	C
0	0110	01rr	rrrr	06rr	RRC	R		R(n) → R(n-1), R(0) → C, C → R(7)	C
0	0110	10rr	rrrr	06rr	RLCA	R		R(n) → A(n+1), R(7) → C, C → A(0)	C
0	0110	11rr	rrrr	06rr	RLC	R		R(n) → R(n+1), R(7) → C, C → R(0)	C
0	0111	00rr	rrrr	07rr	SWAPA	R		R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0	0111	01rr	rrrr	07rr	SWAP	R		R(0-3) ↔ R(4-7)	None
0	0111	10rr	rrrr	07rr	JZA	R		R+1 → A, skip if zero	None
0	0111	11rr	rrrr	07rr	JZ	R		R+1 → R, skip if zero	None
0	100b	bbrr	rrrr	0xxx	BC	R,	b	0 → R(b)	None
0	101b	bbrr	rrrr	0xxx	BS	R,	b	1 → R(b)	None

INSTRUCTION BINARY				HEX	MNEMONIC			OPERATION	STATUS AFFECTED
0	110b	bbrr	rrrr	0xxx	JBC	R,	b	if R(b)=0, skip	None
0	111b	bbrr	rrrr	0xxx	JBS	R,	b	if R(b)=1, skip	None
1	00kk	kkkk	kkkk	1kkk	CALL	k		PC+1 → [SP], (Page, k) → PC	None
1	01kk	kkkk	kkkk	1kkk	JMP	k		(Page, k) → PC	None
1	1000	kkkk	kkkk	18kk	MOV	A,	k	k → A	None
1	1001	kkkk	kkkk	19kk	OR	A,	k	A ∨ k → A	Z
1	1010	kkkk	kkkk	1Akk	AND	A,	k	A & k → A	Z
1	1011	kkkk	kkkk	1Bkk	XOR	A,	k	A ⊕ k → A	Z
1	1100	kkkk	kkkk	1Ckk	RETL	k		k → A, [Top of Stack] → PC	None
1	1101	kkkk	kkkk	1Dkk	SUB	A,	k	k-A → A	Z, C, DC
1	1110	1000	00kk	1E8k	PAGE	k		k->R5(1:0)	None
1	1110	1001	00kk	1E9K	BANK	k		k->R4(7:6)	None
1	1111	kkkk	kkkk	1Fkk	ADD	A,	k	k+A → A	Z, C, DC

<Note1> This instruction is applicable to IOC50 ~ IOCF0, IOC61 ~ IOCE1

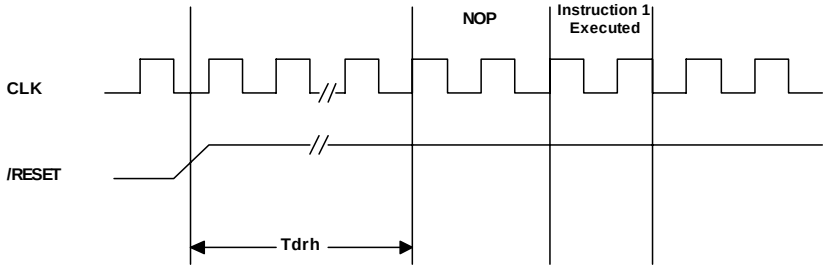
4.13 Timing Diagram

AC Test Input/Output Waveform

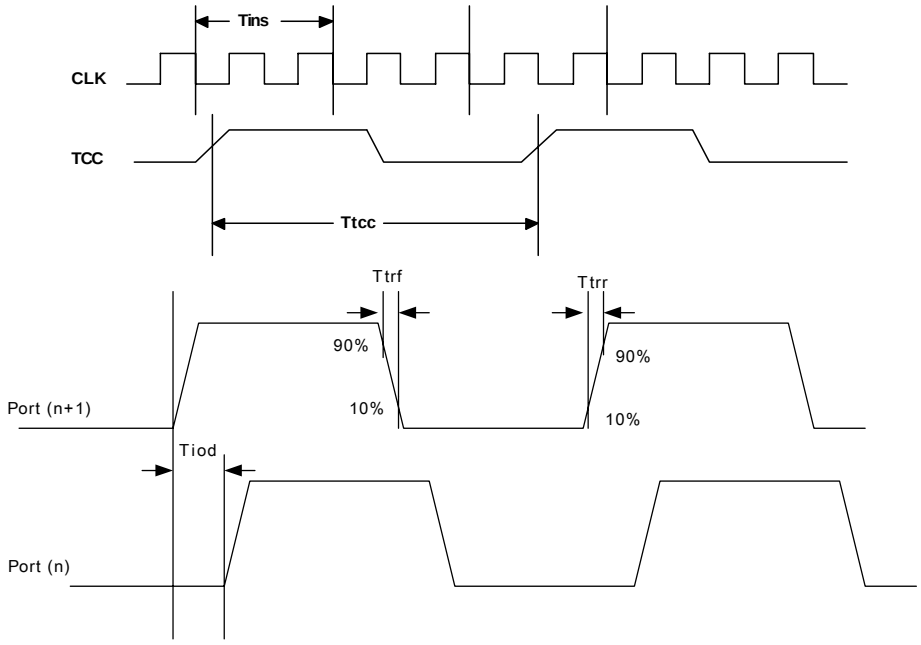


AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



*n=0、2、4、6

5 ABSOLUTE MAXIMUM RATINGS

Items	Symbol	Condition	Rating		Unit
			Min.	Max.	
Supply voltage	VDD		GND-0.3	+7.0	V
Input voltage	V_I	PORT 5, PORT 6, PORT 7, PORT 8	GND-0.3	VDD+0.3	V
Output voltage	V_O	PORT 5, PORT 6, PORT 7, PORT 8	GND-0.3	VDD+0.3	V
Operation temperature	T_{OPR}		-40	85	℃
Storage temperature	T_{STG}		-65	150	℃
Power dissipation	P_D			500	mW
Operating Frequency			32.768K	10M	Hz

6 ELECTRICAL CHARACTERISTIC

6.1 DC Electrical Characteristics

(Ta= 25 °C, VDD= 5.0V, GND= 0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	XTAL: VDD to 5V	Two cycle with two clocks	32.768K	8M	10M	Hz
Fs	Sub-oscillator	Two cycle with two clocks		32.768		KHz
ERIC	External R, internal C for sub-oscillator	R: 300KΩ, internal capacitance	270	384	500	KHz
	External R, internal C for sub-oscillator	R: 2.2MΩ, internal capacitance	22.9	32.768	42.6	KHz
IIL	Input Leakage Current for input pins	VIN = VDD, GND	-1	0	1	μA
VIH1	I Input High Threshold Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	2.4			V
VIL1	Input High Threshold Voltage (Schmitt trigger)	Ports 5, 6, 7, 8			0.8	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	2.4			V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET			0.8	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC, INT0, INT1	2.4			V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC, INT0, INT1			0.8	V
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = 2.4V, IROCS=”0”	-10			mA
IOL1	Output Low Voltage (Ports 5, 6, 7, 8)	VOL = 0.4V, IROCS=”0”			10	mA
IOH1	Output high voltage (P5.7/IROUT pin)	VOH = 2.4V, IROCS=”1”	-20			mA
IOL2	Output Low Voltage (P5.7/IR OUT pin)	VOL = 0.4V, IROCS=”1			20	mA
IPH	Pull-high current	Pull-high active, input pin at GND	-55	-75	-95	μA
IPL	Pull-low current	Pull-low active, input pin at VDD	55	75	95	μA
ISB	Sleep mode current	All input and I/O pins at VDD, output pin floating, WDT disabled		0.5	1.5	μA
ICC1	Idle mode current	/RESET= 'High', CPU OFF, sub-oscillator clock (32.768KHz) ON, output pin floating, LCD enable, no load		14	18	μA
ICC2	Green mode current	/RESET= 'High', CPU ON, used sub-oscillator clock (32.768KHz), output pin floating, WDT enabled, LCD enable		22	30	μA
ICC3	Normal mode	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), output pin floating		2.2	3	mA
ICC4	Normal mode	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), output pin floating		3.1	4	mA

(Ta= 25 °C, VDD= 3.0V, GND= 0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	XTAL: VDD to 5V	Two cycle with two clocks	32.768K	8M	10M	Hz
Fs	Sub-oscillator	Two cycle with two clocks		32.768		KHz
ERIC	External R, internal C for sub-oscillator	R: 300KΩ, internal capacitance	270	384	500	KHz
	External R, internal C for sub-oscillator	R: 2.2MΩ, internal capacitance	22.9	32.768	42.6	KHz
IIL	Input Leakage Current for input pins	VIN = VDD, GND	-1	0	1	μA
VIH1	Input High Threshold Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	1.8			V
VIL1	Input Low Threshold Voltage (Schmitt trigger)	Ports 5, 6, 7, 8			0.6	V
VIHT1	Input High Threshold Voltage (Schmitt trigger)	/RESET	1.8			V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET			0.6	V
VIHT2	Input High Threshold Voltage (Schmitt trigger)	TCC, INT0, INT1	1.8			V
VILT2	Input Low Threshold Voltage (Schmitt trigger)	TCC, INT0, INT1			0.6	V
IOH1	Output High Voltage (Ports 5, 6, 7, 8)	VOH = 2.4V, IROCS="0"	-1.8			mA
IOL1	Output Low Voltage (Ports 5, 6, 7, 8)	VOL = 0.4V, IROCS="0"			6	mA
IOH1	Output high voltage (P5.7/IROUT pin)	VOH = 2.4V, IROCS="1	-3.5			mA
IOL2	Output Low Voltage (P5.7/IR OUT pin)	VOL = 0.4V, IROCS="1			12	mA
IPH	Pull-high current	Pull-high active, input pin at GND	-16	-23	-30	μA
IPL	Pull-low current	Pull-low active, input pin at VDD	16	23	30	μA
ISB	Sleep mode current	All input and I/O pins at VDD, output pin floating, WDT disabled		0.1	1	μA
ICC1	Idle mode current	/RESET= 'High', CPU OFF, sub-oscillator clock (32.768KHz) ON, output pin floating, LCD enable, no load		4	8	μA
ICC2	Green mode current	/RESET= 'High', CPU ON, used sub-oscillator clock (32.768KHz), output pin floating, WDT enabled, LCD enable		10	20	μA
ICC3	Normal mode	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), output pin floating		0.73	1.2	mA

6.2 AC Electrical Characteristics

(Ta=- 40°C ~ 85 °C, VDD=5V±5%, GND=0V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle		45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100		DC	ns
		RC type	500		DC	ns
Ttcc	TCC input period		(Tins+20)/N*			ns
Tdrh	Device reset hold time	Ta = 25°C	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000			ns
Twdt	Watchdog timer period	Ta = 25°C	11.3	16.2	21.6	ms
Tset	Input pin setup time			0		ns
Thold	Input pin hold time			20		ns
Tdelay	Output pin delay time	Cload=20pF		50		ns

* N= selected pre-scaler ratio.

6.3 Device Characteristic

The graphs provided in the following pages were derived based on a limited number of samples and are shown here for reference only. The device characteristic illustrated herein are not guaranteed for it accuracy. In some graphs, the data maybe out of the specified warranted operating range.

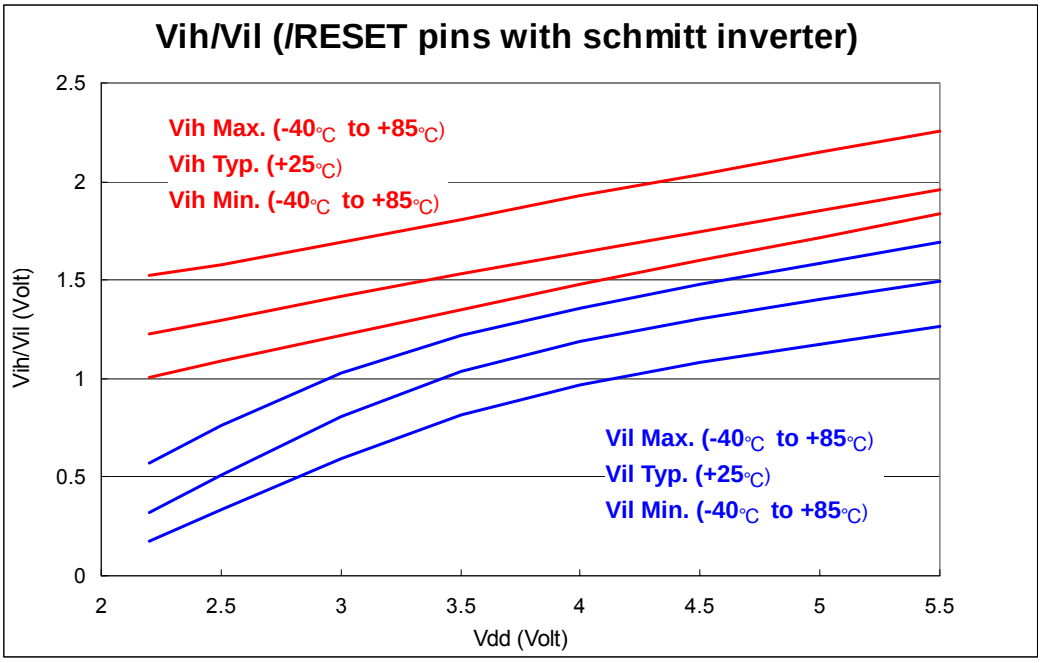


Fig. 28 Vih, Vil of /RESET Pin vs. VDD

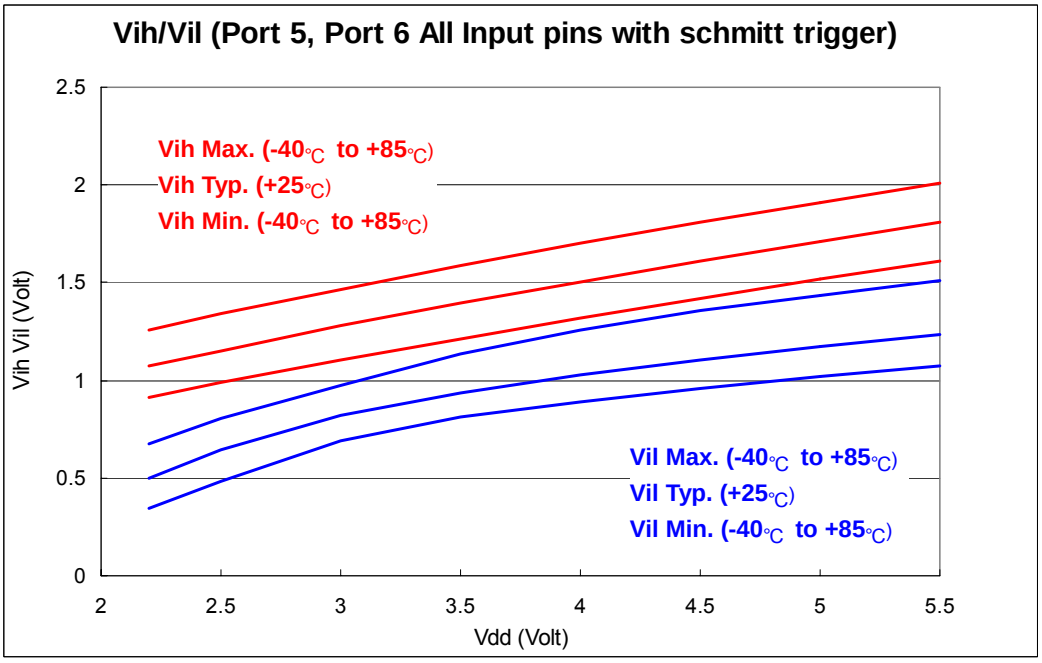


Fig. 29 Vih, Vil of PORT 5 and PORT 6 vs. VDD

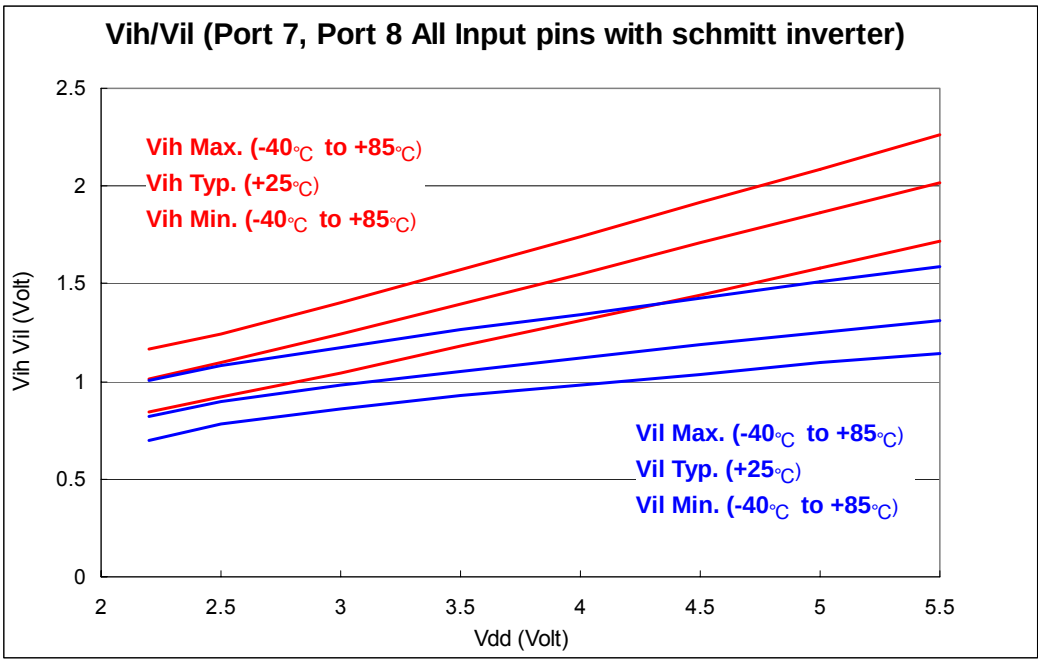


Fig. 30 Vih, Vil of PORT 7 and PORT 8 vs. VDD

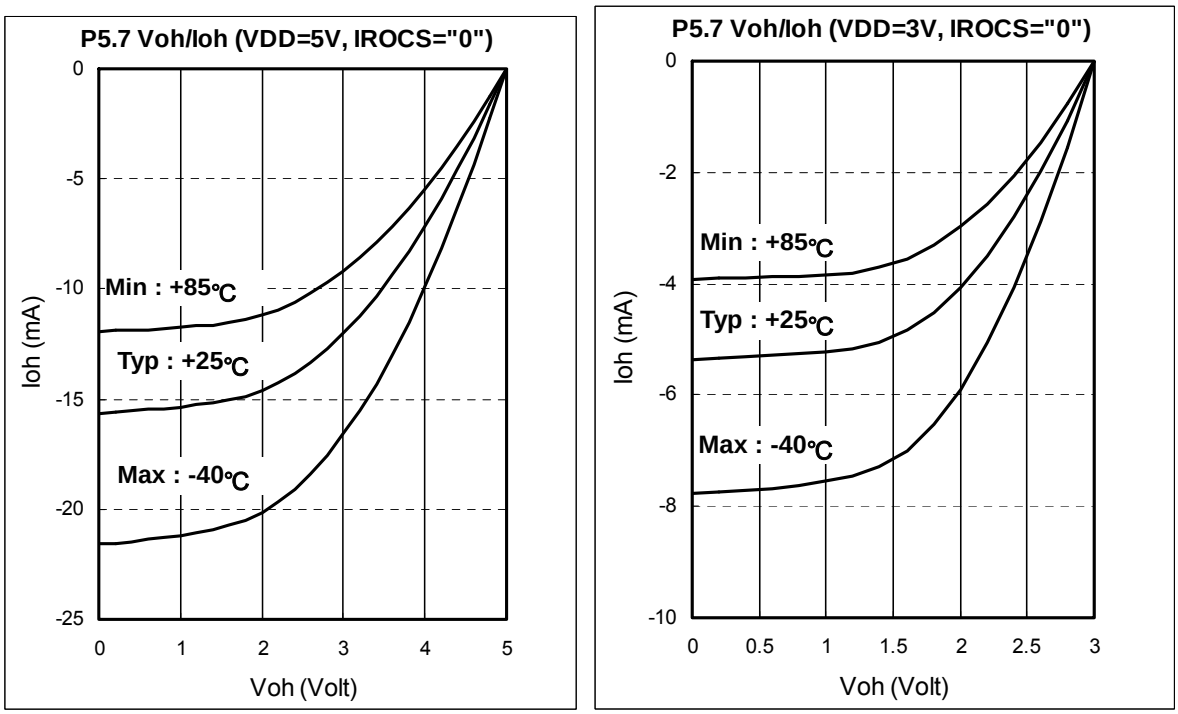


Fig. 31 Port 5.7 Voh vs. Ioh, [VDD=3V, 5V, IROCS (Bit 7 of IOC61) =" 0 "]

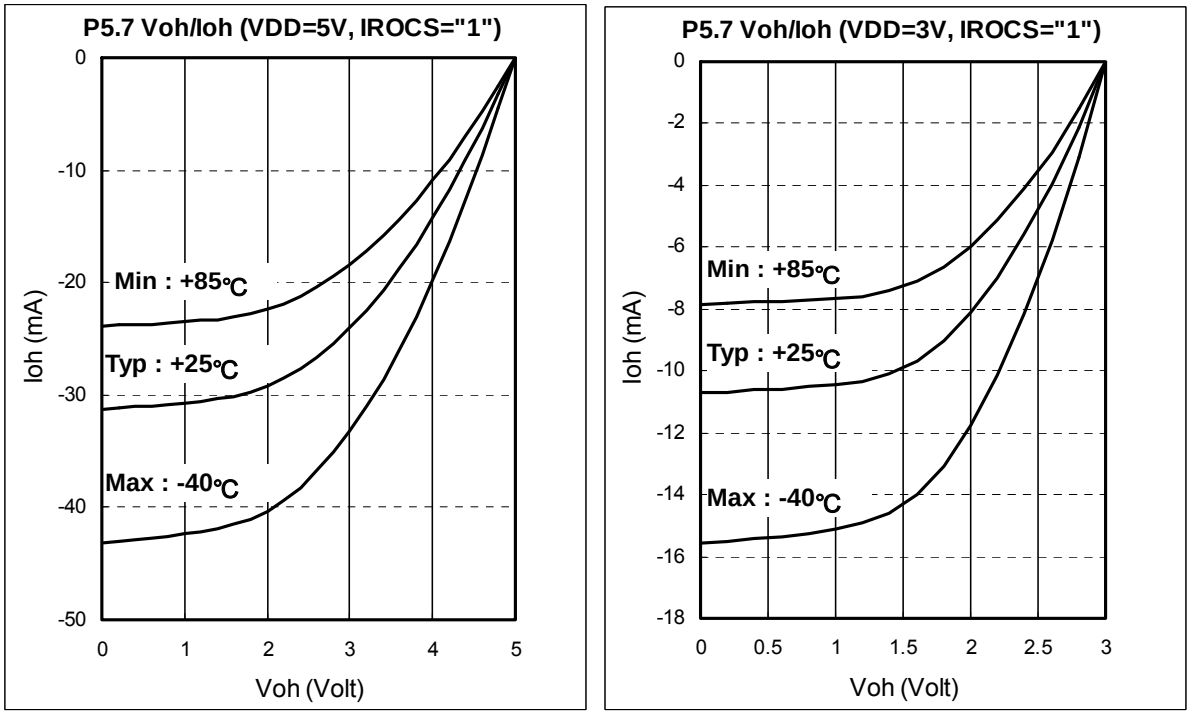


Fig. 32 Port 5.7 Voh vs. Ioh, [VDD=3V, 5V, IROCS (Bit 7 of IOC61) =" 1 "]

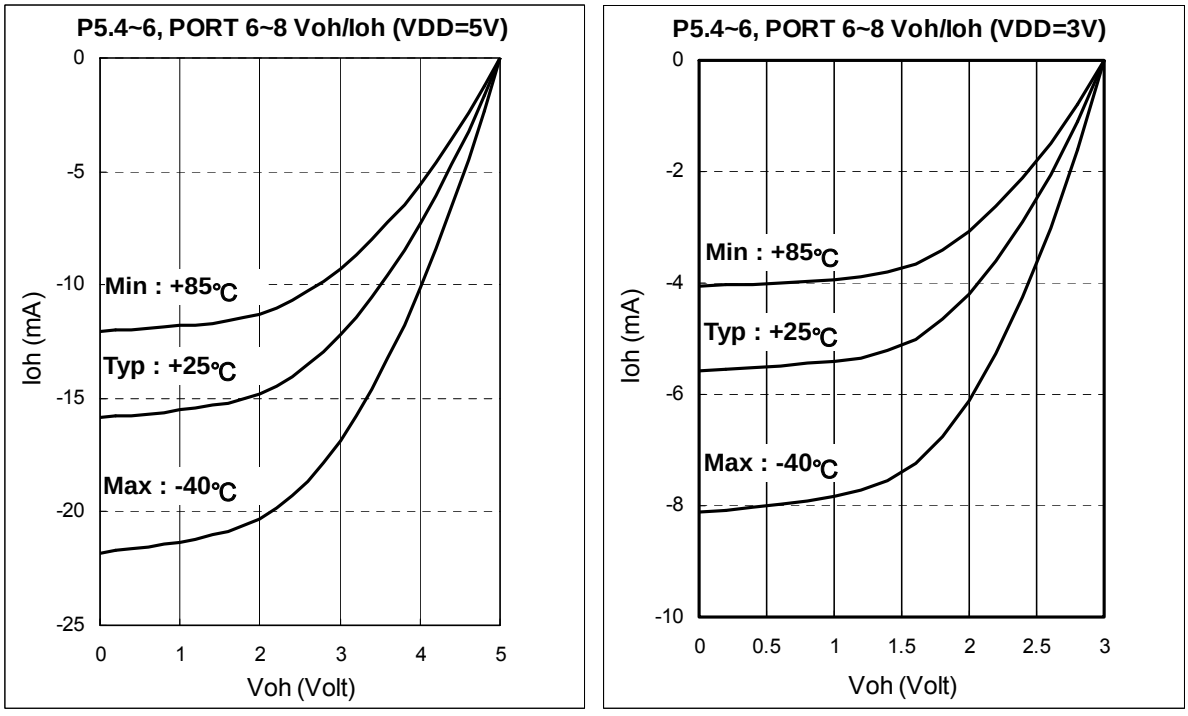


Fig. 33 Port 6, Port 7 and Port 8 Voh vs. Ioh [VDD=3V, 5V]

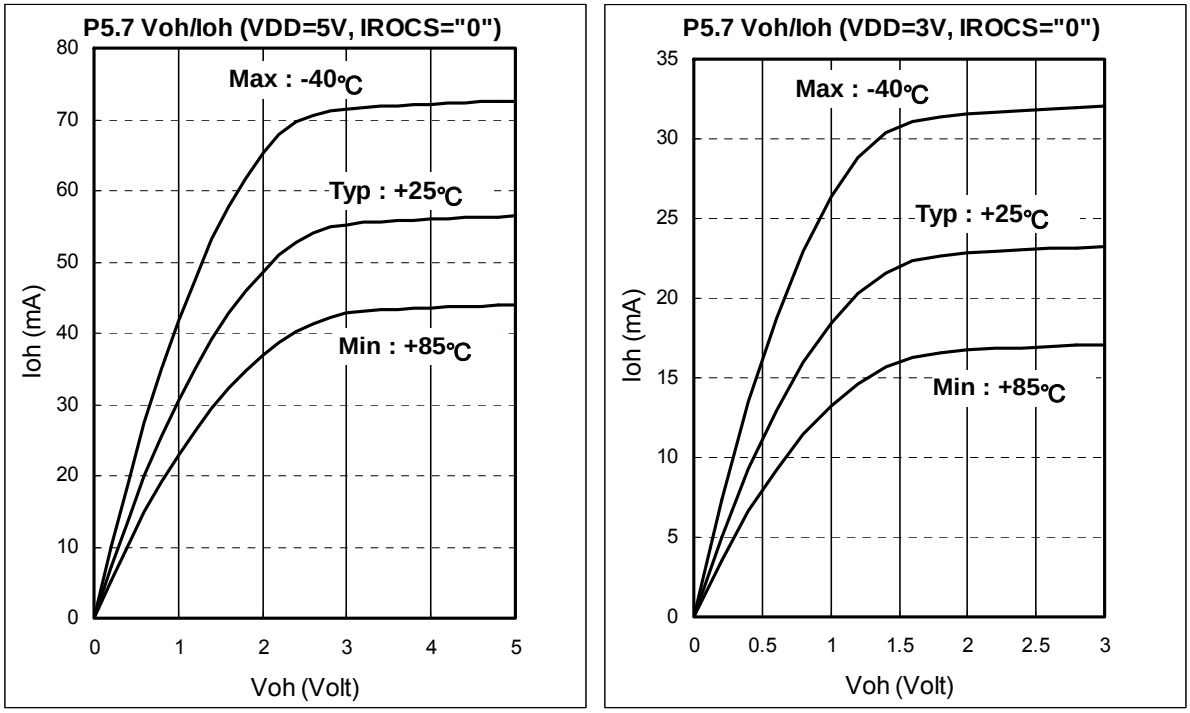


Fig. 34 Port 5.7 Vol vs. Iol, [VDD=3V, 5V, IROCS (Bit 7 of IOC61) =" 0 "]

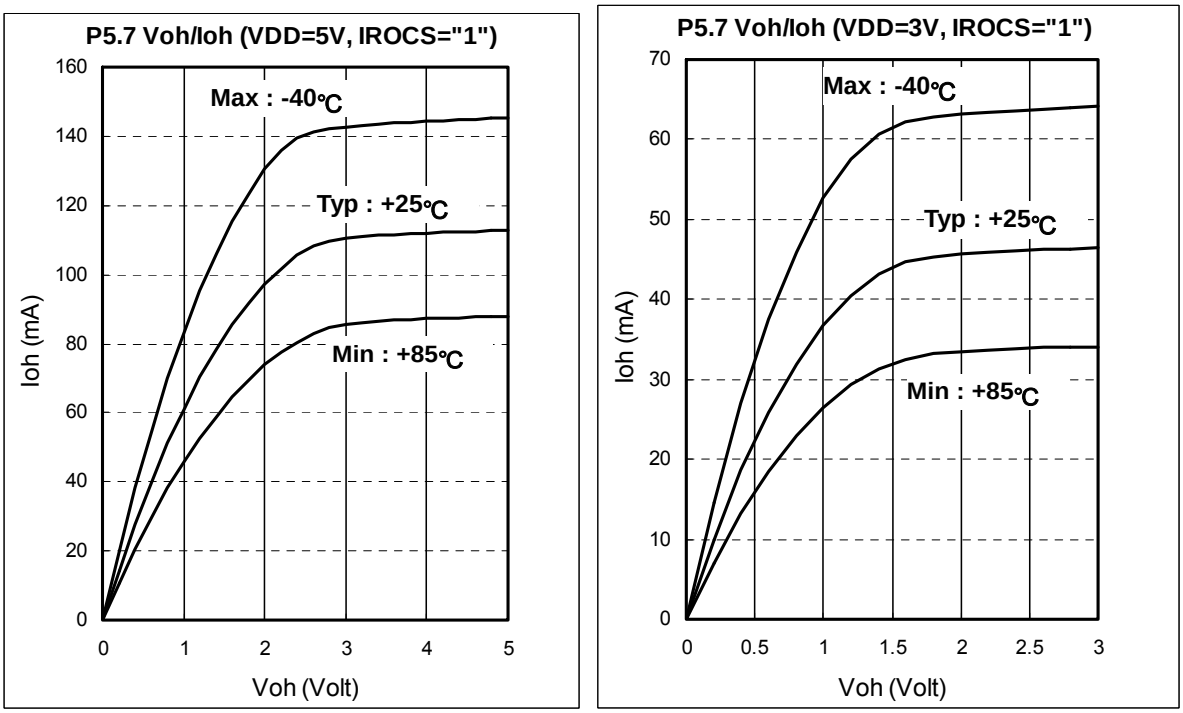


Fig. 35 Port 5.7 Vol vs. Iol, [VDD=3V, 5V, IROCS (Bit 7 of IOC61) =" 1 "]

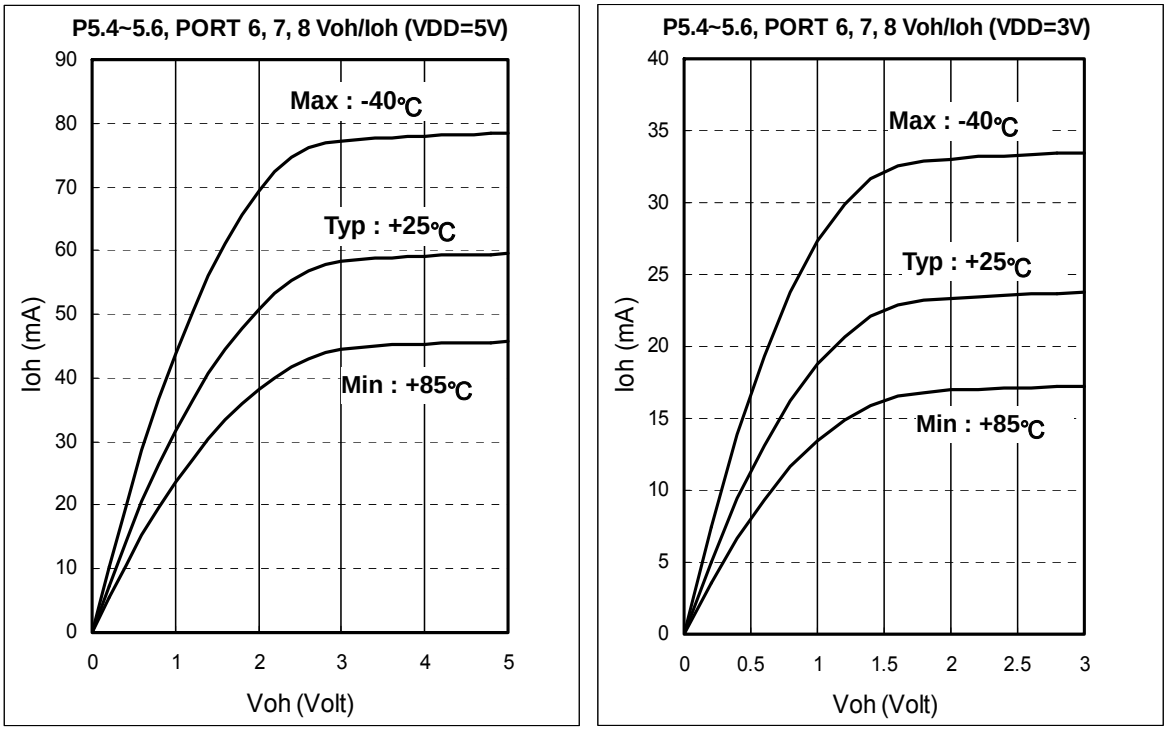


Fig. 36 Port 6, Port 7 and Port 8 Vol vs. Iol [VDD=3V, 5V]

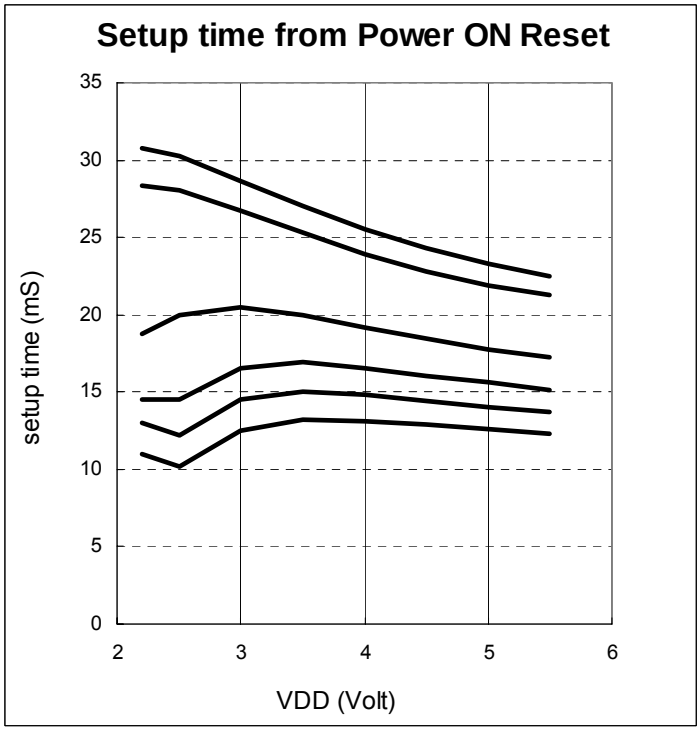


Fig. 37 WDT time out period vs. VDD, pre-scaler set to 1:1

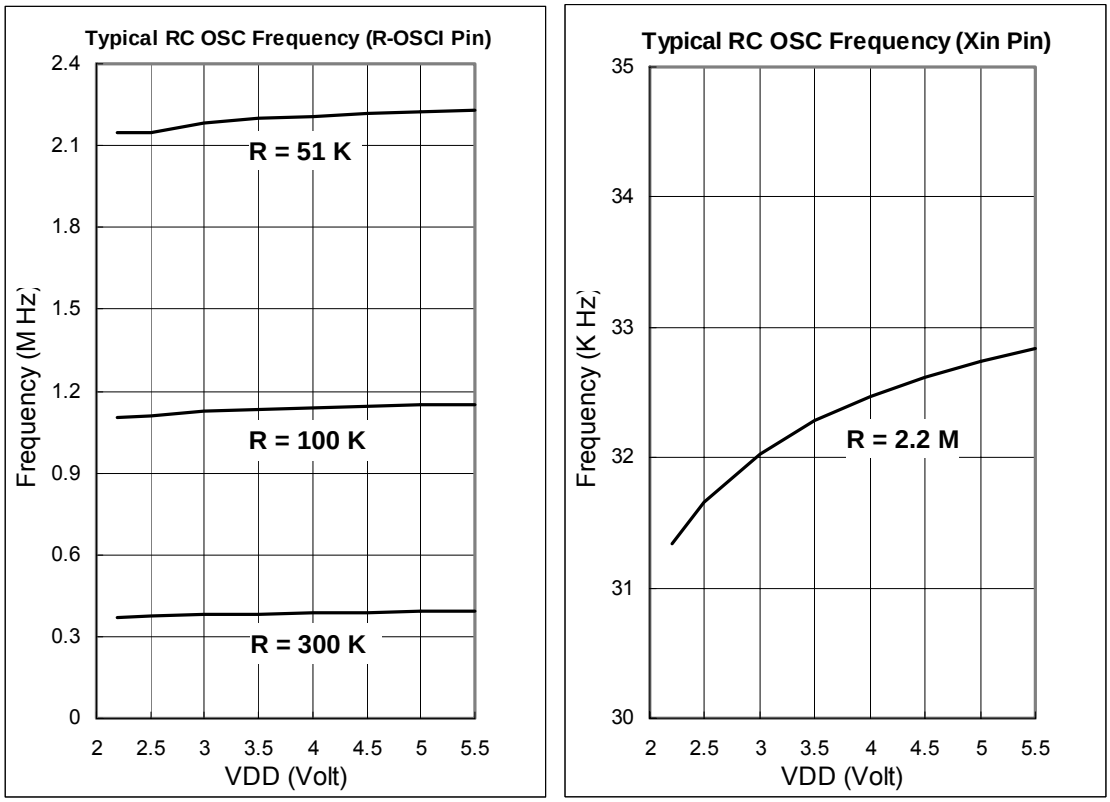


Fig. 38 Typical ERIC OSC Frequency vs. VDD (Temperature at 25℃)

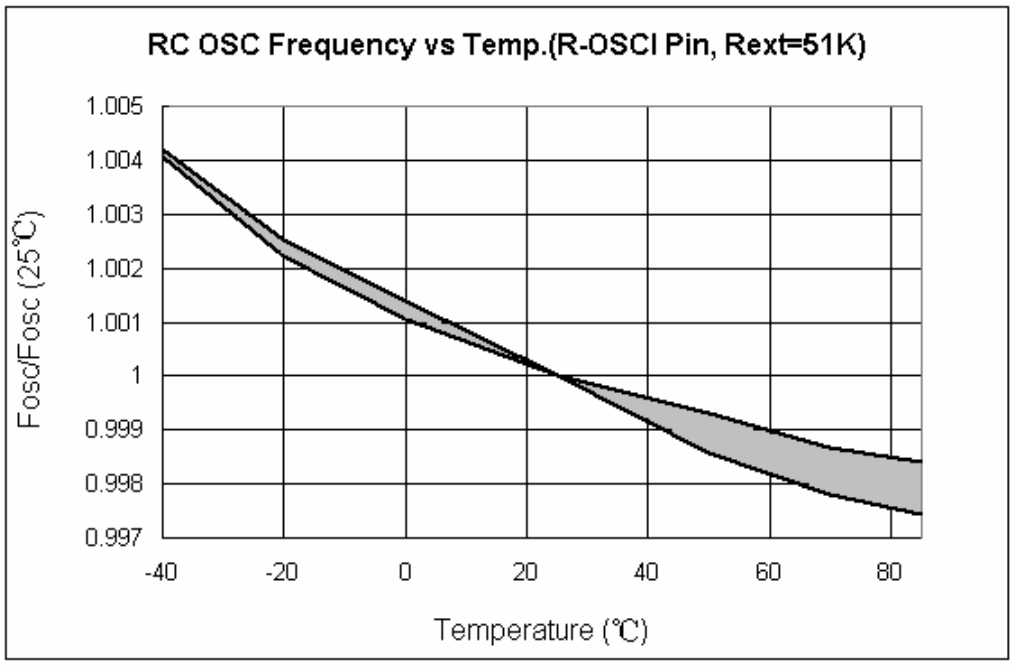


Fig. 39 Typical ERIC OSC Frequency vs. Temperature (R-OSCI Pin)

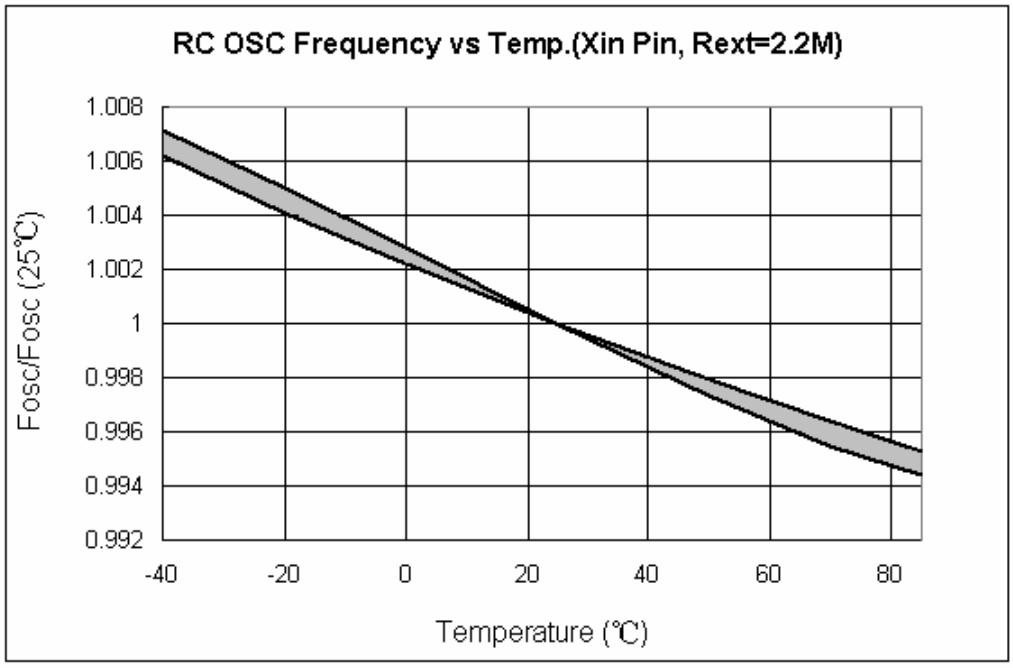


Fig. 40 Typical ERIC OSC Frequency vs. Temperature (Xin Pin)

Four conditions exist with the Operating Current ICC1 to ICC4. These conditions are as follows:

ISB (sleep mode): Fm and Fs is stop, all function off.

ICC1 (idle mode): Fm Stop and Fs=32K Hz, 2 clocks, CPU off, LCD enable and WDT Enable.

ICC2 (green mode): Fm Stop and Fs=32K Hz, 2 clocks, CPU running on Fs frequency, LCD enable and WDT Enable

ICC3 (normal mode): Fm=4M Hz and Fs=32K Hz, 2 clocks, CPU running on Fm frequency, LCD enable and WDT Enable

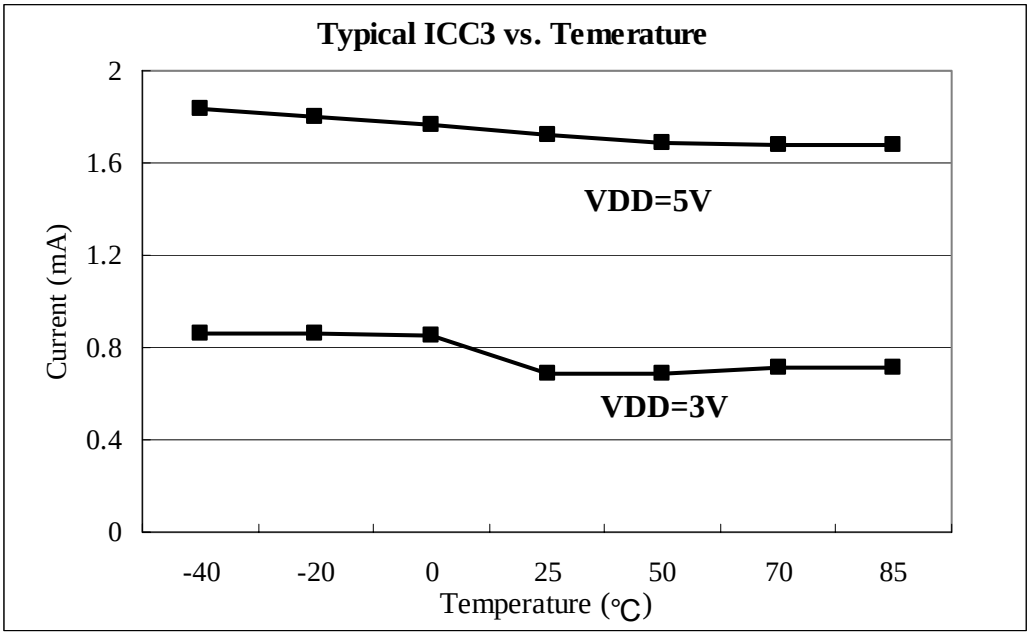


Fig. 40 Typical power consumption on normal mode operation (Fm=4MHz)

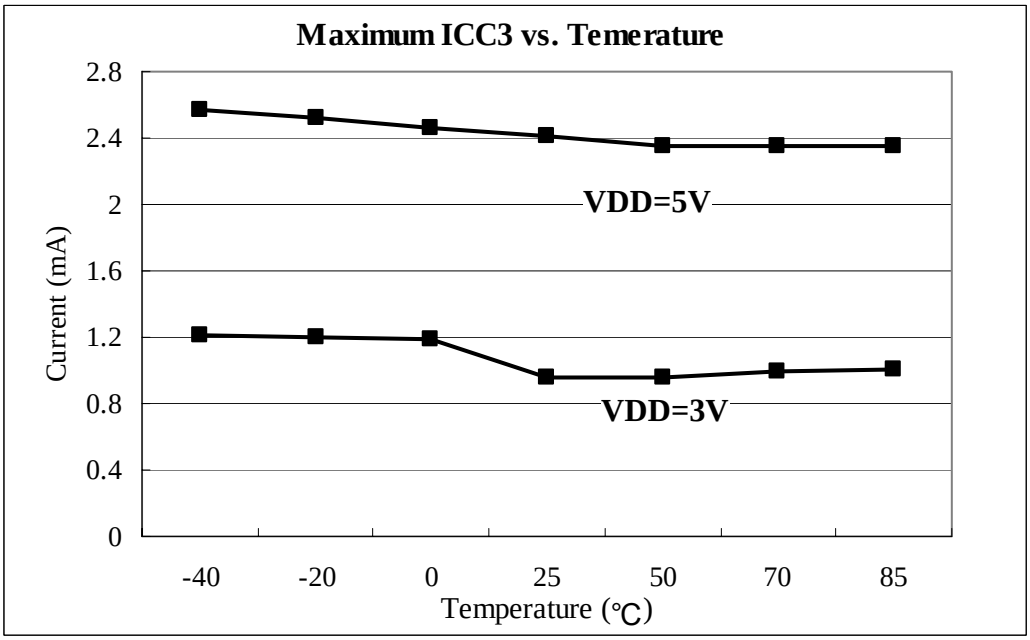


Fig. 41 Maximum power consumption on normal mode operation (Fm=4MHz)

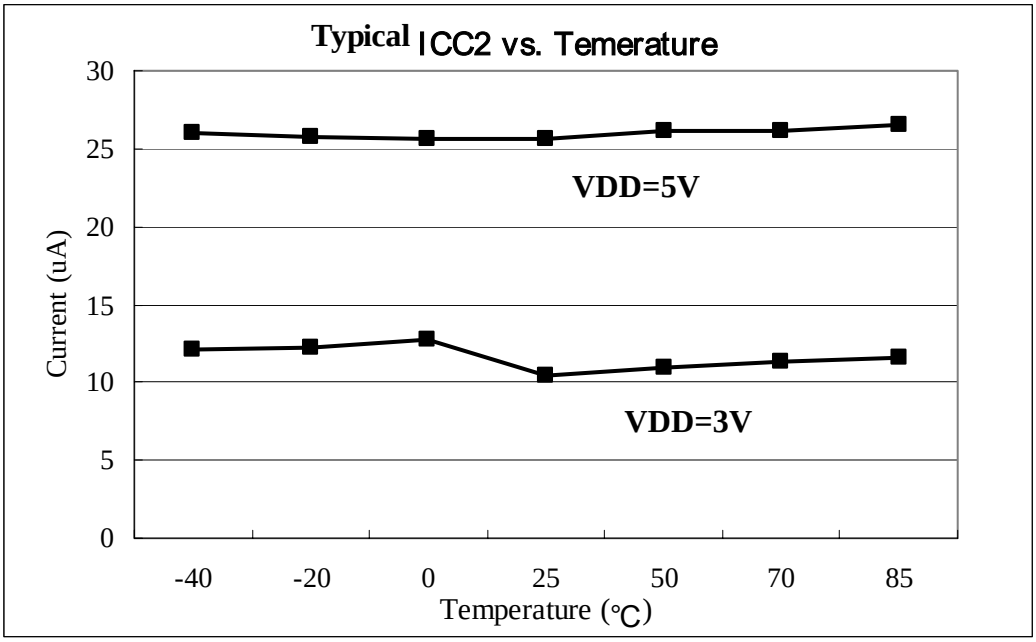


Fig. 42 Typical power consumption on green mode operation

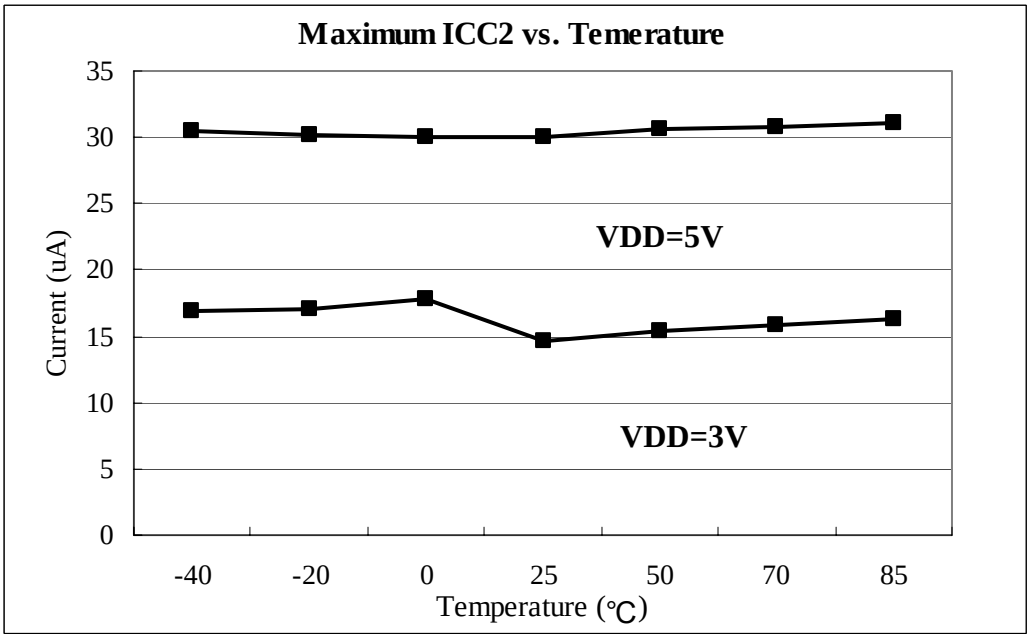


Fig. 43 Maximum power consumption on green mode operation

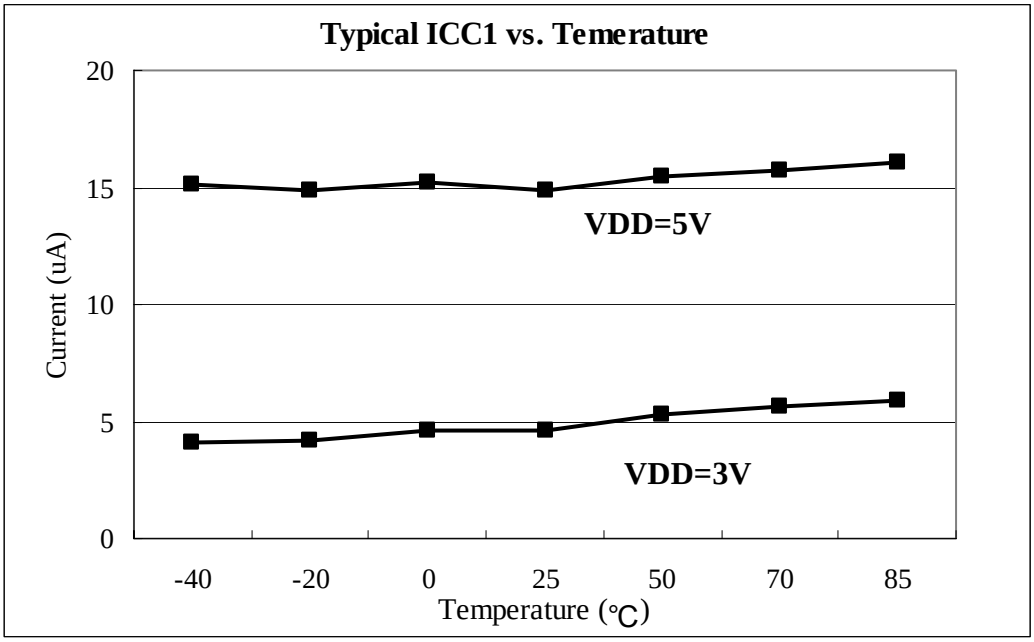


Fig. 44 Typical power consumption on idle mode operation

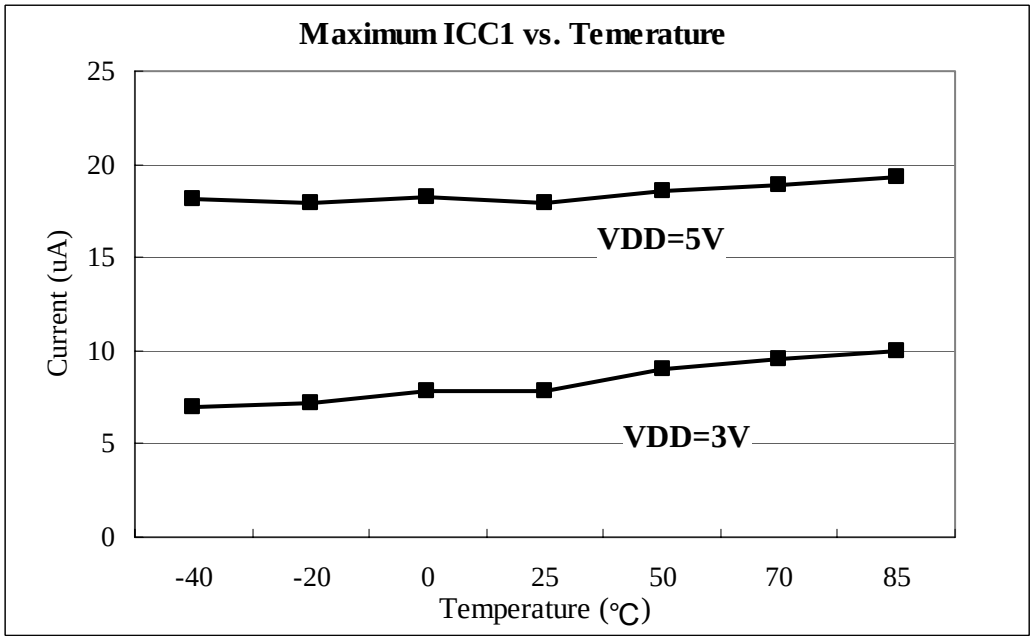


Fig. 45 Maximum power consumption on idle mode operation

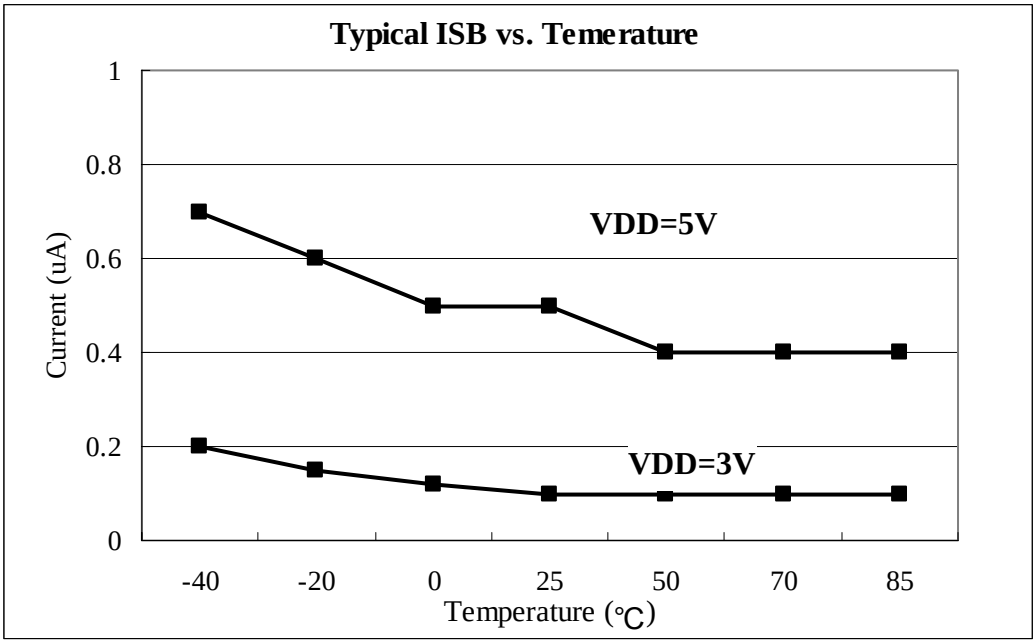


Fig. 46 Typical power consumption on sleep mode operation

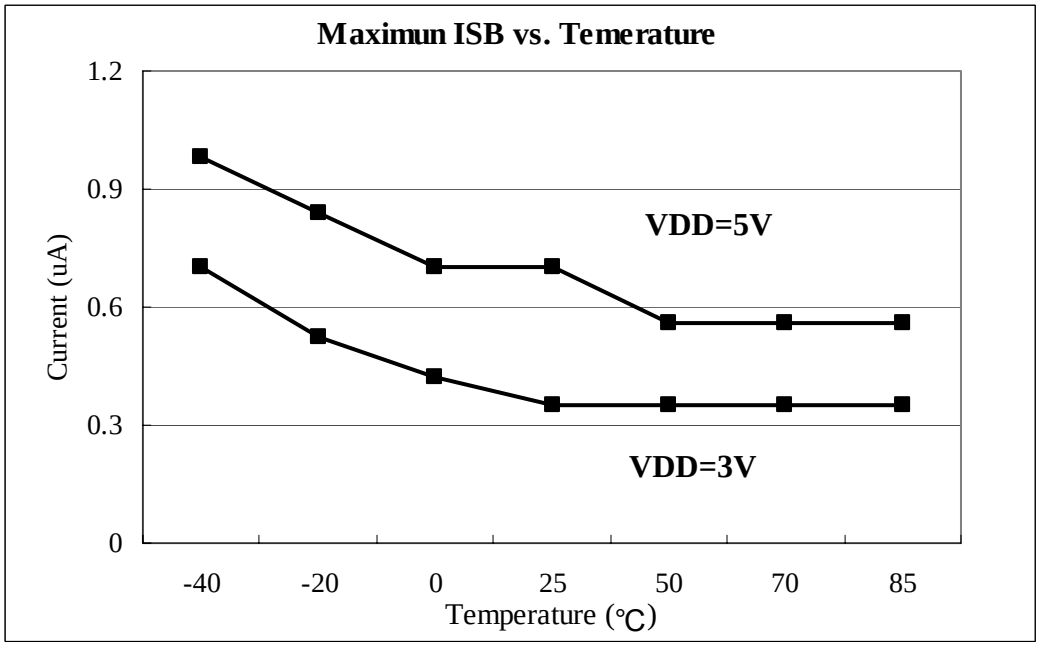


Fig. 47 Maximum power consumption on sleep mode operation

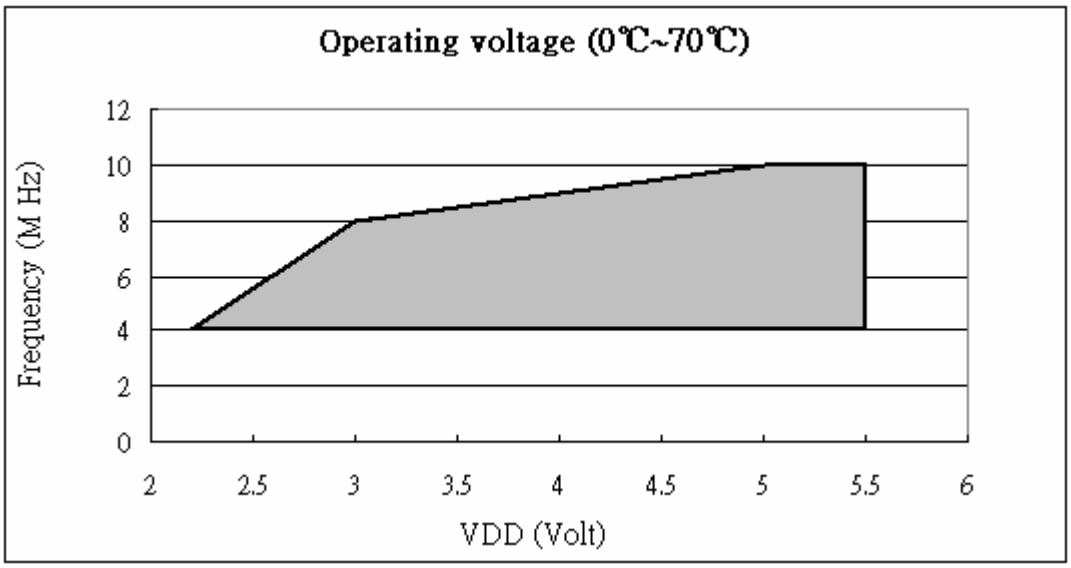


Fig. 48 Operating voltage under temperature range of 0℃ to 70℃

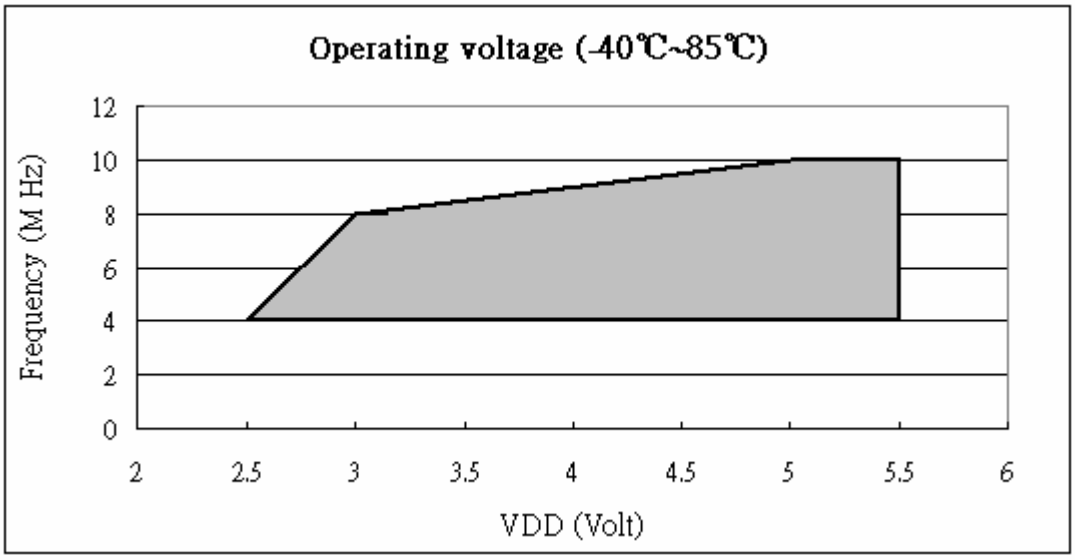


Fig. 49 Operating voltage under temperature range of -40℃ to +85℃

7 APPLICATION CIRCUIT

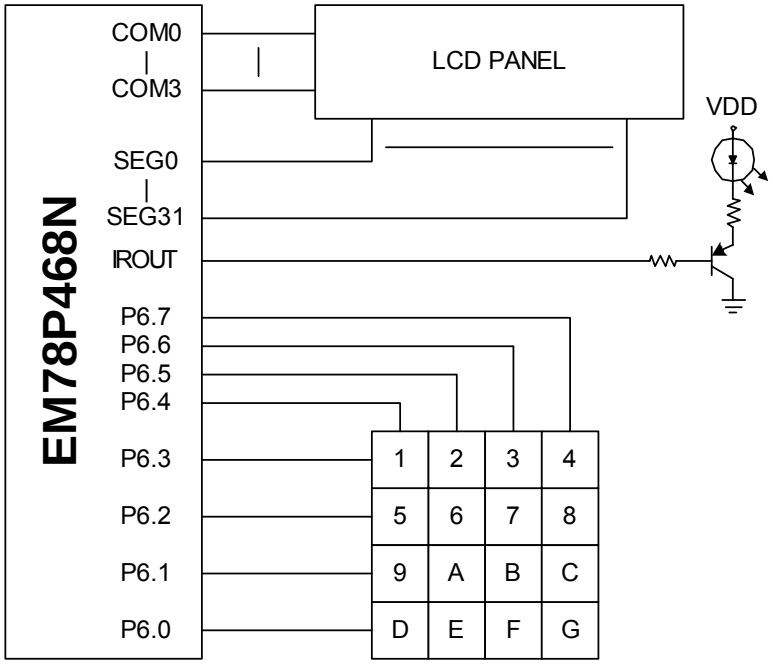


Fig. 50 IROUT control external BJT circuit to drive infrared emitting diodes

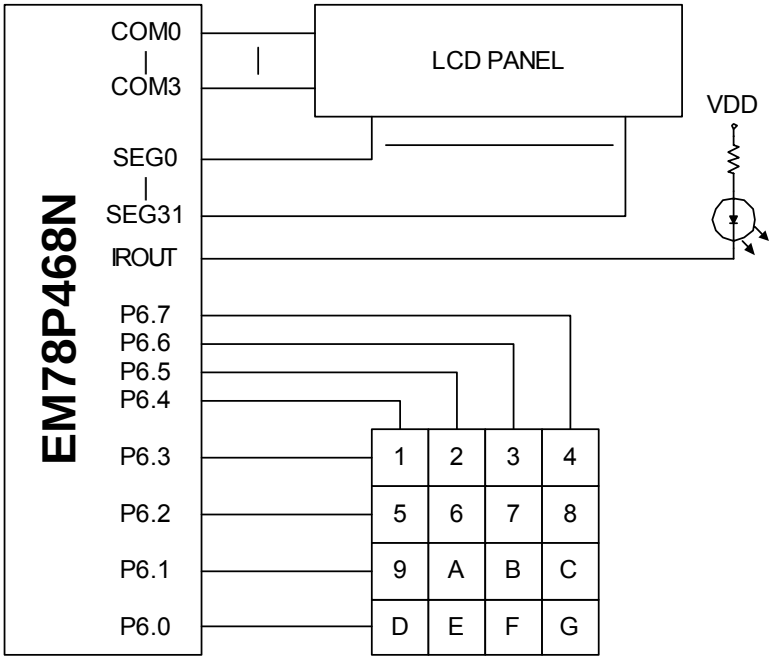


Fig. 51 IROUT direct drive infrared emitting diodes

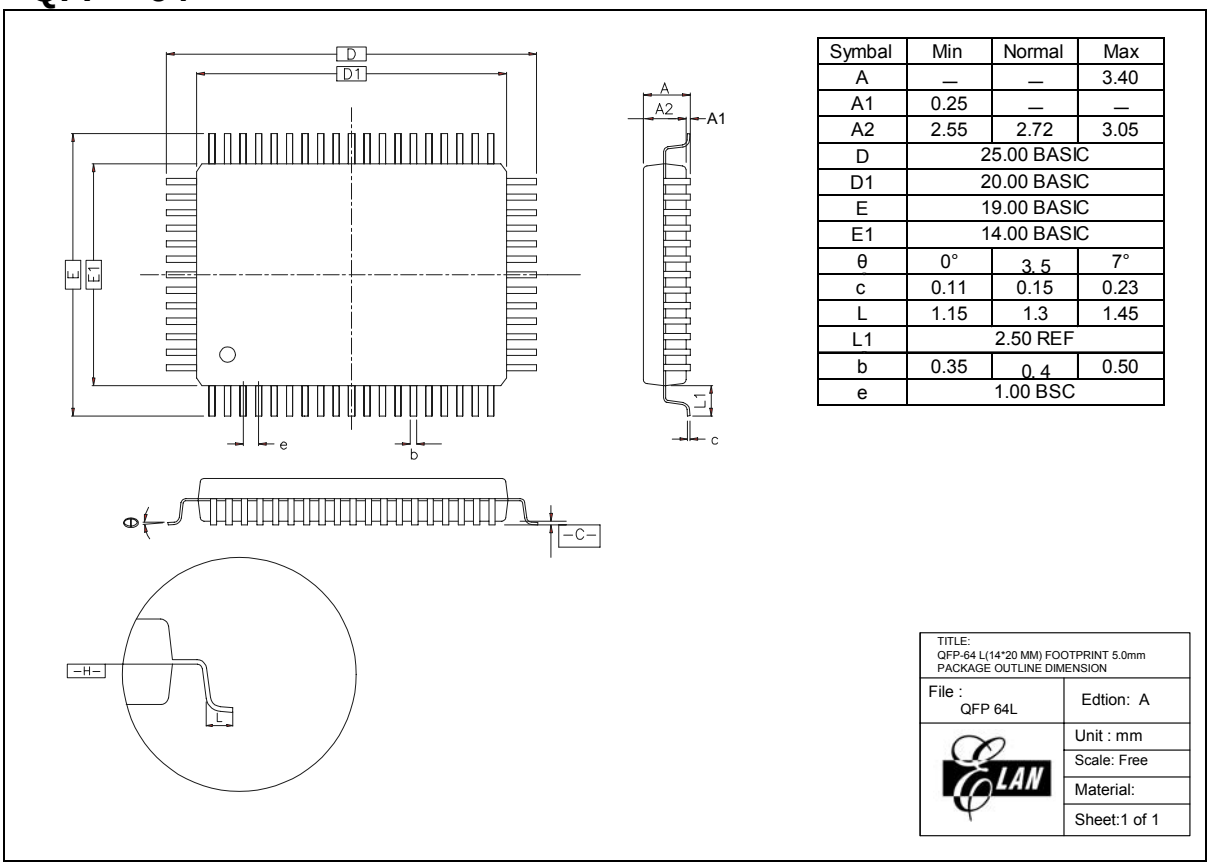
APPENDIX A:

A.1 Package Types:

Name	Package Type	Pin Count	Package Body Size
EM78P468NH	Dice	59	
EM78P468NQ	QFP	64	14 mm * 20 mm
EM78P468NAQ	LQFP	64	7 mm * 7 mm
EM78P468NBQ	LQFP	44	10 mm * 10 mm
EM78P468NCQ	QFP	44	10 mm * 10 mm

A.2 Package Information:

QFP – 64



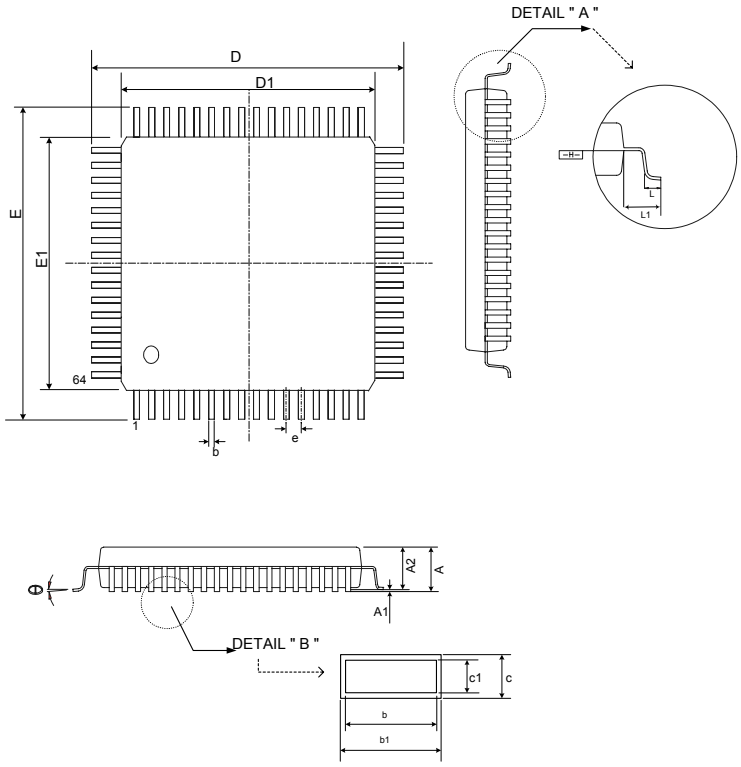
Symbal	Min	Normal	Max
A	—	—	3.40
A1	0.25	—	—
A2	2.55	2.72	3.05
D	25.00 BASIC		
D1	20.00 BASIC		
E	19.00 BASIC		
E1	14.00 BASIC		
θ	0°	3.5	7°
c	0.11	0.15	0.23
L	1.15	1.3	1.45
L1	2.50 REF		
b	0.35	0.4	0.50
e	1.00 BSC		

TITLE:
QFP-64 L(14*20 MM) FOOTPRINT 5.0mm
PACKAGE OUTLINE DIMENSION

File : QFP 64L | Edtion: A

Unit : mm
Scale: Free
Material:
Sheet:1 of 1

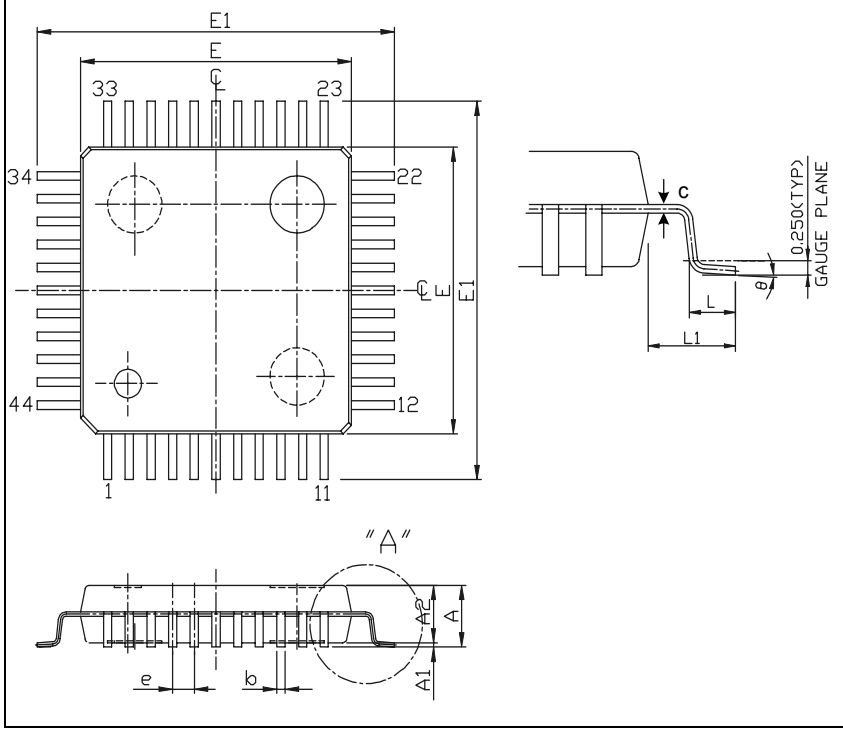
LQFP – 64



Symbal	Min	Normal	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	8.90	9.00	9.10
D1	6.90	7.00	7.10
E	8.90	9.00	9.10
E1	6.900	7.00	7.100
e	0.4 BSC		
c	0.09	-	0.20
c1	0.09	-	0.16
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
L	0.45	0.60	0.75
L1	1.00 REF.		
θ	0°	3.5°	7°

TITLE: LQFP 64L (7*7 MM) FOOTPRINT 2.0 mm PACKAGE OUTLINE DIMENSION	
File : LQFP 64L	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

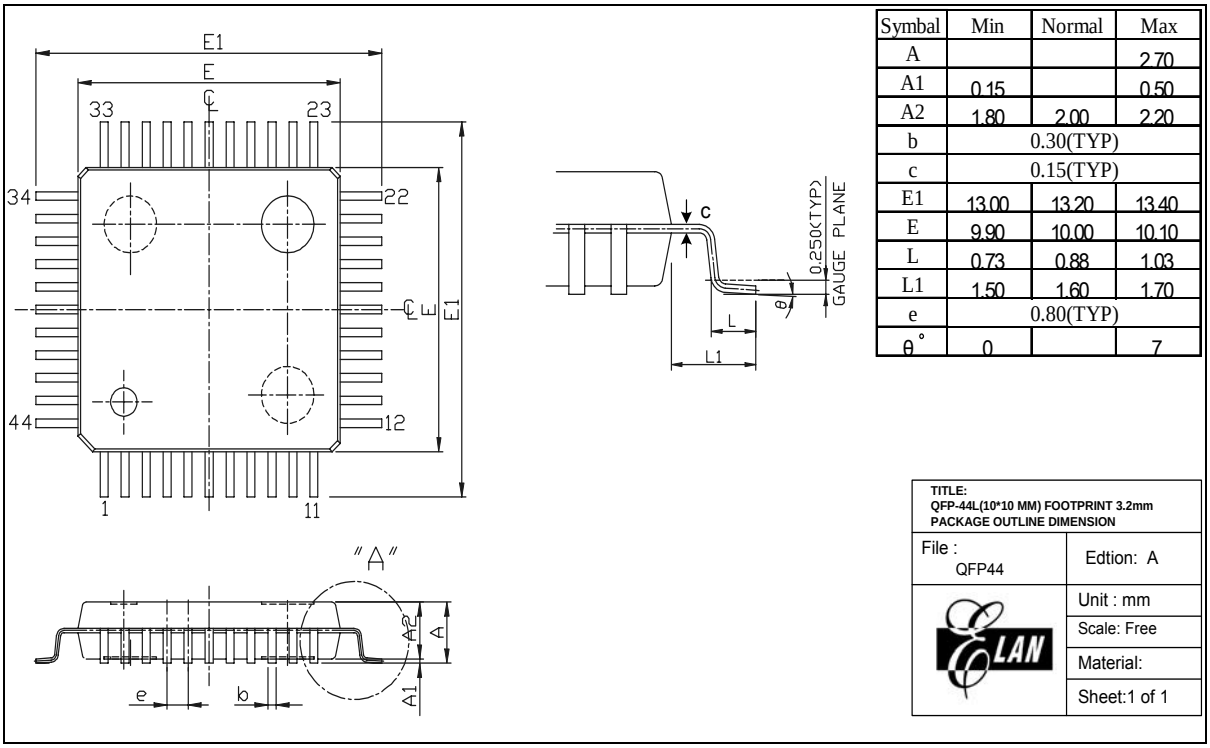
LQFP – 44



Symbal	Min	Normal	Max
A			1.600
A1	0.050		0.150
A2	1.350	1.400	1.450
b	0.300	0.370	0.450
c	0.090		0.200
E1	12.00 BASIC		
E	10.00 BASIC		
L	0.450	0.600	0.750
L1	1.0(BASIC)		
e	0.8(BASIC)		
θ°	0	3.5	7

TITLE: LQFP-44L(10*10 MM) FOOTPRINT 2.0mm PACKAGE OUTLINE DIMENSION	
File : LQFP44	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

QFP – 44



Symbal	Min	Normal	Max
A			2.70
A1	0.15		0.50
A2	1.80	2.00	2.20
b		0.30(TYP)	
c		0.15(TYP)	
E1	13.00	13.20	13.40
E	9.90	10.00	10.10
L	0.73	0.88	1.03
L1	1.50	1.60	1.70
e		0.80(TYP)	
θ°	0		7

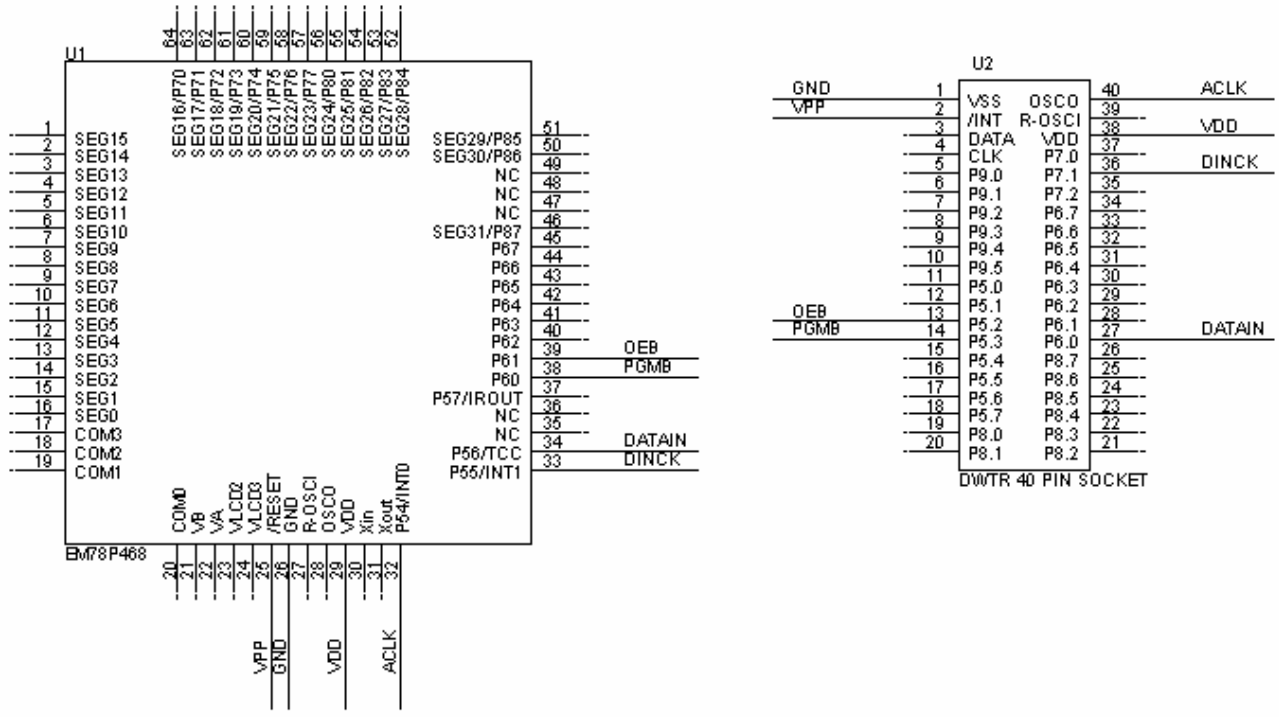
TITLE: QFP-44L(10*10 MM) FOOTPRINT 3.2mm PACKAGE OUTLINE DIMENSION	
File : QFP44	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

APPENDIX B: EM78P468N Program Pin List

It uses DWRT to program EM78P468N IC's. The connector of DWTR select by CON4 (EM78P451), and the software is selected by EM78P468N.

Program Pin Name	IC Pin Name	L/QFP-64 Pin Number	L/QFP-44 Pin Number
VPP	/RESET	25	14
ACLK	P54/INT0	32	21
DINCLK	P55/INT1	33	22
DATAIN	P56/TCC	34	23
/PGMB	P60	38	25
/OEB	P61	39	26
VDD	VDD	29	18
GND	GND	26	15

Wiring diagram is for ELAN DWTR

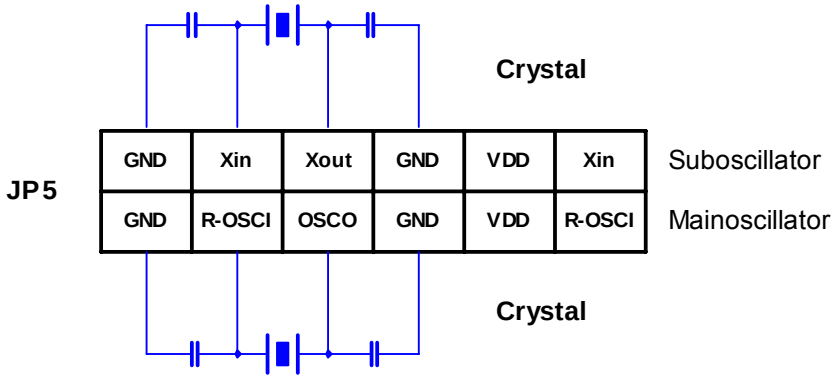


APPENDIX C:

C.1 ICE 468XA Oscillator circuit (JP 5)

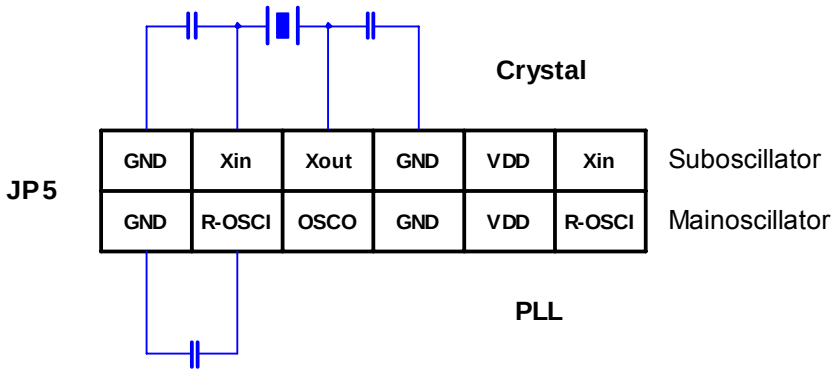
Mode1:

Main oscillator: Crystal mode, Sub oscillator: Crystal mode



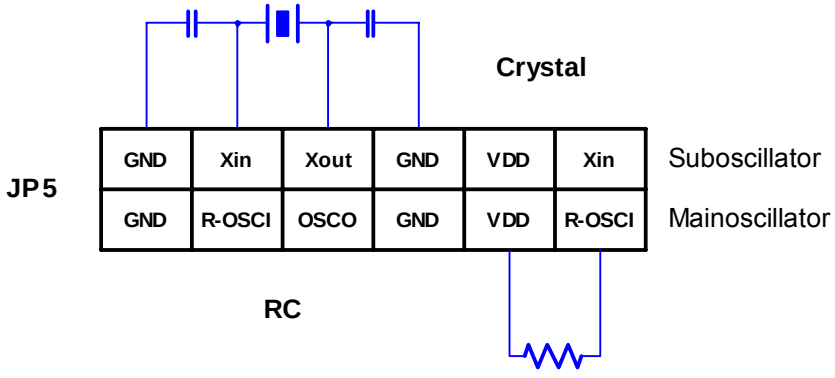
Mode2:

Main oscillator: PLL mode, Sub oscillator: Crystal mode



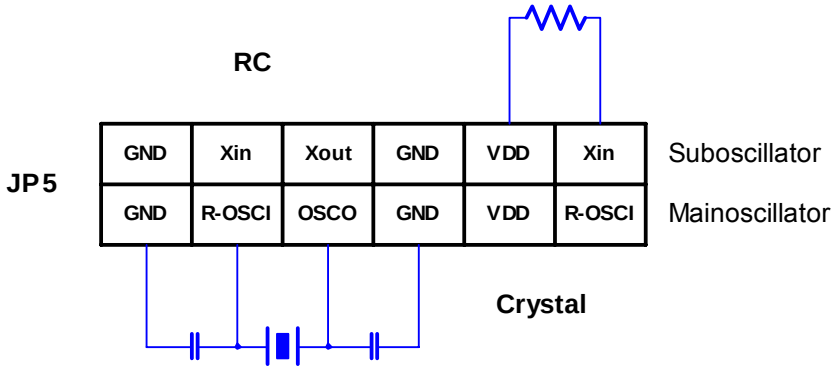
Mode3:

Main oscillator: RC mode, Sub oscillator: Crystal



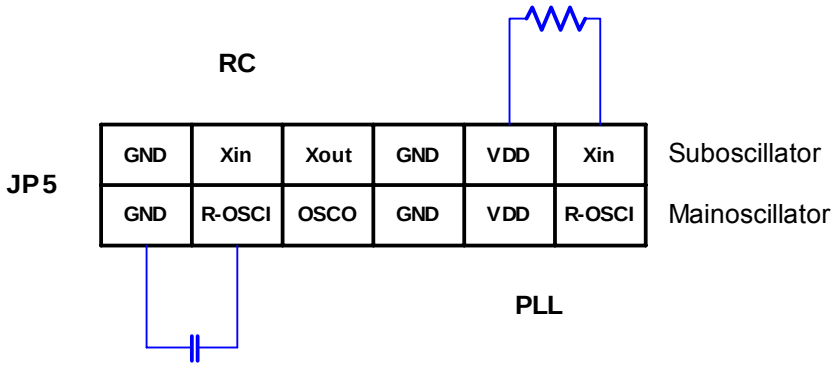
Mode4:

Main oscillator: Crystal mode, Sub oscillator: RC mode



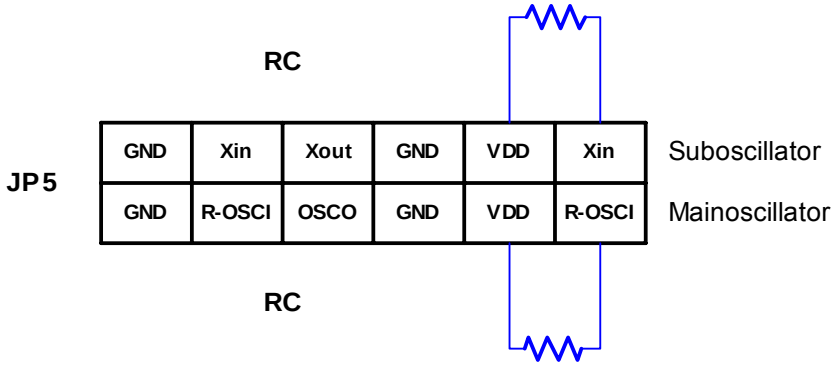
Mode5:

Main oscillator: PLL mode, Sub oscillator: RC mode



Mode6:

Main oscillator: RC mode, Sub oscillator: RC mode



C.2 ICE 468XA output pin assignment (JP 3)