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EMC6D100/EMC6D101*

Environmental Monitoring and Control Device with Automatic Fan Capability

***NOTE: The EMC6D101 is not recommended for new designs. The EMC6D102 Fan Control Device with Hardware Monitoring and Acoustic Noise Reduction Features is the replacement device recommended for new designs.**

The EMC6D100 & EMC6D101 monitor external voltages, temperatures, and fan speeds. They use this monitoring capability to alert the system to out of limit conditions and can automatically control the speeds of multiple fans in a PC or embedded system. The EMC6D101, available in a 24-pin SSOP package, and the EMC6D100, available in a 28-pin SSOP package, are designed to be register compatible. The EMC6D100 offers all the features of the EMC6D101 plus additional voltage monitoring and system control features. The following is a summary of the features offered in both packages:

Product Features

- 3.3 Volt Operation (5 Volt Tolerant Input Buffers)
- SMBus 2.0 compliant interface
- Fan Control
  - PWM (Pulse width Modulation) Outputs (3)
  - Fan Tachometer Inputs (4)
  - Programmable automatic fan control based on temperature
- Temperature Monitor
  - Monitoring of Two Remote Thermal Diodes
  - (+/- 3 deg. C accuracy)
  - Internal Ambient Temperature Measurement
  - Limit Comparison of all Monitored Values
  - Interrupt Pin for out-of-limit Temperature Indication (EMC6D100 only)
  - Configurable offset for internal or external temperature channels
- Voltage Monitor
  - Monitor Power supplies (+2.5V, +5V, +12V, Vccp, and VCC)
  - EMC6D100 monitors additional power supplies (+3.3V, +1.5V, +1.8V)
  - Limit Comparison of all Monitored Values
  - Interrupt Pin for out-of-limit Voltage Indication (EMC6D100 only)
  - 5 VID (Voltage Identification) inputs
- XNOR Tree test mode
- Mechanical Packages
  - 24 Pin SSOP Package (EMC6D101)
  - 28 Pin SSOP Package (EMC6D100)

ORDERING INFORMATION

Order Number(s):

EMC61D100-DK for 28 Pin SSOP Package

EMC61D101-CK for 24 Pin SSOP Package

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EMC6D100/101 Revisions

PAGE(S)	SECTION/FIGURE/ENTRY	CORRECTION	DATE REVISED
Cover		Note added advising of replacement of EMC6D101 with EMC6D102 as recommended device for new designs.	09/09/04
68	9.2 Ratings for Operation	Vcc Supply Current, max sleep mode changed from 300 to 500	01/07/03
21	6.3 Monitoring Modes	Updated temperature conversion values: changed 2.133ms to 2ms changed 1.511ms to 1.5ms Updated total times: Option 1 – Changed 362.616ms to 624 ms Option 2 - Changed 45.327ms to 78ms (See italicized text)	04/04/02
22	6.3.1 Continuous Monitoring Mode	Updated values: changed 362.616ms to 624 ms (see italicized text)	04/04/02
68	9.2 Ratings for Operation	Updated typical values for the conversion time: Option 1 - changed from 363 to 624 Option 2 - changed from 45 to 78 Modified Note 3 to reflect these value changes. (See italicized text)	04/04/02
73	11.1 24 Pin SSOP Package Outline, 0.150” Wide Body, 0.025” Pitch	Updated package outline.	04/04/02
74	11.2 28 Pin SSOP Package Outline, 0.150” Wide Body, 0.025” Pitch	Updated package outline.	04/04/02
9	General Description	Reference to “Dual Footprint” removed.	11/19/01
10	EMC6D101	Reference to “Dual Footprint” removed.	11/19/01

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Chapter 1 General Description

The EMC6D100 & EMC6D101 are environmental monitoring and control devices with automatic fan control capability for PCs and embedded systems. These ACPI compliant devices provide hardware monitoring for up to eight voltages and three thermal zones, measure the speed of up to four fans, and control the speed of multiple DC fans using three Pulse Width Modulators (PWM). Note that it is possible to control more than three fans by connecting two fans to one PWM output.

The EMC6D101 is available in a 24-pin SSOP package and the EMC6D100 is available in a 28-pin SSOP package. These devices are designed to be register compatible. The EMC6D100 offers all the features of the EMC6D101 plus additional voltage monitoring and system control features.

The EMC6D100 & EMC6D101 hardware monitoring provides analog inputs for monitoring external voltages of +2.5V, +5V, +12V and Vccp. These devices have the capability to monitor their own internal VCC or VSB. In addition to monitoring the processor voltage, VID inputs are available to identify the voltage specification. The EMC6D100 has the added functionality of monitoring +3.3V, +1.5V and +1.8V. External components are not required for voltage scaling or similar treatment.

These devices include support for monitoring three thermal zones: two external and one internal. The external temperatures are measured via thermal diode inputs capable of monitoring remote devices. In addition, they are equipped with an ambient temperature sensor for measuring the internal temperature.

Pulse Width Modulators (PWM) control the speed of the fans by varying the output duty cycle of the PWM. The speed of each fan is monitored by a Fan Tachometer input. The measured values are compared to values stored in Limit Registers to detect if a fan has stalled or seized.

Fan speed may be under host software control or automatic control of the EMC6D100 & EMC6D101. In host control mode, the host software continuously monitors temperature and fan speed registers, makes decisions as to desired fan speed and sets the PWM's to drive the required fan speed. The EMC6D100 has an interrupt pin (INT#), which may be used to interrupt the host on out-of-limit temperature or voltage condition enabling an ACPI response as opposed to the host software continuously monitoring status. In auto "zone" mode, the EMC6D100 & EMC6D101 logic continuously monitors the temperature and fan speeds and adjusts speeds without intervention from the host CPU. Fan speed is adjusted according to an algorithm using the temperature measured in the selected zone, the high and low limits set by the user, and the current fan speed.

The EMC6D100 & EMC6D101 registers are accessible through the SMBus interface in both "standby mode" and "active mode".

Chapter 2 Pin Configurations

The Environmental Monitoring and Control device (EMC) is offered in two packages: the EMC6D101, which is a 24 pin SSOP, and the EMC6D100, which is a 28 pin SSOP.

2.1 EMC6D101

The EMC6D101 is a 24 pin SSOP.

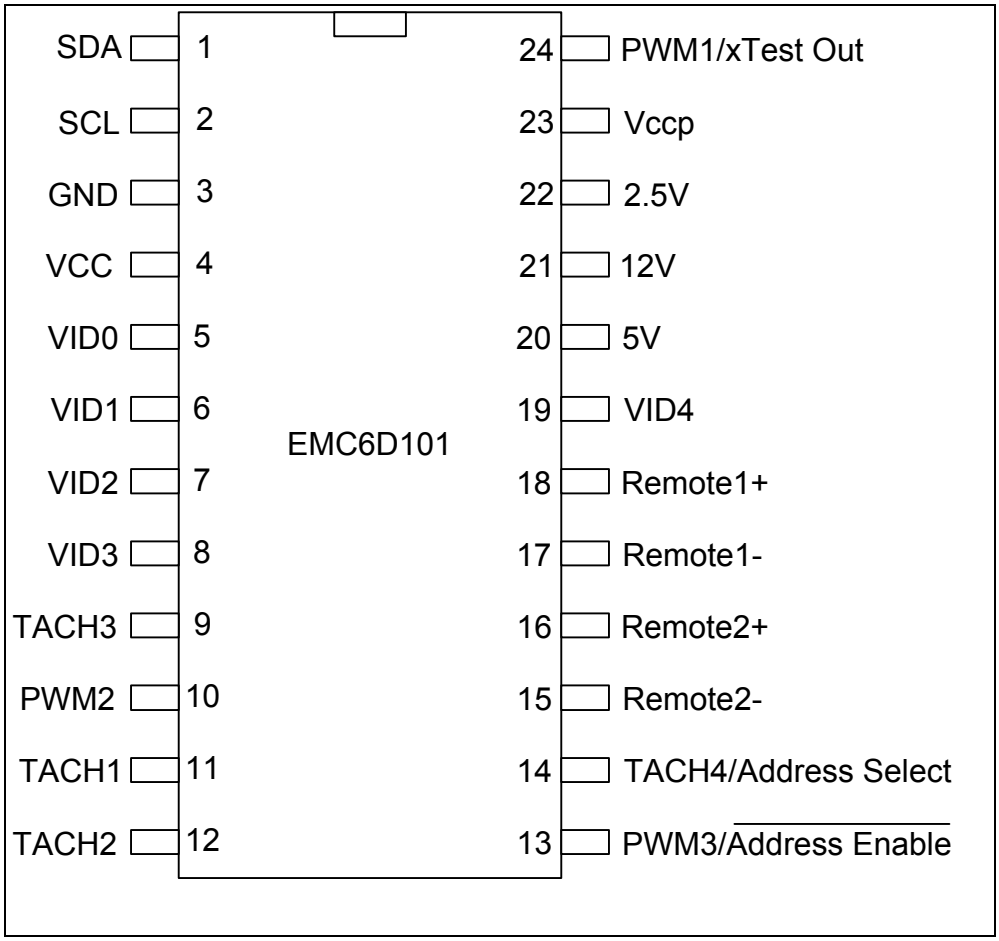


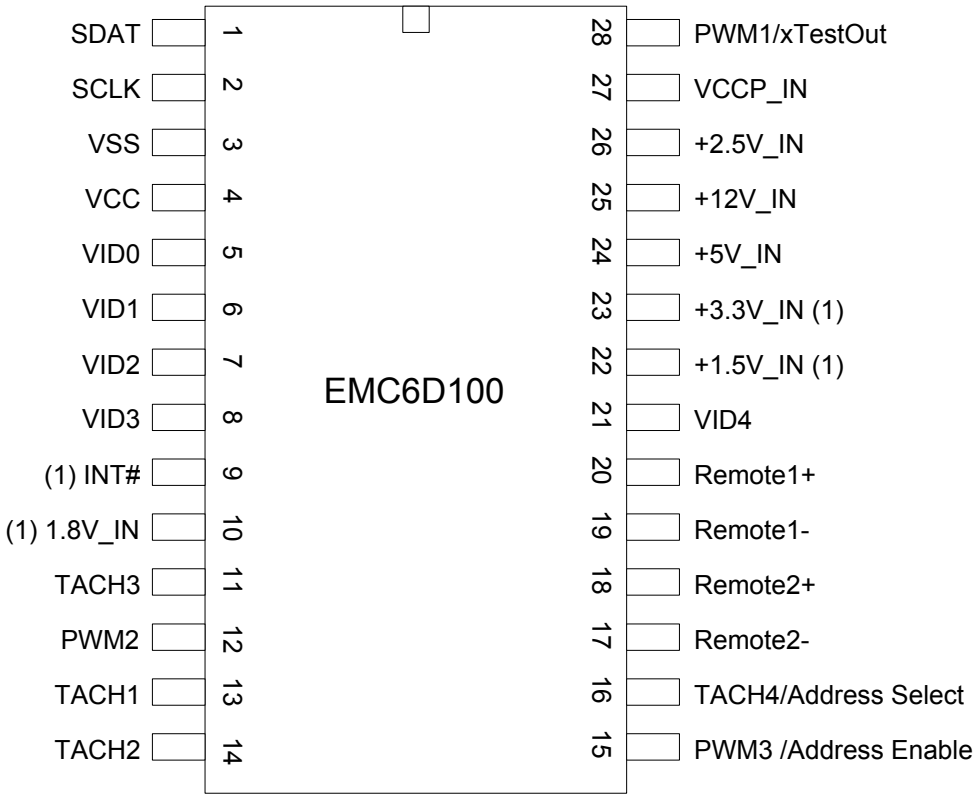
FIGURE 2.1 – PIN CONFIGURATION FOR EMC6D101

2.2 EMC6D100

The EMC6D100 is a 28 pin SSOP. The functions that this chip supports in addition to the EMC6D101 are listed below.

Additional Features offered in EMC6D100:

- Voltage monitoring for +3.3V, +1.5V, +1.8V inputs
- Interrupt pin



(1) Fan Control signal differs from EMC6D101

FIGURE 2.2 – PIN CONFIGURATION FOR EMC6D100

Chapter 3 Recommended Implementation

The following figures show the recommended circuitry on the board for the PWM outputs, tachometer inputs, and remote diodes. FIGURE 3.1 shows how the part can be used to control additional fans by connecting two fans to one PWM output.

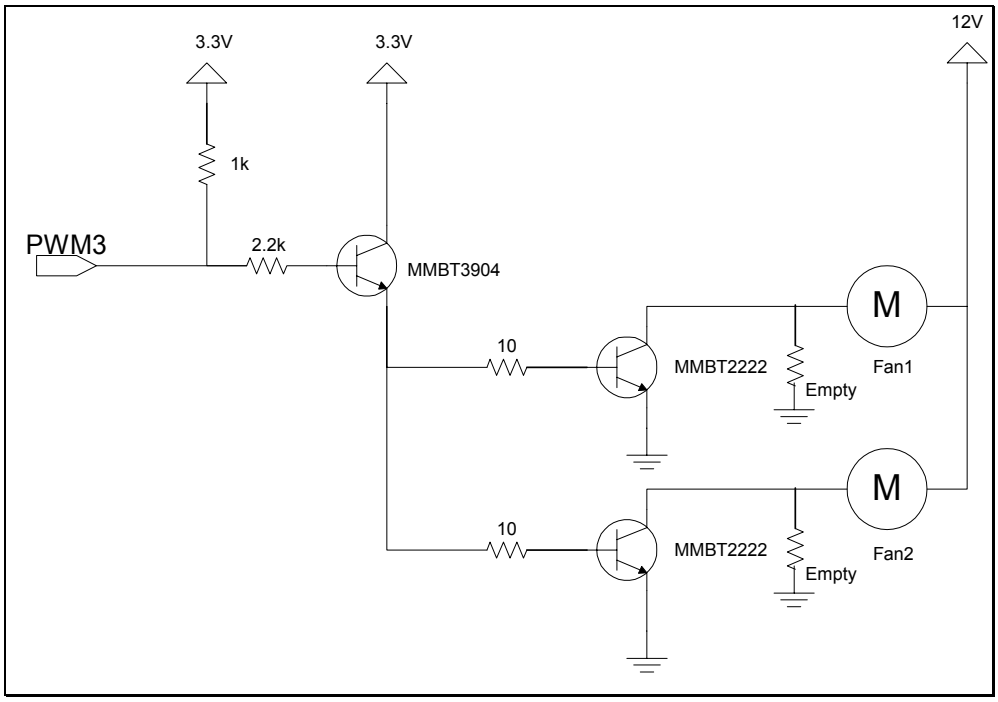


FIGURE 3.1 - FAN DRIVE CIRCUITRY (APPLY TO PWM DRIVING TWO FANS)

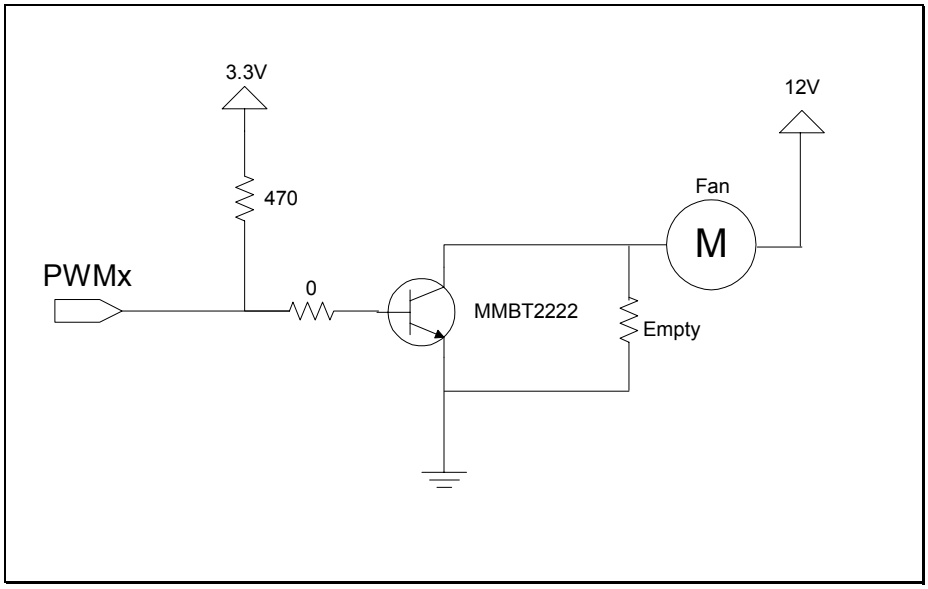


FIGURE 3.2 - FAN DRIVE CIRCUITRY (APPLY TO PWM DRIVING ONE FAN)

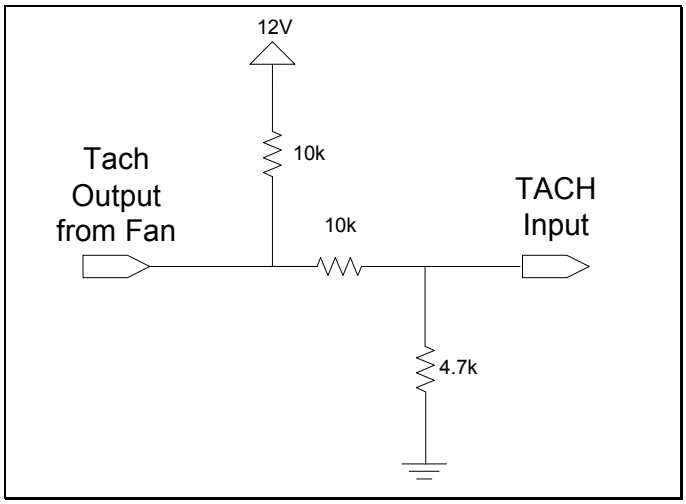


FIGURE 3.3 - FAN TACHOMETER CIRCUITRY (APPLY TO EACH FAN)

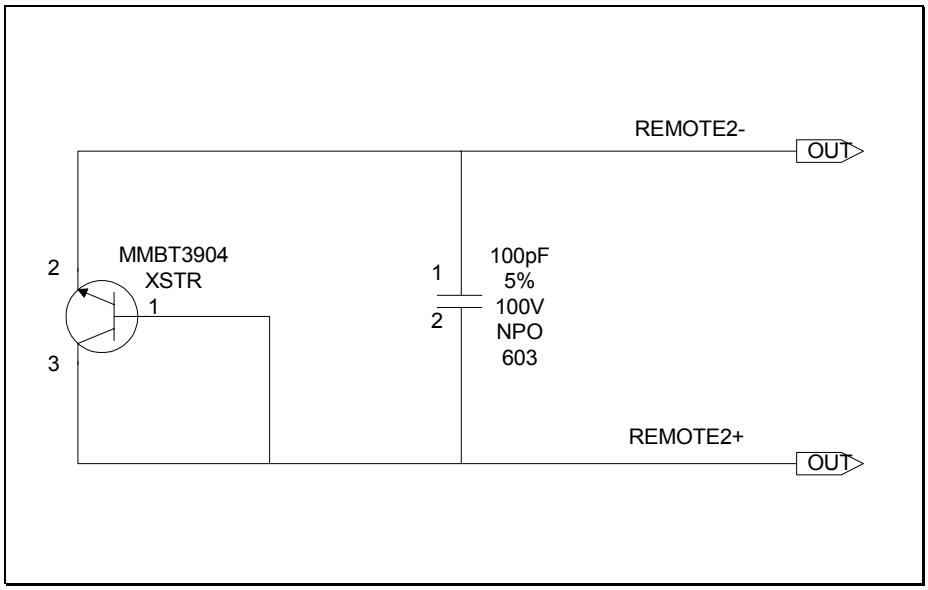


FIGURE 3.4 - REMOTE DIODE (APPLY TO REMOTE2 LINES)

Notes:

- 100pf cap is optional and should be placed close to the EMC6D100/EMC6D101 if used.
- The voltage at PWM3 must be at least 2.0V to avoid triggering Address Enable.

Chapter 4 Pin Description

	SYMBOL	PIN (EMC6D101)	PIN (EMC6D100)	TYPE	NAME AND FUNCTION
SMBus	SDA	1	1	Digital I/O (Open Drain)	System Management Bus Data. Open-drain output. 5V tolerant. SMBus 2.0 compliant.
	SCL	2	2	Digital I/O (Open Drain)	System Management Bus Clock. Open-drain output. 5V tolerant. SMBus 2.0 Compliant.
Processor VID Lines	VID0	5	5	Digital Input	Voltage Identification signal from the processor. This value is read in the VID0-VID4 Status Register. Input only.
	VID1	6	6	Digital Input	Voltage Identification signal from the processor. This value is read in the VID0-VID4 Status Register. Input only.
	VID2	7	7	Digital Input	Voltage Identification signal from the processor. This value is read in the VID0-VID4 Status Register. Input only.
	VID3	8	8	Digital Input	Voltage Identification signal from the processor. This value is read in the VID0-VID4 Status Register. Input only.
	VID4	19	21	Digital Input	Voltage Identification signal from the processor. This value is read in the VID0-VID4 Status Register. Input only.
Power	VSS	3	3	GROUND	Ground for all analog and digital circuitry.
	VCC	4	4	POWER	Positive Power Supply. Nominal 3.3V. VCC is monitored by the Hardware Monitoring Block. [Can be powered by +3.3V Standby power if monitoring in low power states is required.]
Voltage Monitoring	+5V	20	24	Analog Input	Analog input for +5V monitoring.
	+2.5V	22	26	Analog Input	Analog input for +2.5V monitoring.
	Vccp	23	27	Analog Input	Analog input for +Vccp (processor voltage) monitoring.
	+12V	21	25	Analog Input	Analog Input for +12V monitoring.
	+1.5V (note 1)	-	22	Analog Input	Analog input for +1.5V monitoring.
	+1.8V (note 1)	-	10	Analog Input	Analog input for +1.8V monitoring.
	+3.3V (note 1)	-	23	Analog Input	Analog Input for +3.3V monitoring.

	SYMBOL	PIN (EMC6D101)	PIN (EMC6D100)	TYPE	NAME AND FUNCTION
Temperature Monitoring	Remote1-	17	19	Remote Thermal Diode Negative Input	Negative input (current sink) from the first remote thermal diode.
	Remote1+	18	20	Remote Thermal Diode Positive Input	Positive input (current source) from the first remote thermal diode.
	Remote2-	15	17	Remote Thermal Diode Negative Input	Negative input (current sink) from the second remote thermal diode.
	Remote2+	16	18	Remote Thermal Diode Positive Input	Positive input (current source) from the second remote thermal diode.
Fan Tachometer	TACH1	11	13	Digital Input	Input for monitoring tachometer of fan 1
	TACH2	12	14	Digital Input	Input for monitoring tachometer of fan 2
	TACH3	9	11	Digital Input	Input for monitoring tachometer of fan 3
	TACH4/ Address Select	14	16	Digital Input	Input for monitoring tachometer of fan 4. If in Address Select Mode, determines the SMBus address of the device.
Fan Control	PWM1/xTest Out	24	28	Digital Open Drain Output	PWM Output 1 controlling speed of fan. When in XNOR tree test mode, functions as XNOR Tree output.
	PWM2	10	12	Digital Open Drain Output	PWM Output 2 controlling speed of fan.
	PWM3/Address Enable#	13	15	Digital Open Drain Output	PWM Output 3 controlling speed of fan. Note: If pulled to ground at power on, enables Address Select Mode (Address Select pin controls SMBus address of the device).
	INT# (note 1)	-	9	Digital Open Drain Output	Interrupt Output.

Note 1: These pins are in EMC6D100 only.

4.1 3.3V Operation, 5V Tolerance

The EMC6D100/EMC6D101 is intended to operate with a nominal 3.3V power supply. The analog voltage pins are connected to voltage sources at their respective nominal levels. All digital signal pins are 3V switching but are tolerant to 5V.

Chapter 5 SMBus Interface

The host processor communicates with the Environmental Monitoring and Control device (EMC), through a series of read/write registers, via the SMBus interface. SMBus is a serial communication protocol between a computer host and its peripheral devices.

5.1 Slave Address

The default Slave Address is 0101110b. If this address is desired, the designer should not ground the Address Enable# pin and should not apply a strapping resistor to the Address Select pin.

If multiple devices are implemented in a system or another SMBus device requires address 0101110b, TACH4 and PWM3 must be disabled. In this case, addressing is implemented as follows:

The board designer will apply a 10KΩ pull-down resistor to ground on the Address Enable# pin. Upon power up, the EMC6D100/EMC6D101 device will be placed into Address Enable mode and assign itself an SMBus address according to the Address Select input. The device will latch the address during the first valid SMBus transaction in which the first five bits of the targeted address match those of the EMC6D100/EMC6D101 address. This feature eliminates the possibility of a glitch on the SMBus interfering with address selection.

ADDRESS SELECT	BOARD IMPLEMENTATION	SMBUS ADDRESS
0	Pulled to ground through a 10kΩ resistor	0101100b
1	Pulled to 3.3V through a 10kΩ resistor	0101101b

In this way, there can be up to three EMC6D100/EMC6D101 devices on the SMBus at any time. Multiple EMC6D100/EMC6D101 devices can be used to monitor additional processors and temperature zones.

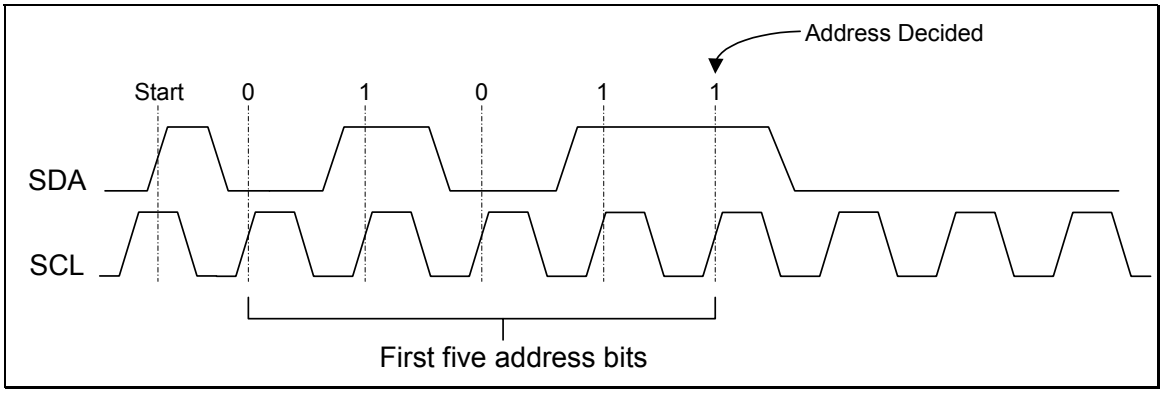


FIGURE 5.1 - ADDRESS SELECTION ON EMC6D100/EMC6D101

5.2 SMBus Slave Interface

The EMC6D100/EMC6D101 Device SMBus implementation is a subset of the SMBus interface to the host. The Device is a *slave-only* SMBus device. The implementation in the Device is a subset of SMBus since it only supports four protocols.

The Write Byte, Read Byte, Send Byte, and Receive Byte protocols are the only valid SMBus protocols for the Device. This part responds to other protocols as described in the Invalid Protocol Section. Reference the System Management Bus Specification, Rev 2.0.

The SMBus interface is used to read and write the registers in the Device. The register set is shown in section Chapter 8 Register Set on page 37.

5.3 Bus Protocols

Typical Write Byte, Read Byte, Send Byte, and Receive Byte protocols are shown below. Register accesses are performed using 7-bit slave addressing, an 8-bit register address field, and an 8-bit data field. The shading indicates the EMC device is driving data on the SDA line; otherwise, host data is on the SDA line.

The slave address is the unique SMBus Interface Address for the EMC device that identifies it on SMBus. The register address field is the internal address of the register to be accessed. The register data field is the data that the host is attempting to write to the register or the contents of the register that the host is attempting to read.

Note: Data bytes are transferred MSB first.

5.3.1 BYTE PROTOCOLS

When using the EMC SMBus Interface for byte transfers, a write will always consist of the SMBus Interface Address byte, followed by the Internal Address Register byte, then the data byte. There are two cases for a read:

1. The normal read protocol consists of a write to the EMC device with the SMBus Interface Address byte, followed by the Internal Address Register byte. Then restart the Serial Communication with a Read consisting of the SMBus Interface Address byte, followed by the data byte read from the EMC device. This can be accomplished by using the Read Byte protocol or by using the Send Byte protocol followed by the Receive Byte protocol.

2. If the Internal Address Register is known to be at the desired Address, simply read the EMC register with the SMBus Interface Address byte, followed by the data byte read from the EMC register block. This corresponds to the Receive Byte protocol.

Write Byte

The Write Byte protocol is used to write data to the registers. The data will only be written if the protocol shown in Table 5.1 is performed correctly. Only one byte is transferred at time for a Write Byte protocol.

Table 5.1 -SMBus Write Byte Protocol

FIELD:	START	SLAVE ADDR	WR	ACK	REG. ADDR	ACK	REG. DATA	ACK	STOP
BITS:	1	7	1	1	8	1	8	1	1

Read Byte

The Read Byte protocol is used to read data from the registers. The data will only be read if the protocol shown in Table 5.2 is performed correctly. Only one byte is transferred at time for a Read Byte protocol.

Table 5.2 - SMBus Read Byte Protocol

FIELD:	START	SLAVE ADDR	WR	ACK	REG. ADDR	ACK	START	SLAVE ADDR	RD	ACK	REG. DATA	NACK	STOP
BITS:	1	7	1	1	8	1	1	7	1	1	8	1	1

Send Byte

The Send Byte protocol is used to set the Internal Address Register to the correct register in the EMC Register Block. No data is transferred for a Send Byte protocol. The Send Byte can be followed by the Receive Byte protocol described below in order to read data from the register. The send byte protocol cannot be used to write data - if data is to be written to a register then the write byte protocol must be used as described in subsection above. The send byte protocol is shown in the table below.

Table 5.3 - SMBus Send Byte Protocol

FIELD:	START	SLAVE ADDR	WR	ACK	REG. ADDR	ACK	STOP
BITS:	1	7	1	1	8	1	1

Receive Byte

The Receive Byte protocol is used to read data from the registers when the register address is known to be at the desired address (using the Internal Address Register). This is used when the register address has been written to the desired address using the Send Byte protocol. This can be used for successive reads of the same register. The data will only be read if the protocol shown in Table 5.4 is performed correctly. Only one byte is transferred at time for a Receive Byte protocol.

Table 5.4 - SMBus Receive Byte Protocol

FIELD:	START	SLAVE ADDR	RD	ACK	REG. DATA	NACK	STOP
BITS:	1	7	1	1	8	1	1

5.4 Invalid Protocol Response Behavior

Registers that are accessed with an invalid protocol will not be updated. A register will only be updated following a valid protocol. The only valid protocols are the Write Byte, Read Byte, Send Byte, and Receive Byte protocols, which are described above.

The EMC6D100/EMC6D101 device responds to three SMBus slave addresses:

1) The SMBus slave address that supports the valid protocols defined in the previous sections is determined by the level on the Address Select and Address Enable pins as shown in section 5.1 Slave Address on page 16.

2) SMBus General Call Address (0001 100). The SMBus will only respond to the General Call Address if the SMBus Alert Response interrupt was generated to request a response from the Host. The SMBus Allert Response is defined in section 5.10 SMBus Alert Response Address on page 19.

Attempting to communicate with the EMC device over the SMBus with an invalid slave address, or invalid protocol will result in no response, and the SMBus Slave Interface will return to the idle state.

The only valid registers that are accessible by the SMBus slave address are the registers defined in the Registers Section. See section below for response to undefined registers.

5.4.1 UNDEFINED REGISTERS

Reads to undefined registers return 00h. Writes to undefined registers have no effect and return no error.

5.5 General Call Address Response

The EMC device will not respond to a general call address of 0000_000.

5.6 Slave Device Time-Out

According to SMBus specification, v2.0 devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25ms ($T_{TIMEOUT, MIN}$). Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than 35ms ($T_{TIMEOUT, MAX}$).

Note: Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or stop condition

5.7 Stretching the SCLK Signal

The EMC device supports stretching of the SCLK by other devices on the SMBus. The EMC device does not stretch the SCLK.

5.8 SMBus Timing

The SMBus Slave Interface complies with the SMBus AC Timing Specification. See the SMBus timing in the “Timing Diagram” section.

5.9 Bus Reset Sequence

The SMBus Slave Interface will reset and return to the idle state upon a START field followed immediately by a STOP field.

5.10 SMBus Alert Response Address

EMC6D100:

The EMC6D100 device implements the SMBALERT# signal. The INT# interrupt pin can be used as the SMBALERT#. SMBALERT# is used in conjunction with the SMBus General Call Address, 0001 100. In order for the INT# signal to become active and for the device to respond to the Alert Response address, the INTEN bit (register 7Ch bit 2) must be set and the event must be properly enabled onto the INT# pin. Each interrupt event must be enabled into the interrupt status registers, and the status bits must be

enabled onto the INT# pin via the enable bits for each type of event (i.e., temperature, voltage and fan). See the “INTERRUPT STATUS REGISTER” section.

The device can signal the host that it wants to talk by pulling the SMBALERT# low, if a status bit is set in one of the interrupt status registers and properly enabled onto the INT# pin. The host processes the interrupt and simultaneously accesses all SMBALERT# devices through a modified Receive Byte operation with the Alert Response Address (ARA).

The EMC6D100/EMC6D101 Device, which pulled SMBALERT# low, will acknowledge the Alert Response Address and respond with its device address.

The host performs a modified Receive Byte operation with the alert response address. The 7-bit device address provided by the EMC6D100/EMC6D101 device is placed in the 7 most significant bits of the byte. The eighth bit can be a zero or one.

Table 5.5 - Modified SMBus Receive Byte Protocol Response to ARA

FIELD:	START	ALERT RESPONSE ADDRESS	RD	ACK	EMC6D100/EMC6D101 SLAVE ADDRESS	NACK	STOP
BITS:	1	7	1	1	8	1	1

After acknowledging the slave address, the EMC6D100/EMC6D101 device will disengage the SMBALERT# pulldown by clearing the INT enable bit. If the condition that caused the interrupt remains, the Fan Control device will reassert the SMBALERT# on the next monitoring cycle, provided the INT enable bit has been set back to ‘1’ by software.

EMC6D101:

The EMC6D101 part does not have an interrupt pin. This part does not normally acknowledge or respond to the Alert Response Address. However, the Device will respond as described above if the INTEN bit (register 7Ch bit 2) is set, and if a status bit is set in one of the interrupt status registers and is properly enabled onto the INT# signal. Each interrupt event must be enabled into the interrupt status registers, and the status bits must be enabled onto the INT# signal via the enable bits for each type of event (i.e., temperature, voltage and fan). See the “INTERRUPT STATUS REGISTER” section.

Chapter 6 Hardware Monitoring

The following sub-sections describe the Hardware Monitoring Block.

6.1 Input Monitoring

The EMC6D100/EMC6D101 Device's monitoring function is started by writing a '1' to the START bit in the **Ready/Lock/Start** Register (0x40). Measured values from the analog inputs and temperature sensors are stored in Reading Registers. The values in the reading registers can be accessed via the SMBus interface. These values are compared to the programmed limits in the Limit Register. The out-of-limit and diode fault conditions are stored in the Interrupt Status Registers.

Note: All limit and parameter registers must be set before the START bit is set to '1'. Once the start bit is set, these registers become read-only.

6.2 Resetting the Hardware Monitoring Block

6.2.1 POWER ON RESET

All the registers in the Hardware Monitor Block, except the reading registers, reset to a default value when power is applied to the block. The default state of the register is shown in the table in the Register Summary subsection. The default state of Reading Registers are not shown because these registers have indeterminate power on values.

Note: Usually the first action after power up is to write limits into the Limit Registers.

6.2.2 SOFT RESET (INITIALIZATION)

Setting bit 7 of the CONF register performs a soft reset. This bit is self-clearing. Soft Reset performs reset on all the registers except the Reading Registers.

6.3 Monitoring Modes

The Hardware Monitor Block supports two Monitoring modes: Continuous Mode and Cycle Mode. These modes are selected using bit 1 of the Special Function Register (7Ch). The following subsections contain a description of these monitoring modes.

For each mode, there are two options for the number of measurements that are performed on each temperature and voltage reading. These options are selected using bit 5 of the special function register (7Ch). These options are as follows:

1. 128 measurements are averaged for the remote diode temperature reading and 8 measurements are averaged for all voltage and the internal temperature reading.

2. 16 measurements are averaged for the remote diode temperature reading and a single measurement is taken for all voltage and the internal temperature reading (i.e., no averaging). This is a power saving option. This is the default operation.

For option 1, the block performs a total of (2 x 128) + (1 x 8) + (8 x 8) = 328 conversions.

Option 2 reduces the number of conversions to (2 x 16) + (1 x 1) + (8 x 1) = 41.

Each temperature conversion takes 2 ms approx. and each voltage conversion takes 1.5 ms approx.

The total time for option 1 (328 conversions) is (2x128x2) + (1x8x2) + (8x8x1.5) = 624 ms.

The total time for option 2 (41 conversions) is (2x16x2) + (1x1x2) + (8x1x1.5) = 78 ms.

6.3.1 CONTINUOUS MONITORING MODE

In the continuous monitoring mode, the sampling and conversion process is performed continuously for each voltage and temperature reading after the Start bit is set high. The time for each voltage and temperature reading is shown above for each measurement option.

The continuous monitoring function is started by doing a write to the Ready/Lock/Start Register, setting the Start bit (Bit 0) high. The part then performs a “round robin” sampling of the inputs, in the order shown below (corresponding to locations in the RAM). *Sampling of all values occurs in 624 ms (or 78 ms - see above).*

SAMPLING ORDER	REGISTER
1	Remote Diode Temp Reading 1
2	Ambient Temperature reading
3	VCC reading
4	+12V reading
5	+5V reading
6	+3.3V reading
7	+2.5V reading
8	Vccp (processor) reading
9	Remote Diode Temp Reading 2
10	+1.8V reading
11	+1.5V reading

When the continuous monitoring function is started, it cycles through each measurement in sequence, and it continuously loops through the sequence approximately once every 624 ms (or 78 ms – see above). Each measured value is compared to values stored in the Limit registers. When the measured value violates (or is equal to) the programmed limit the Hardware Monitor Block will set a corresponding status bit in the Interrupt Status Registers.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See section **7.4.2 Auto Fan Control Operating Mode** on page 31.

The results of the sampling and conversions can be found in the Reading Registers and are available at any time.

6.3.2 CYCLE MONITORING MODE

In cycle monitoring mode, the part completes all sampling and conversions, then waits to repeat the process. It repeats the sampling and conversion process every second (1.4 sec max). The sampling and

conversion of each voltage and temperature reading is performed once every monitoring cycle. This is a power saving mode.

The cycle monitoring function is started by doing a write to the Ready/Lock/Start Register, setting the Start bit (Bit 0) high. The part then performs a “round robin” sampling of the inputs, in the order shown above.

When the cycle monitoring function is started, it cycles through each measurement in sequence, and it performs a single conversion for each voltage and temperature approximately once every second. Each measured value is compared to values stored in the Limit registers. When the measured value violates (or is equal to) the programmed limit the Hardware Monitor Block will set a corresponding status bit in the Interrupt Status Registers.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See section **7.4.2 Auto Fan Control Operating Mode** on page 31.

The results of each sampling and conversion can be found in the Reading Registers and are available at any time, however, they are only updated once every 1-1.4 seconds.

6.4 Interrupt Status Registers

The Hardware Monitor Block contains three interrupt status registers. These registers are used to reflect the state of all temperature, voltage and fan violation of limit error conditions and diode fault conditions that the Hardware Monitor Block monitors.

When an error occurs during the conversion cycle, its corresponding bit is set in its respective interrupt status register. The bit remains set until the register is read by software, at which time the bit will be cleared to ‘0’ if the associated error event no longer violates the limit conditions or if the diode fault condition no longer exists. Reading the register will not cause a bit to be cleared if the source of the status bit remains active.

These registers are read only – a write to these registers have no effect. These registers default to 0x00 on VCC POR and Initialization.

See the description of the Interrupt Status registers in section Chapter 8 Register Set.

Each interrupt event can be enabled into the interrupt status registers. See the figure below for the status and enable bits used to control the interrupt bits and INT# pin.

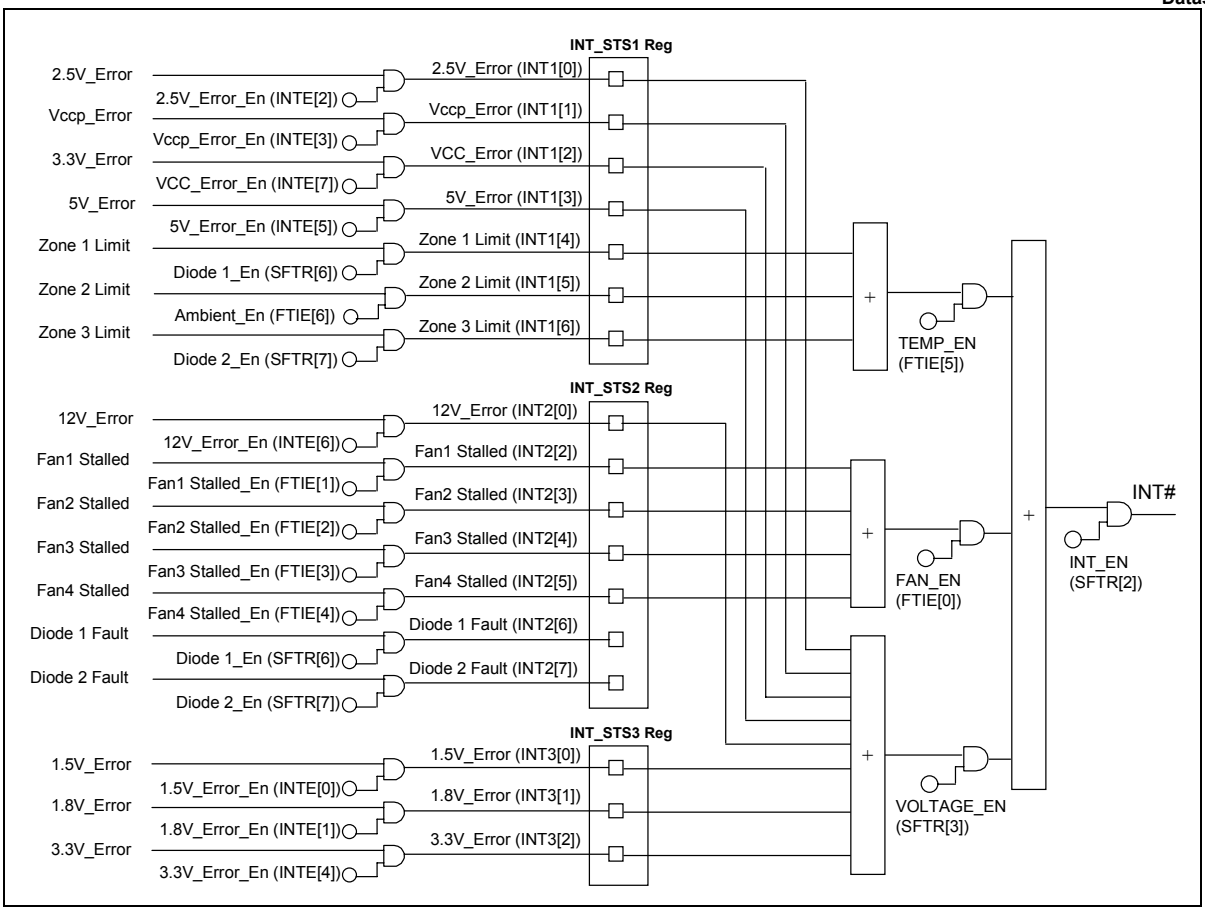


FIGURE 6.1 - INTERRUPT AND INTERRUPT STATUS REGISTER CONTROL

6.4.1 DIODE FAULT

The EMC6D100/EMC6D101 Chip automatically sets the associated diode fault bit to 1 when there is either a short or open circuit fault on the Remote x+ or Remote x- thermal diode input pins. The occurrence of a fault will cause 80h to be loaded into the associated reading register, which will cause the corresponding zone error bit to be set. This will cause the INT# pin to become active if enabled.

It will also cause the auto fan algorithm to turn any fans associated with that zone on full when it sees a reading of 80h.

If the diode is disabled, the fault bit in the interrupt status register will not be set. In this case, the occurrence of a fault will cause 00h to be loaded into the associated reading register. The limits must be programmed accordingly to prevent unwanted fan speed changes based on this temperature reading. If the diode is disabled and a fault condition does not exist on the diode pins, then the associated reading register will contain a “valid” reading.

6.5 Interrupt Pin

EMC6D100 only.

The INT# function is used as an interrupt output for out-of-limit temperature, voltage events, and/or fan errors.

- To enable the INT# pin for the interrupt function, set bit 1 of the CONF register (7Fh) to '1'.
- To enable the interrupt pin to go active, set bit 2 of the Special Function Register (7Ch) to '1'.

To enable temperature event, voltage events and/or fan events onto the INT# pin:

- To enable out-of-limit temperature events set bit 5 of the Fan Temp Interrupt Enable register (80h) to '1'.
- To enable out-of-limit voltage events set bit 3 of the Special Function Register (7Ch) to '1'
- To enable Fan tachometer error events set bit 0 of the Fan Temp Interrupt Enable register (80h) to '1'.

See FIGURE 6.1 above. The following description assumes that the interrupt enable bits for all events are set to enable the interrupt status bits to be set.

If the internal or remote temperature reading is not within the low or high temperature limits, INT# will be active low (if the TEMP_EN bit is set). This pin will remain low while the Internal Temp Error bit or one or both of the the Remote Temp Error bits in Interrupt Status 1 Register is set and the enable bit is set.

The INT# pin will not become active low as a result of the remote diode fault bits becoming set. However, the occurrence of a fault will cause 80h to be loaded into the associated reading register, which will cause the corresponding zone error bit to be set. This will cause the INT# pin to become active if enabled.

The INT# pin can be enabled to indicate out-of-limit voltages. Bit 3 of the Special Function register (7Ch) is used to enable this option. When this bit is set, if one or more of the voltage readings is not within the low or high limits, INT# will be active low. This pin will remain low while the associated voltage error bit in the Interrupt Status Register 1, Interrupt Status Register 2 and Interrupt Status Register 3 is set.

The INT# pin can be enabled to indicate fan errors. Bit 0 of the Fan Temp Interrupt Enable register (80h) is used to enable this option. This pin will remain low while the associated fan error bit in the Interrupt Status Register 2 is set.

The INT# pin will remain low while any bit is set in any of the Interrupt Status Registers. Reading the interrupt status registers will cause the logic to attempt to clear the status bits; however, the status bits will not clear if the interrupt stimulus is still active. The interrupt enable bit (Special Function Register bit[2]) should be cleared by software before reading the interrupt status registers to insure that the INT# pin will be re-asserted while an interrupt event is active, when the INT_EN bit is written to '1' again.

The INT# pin can also be deasserted by issuing an Alert Response Address Call. See the description in the "SMBus Interface" section.

The INT# pin may only become active while the monitor block is operational.

6.6 Low Power Modes

The Hardware Monitor Block can be placed in a low-power mode by writing a '0' to Bit[0] of the Ready/Lock/Start Register (0x40). The low power mode that is entered is either sleep mode or shutdown mode as selected using Bit[0] of the Special Function Register (7Ch). These modes do not reset any of the registers of the Hardware Monitor Block. In both of these modes, the PWM pins are at 100% duty cycle.

6.6.1 SLEEP MODE

This is a low power mode in which bias currents are 'on' but the Hardware Monitor Block is not operating. In this mode, the A/D converter and monitoring cycle will be turned off. Serial bus communication is still possible with any register in the Hardware Monitor Block while in this low-power mode.

6.6.2 SHUTDOWN MODE

This is a low power mode in which bias currents are 'off' and the Hardware Monitor Block is not operating. In this mode, the A/D converter and monitoring cycle will be turned off. Serial bus communication is still possible with any register in the Hardware Monitor Block while in this low-power mode.

6.7 Analog Voltage Measurement

- EMC6D101 monitors power supplies +2.5V, +5V, +12V, Vccp, and VCC
- EMC6D100 monitors additional power supplies +3.3V, +1.5V, +1.8V

The Hardware Monitor Block contains inputs for directly monitoring the power supplies (+12 V, +5 V, +3.3V, +2.5V, +1.8V, +1.5V, +Vccp and VCC). These inputs are scaled internally to a internal reference source, converted via an 8 bit successive approximation register ADC or a Delta-Sigma ADC (Analog-to-Digital Converter), and scaled such that the correct value refers to 3/4 scale or 192 decimal (except the Vccp input). This removes the need for external resistor dividers and allows for a more accurate means of measurement since the voltages are referenced to a known value. Since any of these inputs can be above VCC or below Ground, they are not diode protected to the power rails. The measured values are stored in the Reading registers and compared with the Limit registers. The status bits in the Interrupt Status Register 1, 2 and 3 are set if the measured values are outside (or equal to) the programmed limits.

The Vccp voltage input measures the processor voltage, which will lie in the range of 0V to 3.0V.

The following table shows the values of the analog inputs that correspond to the min and max output codes of the A/D converter. For a complete list of the ADC conversions see Appendix B.

INPUT VOLTAGE	$+12V_{IN}$	$+5V_{IN}$	$V_{CC}/3.3V_{IN}$	$+2.5V_{IN}$	$+1.8V_{IN}$	$+1.5V_{IN}$	$+V_{CCP}$
Min Value (Corresponds to A/D output 00000000)	<0.062	<0.026	<0.017	<0.013	<0.009	<0.008	<0.012
Max Value (Corresponds to A/D output 11111111)	>15.938	>6.640	>4.383	>3.320	>2.391	>1.992	>2.988

6.8 Voltage ID

VID0-VID4 digital inputs are used to store processor Voltage ID codes (for processor operating voltage) in the VID0-4 register (43h). These VIDs can be read out by the management system using the SMBus interface.

6.9 Temperature Measurement

Temperatures are measured internally by bandgap temperature sensor and externally using two sets of diode sensor pins (for measuring two external temperatures). See subsections below.

Note: The temperature sensing circuitry for the two remote diode sensors is calibrated for a Pentium diode.

6.9.1 INTERNAL TEMPERATURE MEASUREMENT

Internal temperature can be measured by bandgap temperature sensor. The measurement is converted into digital format by internal ADC. This data is converted in two's complement format since both negative and positive temperature can be measured. This value is stored in Internal (Zone 2) Temperature Reading register (26h) and compared to the Temperature Limit registers (50h – 51h). If this value violates the

programmed limits in the Internal (Zone 2) High Temperature Limit register (51h) and the Internal (Zone 2) Low Temperature Limit register (50h) the corresponding status bit in Interrupt Status Register 1 is set.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See section **7.4.2 Auto Fan Control Operating Mode**.

6.9.2 EXTERNAL TEMPERATURE MEASUREMENT

The Hardware Monitor Block also provides a way to measure two external temperatures using diode sensor pins (Remote x+ and Remote x-). The value is stored in the Processor (Zone 1) Temperature Reading register (25h) for Remote1+ and Remote1- pins. The value is stored in the Remote (Zone 3) Temperature Reading register (27h) for Remote2+ and Remote2- pins. If these values violate the programmed limits in the associated limit registers, then Zone (1 or 3) Limit Exceeded status bit is set in the Interrupt Status Register 1.

If auto fan option is selected, the hardware will adjust the operation of the fans accordingly. See section **7.4.2 Auto Fan Control Operating Mode** on page 31.

There are Remote Diode (1 or 2) Fault status bits in Interrupt Status Register 2 (42h), which, when one, indicate a short or open-circuit on remote thermal diode inputs (Remote x+ and Remote x-). Before a remote diode conversion is updated, the status of the remote diode is checked. In the case of a short or open-circuit on the remote thermal diode inputs, the value in the corresponding reading register will be 80h. Note that this will cause the associated zone limit exceeded status bit to be set.

The temperature change is computed by measuring the change in Vbe at two different operating points of the diode to which the Remote x+ and Remote x- pins are connected. But accuracy of the measurement also depends on non-ideality factor of the process the diode is manufactured on.

6.9.3 TEMPERATURE DATA FORMAT

Temperature data can be read from the three temperature registers. One is the Internal (Zone 2) Temperature Reading register (26h), the second is the Processor (Zone 1) Temperature Reading register (25h), and the third is the Remote (Zone 3) Temperature Reading register (27h).

The following table shows several examples of the format of the temperature digital data, represented by an 8-bit, two's complement word with an LSB equal to 1.0 ^{0}C.

TEMPERATURE	READING (DEC)	READING (HEX)	DIGITAL OUTPUT
-127^{0}C	-127	81h	1000 0001
…	…	…	…
-50 ^{0}C	-50	CEh	1100 1110
…	…	…	…
-25 ^{0}C	-25	E7h	1110 0111
…	…	…	…
-1 ^{0}C	-1	FFh	1111 1111
0 ^{0}C	0	00h	0000 0000
+1 ^{0}C	1	01h	0000 0001
…	…	…	…
+25 ^{0}C	25	19h	0001 1001
…	…	…	…
+50^{0}C	50	32h	0011 0010
…	…	…	…

TEMPERATURE	READING (DEC)	READING (HEX)	DIGITAL OUTPUT
+127^{0}C	127	7Fh	0111 1111
SENSOR ERROR	128	80h	1000 0000

6.9.4 OFFSET REGISTER

Offset Register 1 is used for internal (Zone 2) or Processor (Zone 1) temperature reading. The Offset Register 1 (1Fh) contain a 2's complement value which is added (or subtracted if the number is negative) to the temperature reading. The default value in the offset register is zero, so initially zero is always added to the temperature reading. This offset register is configured for the external temperature channel by default. It may be switched to the internal channel by setting bit 4 of the Special Function Register to 1.

6.9.5 SECOND OFFSET REGISTER

The Offset Register 2 at 1Eh is for remote (Zone 3) temperature reading. This register contains a 2's complement value which is added (or subtracted if the number is negative) to the second external temperature reading. Note that the default value in the offset register is zero, so initially zero is always added to the second temperature reading. This offset register only applies to remote (Zone 3) diode temperature reading. No configuration bit is required.

6.10 Temperature Smoothing

The part implements temperature “spike” smoothing to prevent the fan from spinning up rapidly as a result of a spike in temperature. The spike smoothing registers allow the smoothing interval to be selected for each zone. See the description of registers 62h and 63h.

Chapter 7 Fan Control

The following sections describe the various fan control and monitoring modes in the part.

7.1 General Description

The EMC6D100/EMC6D101 device is capable of driving three DC fans and monitoring up to four fans with tachometer outputs in either Manual Fan Control mode or in Auto Fan Control mode.

The fan outputs (PWMx pins) are controlled by a Pulse Width Modulation (PWM) scheme.

The four pins dedicated to monitoring the operation of each fan are the TACH[1:4] pins. Fans equipped with Fan Tachometer outputs may be connected to these pins to monitor the speed of the fan.

7.2 Limit and Configuration Registers

At power up, all the registers are reset to their default values and PWM[1:3] are set to “Fan always on Full” mode. Before initiating the monitoring cycle for either manual or auto mode, the values in the limit and configuration registers should be set.

The limit and configuration registers are:

Registers 4Eh – 53h: Zone x Temperature Low/High Limit registers

Registers 54h – 5Bh: TACHx Minimum

Registers 5Fh – 61h: Zone x Range/FANx Frequency

Registers 5Ch – 5Eh: FANx Configuration

Registers 62h – 63h: Min/Off, Zone x Spike Smoothing

Registers 64h – 66h: FANx PWM Minimum

Registers 67h – 69h: Zone x Fan Temp LIMIT

Registers 6Ah – 6Ch: Zone x Temp Absolute Limit – all fans to full

Registers 6Dh – 6Eh: Zone x Hysteresis

The limit and configuration registers are defined in section Chapter 8 Register Set on page 37.

Notes:

1) The START bit in Register 40h Ready/Lock/Start Register must be set to ‘1’ to start temperature monitoring functions.

2) Setting the Fan Configuration register to Auto Mode will not take effect until after the START bit is set.

7.3 Device Set-Up

BIOS will follow the steps listed below to configure the fan registers on the device. The registers corresponding to each function are listed. All steps may not be necessary if default values are acceptable. Regardless of all changes made by the BIOS to the limit and parameter registers during configuration, the EMC6D100/EMC6D101 will continue to operate based on default values until the Start bit, in the Ready/Lock/Start register, is set. Once the Start bit is set, the EMC6D100/EMC6D101 will operate according to the values that were set by BIOS in the limit and parameter registers.

1. Set limits and parameters (not necessarily in this order)
   a) [5F-61h] Set PWM frequencies and auto fan control range.
   b) [62-63h] Set spike smoothing and min/off
   c) [5C-5Eh] Set the fan spin-up delays.
   d) [5C-5Eh] Match each fan with a corresponding thermal zone.
   e) [67-69h] Set the fan temperature limits.
   f) [6A-6Ch] Set the temperature absolute limits.
   g) [64-66h] Set the PWM minimum duty cycle.
   h) [5F-61h] Set the Auto Fan Control Range.
   i) [6D-6Eh] Set the temperature Hysteresis values.

2. [40h] Set bit 0 (Start) to start monitoring.
3. [40h] Set bit 1 (Lock) to lock the limit and parameter registers (optional)

7.4 PWM Fan Speed Control

Note: The following description applies to PWM1, PWM2, and PWM3.

When describing the operation of the PWMs, the terms “Full on” and “100% duty cycle” means that the PWM output will be high (OD) for 255 clocks, and low for 1 clock (INVERT bit = 0). The exception to this is during fan spin-up when the PWM pin will be forced high (OD) for the duration of the spin-up time.

Note: During the low time of each PWM output, the part will generate multiple positive pulses for system synchronization. See section 7.7 System Synchronization on page 36 for a description of these pulses.

7.4.1 MANUAL FAN CONTROL OPERATING MODE

When operating in Manual Fan Control Operating Mode software controls the fans. The operation of the fans can be monitored based on reading the temperature and tachometer reading registers and/or by polling the interrupt status registers. The EMC6D100 offers the option of generating an interrupt indicated by the INT# pin.

To control the fans:

To set the mode to operate in manual mode, write ‘111’ to bits[7:5] Zone/Mode, located in Registers 5Ch-5Eh: Fan Configuration.

The speed of the fan is controlled by the duty cycle set for that device. The duty cycle must be programmed in Registers 30h-32h: Current PWM Duty

To monitor the fans:

If an out-of-limit condition occurs, the corresponding status bit will be set in the Interrupt Status registers. Setting this status bit will generate an interrupt signal on the INT# pin (if enabled – EMC6D100 only). Software must handle the interrupt condition and modify the operation of the EMC6D100/EMC6D101 accordingly. Software can evaluate the operation of the device through the Temperature and Fan Tachometer Reading registers.

When in manual mode, the current PWM duty cycle registers can be written to adjust the speed of the fans, when the start bit is set. These registers are not writeable when the lock bit is set.

7.4.2 AUTO FAN CONTROL OPERATING MODE

The EMC6D100/EMC6D101 chip implements automatic fan control. In Auto Fan Mode, the chip automatically adjusts the PWM duty cycle of the PWM outputs, according to the flow chart below. PWM outputs are assigned to a thermal zone based on the fan configuration registers. It is possible to have more than one PWM output assigned to a thermal zone. For example, PWM outputs 2 and 3, connected to two chassis fans, may both be controlled by thermal zone 2. At any time, if the temperature of a zone exceeds its absolute limit, all PWM outputs go to 100% duty cycle to provide maximum cooling to the system (except those fans that are disabled).

It is possible to have a single fan controlled by multiple zones, turning on when either zone requires cooling based on its individual settings.

A VCC POR resets all values to their initial or default states. If the device is not in reset and the start bit is set to ‘1’ the configuration and parameter registers become read only when the start bit is set and are not latched inside of the auto fan block.

If the start bit is one the Auto Fan Control block will evaluate the temperature in the zones configured for each Fan in a round robin method. The Auto Fan Control block completely evaluates the zones for all three fans in a maximum of 0.25sec.

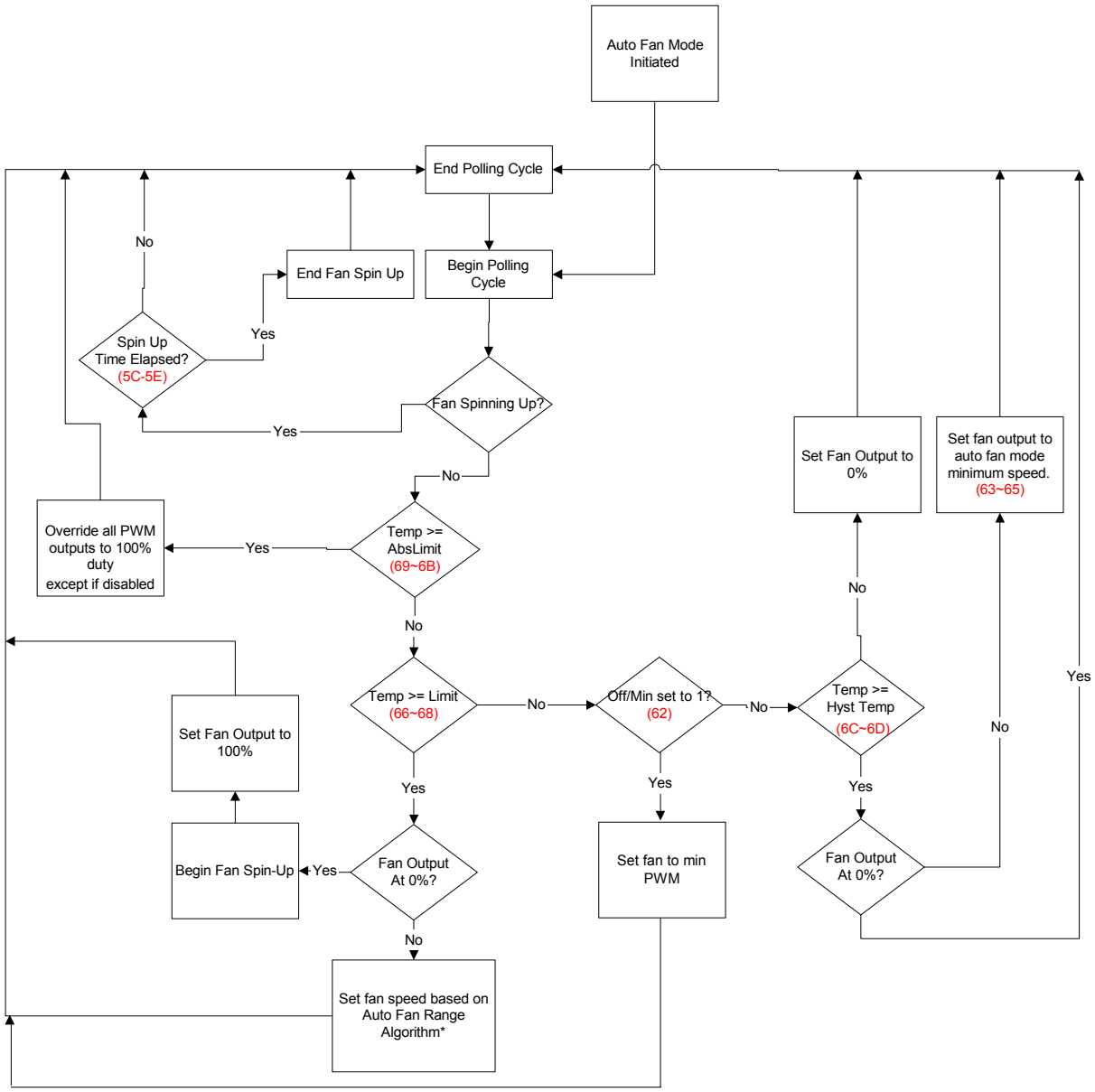


FIGURE 7.1 - AUTOMATIC FAN CONTROL FLOW DIAGRAM

*See section 8.18 Registers 5C-5Eh: Fan Configuration on page 51 for details.

When operating in Auto Fan Control Operating Mode the hardware controls the fans directly based on monitoring of temperature and speed.

To control the fans:

1. Set the minimum temperature that will turn the fans on/off. This value is programmed in Registers 67h-69h: Zone x Temp LIMIT (Auto Fan Mode Only).

2. Set the hysteresis value for the minimum temperature that will turn the fans off. This value will hold the fans on until the temperature goes a certain amount below the value programmed in the Zone x Temp Limit registers. This value will prevent the fan from oscillating between on and off if the

temperature is around the minimum temperature limit. This value is programmed in Registers 6Dh-6Eh: Zone Hysteresis registers.

3. The speed of the fan is controlled by the duty cycle set for that device. The duty cycle for the minimum fan speed must be programmed in Registers 64h-66h: Fanx PWM Minimum. This value corresponds to the speed of the fan when the temperature reading is equal to the minimum temperature LIMIT setting. As the actual temperature increases/decreases and is above the Zone LIMIT temperature and below the Absolute Temperature Limit, the PWM will be determined by a linear function based on the Auto Fan Speed Range bits in Registers 5Fh-61h.

4. Set the absolute temperature for each zone in Registers 6Ah-6Ch: Absolute Limit (Auto Fan Mode only). If the actual temperature is equal to or exceeds the absolute temperature in one or more zones, all Fans will be set to Full on, regardless of which zone they are operating in (except those that are disabled). Note: fans can be disabled via the Fan Configuration registers and the absolute temperature safety feature can be disabled by writing 80h into the Absolute Temp Limit registers.

5. To set the mode to operate in auto mode, set Bits[7:5] Zone/Mode, located in Registers 5Ch-5Eh: Fan Configuration: Bits[7:5]='000' for Fan on Zone 1; Bits[7:5]='001' for Fan on Zone 2; Bits[7:5]='010' for Fan on Zone 3. If the "Hottest" option is chosen (101 or 110), then the fan is controlled by the zone that results in the highest PWM duty cycle value.

Notes:

Software can be alerted of an out-of-limit condition by the INT# pin if a status bit is set and enabled (EMC6D100 only).

Software can monitor the operation of the Fans through the Fan Tachometer Reading registers and by the Fan x Current PWM duty registers. It can also monitor current temperature readings through the Temperature Limit Registers if hardware monitoring is enabled.

Fan control in auto mode is implemented without any input from external processor and without any consideration of the fan tachometer register values except during spin up. See description below.

In auto "Zone" mode, the speed is adjusted automatically as shown in the figure below. Fans are assigned to a zone. It is possible to have more than one fan in a thermal zone or one fan monitoring two or three fans.

FIGURE 7.2 shows the control flow for the auto fan algorithm. The part allows a minimum temperature to be set, below which the fan will not run or will run at minimum speed. A hysteresis value is included to prevent the fan continuously switching on and off if the temperature is close to the minimum. A temperature range is specified over which the part will automatically adjust the fan speed. When the temperature exceeds the minimum, the fan will "spin up" by going on full for a programmable amount of time. Following this spin up time, the fan will go to a duty cycle computed by the auto fan algorithm. As the temperature rises, the duty cycle will increase until the fan is running at full-speed when the temperature reaches the minimum plus the range value. The effect of this is a temperature feedback loop, which will cause the temperature to reach equilibrium between the minimum temperature and the minimum temperature plus the range. Provided that the fan has adequate cooling capacity for all environmental and power dissipation conditions, this system will maintain the temperature within acceptable limits, while allowing the fan to run slower (and quieter) when less cooling is required.

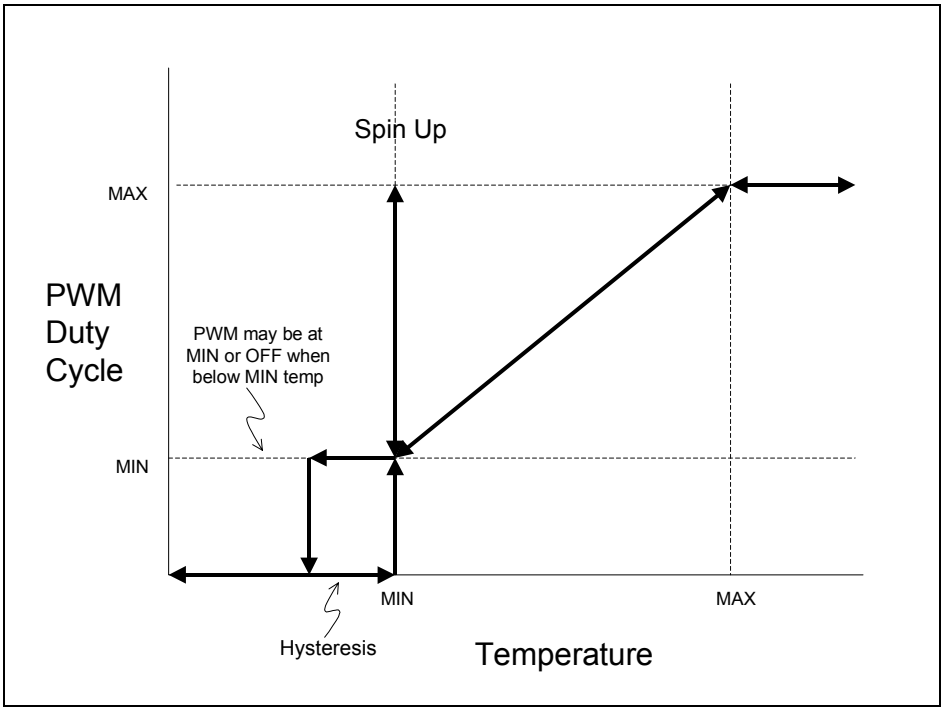


FIGURE 7.2 - AUTOMATIC FAN CONTROL

7.4.3 SPIN UP

When a fan is being started from a stationary state, the part will cause the fan to “spin up” by going to 100% duty cycle for a programmable amount of time to overcome the inertia of the fan. Following this spin up time, the fan will go to a duty cycle computed by the auto fan algorithm.

During spin-up, the PWM duty cycle is reported as 0%.

To limit the spin-up time and thereby reduce fan noise, the part uses feedback from the tachometers to determine when each fan has started spinning properly. The following tachometer feedback is included into the auto fan algorithm during spin-up. This feature defaults to enabled; it can be disabled by clearing bit 4 of the Configuration register (7Fh). If disabled, the all fans go to 100% duty cycle for the duration of their associated spin up time. Note that the Tachometer x minimum registers must be programmed to a value less than FFFFh in order for the spin up reduction to work properly.

1. The PWM goes to 100% duty cycle until the tachometer reading register is below the minimum limit, or the spin-up time expires, whichever comes first. This causes spin-up to continue until the tachometer enters the valid count range, unless the spin up time expires. If the spin up expires before the tachometer enters the valid range, an interrupt status bit will be set once spin-up expires. Note that more than one tachometer may be associated with a PWM, in which case all tachometers associated with a PWM must be in the valid range for spin-up to end.

2. The tachometer reading register always gives the actual reading of the tachometer input.

3. No interrupt bits are set during spin-up.

7.4.4 HOTTEST OPTION

If the “Hottest” option is chosen (101 or 110), then the fan is controlled by the limits and parameters associated with the zone that requires the highest PWM duty cycle value, as calculated by the auto fan algorithm.

7.5 Fan Speed Monitoring

The chip monitors the speed of the fans by utilizing fan tachometer input signals from fans equipped with tachometer outputs. The fan tachometer inputs are monitored by using the fan tachometer registers. These signals, as well as the Fan Tachometer registers, are described below.

7.5.1 FAN TACHOMETER INPUTS

A fan tachometer input is used to measure the speed at which a fan is rotating. The fan tachometer input is a train of square pulses with a 50% duty cycle (see FIGURE 7.3) that are derived from the magnetic fields generated by the rotating rotor of the fan. The speed of the fan can be determined by calculating the period of the Fan Tachometer input pulse.

Note: All calculations are based on fans that emit 2 square pulses per revolution. Reading registers reflect a count value for one complete revolution (2 pulses).

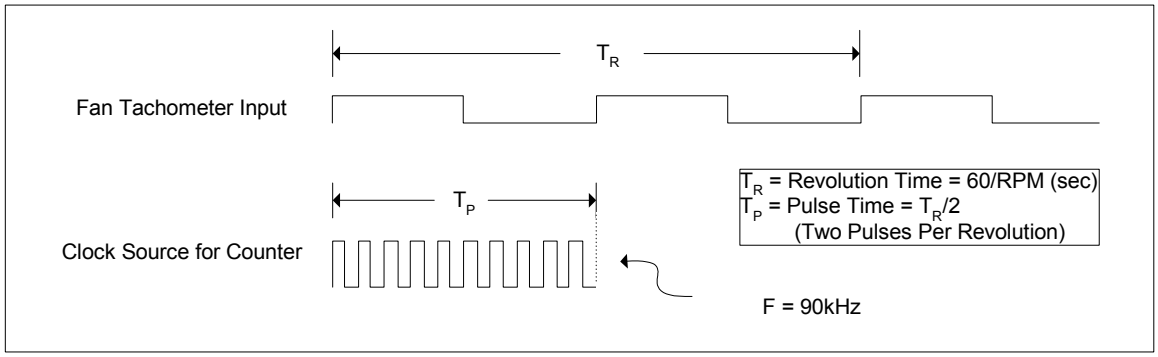


FIGURE 7.3 - FAN TACHOMETER INPUT AND CLOCK SOURCE

The counter is used to determine the period of the Fan Tachometer input pulse. This counter is reset on the rising edge of every other fan tachometer input pulse, and thus measures the number of clock pulses generated by the clock source for the duration of one fan tachometer revolution. Since two fan tachometer input pulses are generated per revolution of the fan rotor, the speed of the fan is easily calculated. The fan tachometer input resets the counter on every other pulse and simultaneously loads the count into its respective reading register. This value is used by the operating system to monitor the speed of the fan.

The fan tachometer reading registers contain the number of 11.111us periods (90kHz) between full fan revolutions. Fans produce 2 pulses per revolution.

The Tachometer Reading registers are 16 bits. The value FFFFh indicates that the fan is not spinning, or the tachometer input is not connected to a valid signal (this could be triggered by a counter overflow). These registers are read only – a write to these registers has no effect.

The Fan Tachometer Reading registers contain the number of periods of a full tachometer revolution (every two pulses). These registers are updated at least once every second. The frequency of the clock source for the tachometer logic is 90kHz. This register is latched on the rising edge of every other fan tachometer pulse and when the fan count reaches FFFFh. This latter condition is the stalled fan event.

7.5.2 DETECTION OF A STALLED FAN

The fan failure bit in the interrupt status register is set in the event of a stalled fan. Note: the fan tachometer reading register, which holds the count value, does not roll over - it stays at FFFFh in the event of a stalled fan. The internal count register does rollover, however, and continuously counts to FFFFh as long as the fan is stalled.

In the event the counter reaches FFFFh, the status bit is set and the count value is latched into the register. The second subsequent fan tach pulse resets the counter but does not latch the count value. Every second fan tach pulse latches the fan count value into the fan tachometer register except for this special case.

The status bit for a fan failure is set when the tach reading is above the value set in the tach minimum register. This interrupt status bit cannot be cleared by reading the status register as long as the count value is above the minimum.

The tachometer can generate an INT# if properly enabled (EMC6D100 only).

7.5.3 FAN INTERRUPT STATUS BITS

The status bits for the fan events are in Interrupt Status Register 2 (42h). These bits are set when the reading register is above the tachometer minimum. No interrupt status bits are set for fan events (even if the fan is stalled) if the associated tachometer minimum is set to FFFFh (registers 54h-5Bh).

7.6 Linking Fan Tachometers to PWMs

The Fan Tach/PWM Interrupt select register is used to link the tachometers to the PWMs. This association is used by the fan logic to determine when to prevent a bit from being set in the interrupt status registers. See the description of the PWM_TACH register. The default configuration is:

PWM1 -> TACH1.

PWM2 -> TACH2.

PWM3 -> TACH3 & TACH4.

7.7 System Synchronization

System Synchronization Pulses

Under normal operation, the PWM outputs will exhibit synchronization pulses in addition to the normal PWM pulses. These pulses are 44us in duration, and repeat every 711us. These synchronization pulses may be controlled by Register 83h: Synch Pulse Configuration Register: On/Off.

See section Chapter 8 Register Set for a description of this register.

See section Chapter 10 Timing Diagrams on page 71 for timing diagrams that illustrate PWM or synchronization pulses, PWM's with synchronization, and PWM's without synchronization.

Chapter 8 Register Set

Definition for the Lock and Start columns:

Yes = Register is made read-only when the related bit is set;

No = Register is **not** made read-only when the related bit is set.

Register Address	Read/ Write	Register Name	Abbr.	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value	Lock	Start
10h	R/W	SMSC Test Register	SMSC	7	6	5	4	3	2	1	0	00h	No	No
1Eh	R/W	Offset Register 2	OF2R	7	6	5	4	3	2	1	0	00h	Yes	Yes
1Fh	R/W	Offset Register 1	OF1R	7	6	5	4	3	2	1	0	00h	Yes	Yes
20h	R	2.5V	V25R	7	6	5	4	3	2	1	0	N/A	No	No
21h	R	Vccp	VCPR	7	6	5	4	3	2	1	0	N/A	No	No
22h	R	VCC	VCCR	7	6	5	4	3	2	1	0	N/A	No	No
23h	R	5V	V50R	7	6	5	4	3	2	1	0	N/A	No	No
24h	R	12V	V12R	7	6	5	4	3	2	1	0	N/A	No	No
25h	R	Processor (Zone1) Temp	TRD1	7	6	5	4	3	2	1	0	N/A	No	No
26h	R	Internal (Zone2) Temp	TAMR	7	6	5	4	3	2	1	0	N/A	No	No
27h	R	Remote (Zone3) Temp	TRD2	7	6	5	4	3	2	1	0	N/A	No	No
28h	R	Tach1 LSB	FTL1	7	6	5	4	3	2	1	0	N/A	No	No
29h	R	Tach1 MSB	FTM1	15	14	13	12	11	10	9	8	N/A	No	No
2Ah	R	Tach2 LSB	FTL2	7	6	5	4	3	2	1	0	N/A	No	No
2Bh	R	Tach2 MSB	FTM2	15	14	13	12	11	10	9	8	N/A	No	No
2Ch	R	Tach3 LSB	FTL3	7	6	5	4	3	2	1	0	N/A	No	No
2Dh	R	Tach3 MSB	FTM3	15	14	13	12	11	10	9	8	N/A	No	No
2Eh	R	Tach4 LSB	FTL4	7	6	5	4	3	2	1	0	N/A	No	No
2Fh	R	Tach4 MSB	FTM4	15	14	13	12	11	10	9	8	N/A	No	No
30h	R/W[1]	Fan1 Current PWM Duty	FCD1	7	6	5	4	3	2	1	0	N/A	Yes[1]	No[1]
31h	R/W[1]	Fan2 Current PWM Duty	FCD2	7	6	5	4	3	2	1	0	N/A	Yes[1]	No[1]
32h	R/W[1]	Fan3 Current PWM Duty	FCD3	7	6	5	4	3	2	1	0	N/A	Yes[1]	No[1]
3Eh	R	Company ID	COID	7	6	5	4	3	2	1	0	5Ch	No	No
3Fh	R	Version / Stepping	STNV	VER3	VER2	VER1	VER0	STP3	STP2	STP1	STP0	60h	No	No
40h	R/W[2]	Ready/Lock/Start	RLST	RES	RES	RES	RES	OVRID	READY	LOCK	START	00h	Yes[2]	No
41h	R-C[3]	Interrupt Status Register 1	INT1	INT23	ZN3	ZN2	ZN1	5V	VCC	Vccp	2.5V	00h	No	No
42h	R-C[3]	Interrupt Status Register 2	INT2	ERR2	ERR1	FAN4	FAN3	FAN2	FAN1	RES	12V	00h	No	No
43h	R	VID0-4	VIDR	RES	RES	RES	VID4	VID3	VID2	VID1	VID0	N/A	No	No
44h	R/W	2.5V Low Limit	V25L	7	6	5	4	3	2	1	0	00h	No	Yes
45h	R/W	2.5V High Limit	V25H	7	6	5	4	3	2	1	0	FFh	No	Yes
46h	R/W	Vccp Low Limit	VCPL	7	6	5	4	3	2	1	0	00h	No	Yes
47h	R/W	Vccp High Limit	VCPH	7	6	5	4	3	2	1	0	FFh	No	Yes
48h	R/W	VCC Low Limit	VCCL	7	6	5	4	3	2	1	0	00h	No	Yes
49h	R/W	VCC High Limit	VCCH	7	6	5	4	3	2	1	0	FFh	No	Yes

Register Address	Read/ Write	Register Name	Abbr.	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value	Lock	Start
4Ah	R/W	5V Low Limit	V50L	7	6	5	4	3	2	1	0	00h	No	Yes
4Bh	R/W	5V High Limit	V50H	7	6	5	4	3	2	1	0	FFh	No	Yes
4Ch	R/W	12V Low Limit	V12L	7	6	5	4	3	2	1	0	00h	No	Yes
4Dh	R/W	12V High Limit	V12H	7	6	5	4	3	2	1	0	FFh	No	Yes
4Eh	R/W	Processor (Zone1) Low Temp	TRL1	7	6	5	4	3	2	1	0	81h	No	Yes
4Fh	R/W	Processor (Zone1) High Temp	TRH1	7	6	5	4	3	2	1	0	7Fh	No	Yes
50h	R/W	Internal (Zone2) Low Temp	TALL	7	6	5	4	3	2	1	0	81h	No	Yes
51h	R/W	Internal (Zone2) High Temp	TAHL	7	6	5	4	3	2	1	0	7Fh	No	Yes
52h	R/W	Remote (Zone3) Low Temp	TRL2	7	6	5	4	3	2	1	0	81h	No	Yes
53h	R/W	Remote (Zone3) High Temp	TRH2	7	6	5	4	3	2	1	0	7Fh	No	Yes
54h	R/W	Tach1 Minimum LSB	FML1	7	6	5	4	3	2	1	0	FFh	No	Yes
55h	R/W	Tach1 Minimum MSB	FMM1	15	14	13	12	11	10	9	8	FFh	No	Yes
56h	R/W	Tach2 Minimum LSB	FML2	7	6	5	4	3	2	1	0	FFh	No	Yes
57h	R/W	Tach2 Minimum MSB	FMM2	15	14	13	12	11	10	9	8	FFh	No	Yes
58h	R/W	Tach3 Minimum LSB	FML3	7	6	5	4	3	2	1	0	FFh	No	Yes
59h	R/W	Tach3 Minimum MSB	FMM3	15	14	13	12	11	10	9	8	FFh	No	Yes
5Ah	R/W	Tach4 Minimum LSB	FML4	7	6	5	4	3	2	1	0	FFh	No	Yes
5Bh	R/W	Tach4 Minimum MSB	FMM4	15	14	13	12	11	10	9	8	FFh	No	Yes
5Ch	R/W	Fan 1 Configuration	FCF1	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	Yes	Yes
5Dh	R/W	Fan 2 Configuration	FCF2	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	Yes	Yes
5Eh	R/W	Fan 3 Configuration	FCF3	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62h	Yes	Yes
5Fh	R/W	Zone 1 Range/Fan 1 Frequency	FRF1	RAN3	RAN2	RAN1	RAN0	RES	FRQ2	FRQ1	FRQ0	C3h	Yes	Yes
60h	R/W	Zone 2 Range/Fan 2 Frequency	FRF2	RAN3	RAN2	RAN1	RAN0	RES	FRQ2	FRQ1	FRQ0	C3h	Yes	Yes
61h	R/W	Zone 3 Range/Fan 3 Frequency	FRF3	RAN3	RAN2	RAN1	RAN0	RES	FRQ2	FRQ1	FRQ0	C3h	Yes	Yes
62h	R/W	Min/Off, Zone 1 Spike Smoothing	SSZ1	OFF3	OFF2	OFF1	RES	ZN1E	ZN1-2	ZN1-1	ZN1-0	00h	Yes	Yes
63h	R/W	Zone 2, Zone 3 Spike Smoothing	SS23	ZN2E	ZN2-2	ZN2-1	ZN2-0	ZN3E	ZN3-2	ZN3-1	ZN3-0	00h	Yes	Yes
64h	R/W	Fan1 PWM Minimum	DCM1	7	6	5	4	3	2	1	0	80h	Yes	Yes
65h	R/W	Fan2 PWM Minimum	DCM2	7	6	5	4	3	2	1	0	80h	Yes	Yes
66h	R/W	Fan3 PWM Minimum	DCM3	7	6	5	4	3	2	1	0	80h	Yes	Yes
67h	R/W	Zone 1 Fan Temp Limit	TLF1	7	6	5	4	3	2	1	0	5Ah	Yes	Yes
68h	R/W	Zone 2 Fan Temp Limit	TLF2	7	6	5	4	3	2	1	0	5Ah	Yes	Yes
69h	R/W	Zone 3 Fan Temp Limit	TLF3	7	6	5	4	3	2	1	0	5Ah	Yes	Yes
6Ah	R/W	Zone 1 Temp Absolute Limit	TAF1	7	6	5	4	3	2	1	0	64h	Yes	Yes
6Bh	R/W	Zone 2 Temp Absolute Limit	TAF2	7	6	5	4	3	2	1	0	64h	Yes	Yes
6Ch	R/W	Zone 3 Temp Absolute Limit	TAF3	7	6	5	4	3	2	1	0	64h	Yes	Yes

Register Address	Read/ Write	Register Name	Abbr.	Bit 7 (MSb)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSb)	Default Value	Lock	Start
6Dh	R/W	Zone 1, Zone 2 Hysteresis	HY12	H1-3	H1-2	H1-1	H1-0	H2-3	H2-2	H2-1	H2-0	44h	Yes	Yes
6Eh	R/W	Zone 3, Hysteresis	HYS3	H3-3	H3-2	H3-1	H3-0	RES	RES	RES	RES	40h	Yes	Yes
6Fh	R/W	XOR Test Tree Enable	XORT	RES	RES	RES	RES	RES	RES	RES	XEN	00h	Yes	Yes
70h	R	+3.3V Reading	V33R	7	6	5	4	3	2	1	0	NA	No	No
71h	R	+1.5 Reading	V15R	7	6	5	4	3	2	1	0	NA	No	No
72h	R	+1.8 Reading	V18R	7	6	5	4	3	2	1	0	NA	No	No
73h	R/W	+3.3V Low Limit	V33L	7	6	5	4	3	2	1	0	00h	No	Yes
74h	R/W	+3.3V High Limit	V33H	7	6	5	4	3	2	1	0	FFh	No	Yes
75h	R/W	+1.5 Low Limit	V15L	7	6	5	4	3	2	1	0	00h	No	Yes
76h	R/W	+1.5 High Limit	V15H	7	6	5	4	3	2	1	0	FFh	No	Yes
77h	R/W	+1.8 Low Limit	V18L	7	6	5	4	3	2	1	0	00h	No	Yes
78h	R/W	+1.8 High Limit	V18h	7	6	5	4	3	2	1	0	FFh	No	Yes
79h	R/W	Test Mode Register	MOTR	ANTST2	ANTST1	ANTST0	OSCSEL	ADCAVG	EXTCLK	DIGTST	ADCTST	00h	Yes	Yes
7Ah	R	Error Debug Register	ERDR	RES	ARA	STOP	INVADD	RCV	ROWR	INVRW	NONAC	00h	No	No
7Bh	R/W	Test Digital Value Register	DVTR	7	6	5	4	3	2	1	0	00h	Yes	Yes
7Ch	R/W[4]	Special Function Register	SFTR	D2EN	D1EN	AVG	OFFCFG	VOLTEN	INTEN	MONMD	LPMD	E0h	Yes[4]	Yes[4]
7Dh	R-C[3]	Interrupt Status Register 3	INT3	RES	RES	RES	RES	RES	33V	18V	15V	00h	No	No
7Eh	R/W	Interrupt Enable	INTE	VCC	12V	5V	33V	VCCP	25V	18V	15V	ECh	Yes	Yes
7Fh	R/W	Configuration	CONF	INIT	FTTST	RES	SUREN	TRDY	RES	P4INT	RES	10h	Yes	Yes
80h	R/W	Fan Temp Interrupt Enable	FTIE	RES	AMB	TEMP	FAN4	FAN3	FAN2	FAN1	FAN	5Eh	Yes	Yes
81h	R/W	Fan Tach/PWM Interrupt Select	FTIS	T4H	T4L	T3H	T3L	T2H	T2L	T1H	T1L	A4h	Yes	Yes
82h	R/W	Reserved	N/A	RES	RES	RES	RES	RES	RES	RES	RES	FFh	Yes	No
83h	R/W	Sync Pulse Configuration Register: ON/OFF	FCF4	RES	RES	RES	ON	RES	RES	RES	RES	62h	Yes	Yes
84h	R/W	Reserved	N/A	RES	RES	RES	RES	RES	RES	RES	RES	03h	Yes	Yes
85h	R/W	Reserved	N/A	RES	RES	RES	RES	RES	RES	RES	RES	80h	Yes	Yes
86h	R	Smooth Remote Diode Reading 1	SRD1	7	6	5	4	3	2	1	0	N/A	No	No
87h	R	Smooth Ambient Reading	SAMR	7	6	5	4	3	2	1	0	N/A	No	No
88h	R	Smooth Remote Diode Reading 2	SRD2	7	6	5	4	3	2	1	0	N/A	No	No
89h	R	ADC 2 LSB Test	ADTR	7	6	5	4	3	2	1	0	N/A	No	No
8Ah	R	Input Test Reg 1	CBI1	RES	6	5	4	3	2	1	0	4Dh	No	No
8Bh	R/W	Output Test Reg 1	CBO1	7	6	5	4	3	2	1	0	4Dh	Yes	Yes
8Ch	R	Input Test Reg 2	CBI2	RES	RES	RES	4	3	2	1	0	0Eh	No	No
8Dh	R/W	Output Test Reg 2	CBO2	RES	RES	RES	4	3	2	1	0	0Eh	Yes	Yes

Notes:

1. The Fan x Current Duty Cycle Registers are only writeable when the associated fan is in manual mode. In this case, the register is writeable when the start bit is set, but not when the lock bit is set.

2. The Lock and Start bits in the Ready/Lock/Start register are locked by the Lock Bit. The OVRID bit is always writeable, both when the start bit is set and when the lock bit is set.

3. The Interrupt status registers are cleared on a read if no events are active.

4. The INTEN bit in register 7Ch is always writeable, both when the start bit is set and when the lock bit is set.

8.1 Undefined Registers

The registers shown in the table above are the defined registers in the part. Any reads to undefined registers always return 00h. Writes to undefined registers have no effect and do not return an error.

8.2 Register 10h: SMSC Test Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
10h	R/W	SMSC TEST	7	6	5	4	3	2	1	0	00h

Setting the Lock bit has no effect on this register.

This register must not be written. Writing this register may produce unexpected results.

8.3 Register 1E, 1Fh: Offset Registers

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
1Eh	R/W	Offset Register 2	7	6	5	4	3	2	1	0	00h
1Fh	R/W	Offset Register 1	7	6	5	4	3	2	1	0	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

Offset Register 2

Only applies to the remote diode temperature reading 2. This register contains a 2's complement value which is added (or subtracted if the number is negative) to external temperature reading 2. The default value in the offset register is zero, so initially zero is always added to the temperature reading.

Offset Register 1

Applies to the remote diode temperature reading 1 or the ambient reading. This register contains a 2's complement value which is added (or subtracted if the number is negative) to either the internal or external temperature 1 reading. The default value in the offset register is zero, so initially zero is always added to the temperature reading. The offset register is configured for the external temperature 1 channel by default. It may be switched to the internal channel by setting bit 4 of the Special Function Register to 1.

8.4 Registers 20-24h, 70-72h: Voltage Reading

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
20h	R	2.5V	7	6	5	4	3	2	1	0	N/A
21h	R	Vccp	7	6	5	4	3	2	1	0	N/A

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
22h	R	3.3V	7	6	5	4	3	2	1	0	N/A
23h	R	5V	7	6	5	4	3	2	1	0	N/A
24h	R	12V	7	6	5	4	3	2	1	0	N/A
70h	R	+3.3V	7	6	5	4	3	2	1	0	N/A
71h	R	+1.5V	7	6	5	4	3	2	1	0	N/A
72h	R	+1.8V	7	6	5	4	3	2	1	0	N/A

Note: registers 70h-72h are only applicable to the EMC6D100.

The Voltage Reading registers reflect the current voltage of the EMC6D100/EMC6D101 voltage monitoring inputs. Voltages are presented in the registers at ¾ full scale for the nominal voltage, meaning that at nominal voltage, each register will read C0h.

Table 8.1 - Voltage vs. Register Reading

INPUT	NOMINAL VOLTAGE	REGISTER READING AT NOMINAL VOLTAGE	MAXIMUM VOLTAGE	REGISTER READING AT MAXIMUM VOLTAGE	MINIMUM VOLTAGE	REGISTER READING AT MINIMUM VOLTAGE
1.5V	1.5V	C0h	1.99V	FFh	0V	00h
1.8V	1.8V	C0h	2.39V	FFh	0V	00h
2.5V	2.5V	C0h	3.32V	FFh	0V	00h
Vccp	2.25V	C0h	3.00V	FFh	0V	00h
VCC	3.3V	C0h	4.38V	FFh	0V	00h
3.3V	3.3V	C0h	4.38V	FFh	0V	00h
5V	5.0V	C0h	6.64V	FFh	0V	00h
12V	12.0V	C0h	16.00V	FFh	0V	00h

The Voltage Reading registers will be updated automatically by the EMC6D100/EMC6D101 Chip with a minimum frequency of 4Hz. These registers are read only – a write to these registers has no effect.

8.5 Registers 25-27h: Temperature Reading

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
25h	R	Processor (Zone1) Temp	7	6	5	4	3	2	1	0	N/A
26h	R	Internal (Zone2) Temp	7	6	5	4	3	2	1	0	N/A
27h	R	Remote (Zone3) Temp	7	6	5	4	3	2	1	0	N/A

The Temperature Reading registers reflect the current temperatures of the internal and remote diodes. Processor (Zone1) Temp register reports the temperature measured by the Remote1- and Remote1+ pins, Remote (Zone3) Temp register reports the temperature measured by the Remote2- and Remote2+ pins and the Internal (Zone2) Temp register reports the temperature measured by the internal (ambient) temperature sensor. Current temperatures are represented as 8 bit, 2's complement, signed numbers in Celsius, as shown below in Table 8.2. The Temperature Reading register will return a value of 80h if the remote diode pins are not implemented by the board designer or are not functioning properly (this corresponds to the diode fault interrupt status bits). The Temperature Reading registers will be updated automatically by the EMC6D100/EMC6D101 Chip with a minimum frequency of 4Hz. These registers are read only – a write to these registers has no effect.

Table 8.2 - Temperature vs. Register Reading

TEMPERATURE	READING (DEC)	READING (HEX)
-127°c	-127	81h
⋮	⋮	⋮
-50°c	-50	CEh
⋮	⋮	⋮
0°c	0	00h
⋮	⋮	⋮
50°c	50	32h
⋮	⋮	⋮
127°c	127	7Fh
(SENSOR ERROR)		80h

8.6 Registers 28-2Fh: Fan Tachometer Reading

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
28h	R	Tach1 LSB	7	6	5	4	3	2	1	0	**N/A**
29h	R	Tach1 MSB	15	14	13	12	11	10	9	8	**N/A**
2Ah	R	Tach2 LSB	7	6	5	4	3	2	1	0	**N/A**
2Bh	R	Tach2 MSB	15	14	13	12	11	10	9	8	**N/A**
2Ch	R	Tach3 LSB	7	6	5	4	3	2	1	0	**N/A**
2Dh	R	Tach3 MSB	15	14	13	12	11	10	9	8	**N/A**
2Eh	R	Tach4 LSB	7	6	5	4	3	2	1	0	**N/A**
2Fh	R	Tach4 MSB	15	14	13	12	11	10	9	8	**N/A**

The Fan Tachometer Reading registers contain the number of 11.111µs periods (90KHz) between full fan revolutions. Fans produce two tachometer pulses per full revolution. These registers are updated at least once every second.

This value is represented for each fan in a 16 bit, unsigned number.

The Fan Tachometer Reading registers always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional, including when the start bit=0.

When one byte of a 16-bit register is read, the other byte latches the current value until it is read, in order to ensure a valid reading. The order is LSB first, MSB second.

FFFFh indicates that the fan is not spinning, or the tachometer input is not connected to a valid signal (This could be triggered by a counter overflow).

These registers are read only – a write to these registers has no effect.

8.7 Registers 30-32h: Current PWM Duty

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
30h	R/W[1]	Fan1 Current	7	6	5	4	3	2	1	0	N/A

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
		PWM Duty									
31h	R/W[1]	Fan2 Current PWM Duty	7	6	5	4	3	2	1	0	N/A
32h	R/W[1]	Fan3 Current PWM Duty	7	6	5	4	3	2	1	0	N/A

Note 1: these registers are only writeable when the associated fan is in manual mode. These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The Current PWM Duty registers store the duty cycle that the EMC6D100/EMC6D101 Chip is currently driving the PWM signals at. At initial power-on, the duty cycle is 100% and thus, when read, this register will return FFh. After the **Ready/Lock/Start** Register Start bit is set, this register and the PWM signals are updated based on the algorithm described in the Auto Fan Control Operating Mode section, unless the associated fan is in manual mode – see below.

When read, the Current PWM Duty registers return the current PWM duty cycle for the respective PWM signal.

These registers are read only – a write to these registers has no effect.

Note: If the current PWM duty cycle registers are written while the part is not in manual mode and the start bit is zero, data will be stored in a hidden registers that will only be active and observable when the start bit is set. While the part is not in manual mode and the start bit is zero, the current PWM duty cycle registers will read back FFh.

8.7.1 MANUAL MODE

In manual mode, the current duty cycle registers are writeable to control the PWMs. In manual mode, when the start bit is set to 1, the current duty cycle registers are writeable to control the PWMs. Also in manual mode, when the lock bit is set to 1, the current duty cycle registers are Read-Only.

The PWM duty cycle is represented as follows:

Table 8.3 - PWM Duty vs. Register Reading

CURRENT DUTY	VALUE (DECIMAL)	VALUE (HEX)
0%	0	00h
⋮	⋮	⋮
25%	64	40h
⋮	⋮	⋮
50%	128	80h
⋮	⋮	⋮
100%	255	FFh

During spin-up, the PWM duty cycle is reported as 0%.

8.8 Register 3Eh: Company ID

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
3Eh	R	Company ID	7	6	5	4	3	2	1	0	5Ch

The Company ID register contains the company identification number. This number is a method for uniquely identifying the part manufacturer.

This register is read only – a write to this register has no effect.

8.9 Register 3Fh: Version / Stepping

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
3Fh	R	Version / Stepping	VER3	VER2	VER1	VER0	STP3	STP2	STP1	STP0	60h

The four least significant bits of the Version / Stepping register [3:0] contain the current stepping of the EMC6D100/EMC6D101 silicon. The four most significant bits [7:4] reflect the EMC6D100/EMC6D101 version number. The EMC6D100/EMC6D101 has a fixed version number of 0110b. For the A0 stepping of EMC6D100/EMC6D101, this register will read 01100000b. For the A1 stepping of the EMC6D100/EMC6D101, this register will read 01100001b.

The register is used by application software to identify which device in the EMC family of monitoring ASICs has been implemented in the given system. Based on this information, software can determine which registers to read from and write to. Further, application software may use the current stepping to implement work-arounds for bugs found in a specific silicon stepping.

This register is read only – a write to this register has no effect.

8.10 Register 40h: Ready/Lock/Start Monitoring

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
40h	R/W	Ready/Lock/Start	*RES*	*RES*	*RES*	*RES*	OVRID	READY	LOCK	START	00h

Setting the Lock bit makes the Lock and Start bits read-only.

BIT	NAME	R/W	DEFAULT	DESCRIPTION
0	START	R/W	0	When software writes a 1 to this bit, the EMC6D100/EMC6D101 enables monitoring and PWM output control functions based on the limit and parameter registers. Before this bit is set, the part does not update register values. Whenever this bit is set to 0, the monitoring and PWM output control functions are based on the default limits and parameters, regardless of the current values in the limit and parameter registers. The EMC6D100/EMC6D101 preserves the values currently stored in the limit and parameter registers when this bit is set or cleared. This bit becomes read only when the Lock bit is set. **Note:** When this bit is 0, all fans are on full 100% duty cycle, i.e., PWM pins are high (OD) for 255 clocks, low for 1 clock. When this bit is 0, the part is not monitoring. It is expected that all limit and parameter registers will be set by BIOS or application software prior to setting this bit because these registers cannot be written once the start bit is set.
1	LOCK	R/W	0	Setting this bit to 1 locks specified limit and parameter registers. Once this bit is set, limit and parameter registers become read only and will remain locked until the device is powered off. This register bit becomes read only once it is set.
2	READY	R	0	The EMC6D100/EMC6D101 sets this bit automatically after the part is fully powered up, has completed the power-up-reset process, and after all A/D converters are functioning (all bias conditions for the A/Ds have stabilized and the A/Ds are in operational mode). (Always reads back ‘1’.)
3	OVRID	R/W	0	If this bit is set to 1, all PWM outputs go to 100% duty cycle regardless of whether or not the lock bit is set.
4-7	Reserved	R	0	Reserved

Note: There is a start-up time of up to 82ms for monitoring after the start bit is set to ‘1’, during which time the reading registers are not valid.

The following summarizes the operation of the part based on the Start bit:

1. If Start bit = '0' then:
   a) Fans are set to Full On.
   b) No voltage, temperature, or fan tach monitoring is performed. The values in the reading registers will be N/A (Not Applicable), which means these values will not be considered valid readings until the Start bit = '1'. The exception to this is the Tachometer reading registers, which always give the actual reading on the TACH pins.
   c) No Status bits are set.

2. If Start bit = '1' then:
   a) All fan control and monitoring will be based on the current values in the registers. There is no need to preserve the default values after software has programmed these registers because no monitoring or auto fan control will be done when Start bit = '0'.
   b) Status bits may be set.
   c) The limit and parameter registers are read-only when the start bit is 1. Only the Current PWM Duty Cycle and Ready/Lock /Start registers are writeable when the associated fan is in manual mode. The INTEN bit in register 7Ch is also writeable when the start bit is set.

Note: Once programmed, the register values will be saved when start bit is reset to ‘0’.

8.11 Register 41h: Interrupt Status Register 1

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
41h	R-C[1]	Interrupt Status 1	INT23	ZN3	ZN2	ZN1	5V	3.3V	Vccp	2.5V	00h

Note 1: This register is cleared on a read if no events are active

The Interrupt Status Register 1 bits are automatically set by the EMC6D100/EMC6D101 whenever the 2.5V, Vccp, 3.3V, or 5V input voltages violate the limits set in the limit and parameter registers or when the measured temperature violates the limits set in the limit and parameter registers for any of the three thermal zones.

This register holds a set bit until the event is read by software. The contents of this register are cleared (set to 0) automatically by the EMC6D100/EMC6D101 after it is read by software, if the voltage or temperature no longer violates the limits set in the limit and parameter registers. Once set, the Interrupt Status Register 1 bits remain set until a read event occurs, even if the voltage or temperature no longer violate the limits set in the limit and parameter registers.

This register contains a bit that indicates that a bit is set in one of the other interrupt status registers. If bit 7 is set, then a status bit is set in either Interrupt Status Register 2 or 3 (or both). Therefore, S/W can poll this register, and only if bit 7 is set do the other registers need to be read. This bit is cleared (set to 0) automatically by the EMC6D100/EMC6D101 if there are no bits set in Interrupt Status Registers 2 and 3.

This register is read only – a write to this register has no effect.

BIT	NAME	R/W	DEFAULT	DESCRIPTION
0	2.5V_Error	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when the 2.5V input voltage is less than or equal to the limit set in the 2.5V Low Limit register or greater than the limit set in the 2.5V High Limit register.
1	Vccp_Error	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when the Vccp input voltage is less than or equal to the limit set in the Vccp Low Limit register or greater than the limit set in the Vccp High Limit register.
2	3.3V_Error	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when the 3.3V input voltage is less than or equal to the limit set in the 3.3V Low Limit register or greater than the limit set in the 3.3V High Limit register.
3	5V_Error	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when the 5V input voltage is less than or equal to the limit set in the 5V Low Limit register or greater than the limit set in the 5V High Limit register.
4	Zone 1 Limit Exceeded	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when the temperature input measured by the Remote1- and Remote1+ is less than or equal to the limit set in the Processor (Zone1) Low Temp register or greater than the limit set in Processor (Zone1) High Temp register.
5	Zone 2 Limit Exceeded	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when the temperature input measured by the internal temperature sensor is less than or equal to the limit set in the Internal (Zone2) Low Temp register or greater than the limit set in the Internal (Zone2) High Temp register.
6	Zone 3 Limit Exceeded	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when the temperature input measured by the Remote2- and Remote2+ is less than or equal to the limit set in the Remote (Zone3) Low Temp register or greater than the limit set in the Remote (Zone3) High Temp register.

BIT	NAME	R/W	DEFAULT	DESCRIPTION
7	INT2, 3 Event Active	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when a status bit is set in either Interrupt Status Register 2 or 3.

8.12 Register 42h: Interrupt Status Register 2

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
42h	R-C[1]	Interrupt Status Register 2	ERR2	ERR1	FAN4	FAN3	FAN2	FAN1	RES	12V	00h

Note 1: This register is cleared on a read if no events are active

The Interrupt Status Register 2 bits is automatically set by the EMC6D100/EMC6D101 whenever a remote temperature sensor error occurs, a fan is above the minimum speed set in the tachometer minimum registers, or whenever the 12V input voltage violates the limits set in the limit and parameter registers. The Interrupt Status Register 2 register holds a set bit until the event is read by software.

The contents of this register are cleared (set to 0) automatically by the EMC6D100/EMC6D101 after it is read by software, if the voltage or temperature no longer violates the limits set in the limit and parameter registers, or if the fan reading register is no longer above the minimum. Once set, the Interrupt Status Register 2 bits remain set until a read event occurs, even if the voltage or temperature no longer violates the limits set in the limit and parameter registers or if the fan reading register is below the minimum.

The remote diode fault bits do not clear on a read while the fault condition exists. A fault event loads 80h into the associated temperature reading register when the start bit is set, which will cause the associated diode limit error bit to be set (Zone 1 Limit Exceeded or Zone 3 Limit Exceeded) in addition to the diode fault bit. Disabling the enable bit for the diode will clear both the fault bit and the error bit for that diode.

This register is read only – a write to this register has no effect.

BIT	NAME	R/W	DEFAULT	DESCRIPTION
0	+12v_Error	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when the 12V input voltage is less than or equal to the limit set in the 12V Low Limit register or greater than the limit set in the 12V High Limit register.
1	Reserved	R	0	Reserved
2	Fan1 Stalled	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when the TACH1 input reading is above the value set in the Tach1 Minimum MSB and LSB registers.
3	Fan2 Stalled	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when the TACH2 input reading is above the value set in the Tach2 Minimum MSB and LSB registers.
4	Fan3 Stalled	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when the TACH3 input reading is above the value set in the Tach3 Minimum MSB and LSB registers.
5	Fan4 Stalled	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when the TACH4 input reading is above the value set in the Tach4 Minimum MSB and LSB registers.
6	Remote Diode 1 Fault	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when there is either a short or open circuit fault on the Remote1+ or Remote1- thermal diode input pins.
7	Remote Diode 2 Fault	R	0	The EMC6D100/EMC6D101 automatically sets this bit to 1 when there is either a short or open circuit fault on the Remote2+ or Remote2- thermal diode input pins.

8.13 Register 7Dh: Interrupt Status Register 3

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
7Dh	R-C[1]	Interrupt Status Register 3	RES	RES	RES	RES	RES	33V	18V	15V	00h

Note 1: This register is cleared on a read if no events are active

Note: this register only applies to the EMC6D100.

The Interrupt Status Register 3 bits are automatically set by the EMC6D100 whenever the 1.5V, 1.8V, or 3.3V input voltages violate the limits set in the limit and parameter registers.

This register holds a set bit until the event is read by software. The contents of this register is cleared (set to 0) automatically by the EMC6D100 after it is read by software, if the voltage no longer violates the limit set in the limit and parameter register. Once set, the Interrupt Status Register 3 bits remain set until a read event occurs, even if the voltage or temperature no longer violates the limits set in the limit and parameter registers.

This register is read only – a write to this register has no effect.

BIT	NAME	R/W	DEFAULT	DESCRIPTION
0	+1.5v_Error	R	0	The EMC6D100 automatically sets this bit to 1 when the 1.5V input voltage is less than or equal to the limit set in the 1.5V Low Limit register or greater than the limit set in the 1.5V High Limit register.
1	+1.8V_Error	R	0	The EMC6D100 automatically sets this bit to 1 when the 1.8V input voltage is less than or equal to the limit set in the 1.8V Low Limit register or greater than the limit set in the 1.8V High Limit register.
2	+3.3V_Error	R	0	The EMC6D100 automatically sets this bit to 1 when the 3.3V input voltage is less than or equal to the limit set in the 3.3V Low Limit register or greater than the limit set in the 3.3V High Limit register.
3-7	Reserved	R	0	Reserved

8.14 Register 43h: VID

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
43h	R	VID0-4	*RES*	*RES*	*RES*	VID4	VID3	VID2	VID1	VID0	N/A

The VID register contains the values of EMC6D100/EMC6D101 VID0-VID4 input pins. This register indicates the status of the VID lines that interconnect the processor to the Voltage Regulator Module (VRM). Software uses the information in this register to determine the voltage that the processor is designed to operate at. With this information, software can then dynamically determine the correct values to place in the Vccp Low Limit and Vccp High Limit registers.

This register is read only – a write to this register has no effect.

8.15 Registers 44-4Dh, 73-78h: Voltage Limit Registers

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
44h	R/W	2.5V Low Limit	7	6	5	4	3	2	1	0	00h
45h	R/W	2.5V High Limit	7	6	5	4	3	2	1	0	FFh
46h	R/W	Vccp Low Limit	7	6	5	4	3	2	1	0	00h
47h	R/W	Vccp High Limit	7	6	5	4	3	2	1	0	FFh
48h	R/W	VCC Low Limit	7	6	5	4	3	2	1	0	00h
49h	R/W	VCC High Limit	7	6	5	4	3	2	1	0	FFh
4Ah	R/W	5V Low Limit	7	6	5	4	3	2	1	0	00h
4Bh	R/W	5V High Limit	7	6	5	4	3	2	1	0	FFh
4Ch	R/W	12V Low Limit	7	6	5	4	3	2	1	0	00h
4Dh	R/W	12V High Limit	7	6	5	4	3	2	1	0	FFh
73h	R/W	3.3V Low Limit	7	6	5	4	3	2	1	0	00h
74h	R/W	3.3V High Limit	7	6	5	4	3	2	1	0	FFh
75h	R/W	1.5 Low Limit	7	6	5	4	3	2	1	0	00h
76h	R/W	1.5 High Limit	7	6	5	4	3	2	1	0	FFh
77h	R/W	1.8 Low Limit	7	6	5	4	3	2	1	0	00h
78h	R/W	1.8 High Limit	7	6	5	4	3	2	1	0	FFh

Note: registers 73h-78h are applicable to the EMC6D100 only.

Setting the Lock bit has no effect on these registers.

If a voltage input either exceeds the value set in the voltage high limit register or falls below or equals the value set in the voltage low limit register, the corresponding bit will be set automatically by the EMC6D100/EMC6D101 in the interrupt status registers (41-42h, 7Dh). Voltages are presented in the registers at ¾ full scale for the nominal voltage, meaning that at nominal voltage, each input will be C0h, as shown in Table 8.4.

Table 8.4 – Voltage Limits vs. Register Setting

INPUT	NOMINAL VOLTAGE	REGISTER SETTING AT NOMINAL VOLTAGE	MAXIMUM VOLTAGE	REGISTER SETTING AT MAXIMUM VOLTAGE	MINIMUM VOLTAGE	REGISTER SETTING AT MINIMUM VOLTAGE
1.5V	1.5V	C0h	1.99V	FFh	0V	00h
1.8V	1.8V	C0h	2.39V	FFh	0V	00h
2.5V	2.5V	C0h	3.32V	FFh	0V	00h
Vccp	2.25V	C0h	3.00V	FFh	0V	00h
VCC	3.3V	C0h	4.38V	FFh	0V	00h
3.3V	3.3V	C0h	4.38V	FFh	0V	00h
5V	5.0V	C0h	6.64V	FFh	0V	00h
12V	12.0V	C0h	16.00V	FFh	0V	00h

Note: The voltages 1.5V, 1.8V and 3.3V in the table above are applicable to the EMC6D100 only.

8.16 Registers 4E-53h: Temperature Limit Registers

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
4Eh	R/W	Processor (Zone1) Low Temp	7	6	5	4	3	2	1	0	81h
4Fh	R/W	Processor (Zone1) High Temp	7	6	5	4	3	2	1	0	7Fh
50h	R/W	Internal (Zone2) Low Temp	7	6	5	4	3	2	1	0	81h
51h	R/W	Internal (Zone2) High Temp	7	6	5	4	3	2	1	0	7Fh
52h	R/W	Remote (Zone3) Low Temp	7	6	5	4	3	2	1	0	81h
53h	R/W	Remote (Zone3) High Temp	7	6	5	4	3	2	1	0	7Fh

Setting the Lock bit has no effect on these registers.

If an external temperature input or the internal temperature sensor either exceeds the value set in the high limit register or falls below the value set in the low limit register, the corresponding bit will be set automatically by the EMC6D100/EMC6D101 in the Interrupt Status Register 1 (41h). For example, if the temperature read from the Remote1- and Remote2+ inputs exceeds the Processor (Zone1) High Temp register limit setting, Interrupt Status Register 1 ZN1 bit will be set. The temperature limits in these registers are represented as 8 bit, 2's complement, signed numbers in Celsius, as shown below in Table 8.5.

Table 8.5 - Temperature Limits vs Register Settings

TEMPERATURE	LIMIT (DEC)	LIMIT (HEX)
-127°c	-127	81h
⋮	⋮	⋮
-50°c	-50	CEh
⋮	⋮	⋮
0°c	0	00h
⋮	⋮	⋮
50°c	50	32h
⋮	⋮	⋮
127°c	127	7Fh

8.17 Registers 54-5Bh: Fan Tachometer Low Limit

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
54h	R/W	Tach1 Minimum LSB	7	6	5	4	3	2	1	0	FFh
55h	R/W	Tach1 Minimum MSB	15	14	13	12	11	10	9	8	FFh
56h	R/W	Tach2 Minimum LSB	7	6	5	4	3	2	1	0	FFh
57h	R/W	Tach2 Minimum MSB	15	14	13	12	11	10	9	8	FFh
58h	R/W	Tach3 Minimum LSB	7	6	5	4	3	2	1	0	FFh
59h	R/W	Tach3 Minimum MSB	15	14	13	12	11	10	9	8	FFh
5Ah	R/W	Tach4 Minimum LSB	7	6	5	4	3	2	1	0	FFh
5Bh	R/W	Tach4 Minimum MSB	15	14	13	12	11	10	9	8	FFh

Setting the Lock bit has no effect on these registers.

The Fan Tachometer Low Limit registers indicate the tachometer reading under which the corresponding bit will be set in the Interrupt Status Register 2 register. In Auto Fan Control mode, the fan can run at low speeds, so care should be taken in software to ensure that the limit is low enough not to cause sporadic alerts.

The fan tachometer will not cause a bit to be set in the interrupt status register if the current value in Current PWM Duty registers is 00h or if the fan is disabled via the Fan Configuration Register.

Interrupts will never be generated for a fan if its tachometer minimum is set to FFFFh.

8.18 Registers 5C-5Eh: Fan Configuration

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
5Ch	R/W	Fan 1 Configuration	ZON2	ZON1	ZON0	INV	*RES*	SPIN2	SPIN1	SPIN0	62h
5Dh	R/W	Fan 2 Configuration	ZON2	ZON1	ZON0	INV	*RES*	SPIN2	SPIN1	SPIN0	62h
5Eh	R/W	Fan 3 Configuration	ZON2	ZON1	ZON0	INV	*RES*	SPIN2	SPIN1	SPIN0	62h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

8.18.1 BITS [7:5] ZONE/MODE

Bits [7:5] of the Fan Configuration registers associate each fan with a temperature sensor. When in Auto Fan Mode, the fan will be assigned to a zone, and its PWM duty cycle will be adjusted according to the temperature of that zone. If 'Hottest' option is selected (101 or 110), the fan will be controlled by the hottest of zones 2 and 3, or of zones 1, 2, and 3. If one of these options is selected, the fan is controlled by the

limits and parameters for the zone that requires the highest PWM duty cycle, as computed by the auto fan algorithm.

When in manual control mode, the Current PWM Duty Registers (30h-32h) become Read/Write. It is then possible to control the PWM outputs with software by writing to these registers. See Current PWM Duty Registers description.

When the fan is disabled (100) the corresponding PWM output is driven low (or high, if inverted).

Zone 1: External Diode 1 (processor)

Zone 2: Internal Sensor

Zone 3: External Diode 2

Table 8.6 - Fan Zone Setting

ZON[7:5]	FAN CONFIGURATION
000	Fan on zone 1 auto
001	Fan on zone 2 auto
010	Fan on zone 3 auto
011	Fan always on full
100	Fan disabled
101	Fan controlled by hottest of zones 2,3
110	Fan controlled by hottest of zones 1,2,3
111	Fan manually controlled

8.18.2 BIT [4] PWM INVERT

Bit [4] inverts the PWM output. If set to 1, 100% duty cycle will yield an output that is low for 255 clocks and high for 1 clock. If set to 0, 100% duty cycle will yield an output that is high for 255 clocks and low for 1 clock.

8.18.3 BIT [3] RESERVED

8.18.4 BITS [2:0] SPIN UP

Bits [2:0] specify the ‘spin up’ time for the fan. When a fan is being started from a stationary state, the PWM output is held at 100% duty cycle for the time specified in the table below before scaling to a lower speed. Note: during spin-up, the PWM pin is forced high (OD) for the duration of the spin-up time.

Note: To reduce the spin-up time, the part uses feedback from the tachometers to determine when each fan has started spinning properly. Spin up for a PWM will end when the tachometer reading register is below the minimum limit, or the spin-up time expires, whichever comes first. All tachs associated with a PWM must be below min for spin-up to end. This feature can be disabled by clearing bit 4 of the Configuration register (7Fh). If disabled, the all fans go on full for the duration of their associated spin up time. Note that the Tachx minimum registers must be programmed to a value less than FFFFh in order for the spin up reduction to work properly.

Table 8.7 - Fan Spin-Up Register

SPIN[2:0]	SPIN UP TIME
000	0 sec
001	100ms
010	250ms (default)
011	400ms
100	700ms
101	1000ms
110	2000ms
111	4000ms

8.19 Registers 5F-61h: Auto Fan Speed Range, PWM Frequency

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
5Fh	R/W	Fan 1 Range/Frequency	RAN3	RAN2	RAN1	RAN0	RES	FRQ2	FRQ1	FRQ0	C3h
60h	R/W	Fan 2 Range/Frequency	RAN3	RAN2	RAN1	RAN0	RES	FRQ2	FRQ1	FRQ0	C3h
61h	R/W	Fan 3 Range/Frequency	RAN3	RAN2	RAN1	RAN0	RES	FRQ2	FRQ1	FRQ0	C3h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

In Auto Fan Mode, when the temperature for a zone is above the Temperature Limit (registers 67-69h) and below the Absolute Temperature Limit (registers 6A-6Ch) the speed of a fan assigned to that zone is determined as follows:

When the temperature reaches the Fan Temp Limit for a zone, the PWM output assigned to that zone is at Fan PWM Minimum. Between Fan Temp Limit and (Fan Temp Limit + Range), the PWM duty cycle increases linearly according to the temperature as shown in the figure below.

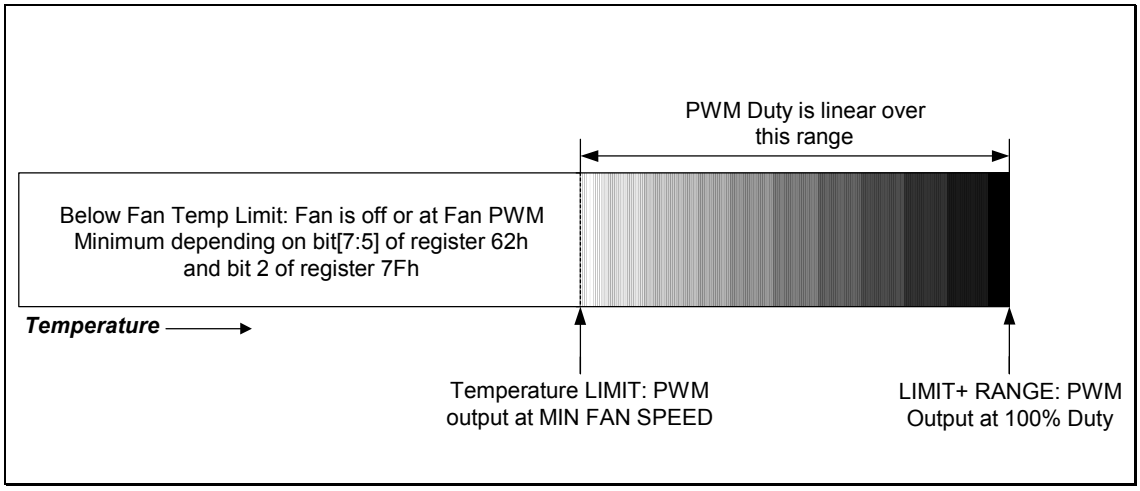


FIGURE 8.1 - FAN ACTIVITY ABOVE FAN TEMP LIMIT

Example for PWM1 assigned to Zone 1:

Zone 1 Fan Temp Limit (Register 67h) is set to 50°C (32h).

Range (Register 5Fh) is set to 8°C (7h)

Fan1 PWM Minimum (Register 64h) is set to 50% (80h)

In this case, the PWM1 duty cycle will be **50% at 50°C**.

Since (**Zone 1 Fan Temp Limit**) + (**Fan 1 Range**) = **50°C** + **8°C** = **58°C**, the fan will run at 100% duty cycle when the temperature of the Zone 1 sensor is at at 58°C.

Since the midpoint of the fan control range is 54°C, and the median duty cycle is 75% (Halfway between the PWM Minimum and 100%), PWM1 duty cycle would be 75% at 54°C.

Above (**Zone 1 Fan Temp Limit**) + (**Fan 1 Range**), the duty cycle must be 100%.

The PWM frequency bits [2:0] determine the PWM frequency for the fan.

Table 8.8 - Register Setting vs. PWM Frequency

PWM Frequency Selection (Default =011=29.3Hz)

FREQ[2:0]	PWM FREQUENCY
000	11.0 Hz
001	14.6 Hz
010	21.9 Hz
011	29.3 Hz
100	35.2 Hz
101	44.0 Hz
110	58.6 Hz
111	87.7 Hz

Table 8.9 - Register Setting vs. Temperature Range

Range Selection (Default =1100=32°C)

RAN[3:0]	RANGE (°C)
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32
1101	40
1110	53.33
1111	80

The range numbers will be used to calculate the slope of the PWM ramp up. For the fractional entries, the PWM will go on full when the temp reaches the next integer value e.g., for 3.33, PWM will be full on at (min temp + 4).

8.20 Register 62h, 63h: Min/Off, Spike Smoothing

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
62h	R/W	Min/Off, Zone 1 Spike Smoothing	OFF3	OFF2	OFF1	RES	ZN1E	ZN1-2	ZN1-1	ZN1-0	00h
63h	R/W	Zone 2, Zone 3 Spike Smoothing	ZN2E	ZN2-2	ZN2-1	ZN2-0	ZN3E	ZN3-2	ZN3-1	ZN3-0	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

The Off/Min Bits [7:5] specify whether the duty cycle will be 0% or Minimum Fan Duty when the measured temperature falls below the Temperature LIMIT register setting (see table below). OFF1 applies to fan 1, OFF2 applies to fan 2, and OFF3 applies to fan 3.

If the Remote1 or Remote2 pins are connected to a processor or chipset, instantaneous temperature spikes may be sampled by the part. If these spikes are not ignored, the CPU fan (if connected to part) may turn on prematurely and produce unpleasant noise. For this reason, any zone that is connected to a chipset or processor should have spike smoothing enabled.

When spike smoothing is enabled, the temperature reading registers still reflect the current value of the temperature – not the ‘smoothed out’ value.

ZN1E, ZN2E, and ZN3E enable temperature smoothing for zones 1, 2, and 3 respectively.

ZN1-2, ZN1-1, and ZN1-0 control smoothing time for Zone 1

ZN2-2, ZN2-1, and ZN2-0 control smoothing time for Zone 2

ZN3-2, ZN3-1, and ZN3-0 control smoothing time for Zone 3

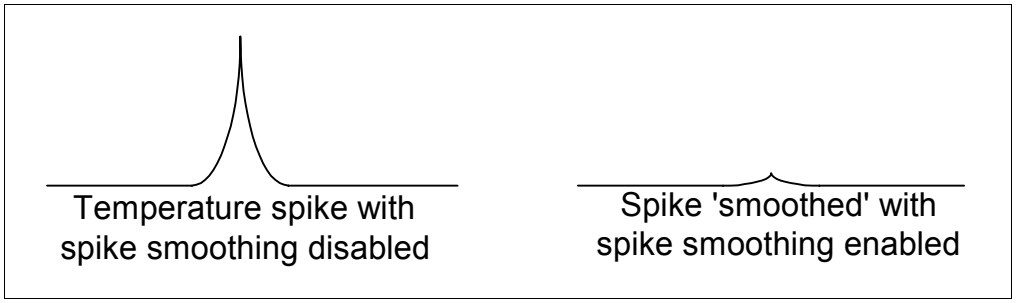


FIGURE 8.2 - WHAT EMC6D100/EMC6D101 SEES WITH AND WITHOUT SPIKE SMOOTHING

Table 8.10 - Spike Smoothing

ZNX-[2:0]	SPIKE SMOOTHED OVER (SEC)
000	35
001	17.6
010	11.8
011	7.0
100	4.4
101	3.0
110	1.6
111	0.8

Table 8.11 - PWM Output Below Limit Depending On Value Of Off/Min

OFF/MIN	PWM ACTION
0	At 0% duty below LIMIT
1	At Min PWM Duty below LIMIT

8.21 Registers 64-66h: Minimum PWM Duty Cycle

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
64h	R/W	Fan1 PWM Minimum	7	6	5	4	3	2	1	0	80h
65h	R/W	Fan2 PWM Minimum	7	6	5	4	3	2	1	0	80h
66h	R/W	Fan3 PWM Minimum	7	6	5	4	3	2	1	0	80h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

These registers specify the minimum duty cycle that the PWM will output when the measured temperature reaches the Temperature LIMIT register setting.

Table 8.12 - PWM Duty vs. Register Setting

MINIMUM PWM DUTY	VALUE (DECIMAL)	VALUE (HEX)
0%	0	00h
⋮	⋮	⋮
25%	64	40h
⋮	⋮	⋮
50%	128	80h
⋮	⋮	⋮
100%	255	FFh

8.22 Registers 67-69h: Temperature LIMIT

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
67h	R/W	Zone 1 Fan Temp Limit	7	6	5	4	3	2	1	0	5Ah
68h	R/W	Zone 2 Fan Temp Limit	7	6	5	4	3	2	1	0	5Ah
69h	R/W	Zone 3 Fan Temp Limit	7	6	5	4	3	2	1	0	5Ah

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

These are the temperature limits for the individual zones. When the current temperature equals this limit, the fan will be turned on if it is not already. When the temperature exceeds this limit, the fan speed will be increased according to the auto fan algorithm based on the setting in the Zone x Range / FANx Frequency register. Default = 90°C=5Ah

Table 8.13 - Temperature Limit vs. Register Setting

LIMIT	LIMIT (DEC)	LIMIT (HEX)
-127°c	-127	81h
⋮	⋮	⋮
-50°c	-50	CEh
⋮	⋮	⋮
0°c	0	00h
⋮	⋮	⋮
50°c	50	32h
⋮	⋮	⋮
127°c	127	7Fh

8.23 Registers 6A-6Ch: Absolute Temperature Limit

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
6Ah	R/W	Zone 1 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h
6Bh	R/W	Zone 2 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h
6Ch	R/W	Zone 3 Temp Absolute Limit	7	6	5	4	3	2	1	0	64h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

In Auto Fan mode, if any zone exceeds the temperature set in the Absolute limit register, all PWM outputs will increase their duty cycle to 100% except those that are disabled via the fan configuration registers. This is a safety feature that attempts to cool the system if there is a potentially catastrophic thermal event.

If an absolute limit register set to 80h (-128°c), the safety feature is disabled for the associated zone. That is, if 80h is written into the Zone x Temp Absolute Limit Register, then regardless of the reading register for the zone, the fans will not turn on-full based on the absolute temp condition.

Default =100°c=64h.

When any fan is in auto fan mode, then if the temperature in any zone exceeds absolute limit, all fans go to full, including any in manual mode, except those that are disabled. Therefore, even if a zone is not associated with a fan, if that zone exceeds absolute, then all fans go to full. In this case, the absolute limit can be chosen to be 7Fh for those zones that are not associated with a fan, so that the fans won't turn on unless the temperature hits 127 degrees.

Table 8.14 - Absolute Limit vs. Register Setting

ABSOLUTE LIMIT	ABS LIMIT (DEC)	ABS LIMIT (HEX)
-127°c	-127	81h
⋮	⋮	⋮
-50°c	-50	CEh
⋮	⋮	⋮
0°c	0	00h
⋮	⋮	⋮
50°c	50	32h
⋮	⋮	⋮
127°c	127	7Fh

8.24 Registers 6D-6Eh: Zone HYSTERESIS Registers

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
6Dh	R/W	Zone 1, Zone 2 Hysteresis	H1-3	H1-2	H1-1	H1-0	H2-3	H2-2	H2-1	H2-0	44h
6Eh	R/W	Zone 3, Hysteresis	H3-3	H3-2	H3-1	H3-0	RES	RES	RES	RES	40h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

If the temperature is above Fan Temp Limit, then drops below Fan Temp Limit, the following will occur:

The fan will remain on, at Fan PWM Minimum, until the temperature goes a certain amount below Fan Temp Limit. That is, when the temperature is less than the temperature limit minus the hysteresis value, the fan will turn off.

The Hysteresis registers control this amount. See below table for details.

Table 8.15 - Hysteresis Settings

SETTING	HYSTERESIS
0h	0°C
⋮	⋮
5h	5°C
⋮	⋮
Fh	15°C

8.25 Register 6F: XOR Test Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
6Fh	R/W	XOR Test Register	RES	RES	RES	RES	RES	RES	RES	XEN	00h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

The part incorporates an XOR tree test mode. When the test mode is enabled by setting the 'XEN' bit high via SMBus, the part enters XOR test mode.

The following signals are included in the XOR test tree:

- VID0, VID1, VID2, VID3, VID4
- TACH1, TACH2, TACH3, TACH4
- PWM2, PWM3, INT#

Since the test mode is XOR tree, the order of the signals in the tree is not important. SDA and SCL are not included in the test tree.

8.26 Register 79h: Test Mode Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
79h	R/W	Test Mode	ANTST2	ANTST1	ANTST0	OSCSEL	ADCAVG	EXTCLK	DIGTST	ADCTST	00h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register contains the following bits:

Bit[0]

Selects the ADC test mode. The default for this bit is zero, which deactivates ADC test mode.

Bit[1]

Selects the digital test mode. The default for this bit is zero, which deactivates digital test mode.

Bit[2]

Selects the external clock test mode. The default for this bit is zero, which deactivates external oscillator clock test mode.

Bit[3]

Selects either 8 or 1 averaging for the ADC test mode. The default for this bit is zero, which sets the averaging to 8 for the ADC test mode. A one in this bit selects no averaging.

Bit[4]

Selects the oscillator clock to be muxed out on the VID2 pin. The default for this bit is zero, which deactivates mux oscillator clock test mode.

Bits[7:5]

Are used by the analog block for test purposes. These three bits of register 4Ah are muxed out on pins dig_test_an_pad[2:0]. These bits are also used to mux out either the SDATA line or the SCLK line to the VID3 pin. If bits[7:5] are '001', then the SDATA line is muxed out onto the VID3 pin. If bits[7:5] are '010', then the SCLK line is muxed out onto the VID3 pin.

8.27 Register 7Ah: Error Debug Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
7Ah	R	Error Debug	RES	ARA	STOP	INVADD	RCV	ROWR	INVRW	NONAC	00h

This register contains the following bits:

Bit[0]

Indicates that no NACK was generated by the host during either a read byte protocol or a receive byte protocol.

Bit[1]

Indicates a read or a write was attempted to an invalid register location.

Bit[2]

Indicates a write to a read only register was attempted

Bit[3

Indicates a receive byte protocol was attempted when the address pointer register pointed to the 00h location. This is the default register location on power on reset. As noted in the "Bus Protocols" section of the "Hardware Monitoring Interface" section, the Internal Address register should be set up with a valid address location by either a send byte protocol or a write byte protocol after power-on-reset, before the receive byte protocol.

Bit[4]

Indicates an invalid slave address was detected.

Bit[5]

Indicates a premature stop was detected.

Bit[6]

Indicates an error was detected during the SMBus Receive Byte Protocol Response to an ARA.

Bit[7]

Reserved.

8.28 Register 7Bh: Test Digital Value Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
7Bh	R/W	Test Digital Value	7	6	5	4	3	2	1	0	00h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

8.29 Register 7Ch: Special Function Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
7Ch	R/W	Special Function	D2EN	D1EN	AVG	OFFCFG	VOLTEN	INTEN	MONMD	LPMD	E0h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register contains the following bits:

Bit[0]

Low-Power Mode Select

0= Sleep Mode (default)

1= Shutdown Mode

Bit[1]

Monitoring Mode Select

0= Continuous Monitor Mode (default)

1= Cycle Monitor Mode

Bit[2]

nINT Enable (EMC6D100 only)

0=Disables nINT pin output function (default)

1=Enables nINT pin output function

Bit[3]

nINT Voltage Enable (EMC6D100 only)

0=Out-of-limit voltages do not affect the state of the nINT pin (default)

1=Enable out-of-limit voltages to make the nINT pin active low

Bit [4]

Offset Register Configure

0= offset register configured to the external temperature channel. (Default)

1= offset register configured to the internal temperature channel.

Bit[5]

Number of measurements of each temperature and voltage reading made.

0= take 128 separate measurements of the data from the analog block for both remote diode temperature readings before averaging the result and storing it in the value register for remote diode temperature measurements; take 8 separate measurements of all other voltage and internal temperature readings before averaging.

1 =use 16 averaging for both remote diode temperature readings and no averaging for all other voltage and internal temperature values. Setting this bit to '1' would be used for power saving. (Default)

Bit[6]

Enable interrupt status register status bit to indicate remote diode 1 thermal error alarm and fault. 0=disable 1=enable (default)

Bit[7]

Enable interrupt status register status bit to indicate remote diode 2 thermal error alarm and fault. 0=disable 1=enable (default).

8.30 Register 7Eh: Interrupt Enable Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
7Eh	R/W	Interrupt Enable	VCC	12V	5V	33V	VCC P	25V	18V	15V	ECh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to enable the voltage events to set the corresponding status bits in the interrupt status registers.

This register contains the following bits:

Bit[0]

1.5V Event Enable (EMC6D100 only)

Bit[1]

1.8V Event Enable (EMC6D100 only)

Bit[2]

2.5V Event Enable

Bit[3]

Vccp Event Enable

Bit[4]

3.3V Event Enable (EMC6D100 only)

Bit[5]

5V Event Enable

Bit[6]

12V Event Enable

Bit[7]

VCC Event Enable

These bits are defined as follows:

0=disable

1=enable.

See the figure in the “Interrupt Status Registers” section.

8.31 Register 7Fh: Configuration Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
7Fh	R/W	Configuration	INIT	FTTST	RES	SUREN	TRDY	RES	INT	RES	10h

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register contains the following bits:

Bit[1]

INT# pin enable: 0=INT# disabled, 1=INT# enabled (EMC6D100 only)

Bit[2]

Reserved

Bit[3]

TRDY: Temperature Reading Ready. This bit indicates that the temperature reading registers have valid values. This bit is used after writing the start bit to '1'. 0= not valid, 1=valid.

Bit[4]

SUREN: Spin-up reduction enable. This bit enables the reduction of the spin-up time based on feedback from all fan tachometers associated with each PWM. 0=disable, 1=enable (default)

Bit[6]

Fan_tach test mode

Bit[7]

Initialization.

8.32 Register 80h: Fan Temp Interrupt Enable Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
80h	R/W	Fan Temp Interrupt Enable	RES	AMB	TEMP	FAN4	FAN3	FAN2	FAN1	FAN	5Eh

These registers become read only when the Lock bit is set. Any further attempts to write to these registers shall have no effect.

This register is used to enable the fan events and the ambient temperature to set the corresponding status bits in the interrupt status registers. It also contains the FAN enable bit to enable fan events to the INT# pin and the TEMP enable bit that enables temperature events to the INT# pin.

This register contains the following bits:

Bit[0]

Fan Interrupt Enable

Bit[1]

Fan 1 Event Enable

Bit[2]

Fan 2 Event Enable

Bit[3]

Fan 3 Event Enable

Bit[4]

FAN4 Event Enable

Bit[5]

Temp Interrupt Enable

Bit[6]

Ambient Event Enable

Bit[7]

Reserved

These bits are defined as follows:

0=disable

1=enable.

See the figure in the “Interrupt Status Registers” section.

8.33 Register 81h: TACH_PWM Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
81h	R/W	Fan Tach/PWM Interrupt Select	T4H	T4L	T3H	T3L	T2H	T2L	T1H	T1L	A4h

These registers become read only when the Lock bit is set. Any further attempts to write to these

registers shall have no effect.

This register is used to associate a PWM with a tachometer input. This association is used by the fan logic to determine when to prevent a bit from being set in the interrupt status registers.

The fan tachometer will not cause a bit to be set in the interrupt status register:

a) if the current value in Current PWM Duty registers is 00h or
b) if the fan is disabled via the Fan Configuration Register.

Note: A bit will never be set in the interrupt status for a fan if its tachometer minimum is set to FFFFh.

See bit definition below.

Bits[1:0] Tach1. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[3:2] Tach2. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[5:4] Tach3. These bits determine the PWM associated with this Tach. See bit combinations below.

Bits[7:6] Tach4. These bits determine the PWM associated with this Tach. See bit combinations below.

BITS[1:0], BITS[3:2], BITS[5:4], BITS[7:6]	PWM ASSOCIATED WITH TACHX
00	PWM1
01	PWM2
10	PWM3
11	Reserved

8.34 Register 83h: Sync Pulse Configuration REGISTER: ON/OFF

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
83h	R/W	Sync Pulse ON/OFF	RES	RES	RES	ON	RES	RES	RES	RES	62h

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

8.34.1 BIT [4] ON

Bit [4] of the Sync Pulse ON/OFF register controls whether the Synchronization Pulse is on or off (active low). The default is ON.

8.35 Registers 86-88h: Smooth Temperature Reading Registers

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
86h	R	Smooth Remote Diode Reading 1	7	6	5	4	3	2	1	0	N/A
87h	R	Smooth Ambient Reading	7	6	5	4	3	2	1	0	N/A
88h	R	Smooth Remote Diode Reading 2	7	6	5	4	3	2	1	0	N/A

The Smooth Temperature Reading registers reflect the smoothed temperatures of the internal and remote diodes. Smoothed temperatures are represented as 8 bit, 2's complement, signed numbers in Celsius, as shown in Table 8.2 - Temperature vs. Register Reading. These registers are read only – a write to these registers has no effect.

These registers hold appropriate values whether smoothing is enabled or not.

8.36 Register 89h: ADC2 LSB Test

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
89h	R	ADC 2 LSB Test	7	6	5	4	3	2	1	0	N/A

8.37 Registers 8A-8Dh: input test Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
8Ah	R	Input Test Reg 1	RES	6	5	4	3	2	1	0	4Dh

8.38 Registers 8E-91h: OUTput test Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
8Bh	R/W	Output Test Reg 1	7	6	5	4	3	2	1	0	4Dh

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register must not be written. Writing this register may produce unexpected results.

8.39 Registers 8A-8Dh: input test Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
8Ch	R	Input Test Reg 2	RES	RES	RES	4	3	2	1	0	0Eh

8.40 Registers 8E-91h: OUTput test Register

REGISTER ADDRESS	READ/ WRITE	REGISTER NAME	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	DEFAULT VALUE
8Dh	R/W	Output Test Reg 1	RES	RES	RES	4	3	2	1	0	0Eh

This register becomes read only when the Lock bit is set. Any further attempts to write to this register shall have no effect.

This register must not be written. Writing this register may produce unexpected results.

Chapter 9 Operational Description

9.1 Maximum Guaranteed Ratings

Operating Temperature Range ..... 0^oC to $+70^oC$
Storage Temperature Range ..... -55° to $+150^oC$
Lead Temperature Range ..... Refer to JEDEC Spec. J-STD-020
Maximum V_{cc} ..... +5.5V
Positive Voltage on any pin (except for analog inputs), with respect to Ground ..... V_{cc}+0.3V
Negative Voltage on any pin (except for analog inputs), with respect to Ground ..... -0.3V

Note: Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

9.2 Ratings for Operation

$T_A = 0^0C - 70^0C$, VCC=+3.3V±10%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
V_{CC} Supply Current						All outputs open, all inputs transitioning from/to 0V to/from 3.3V.
Active Mode	I_{CC}			3	mA	
Sleep Mode	I_{CC}			500	µA	
Shutdown Mode	I_{CC}			3	µA	
Temperature-to-Digital Converter Characteristics						
Internal Temperature Accuracy		-3		+3	^oC	$0^0C <= T_A <= 70^0C$
		-2		+2	^oC	$40^0C <= T_A <= 70^0C$
			±1		^oC	Resolution
External Diode Sensor Accuracy		-5		+5	^oC	$-40^0C <= T_S <= 125^0C$
		-3		+3	^oC	$40^0C <= T_S <= 100^0C$
			±1		^oC	Resolution
Remote Source Current						
High Level			90	130	µA	
Low Level			5.5	7.5	µA	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Analog-to-Digital Converter Characteristics						
Total Unadjusted Error	TUE			±2	%	Note 1
Differential Non-Linearity	DNL		±1		LSB	
Power Supply Sensitivity	PSS		±1		%/V	
Total Monitoring Cycle Time (Cycle Mode)	$t_{C(Cycle)}$		1.0	1.4	sec	Note 2
Conversion Time (Continuous Mode)						Note 3
Option 1	$t_{C(Cts)}$		*624*		msec	
Option 2	$t_{C(Cts)}$		*78*		msec	
Input Resistance			140	200	kΩ	
ADC Resolution						8 bits
Input Buffer (VID0-VID4,TACH1-TACH4)						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		Vcc+0.3	V	
IOD Type Buffer (SCL, SDA, PWM1, PWM2, PWM3/ADDRESS ENABLE, INT#)						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0		Vcc+0.3	V	
Hysteresis	V_{HYS}		500		mV	
Low Output Level	V_{OL}			0.4	V	I_{OL} = +4.0 mA (SCL, SDA) +8.0 mA (PWM1, PWM2, PWM3/ADDRESS ENABLE, INT#)
Leakage Current (ALL - Digital)						(Note 4)
Input High Current	$ILEAK_{IH}$			10	µA	$V_{IN} = V_{CC}$
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
Digital Input Capacitance	C_{IN}			10	pF	

Notes:

- Voltages are measured from the local ground potential, unless otherwise specified.
- Typicals are at TA=25°C and represent most likely parametric norm.
- The maximum allowable power dissipation at any temperature is PD = (TJmax - TA) / QJA.
- Timing specifications are tested at the TTL logic levels, VIL=0.4V for a falling edge and VIH=2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.

Note 1: TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.
Note 2: Total Monitoring Cycle Time includes all temperature conversions, all analog input voltage conversions.
Note 3: The cycle time for option 1 is *624*ms (typical) if 128 measurements are averaged for the remote diode temperature reading and 8 measurements are averaged for all voltage and the internal temperature reading. It is *78*ms (typical) for option 2 if 16 measurements are averaged for the remote diode temperature reading and a single measurement is taken for all voltage and the internal temperature reading (i.e., no averaging).
Note 4: All leakage currents are measured with all pins in high impedance.

Chapter 10 Timing Diagrams

10.1 PWM Outputs

The following sections show the timing for the PWM[1:3] outputs.

10.1.1 WITH SYNCHRONIZATION

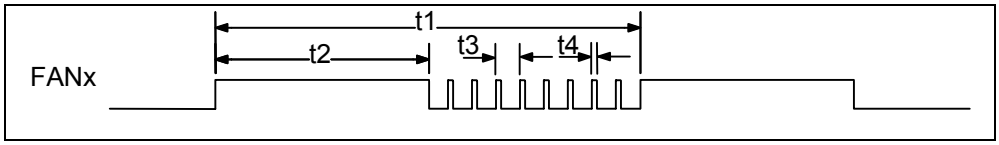


FIGURE 10.1 - PWMX OUTPUT TIMING, SYNC_MSK=0

10.1.2 WITHOUT SYNCHRONIZATION

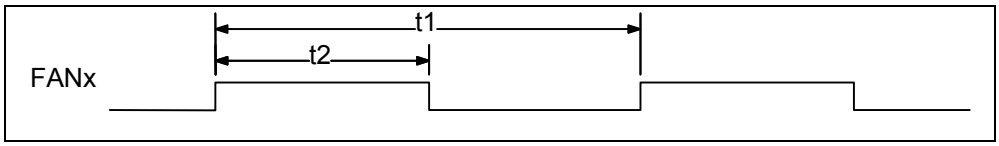


FIGURE 10.2 - PWMX OUTPUT TIMING, SYNC_MSK=1

Table 10.1 - Timing for PWM[1:3] outputs

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PWM Period (Note 1)	11.4		90.9	msec
t2	PWM High Time (Note 2)	0		99.6	%
t3	Sync Pulse Period		711.11		usec
t4	Sync Pulse High Time		44.44		usec

Note 1: This value is programmable by the PWM frequency bits located in the FRFx registers

Note 2: The PWM High Time is based on a percentage of the total PWM period (min=0/256*T_{PWM}, max =255/256*T_{PWM}). During Spin-up the PWM High Time can reach a 100% or Full On. (T_{PWM} = t1)

10.2 SmBus Interface

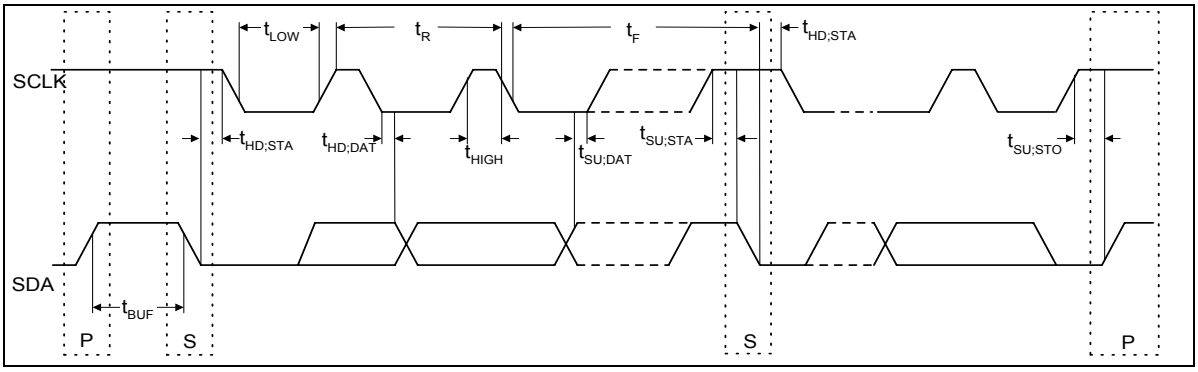


FIGURE 10.3 – SmBus TIMING

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	COMMENTS
F_{SMB}	SMB Operating Frequency	10	400	kHz	Note 1
T_{SP}	Spike Suppression		50	ns	Note 2
T_{BUF}	Bus free time between Stop and Start Condition	1.3		µs	
$T_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	0.6		µs	
$T_{SU:STA}$	Repeated Start Condition setup time	0.6		µs	
$T_{SU:STO}$	Stop Condition setup time	0.6		µs	
$T_{HD:DAT}$	Data hold time	0.3	0.9	µs	
$T_{SU:DAT}$	Data setup time	100		ns	Note 3
T_{LOW}	Clock low period	1.3		µs	
T_{HIGH}	Clock high period	0.6		µs	
T_F	Clock/Data Fall Time	$20+0.1C_b$	300	ns	
T_R	Clock/Data Rise Time	$20+0.1C_b$	300	ns	
C_b	Capacitive load for each bus line		400	pF	

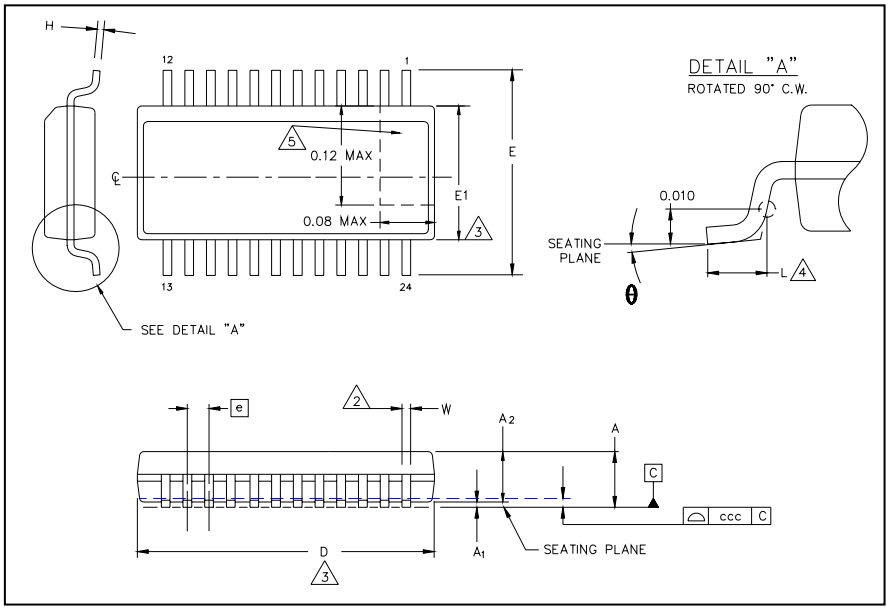
Note 1: The SMBus timing (e.g., max clock frequency of 400kHz) specified exceeds that specified in the System Management Bus Specification, Rev 1.1. This corresponds to the maximum clock frequency for fast mode devices on the I^2C bus. See "The I^2C Bus Specification," version 2.0, Dec. 1998.

Note 2: At 400kHz, spikes of a maximum pulse width of 50ns must be suppressed by the input filter.

Note 3: If using 100 kHz clock frequency, the next data bit output to the SDA line will be 1250 ns (1000 ns (T_R max) + 250 ns ($T_{SU:DAT}$ min) @ 100 kHz) before the SCLK line is released.

Chapter 11 Package Outlines

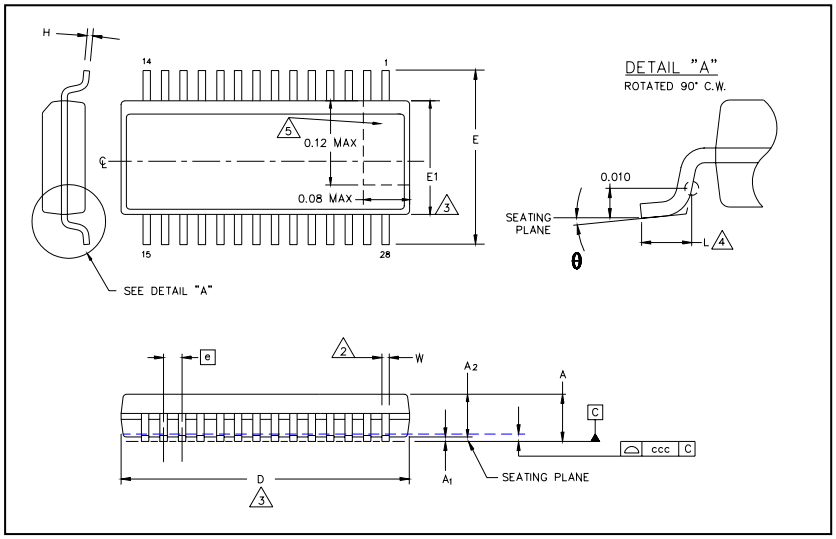
11.1 24 Pin SSOP Package Outline, 0.150” Wide Body, 0.025” Pitch



	MIN	NOMINAL	MAX	REMARKS
A	0.053	~	0.069	Overall Package Height
A1	0.004	~	0.010	Standoff
A2	~	~	0.061	Body Thickness
D	0.337	~	0.344	X Body Size
E	0.228	~	0.244	Y Span
E1	0.150	~	0.157	Y body Size
H	0.007	~	0.010	Lead Frame Thickness
L	0.016	0.025	0.050	Lead Foot Length
e	0.025 Basic			Lead Pitch
θ	0°	~	8°	Lead Foot Angle
W	0.008	0.010	0.012	Lead Width
ccc	~	~	0.004	Coplanarity

Notes:
[1] Controlling Unit: inch.
[2] Tolerance on the true position of the leads is ± 0.0035 inches maximum.
[3] Package body dimensions D and E1 do not include the mold protrusion. Maximum mold protrusion is 0.006 inches for ends, and 0.010 inches for sides.
[4] Dimension for foot length L measured at the gauge plane 0.010 inches above the seating plane.
[5] Details of pin 1 identifier are optional but must be located within the zone indicated.

11.2 28 Pin SSOP Package Outline, 0.150” Wide Body, 0.025” Pitch



	MIN	NOMINAL	MAX	REMARKS
A	0.053	~	0.069	Overall Package Height
A1	0.004	~	0.010	Standoff
A2	~	~	0.061	Body Thickness
D	0.386	~	0.394	X Body Size
E	0.228	~	0.244	Y Span
E1	0.150	~	0.157	Y body Size
H	0.007	~	0.010	Lead Frame Thickness
L	0.016	0.025	0.050	Lead Foot Length
e	0.025 Basic			Lead Pitch
θ	0°	~	8°	Lead Foot Angle
W	0.008	0.010	0.012	Lead Width
ccc	~	~	0.004	Coplanarity

Notes:
[1] Controlling Unit: inch.
[2] Tolerance on the true position of the leads is ± 0.0035 inches maximum.
[3] Package body dimensions D and E1 do not include the mold protrusion. Maximum mold protrusion is 0.006 inches for ends, and 0.010 inches for sides.
[4] Dimension for foot length L measured at the gauge plane 0.010 inches above the seating plane.
[5] Details of pin 1 identifier are optional but must be located within the zone indicated.

Chapter 12 Appendix B – ADC Voltage Conversion

Table 12.1 – Analog-to-Digital Voltage Conversions for Hardware Monitoring Block

Input Voltage							A/D Output	
12 V_{IN}	**5 V_{IN}**	**V_{CC}/3.3 V_{IN}**	**2.5 V_{IN}**	**1.8 V_{IN}**	**1.5 V_{IN}**	**V_{CCPIN}**	**Decimal**	**Binary**
<0.062	<0.026	<0.0172	<0.013	<0.009	<0.008	<0.012	0	0000 0000
0.062–0.125	0.026–0.052	0.017–0.034	0.013–0.026	0.009-0.019	0.008-0.016	0.012–0.023	1	0000 0001
0.125–0.188	0.052–0.078	0.034–0.052	0.026–0.039	0.019-0.028	0.016-0.023	0.023–0.035	2	0000 0010
0.188–0.250	0.078–0.104	0.052–0.069	0.039–0.052	0.028-0.038	0.023-0.031	0.035–0.047	3	0000 0011
0.250–0.313	0.104–0.130	0.069–0.086	0.052–0.065	0.038-0.047	0.031-0.039	0.047–0.058	4	0000 0100
0.313–0.375	0.130–0.156	0.086–0.103	0.065–0.078	0.047-0.056	0.039-0.047	0.058–0.070	5	0000 0101
0.375–0.438	0.156–0.182	0.103–0.120	0.078–0.091	0.056-0.066	0.047-0.055	0.070–0.082	6	0000 0110
0.438–0.500	0.182–0.208	0.120–0.138	0.091–0.104	0.066-0.075	0.055-0.063	0.082–0.093	7	0000 0111
0.500–0.563	0.208–0.234	0.138–0.155	0.104–0.117	0.075-0.084	0.063-0.070	0.093–0.105	8	0000 1000
…	…	…	…	…	…	…	…	…
4.000–4.063	1.666–1.692	1.100–1.117	0.833–0.846	0.600-0.609	0.500-0.508	0.749–0.761	64 (1/4 Scale)	0100 0000
…	…	…	…	…	…	…	…	…
8.000–8.063	3.330–3.560	2.200–2.217	1.667–1.680	1.200-1.209	1.000-1.008	1.499–1.511	128 (1/2 Scale)	1000 0000
…	…	…	…	…	…	…	…	…
12.000–12.063	5.000–5.026	3.300–3.317	2.500–2.513	1.800-1.809	1.500-1.508	2.249–2.261	192 (3/4 Scale)	1100 0000
…	…	…	…	…	…	…	…	…
15.312–15.375	6.380–6.406	4.210–4.230	3.190–3.203	2.297-2.306	1.914-1.922	2.869–2.881	245	1111 0101
15.375–15.437	6.406–6.432	4.230–4.245	3.203–3.216	2.306-2.316	1.922-1.930	2.881–2.893	246	1111 0110
15.437–15.500	6.432–6.458	4.245–4.263	3.216–3.229	2.316-2.325	1.930-1.938	2.893–2.905	247	1111 0111
15.500–15.563	6.458–6.484	4.263–4.280	3.229–3.242	2.325-2.334	1.938-1.945	2.905–2.916	248	1111 1000
15.625–15.625	6.484–6.510	4.280–4.300	3.242–3.255	2.334-2.344	1.945-1.953	2.916–2.928	249	1111 1001
15.625–15.688	6.510–6.536	4.300–4.314	3.255–3.268	2.344-2.353	1.953-1.961	2.928–2.940	250	1111 1010
15.688–15.750	6.536–6.562	4.314–4.330	3.268–3.281	2.353-2.363	1.961-1.969	2.940–2.951	251	1111 1011
15.750–15.812	6.562–6.588	4.331–4.348	3.281–3.294	2.363-2.372	1.969-1.977	2.951–2.964	252	1111 1100
15.812–15.875	6.588–6.615	4.348–4.366	3.294–3.307	2.372-2.381	1.977-1.984	2.964–2.975	253	1111 1101
15.875–15.938	6.615–6.640	4.366–4.383	3.307–3.320	2.381-2.391	1.984-1.992	2.975–2.987	254	1111 1110
>15.938	>6.640	>4.383	>3.320	>2.391	>1.992	>2.988	255	1111 1111