# EP1810 EPLDs

## High-Performance 48-Macrocell Devices

September 1991, ver. 2 Data Sheet



## Features

- High-density replacement for TTL and 74HC
- High-performance 48-macrocell EPLD with $t_{PD}$ = 20 ns and counter frequencies up to 50 MHz
- Zero-power operation (50 µA typical standby)
- Advanced CMOS EPROM technology allowing devices to be erased and reprogrammed
- Individual clocking of all registers or banked register operation from four global Clock inputs
- Programmable registers providing D, T, JK, or SR flip-flops with individual asynchronous Clear control
- 48 macrocells with configurable I/O architecture, allowing up to 64 inputs and 48 outputs
- 100% generically testable to provide 100% programming yield
- Programmable Security Bit for total protection of proprietary designs
- Available in 68-pin J-lead and PGA packages
- Extensive third-party software and programming support

## General Description

The EP1810 Erasable Programmable Logic Devices (EPLDs) offer LSI density, TTL-equivalent speed, and low power consumption. Each EPLD can replace 20 to 30 SSI and MSI packages. These EPLDs are available in 68-pin windowed ceramic and one-time-programmable plastic J-lead (JLCC and PLCC), and windowed ceramic pin-grid array (PGA) packages.

EP1810 EPLDs are designed as LSI replacements for traditional low-power Schottky TTL logic circuits and low-density Programmable Logic Devices (PLDs). These devices have the integration density to replace five CMOS 22V10 devices. The speed and density of the EP1810 EPLDs enable them to implement high-performance, complex functions, such as dedicated peripheral controllers and intelligent support chips. IC count and power requirements are considerably reduced with EP1810 EPLDs, thus minimizing the total size and system cost and significantly increasing reliability.

Logic is implemented with Altera's MAX+PLUS II or A+PLUS development systems. Both systems support schematic capture, Boolean equation, state machine, truth table, and netlist design entry methods. MAX+PLUS II also provides the Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 netlist interface. After the design is entered, the software automatically translates the input files into logic equations, performs Boolean minimization, and fits the design into the EPLD.

MAX+PLUS II automatically partitions larger designs into multiple EPLDs. The device(s) can then be programmed in seconds at the designer's desktop to create customized working silicon. In addition, extensive third-party support exists for design entry, design processing, and device programming.

EP1810 EPLDs use EPROM technology to configure logic connections. User-defined logic functions may be constructed by selectively programming EPROM cells within the EPLD. Moreover, these EPLDs are 100% generically testable and can be erased with UV light. Designs and design modifications can be implemented quickly, eliminating the need for post-programming testing.

## EP1810 EPLDs

The EP1810 EPLD is pin-, function-, and JEDEC-File-compatible with the EP1810T and EP1830 EPLDs. JEDEC Files generated for an EP1810 EPLD can be used for programming EP1810T and EP1830 devices.

### EP1810

The EP1810 EPLD combines speed with low power. It can implement four 12-bit counters at up to 50 MHz, and typically consumes less than 20 mA when operating at 1 MHz. It is available with maximum $t_{PD}$ values of 20, 25, 35, and 45 ns. Both MIL-STD-883B-compliant and DESC-approved parts are available.

### EP1810T

The EP1810T EPLD is a lower-cost version of the EP1810 device. This device operates in Turbo mode only. The Turbo Bit in the EPLD is preset at the factory. The E1810T EPLD is available with maximum $t_{PD}$ values of 20 ns, 25 ns, and 30 ns.

### EP1830

The EP1830 is a fast, low-power version of the EP1810 device. This device can implement four 12-bit counters at up to 50 MHz and typically consumes 20 mA when operating at 1 MHz. It is available with a maximum $t_{PD}$ values of 20 ns and 25 ns.

## Functional Description

EP1810 EPLDs use CMOS EPROM cells to configure internal logic functions. The architecture is 100% user-configurable, accommodating a variety of independent logic functions.

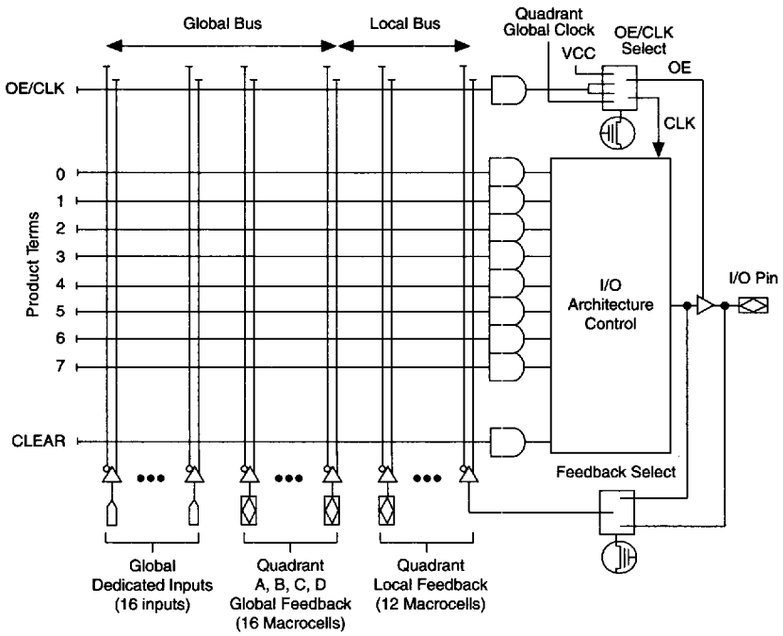
EP1810 EPLDs have 48 macrocells, 16 dedicated data inputs (4 of which can also be used as global Clock inputs), and 48 I/O pins that can be individually configured for input, output, or bidirectional operation on a macrocell-by-macrocell basis. Each macrocell contains 10 product terms for the following functions: 8 product terms are dedicated to logic

implementation; 1 product term is used for Clear control of the internal register; and 1 product term implements either Output Enable or an array Clock.

Of the 48 macrocells, 32 are local (see Figure 1) and 16 are global macrocells (see Figure 2). Local macrocells offer a multiplexed feedback path (with pin or macrocell feedback) and drive the local bus in their quadrants. Global macrocells feature two dedicated feedback paths: one feeds the local bus; the other feeds the global bus. This process, called dual feedback, allows global macrocells to implement buried logic functions while the associated I/O pin is used as an input. Dual feedback ensures maximum I/O flexibility.



***Figure 1. EP1810 Local Macrocell***




Each macrocell consists of a logic array, a tri-state I/O buffer, and a selectable register element that can be programmed for D, T, JK, or SR operation, or bypassed for combinatorial functions. Each macrocell also has programmable output polarity. The logic array has a sum-of-products (AND/OR) structure. The 88 inputs to the programmable-AND array come from true and complement signals of the 16 dedicated data inputs, the 12 I/O feedback signals, and the 16 global feedback signals. The EP1810 EPLD has a total of 480 product terms distributed among 48 macrocells. Each product term represents an 88-input AND gate.

*Figure 2. EP1810 Global Macrocell*

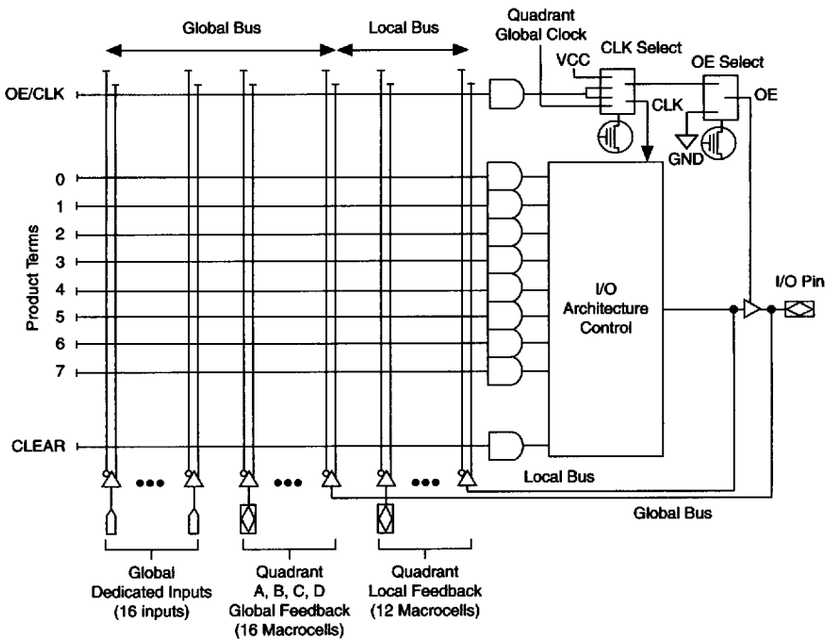



Figure 3 shows the complete block diagram of an EP1810 EPLD. The EP1810 device has four identical quadrants, each containing 12 macrocells. Internal bus structures in these EPLDs feed input signals into the macrocells. Macrocell outputs drive the external pins and internal buses.

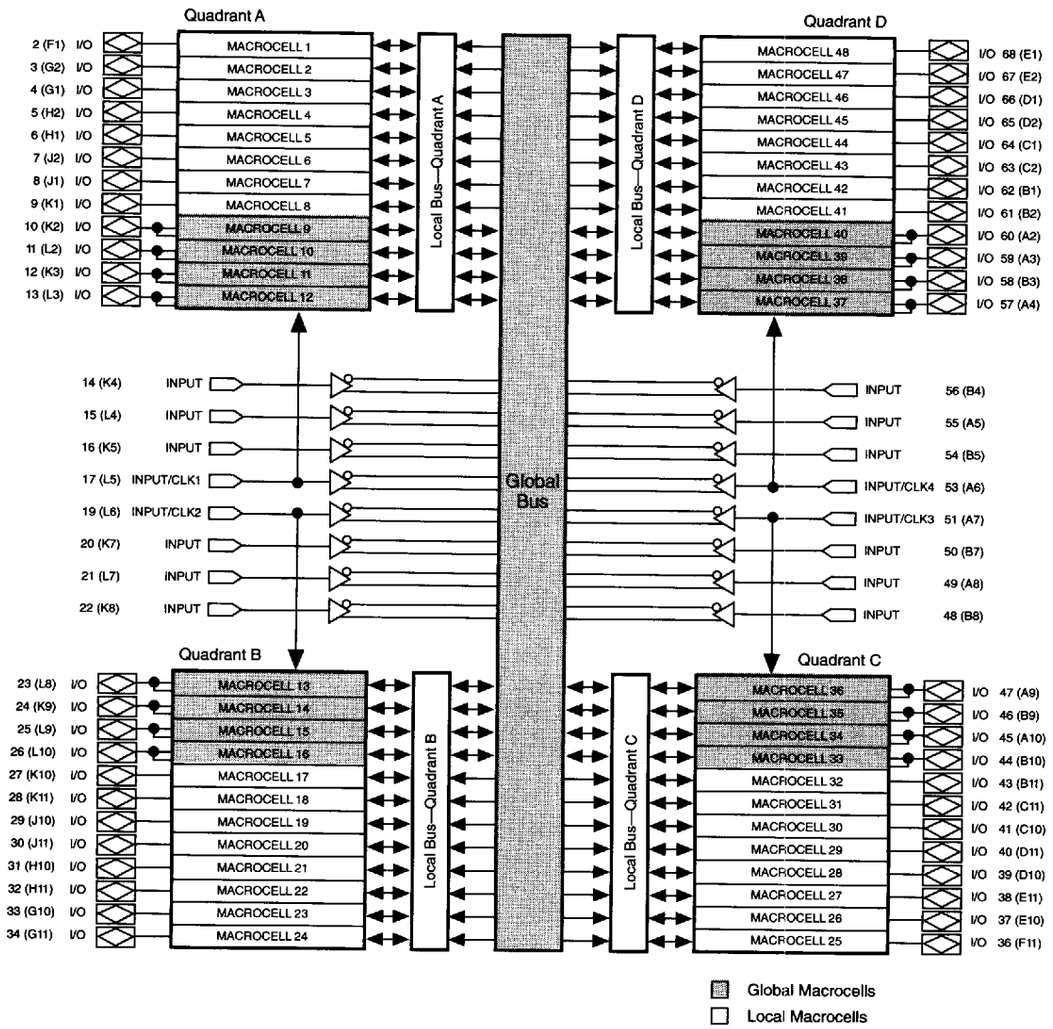
In the erased state, the true and complement of the AND-array inputs are connected to the product terms. An EPROM control cell is located at each intersection of an AND-array input and a product term. During programming, selected connections are opened, allowing any product term to be connected to a true or complement array input signal.

## Clock Options

Each internal flip-flop in EP1810 EPLDs can be clocked independently or in user-defined groups. Each internal register may select its clock source from a dedicated global Clock pin or a product term within the macrocell. Any input or internal logic function can be used as a clock.

Four dedicated inputs also provide global Clock signals (CLK1 to CLK4) to the flip-flops. One global Clock is located in each quadrant; each of which is connected directly to an EP1810 external pin. Global Clocks provide clock-to-output delay times that are faster than internally generated clock signals. Array Clocks provide individual clocking on a macrocell-by-macrocell basis, either directly from pins or through internal logic.

**Figure 3. EP1810 Block Diagram**




Array clock signals allow flip-flops to be configured for positive- or negative-edge-triggered operation. When global Clocks are used, the flip-flops are triggered by the positive edge, i.e., data transitions occur on the rising edge of the clock.

Both global and local macrocells have the same timing characteristics. Switching waveforms for combinatorial, global Clock, and array Clock modes are shown in Figure 4. The timing model is shown in Figure 5.

**Figure 4. EP1810 Switching Waveforms**

*$t_R$ & $t_F$ < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.*

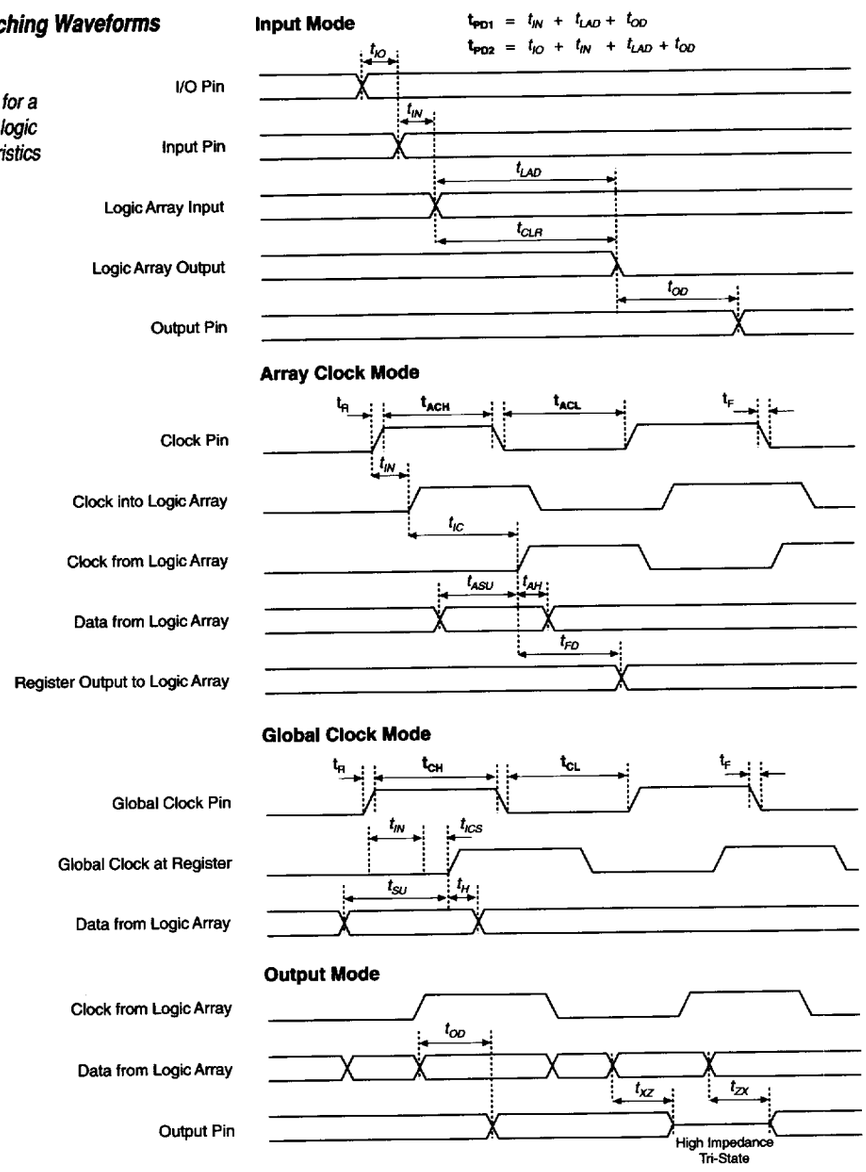
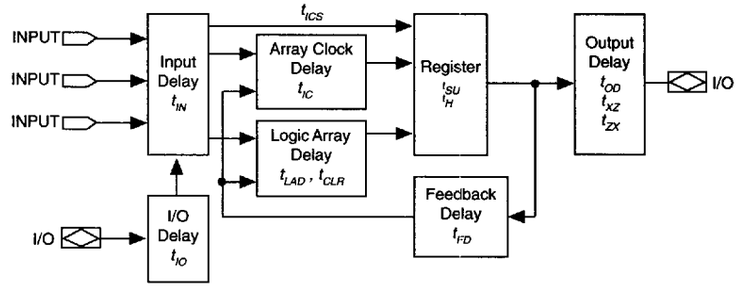


**Figure 5. EP1810 Timing Model**

*If the register is bypassed, the delay between the logic array and the output buffer is zero.*

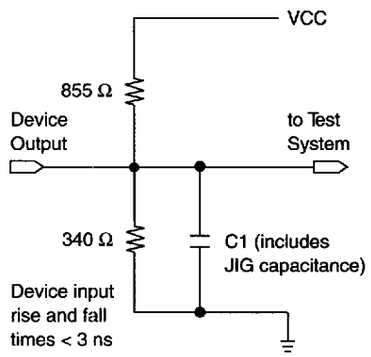



## Functional Testing

EP1810 EPLDs are fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements. A 100% programming yield is ensured. These EPLDs allow test programs to be used and then erased during early stages of production. The ability to use application-independent, general-purpose tests—called generic testing—is unique to EPLDs. The EPLDs also contain on-board test circuitry that allows verification of functions and AC specifications for one-time-programmable packages. AC test measurements are performed under the conditions shown in Figure 6.

**Figure 6. EP1810 AC Test Conditions**

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.*



## Design Security

EP1810 EPLDs contain a programmable Security Bit that controls access to the programmed information. If this Security Bit is used, a proprietary design implemented in the device cannot be copied or retrieved. Since this option makes programmed data within EPROM cells invisible, the designer has a high level of design security. The Security Bit, as well as all other program data, is reset by erasing the EPLD.

## Turbo Bit

All EP1810 EPLDs contain a Turbo Bit, set with the design software, to control the automatic power-down feature that enables the low-standby-power mode. When the Turbo Bit is programmed (Turbo = On), the low-standby-power mode ($I_{CC1}$) is disabled, making the circuit less sensitive to $V_{CC}$ noise transients from the non-turbo mode power-up/power-down cycle. All AC values are tested with the Turbo Bit programmed.

If the design requires low-power operation, the Turbo Bit should be disabled (Turbo = Off). When operating in this mode, some AC parameters may increase. To determine worst-case timing, values given in the AC Non-Turbo Adder specifications must be added to the AC parameter.

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# EP1810 EPLD

## Features

- Highest-performance 48-macrocell EPLD
  - Combinatorial speeds with $t_{PD}$ = 20, 25, 35, and 45 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP1810T and EP1830 EPLDs
- Available in 68-pin windowed ceramic or one-time-programmable (OTP) plastic J-lead chip carrier and windowed ceramic pin-grid array (PGA) packages
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Programmable clock option for independent clocking of all registers
- 100% generically testable to provide 100% programming yield
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

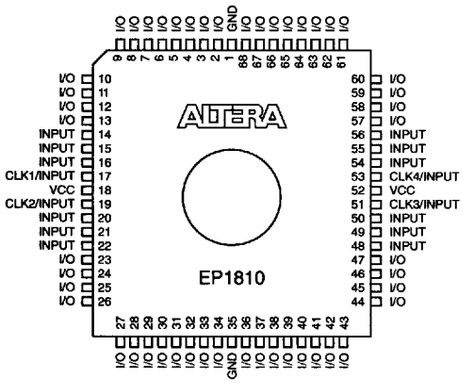
2 Classic EPLDs

## General Description

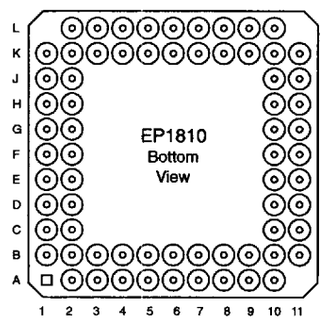
The EP1810 Erasable Programmable Logic Device (EPLD) offers LSI density, TTL-equivalent speed, and low power consumption. It is available in 68-pin windowed ceramic and OTP plastic J-lead chip carrier and windowed ceramic PGA packages. See Figure 7.

***Figure 7. EP1810 Package Pin-Out Diagrams***

*See Table 1 in this data sheet for PGA package pin-outs. Package outlines not drawn to scale.*




J-Lead




PGA

### Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | –2.0 | 7.0 | V |
| $V_{PP}$ | Programming supply voltage | *See Note (1)* | –2.0 | 13.5 | V |
| $V_I$ | DC input voltage | | –2.0 | 7.0 | V |
| $I_{MAX}$ | DC $V_{CC}$ or GND current | | –300 | 300 | mA |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $P_D$ | Power dissipation | | | 1500 | mW |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |

### Recommended Operating Conditions

*See Note (2)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.75 (4.5) | 5.25 (5.5) | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating temperature | For commercial use | 0 | 70 | ° C |
| $T_A$ | Operating temperature | For industrial use | –40 | 85 | ° C |
| $T_C$ | Case temperature | For military use | –55 | 125 | ° C |
| $t_R$ | Input rise time | *See Note (3)* | | 50 | ns |
| $t_F$ | Input fall time | *See Note (3)* | | 50 | ns |

### DC Operating Conditions

*See Notes (2), (4), (5)*

| Symbol | Parameter | Conditions | Speed Grade | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2.0 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | | –0.3 | | 0.8 | V |
| $V_{OH}$ | High-level TTL output voltage | $I_{OH}$ = –4 mA DC | | 2.4 | | | V |
| $V_{OH}$ | High-level CMOS output voltage | $I_{OH}$ = –2 mA DC | | 3.84 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA DC | | | | 0.45 | V |
| $I_I$ | Input leakage current | $V_I = V_{CC}$ or GND | | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-state output off-state current | $V_O = V_{CC}$ or GND | | –10 | | 10 | µA |
| $I_{CC1}$ | $V_{CC}$ supply current | $V_I = V_{CC}$ or GND | -20, -25 | | 50 | 150 | µA |
| | (non-turbo standby) | $I_O$ = 0, *See Note (6)* | -35, -45 | | 35 | 150 | µA |
| $I_{CC2}$ | $V_{CC}$ supply current | $V_I = V_{CC}$ or GND, No load, | -20, -25 | | 20 | 40 | mA |
| | (non-turbo mode) | f = 1.0 MHz, *See Note (7)* | -35, -45 | | 10 | 30 (40) | mA |
| $I_{CC3}$ | $V_{CC}$ supply current | $V_I = V_{CC}$ or GND, No load, | -20, -25 | | 180 | 225 | mA |
| | (turbo mode) | f = 1.0 MHz, *See Note (7)* | -35, -45 | | 100 | 180 (240) | mA |

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### Capacitance *See Note (8)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 20 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 20 | pF |
| $C_{CLK}$ | Clock pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 25 | pF |

### AC Operating Conditions: EP1810-20, EP1810-25 *See Note (5)*

| External Timing Parameters | | | EP1810-20 | | EP1810-25 | | Non-Turbo Adder | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | *See Note (9)* | **Unit** |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 20 | | 25 | 25 | ns |
| $t_{PD2}$ | I/O input to non-registered output | | | 22 | | 28 | 25 | ns |
| $t_{SU}$ | Global clock setup time | | 13 | | 17 | | 25 | ns |
| $t_{H}$ | Global clock hold time | | 0 | | 0 | | 0 | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 15 | | 18 | 0 | ns |
| $t_{CH}$ | Global clock high time | | 8 | | 10 | | 0 | ns |
| $t_{CL}$ | Global clock low time | | 8 | | 10 | | 0 | ns |
| $t_{ASU}$ | Array clock setup time | | 8 | | 10 | | 25 | ns |
| $t_{AH}$ | Array clock hold time | | 8 | | 10 | | 0 | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 20 | | 25 | 25 | ns |
| $t_{CNT}$ | Minimum global clock period | | | 20 | | 25 | 0 | ns |
| $f_{CNT}$ | Maximum internal frequency | *See Note (7)* | 50 | | 40 | | 0 | MHz |
| $f_{MAX}$ | Maximum clock frequency | *See Note (10)* | 62.5 | | 50 | | 0 | MHz |

| Internal Timing Parameters | | | EP1810-20 | | EP1810-25 | | Non-Turbo Adder | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | *See Note (9)* | **Unit** |
| $t_{IN}$ | Input pad and buffer delay | | | 5 | | 7 | 0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 2 | | 3 | 0 | ns |
| $t_{LAD}$ | Logic array delay | | | 9 | | 12 | 25 | ns |
| $t_{OD}$ | Output buffer and pad delay | C1 = 35 pF | | 6 | | 6 | 0 | ns |
| $t_{ZX}$ | Output buffer enable delay | | | 6 | | 6 | 0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF, *Note (11)* | | 6 | | 6 | 0 | ns |
| $t_{SU}$ | Register setup time | | 8 | | 10 | | 0 | ns |
| $t_{H}$ | Register hold time | | 8 | | 10 | | 0 | ns |
| $t_{IC}$ | Array clock delay | | | 9 | | 12 | 25 | ns |
| $t_{ICS}$ | Global clock delay | | | 4 | | 5 | 0 | ns |
| $t_{FD}$ | Feedback delay | | | 3 | | 3 | –25 | ns |
| $t_{CLR}$ | Register clear time | | | 9 | | 12 | 25 | ns |

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### AC Operating Conditions: EP1810-35, EP1810-45 *See Note (5)*

| External Timing Parameters | | | EP1810-35 | | EP1810-45 | | Non-Turbo Adder | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | *See Note (9)* | **Unit** |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 35 | | 45 | 30 | ns |
| $t_{PD2}$ | I/O input to non-registered output | | | 40 | | 50 | 30 | ns |
| $t_{SU}$ | Global clock setup time | | 25 | | 30 | | 30 | ns |
| $t_{H}$ | Global clock hold time | | 0 | | 0 | | 0 | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 20 | | 25 | 0 | ns |
| $t_{CH}$ | Global clock high time | | 12 | | 15 | | 0 | ns |
| $t_{CL}$ | Global clock low time | | 12 | | 15 | | 0 | ns |
| $t_{ASU}$ | Array clock setup time | | 10 | | 11 | | 30 | ns |
| $t_{AH}$ | Array clock hold time | | 15 | | 18 | | 0 | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 35 | | 45 | 30 | ns |
| $t_{CNT}$ | Minimum global clock period | | | 35 | | 45 | 0 | ns |
| $f_{CNT}$ | Maximum internal frequency | *See Note (7)* | 28.6 | | 22.2 | | 0 | MHz |
| $f_{MAX}$ | Maximum clock frequency | *See Note (10)* | 40 | | 33.3 | | 0 | MHz |

| Internal Timing Parameters | | | EP1810-35 | | EP1810-45 | | Non-Turbo Adder | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | *See Note (9)* | **Unit** |
| $t_{IN}$ | Input pad and buffer delay | | | 7 | | 7 | 0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 5 | | 5 | 0 | ns |
| $t_{LAD}$ | Logic array delay | | | 19 | | 27 | 30 | ns |
| $t_{OD}$ | Output buffer and pad delay | C1 = 35 pF | | 9 | | 11 | 0 | ns |
| $t_{ZX}$ | Output buffer enable delay | | | 9 | | 11 | 0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF, *Note (11)* | | 9 | | 11 | 0 | ns |
| $t_{SU}$ | Register setup time | | 10 | | 11 | | 0 | ns |
| $t_{H}$ | Register hold time | | 15 | | 18 | | 0 | ns |
| $t_{IC}$ | Array clock delay | | | 19 | | 27 | 30 | ns |
| $t_{ICS}$ | Global clock delay | | | 4 | | 8 | 0 | ns |
| $t_{FD}$ | Feedback delay | | | 6 | | 7 | –30 | ns |
| $t_{CLR}$ | Register clear time | | | 24 | | 32 | 30 | ns |

### Product Availability

| Operating Temperature | | Availability |
|---|---|---|
| Commercial | (0° C to 70° C) | EP1810-20, EP1810-25, EP1810-35, EP1810-45 |
| Industrial | (–40° C to 85° C) | EP1810-25, EP1810-40, EP1810-45 *(12)* |
| Military | (–55° C to 125° C) | EP1810-45 *(13)* |

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*Notes to tables:*

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP1810-20 and EP1810-25: maximum $V_{PP}$ is 14.0 V.
(2) Numbers in parentheses are for military and industrial temperature versions.
(3) For EP1810-20 and EP1810-25 clocks: $t_R$ and $t_F$ = 20 ns.
(4) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 5 V.
(5) Operating conditions: $V_{CC}$ = 5 V ± 5%, $T_A$ = 0° C to 70° C for commercial use.
$V_{CC}$ = 5 V ± 10%, $T_A$ = –40° C to 85° C for industrial use.
$V_{CC}$ = 5 V ± 10%, $T_C$ = –55° C to 125° C for military use.
(6) When in non-turbo mode, an EPLD will automatically enter standby mode if logic transitions do not occur (approximately 100 ns after the last transition).
(7) Measured with a device programmed as four 12-bit counters.
(8) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. For EP1810-35 and EP1810-45: Pin 19 (high-voltage pin during programming) has a maximum capacitance of 160 pF.
(9) See "Turbo Bit" earlier in this data sheet.
(10) The $f_{MAX}$ values represent the highest frequency for pipelined data.
(11) Sample-tested only for an output change of 500 mV.
(12) DC/AC specifications for EP1810-40 (industrial) are available by calling Altera's Marketing Department at (408) 984-2800.
(13) Only military-temperature-range devices are listed above. MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs), available by calling Altera's Marketing Department. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.



Table 1 shows the pin-outs for the EP1810 PGA package.

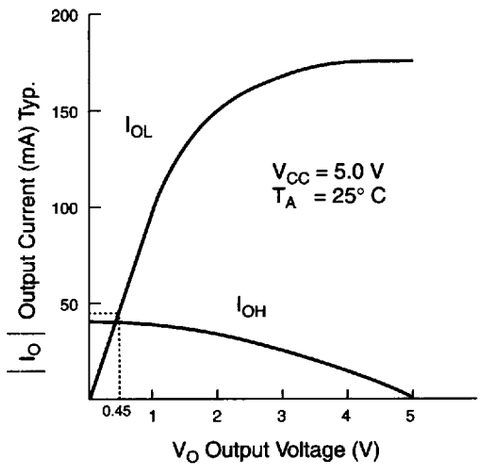
**Table 1. EP1810 PGA Pin-Outs**

| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|---|---|
| A2 | I/O | B9 | I/O | F10 | GND | K4 | INPUT |
| A3 | I/O | B10 | I/O | F11 | I/O | K5 | INPUT |
| A4 | I/O | B11 | I/O | G1 | I/O | K6 | VCC |
| A5 | INPUT | C1 | I/O | G2 | I/O | K7 | INPUT |
| A6 | CLK4/INPUT | C2 | I/O | G10 | I/O | K8 | INPUT |
| A7 | CLK3/INPUT | C10 | I/O | G11 | I/O | K9 | I/O |
| A8 | INPUT | C11 | I/O | H1 | I/O | K10 | I/O |
| A9 | I/O | D1 | I/O | H2 | I/O | K11 | I/O |
| A10 | I/O | D2 | I/O | H10 | I/O | L2 | I/O |
| B1 | I/O | D10 | I/O | H11 | I/O | L3 | I/O |
| B2 | I/O | D11 | I/O | J1 | I/O | L4 | INPUT |
| B3 | I/O | E1 | I/O | J2 | I/O | L5 | CLK1/INPUT |
| B4 | INPUT | E2 | I/O | J10 | I/O | L6 | CLK2/INPUT |
| B5 | INPUT | E10 | I/O | J11 | I/O | L7 | INPUT |
| B6 | VCC | E11 | I/O | K1 | I/O | L8 | I/O |
| B7 | INPUT | F1 | I/O | K2 | I/O | L9 | I/O |
| B8 | INPUT | F2 | GND | K3 | I/O | L10 | I/O |

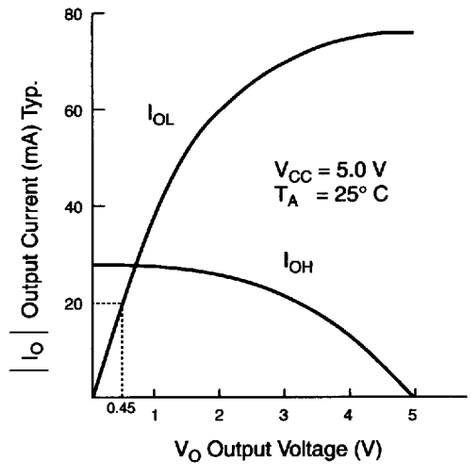
Figure 8 shows output drive characteristics for EP1810 I/O pins and typical supply current versus frequency for the EP1810 EPLD.

*Figure 8. EP1810 Output Drive Characteristics and $I_{CC}$ vs. Frequency*

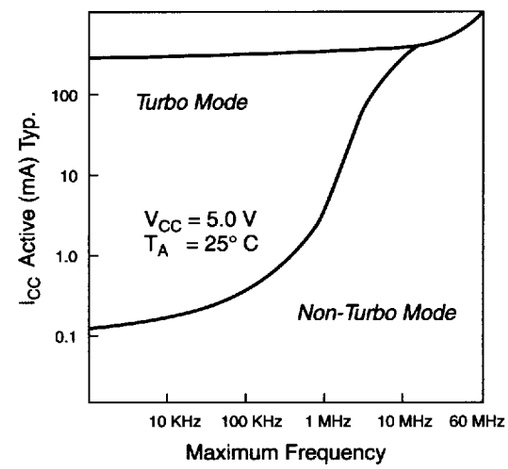
**EP1810-20 and EP1810-25 EPLDs**




**EP1810-35 and EP1810-45 EPLDs**




**All EP1810 EPLDs**



# EP1810T EPLD

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## Features

- Highest-performance 48-macrocell EPLD
  - Combinatorial speeds with $t_{PD}$ = 20 ns, 25 ns, and 35 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP1810 and EP1830 EPLDs
- Available in 68-pin, one-time-programmable (OTP) plastic J-lead chip carrier package (PLCC)
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Programmable clock option for independent clocking of all registers
- 100% generically testable to provide 100% programming yield
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

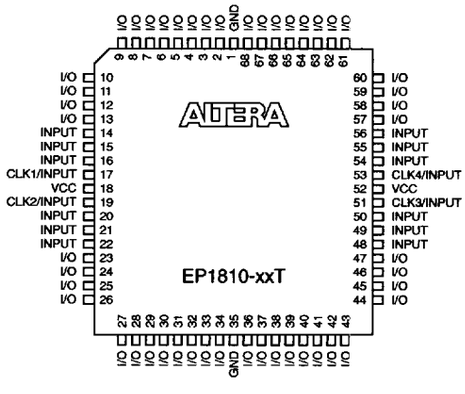


## General Description

Altera's EP1810T Erasable Programmable Logic Device (EPLD) is a low-cost, high-performance version of the EP1810 device. This EPLD operates in a turbo mode that is optimized for high-speed applications. The Turbo Bit in the device is preset at the factory. The EP1810T EPLD is available in OTP plastic 68-pin J-lead chip carrier packages with maximum $t_{PD}$ values of 20 ns, 25 ns, and 35 ns. See Figure 9. It contains 48 macrocells with user-configurable I/O architecture for up to 64 inputs and 48 outputs.

***Figure 9. EP1810T Package Pin-Out Diagram***

*Package outline not drawn to scale.*




J-Lead

### Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | –2.0 | 7.0 | V |
| $V_{PP}$ | Programming supply voltage | *See Note (1)* | –2.0 | 13.5 | V |
| $V_I$ | DC input voltage | | –2.0 | 7.0 | V |
| $I_{MAX}$ | DC $V_{CC}$ or GND current | | –300 | 300 | mA |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $P_D$ | Power dissipation | | | 1500 | mW |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |

### Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.75 | 5.25 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating temperature | For commercial use | 0 | 70 | ° C |
| $t_R$ | Input rise time | *See Note (2)* | | 50 | ns |
| $t_F$ | Input fall time | *See Note (2)* | | 50 | ns |

### DC Operating Conditions

*See Notes (3), (4)*

| Symbol | Parameter | Conditions | Speed Grade | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2.0 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | | –0.3 | | 0.8 | V |
| $V_{OH}$ | High-level TTL output voltage | $I_{OH}$ = –4 mA DC | | 2.4 | | | V |
| $V_{OH}$ | High-level CMOS output voltage | $I_{OH}$ = –2 mA DC | | 3.84 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA DC | | | | 0.45 | V |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or GND | | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-state output off-state current | $V_O$ = $V_{CC}$ or GND | | –10 | | 10 | µA |
| $I_{CC1}$ | $V_{CC}$ supply current (standby) | $V_I$ = $V_{CC}$ or GND, No load | -20T, -25T | | 180 | 250 | mA |
| | | | -35T | | 120 | 215 | mA |
| $I_{CC3}$ | $V_{CC}$ supply current (turbo mode) | $V_I$ = $V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)* | -20T, -25T | | 180 | 250 | mA |
| | | | -35T | | 120 | 215 | mA |

### Capacitance

*See Note (6)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 20 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 20 | pF |
| $C_{CLK}$ | Clock pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 25 | pF |

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## AC Operating Conditions *See Note (4)*

| External Timing Parameters | | | EP1810-20T | | EP1810-25T | | EP1810-35T | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 20 | | 25 | | 35 | ns |
| $t_{PD2}$ | I/O input to non-registered output | | | 22 | | 28 | | 40 | ns |
| $t_{SU}$ | Global clock setup time | | 13 | | 17 | | 25 | | ns |
| $t_{H}$ | Global clock hold time | | 0 | | 0 | | 0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 15 | | 18 | | 20 | ns |
| $t_{CH}$ | Global clock high time | | 8 | | 10 | | 12 | | ns |
| $t_{CL}$ | Global clock low time | | 8 | | 10 | | 12 | | ns |
| $t_{ASU}$ | Array clock setup time | | 8 | | 10 | | 10 | | ns |
| $t_{AH}$ | Array clock hold time | | 8 | | 10 | | 15 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 20 | | 25 | | 35 | ns |
| $t_{CNT}$ | Minimum global clock period | | | 20 | | 25 | | 35 | ns |
| $f_{CNT}$ | Internal maximum frequency | *See Note (5)* | 50 | | 40 | | 28.6 | | MHz |
| $f_{MAX}$ | Maximum frequency | *See Note (7)* | 62.5 | | 50 | | 40 | | MHz |

| Internal Timing Parameters | | | EP1810-20T | | EP1810-25T | | EP1810-35T | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{IN}$ | Input pad and buffer delay | | | 5 | | 7 | | 7 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 2 | | 3 | | 5 | ns |
| $t_{LAD}$ | Logic array delay | | | 9 | | 12 | | 19 | ns |
| $t_{OD}$ | Output buffer and pad delay | C1 = 35 pF | | 6 | | 6 | | 9 | ns |
| $t_{ZX}$ | Output buffer enable delay | | | 6 | | 6 | | 9 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF, *See Note (8)* | | 6 | | 6 | | 9 | ns |
| $t_{SU}$ | Register setup time | | 8 | | 10 | | 10 | | ns |
| $t_{H}$ | Register hold time | | 8 | | 10 | | 15 | | ns |
| $t_{IC}$ | Array clock delay | | | 9 | | 12 | | 19 | ns |
| $t_{ICS}$ | Global clock delay | | | 4 | | 5 | | 4 | ns |
| $t_{FD}$ | Feedback delay | | | 3 | | 3 | | 6 | ns |
| $t_{CLR}$ | Register clear time | | | 9 | | 12 | | 24 | ns |

*Notes to tables:*

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP1810-20T and EP1810-25T: maximum $V_{PP}$ is 14.0 V.
(2) For EP1810-20T and EP1810-25T clocks: $t_R$ and $t_F$ = 20 ns.
(3) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 5 V.
(4) Operating conditions: $V_{CC}$ = 5 V ± 5%, $T_A$ = 0° C to 70° C for commercial use.
(5) Measured with a device programmed as four 12-bit counters.
(6) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only. For EP1810-35T: Pin 19 (high-voltage pin during programming) has a maximum capacitance of 160 pF.
(7) The $f_{MAX}$ values represent the highest frequency for pipelined data.
(8) Sample-tested only for an output change of 500 mV.

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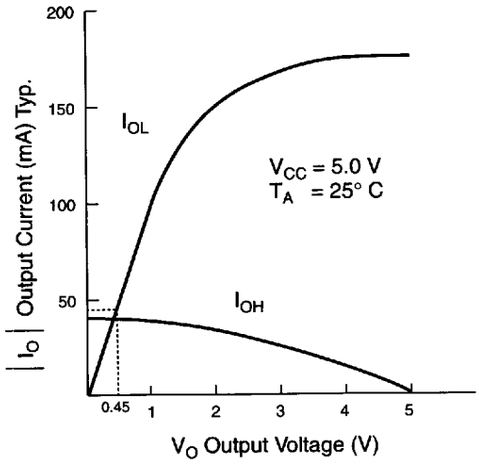
### Product Availability

| Operating Temperature | | Availability |
|---|---|---|
| Commercial | (0° C to 70° C) | EP1810-20T, EP1810-25T, EP1810-35T |
| Industrial | (–40° C to 85° C) | Consult factory |
| Military | (–55° C to 125° C) | Consult factory |

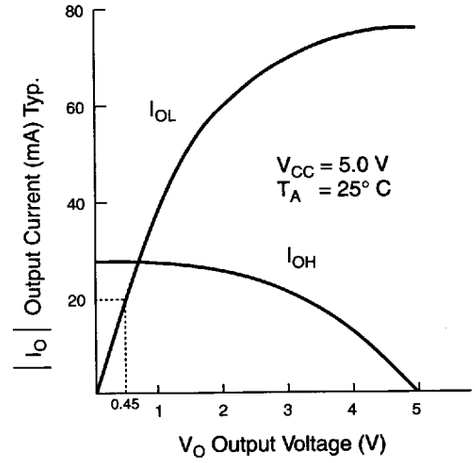
Figure 10 shows the output drive characteristics for EP1810T I/O pins and typical supply current versus frequency for the EP1810T EPLD.

*Figure 10. EP1810T Output Drive Characteristics and $I_{CC}$ vs. Frequency*

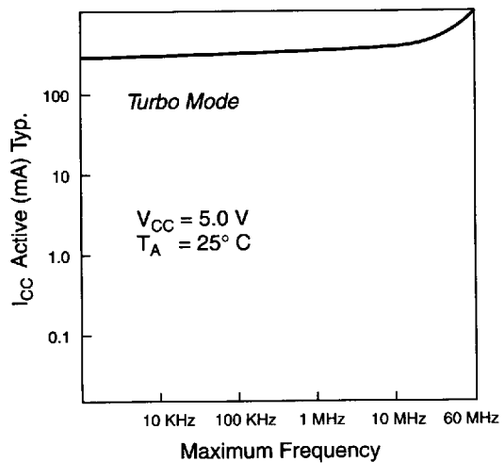
**EP1810-20T and EP1810-25T EPLDs**




**EP1810-35T EPLD**




**All EP1810T EPLDs**



# EP1830 EPLD

T-46-19-09

## Features

- High-performance 48-macrocell EPLD
  - Combinatorial speeds with $t_{PD}$ = 20 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP1810 and EP1810T EPLDs
- Available in 68-pin, one-time-programmable (OTP) plastic J-lead chip carrier package (PLCC)
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Programmable clock option for independent clocking of all registers
- 100% generically testable to provide 100% programming yield
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

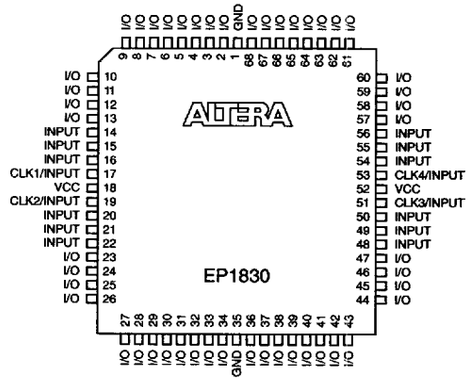


## General Description

Altera's EP1830 Erasable Programmable Logic Device (EPLD) is a fast, low-power version of the EP1810 device. The EP1830 can implement four 12-bit counters at up to 50 MHz and typically consumes 20 mA when operating at 1 MHz. The EP1830 EPLD is available in OTP plastic 68-pin J-lead chip carrier packages with maximum $t_{PD}$ values of 20 ns and 25 ns. See Figure 11.

***Figure 11. EP1830 Package Pin-Out Diagram***

*Package outline not drawn to scale.*




J-Lead

### Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | –2.0 | 7.0 | V |
| $V_{PP}$ | Programming supply voltage | *See Note (1)* | –2.0 | 14.0 | V |
| $V_I$ | DC input voltage | | –2.0 | 7.0 | V |
| $I_{MAX}$ | DC $V_{CC}$ or GND current | | –300 | 300 | mA |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $P_D$ | Power dissipation | | | 1500 | mW |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | °C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | °C |

### Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.75 | 5.25 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating temperature | For commercial use | 0 | 70 | °C |
| $T_A$ | Operating temperature | For industrial use | –40 | 85 | °C |
| $t_R$ | Input rise time | *See Note (2)* | | 50 | ns |
| $t_F$ | Input fall time | *See Note (2)* | | 50 | ns |

### DC Operating Conditions

*See Notes (3), (4)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.8 | V |
| $V_{OH}$ | High-level TTL output voltage | $I_{OH}$ = –4 mA DC | 2.4 | | | V |
| $V_{OH}$ | High-level CMOS output voltage | $I_{OH}$ = –2 mA DC | 3.84 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA DC | | | 0.45 | V |
| $I_I$ | Input leakage current | $V_I = V_{CC}$ or GND | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-state output off-state current | $V_O = V_{CC}$ or GND | –10 | | 10 | µA |
| $I_{CC1}$ | $V_{CC}$ supply current (non-turbo standby) | $V_I = V_{CC}$ or GND<br>$I_O$ = 0, *See Note (5)* | | 50 | 150 | µA |
| $I_{CC2}$ | $V_{CC}$ supply current (non-turbo mode) | $V_I = V_{CC}$ or GND, No load,<br>f = 1.0 MHz, *See Note (6)* | | 20 | 40 | mA |
| $I_{CC3}$ | $V_{CC}$ supply current (turbo mode) | $V_I = V_{CC}$ or GND, No load,<br>f = 1.0 MHz, *See Note (6)* | | 180 | 225 | mA |

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### Capacitance *See Note (7)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 20 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 20 | pF |
| $C_{CLK}$ | Clock pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 25 | pF |

### AC Operating Conditions *See Note (4)*

| External Timing Parameters | | | EP1830-20 | | EP1830-25 | | Non-Turbo Adder | |
|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Conditions | Min | Max | Min | Max | *See Note (8)* | Unit |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 20 | | 25 | 25 | ns |
| $t_{PD2}$ | I/O input to non-registered output | | | 22 | | 28 | 25 | ns |
| $t_{SU}$ | Global clock setup time | | 13 | | 17 | | 25 | ns |
| $t_{H}$ | Global clock hold time | | 0 | | 0 | | 0 | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 15 | | 18 | 0 | ns |
| $t_{CH}$ | Global clock high time | | 8 | | 10 | | 0 | ns |
| $t_{CL}$ | Global clock low time | | 8 | | 10 | | 0 | ns |
| $t_{ASU}$ | Array clock setup time | | 8 | | 10 | | 25 | ns |
| $t_{AH}$ | Array clock hold time | | 8 | | 10 | | 0 | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 20 | | 25 | 25 | ns |
| $t_{CNT}$ | Minimum global clock period | | | 20 | | 25 | 0 | ns |
| $f_{CNT}$ | Internal maximum frequency | *See Note (6)* | 50 | | 40 | | 0 | MHz |
| $f_{MAX}$ | Maximum frequency | *See Note (9)* | 62.5 | | 50 | | 0 | MHz |

| Internal Timing Parameters | | | EP1830-20 | | EP1830-25 | | Non-Turbo Adder | |
|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Conditions | Min | Max | Min | Max | *See Note (8)* | Unit |
| $t_{IN}$ | Input pad and buffer delay | | | 5 | | 7 | 0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 2 | | 3 | 0 | ns |
| $t_{LAD}$ | Logic array delay | | | 9 | | 12 | 25 | ns |
| $t_{OD}$ | Output buffer and pad delay | C1 = 35 pF | | 6 | | 6 | 0 | ns |
| $t_{ZX}$ | Output buffer enable delay | | | 6 | | 6 | 0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF, *Note (10)* | | 6 | | 6 | 0 | ns |
| $t_{SU}$ | Register setup time | | 8 | | 10 | | 0 | ns |
| $t_{H}$ | Register hold time | | 8 | | 10 | | 0 | ns |
| $t_{IC}$ | Array clock delay | | | 9 | | 12 | 25 | ns |
| $t_{ICS}$ | Global clock delay | | | 4 | | 5 | 0 | ns |
| $t_{FD}$ | Feedback delay | | | 3 | | 3 | –25 | ns |
| $t_{CLR}$ | Register clear time | | | 9 | | 12 | 25 | ns |

*Notes to tables:*

(1) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(2) For all clocks: $t_R$ and $t_F$ = 20 ns.
(3) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 5 V.
(4) Operating conditions: $V_{CC}$ = 5 V ± 5%, $T_A$ = 0° C to 70° C for commercial use.
$V_{CC}$ = 5 V ± 10%, $T_A$ = –40° C to 85° C for industrial use.
(5) When in non-turbo mode, an EPLD automatically enters standby mode if logic transitions do not occur (approximately 100 ns after the last transition).
(6) Measured with a device programmed as four 12-bit counters.
(7) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated clock inputs only.
(8) See "Turbo Bit" earlier in this data sheet.
(9) The $f_{MAX}$ values represent the highest frequency for pipelined data.
(10) Sample-tested only for an output change of 500 mV.

### Product Availability

| Operating Temperature | | Availability |
|---|---|---|
| Commercial | (0° C to 70° C) | EP1830-20, EP1830-25, EP1830-30 |
| Industrial | (–40° C to 85° C) | EP1830-25 |
| Military | (–55° C to 125° C) | Consult factory |

Figure 12 shows the output drive characteristics for EP1830 I/O pins and typical supply current versus frequency for the EP1830 EPLD.

**Figure 12. EP1830 Output Drive Characteristics and $I_{CC}$ vs. Frequency**